MP1911

2.5V to 16V, 1A, H-Bridge Driver in an SOT583 Package

DESCRIPTION

The MP1911 is an H-bridge driver, and operates from a 2.5V to 16V power supply voltage, which can supply an output current (I_{OUT}) of up to 1A according to the logic control. The H-bridge consists of four N-channel power MOSFETs and an internal charge pump to generate the required gate-drive voltages.

The MP1911 is controlled by two input pins, IN1 and IN2. The two on/off inputs determine the output mode: forward, reverse, coast, or brake. The brake is applied to stop the driver when IN1 and IN2 are pulled high. A very low standby circuit current can be achieved when IN1 and IN2 are pulled low.

Full protection features include over-current protection (OCP), short-circuit protection (SCP), under-voltage lockout (UVLO), and over-temperature protection (OTP).

The MP1911 requires a minimal number of readily available, standard external components, and is available in an SOT583 package.

FEATURES

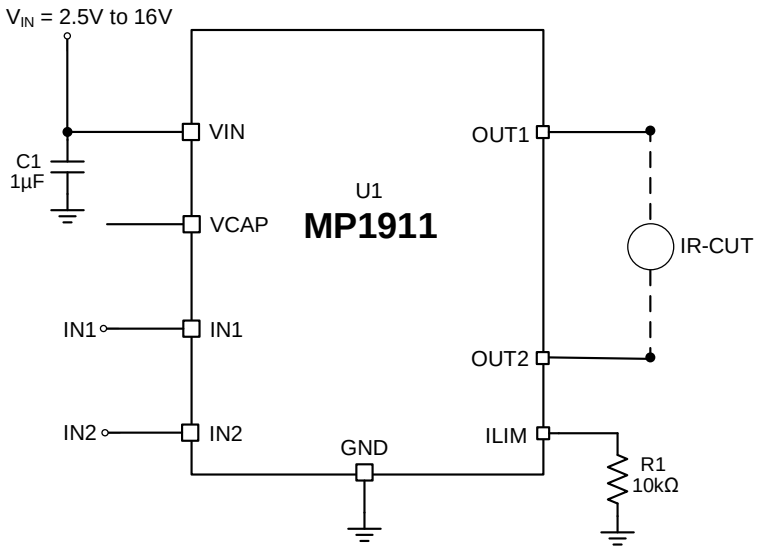
- Wide 2.5V to 16V Operating Input Voltage (V_{IN}) Range
- 1A of Continuous Output Current (I_{OUT})
- Low MOSFET On Resistance ($R_{DS(ON)}$) (Integrated 500mΩ High-Side MOSFET and Low-Side MOSFET)
- Output Modes: Forward, Reverse, Coast, Brake, and Sleep
- 50nA Sleep Mode Circuit Current when IN1 and IN2 are Pulled Low
- Thermal Shutdown
- External, Configurable, Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP)
- Available in an SOT583 Package

APPLICATIONS

- Infrared-Cut (IR-Cut) Cameras
- Smart Meters
- Smart Locks

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP1911GTL	SOT583	*See Below*	1

* For tape & reel, add suffix -Z (e.g. MP1911GTL-Z).

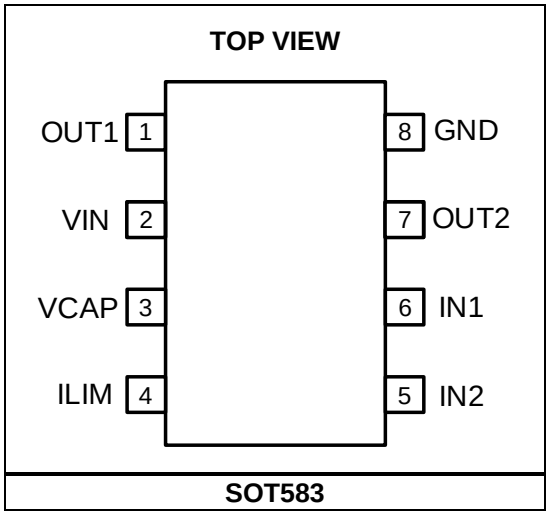
TOP MARKING

BKCY

LLL

BKC: Product code of MP1911GTL
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	OUT1	**Switch output 1.** Connect the OUT1 pin to the winding.
2	VIN	**Supply voltage.** An input capacitor is required to prevent large voltage spikes at the input.
3	VCAP	**Charge pump output.** For switching applications, connect a 100nF ceramic capacitor to VIN. For non-switching applications, the VCAP pin can remain open.
4	ILIM	**Current limit configuring resistor.** Connect a resistor to ground to set the current limit (I_{TRIP}).
5	IN2	**Input 2.** Internal pull-down resistor.
6	IN1	**Input 1.** Internal pull-down resistor.
7	OUT2	**Switch output 2.** Connect the OUT2 pin to the winding.
8	GND	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +18V
V_{OUTx} .....-0.3V to V_{IN} +0.3V
VCAP .....-0.3V to V_{IN} +4V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (4)
..... 1.78W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.5V to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

SOT583
EV1911-TL-00A (4) ..... 70 ..... 13... °C/W
JESD51-7 (5) ..... 100 ..... 63... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EV1911-TL-00A, a 2-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C [6], typical values are tested at T_J = 25°C, over-temperature limit is derived by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Operating supply current	I_Q	50kHz pulse-width modulation (PWM), float OUTx		0.4	0.6	mA
		100Hz PWM, float OUTx		0.2	0.3	mA
Sleep mode supply current	I_S	IN1 = IN2 = 0V		50		nA
Under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_R}$	50kHz PWM, float OUTx	1.6	1.7	1.8	V
UVLO hysteresis threshold	$V_{IN_UVLO_HYS}$	50kHz PWM, float OUTx		100		mV
IN1 and IN2						
Input high voltage	V_{IH}		1.1			V
Input low voltage	V_{IL}				0.4	V
Input high current	I_{IH}	IN1 = IN2 = 3.3V			50	µA
Input low current	I_{IL}	IN1 = IN2 = 0V	-5		+5	µA
Input pull-down resistance	R_{PD}			100		kΩ
Power MOSFETs						
High-side MOSFET (HS-FET) on resistance [7]	$R_{DS(ON)_HS}$	I_{OUT} = 100mA, T_A = 25°C		0.25		Ω
Low-side MOSFET (LS-FET) on resistance [7]	$R_{DS(ON)_LS}$	I_{OUT} = 100mA, T_A = 25°C		0.25		Ω
ILIM						
Minimum off time [7]	t_{ITRIP_MIN}			5		µs
Maximum off time [7]	t_{ITRIP_MAX}			30		µs
ILIM sense ratio	I_{LIM_SR}		74	80	86	µA/A
Current trip voltage rising threshold	V_{ITRIP_R}		1.18	1.21	1.24	V
Current trip voltage falling threshold	V_{ITRIP_F}		0.94	0.97	1	V
Sleep entry time	t_{SLP_ENTRY}	IN1 = IN2 = 0V		1	2	ms
Sleep recovery time	$t_{SLP_RECOVERY}$	IN1 or IN2 or both = high			230	µs
OUT1 and OUT2						
Output enabled time	t_1 [8]				200	ns
Output disabled time	t_2 [8]				300	ns
Delay time	t_3 [8]				270	ns
	t_4 [8]				450	ns
Output rise time	t_{O_R}				220	ns
Output fall time	t_{O_F}				170	ns
Dead time (DT)	t_{DT}			150		ns
Thermal Protection						
Thermal shutdown threshold [7]	T_{TSD}			150		°C
Thermal shutdown hysteresis [7]	T_{SD_HYS}			30		°C

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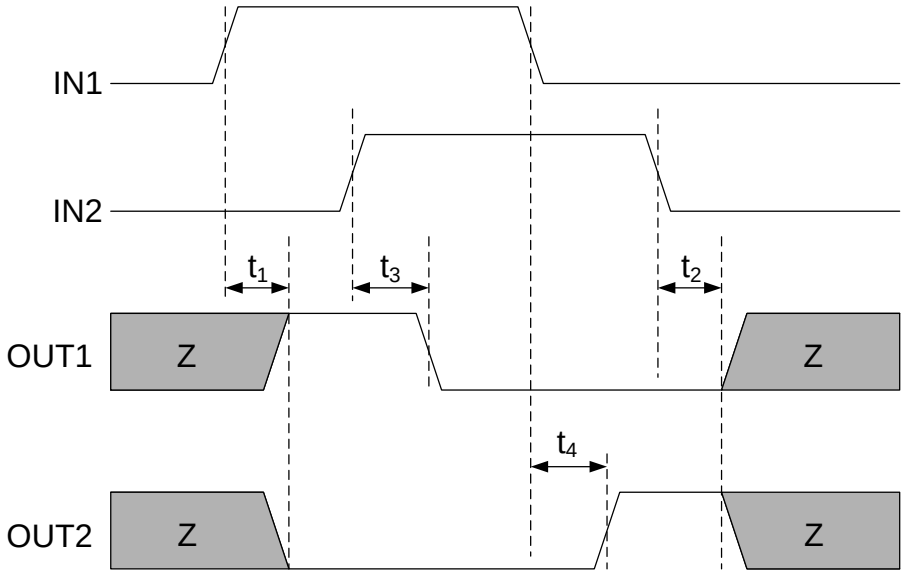


Figure 1: Input and Output Timing Diagram

Notes:

6) Not tested in production. Derived by over-temperature correlation.
7) Derived by sample characterization. Not tested in production.
8) See Figure 1.

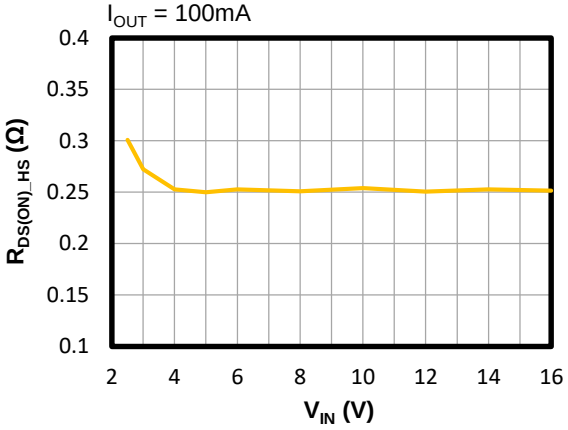
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TYPICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

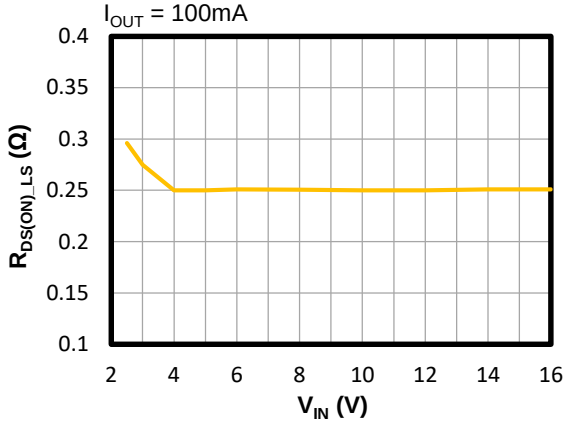
HS-FET On Resistance vs. Input Voltage

I_{OUT} = 100mA

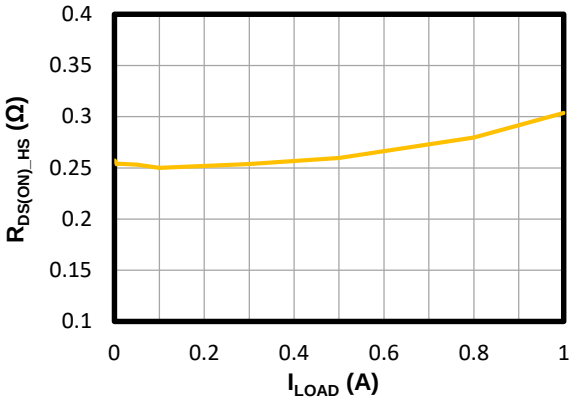


LS-FET On Resistance vs. Input Voltage

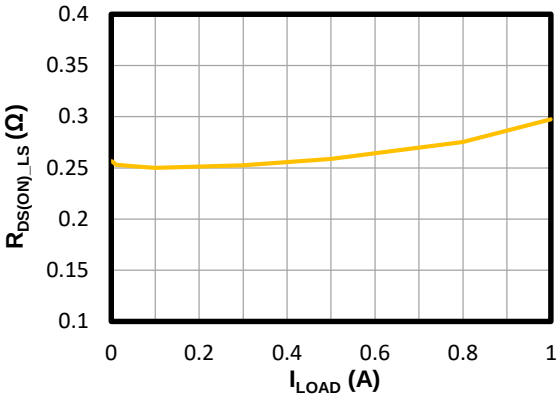
I_{OUT} = 100mA



HS-FET On Resistance vs. Load Current

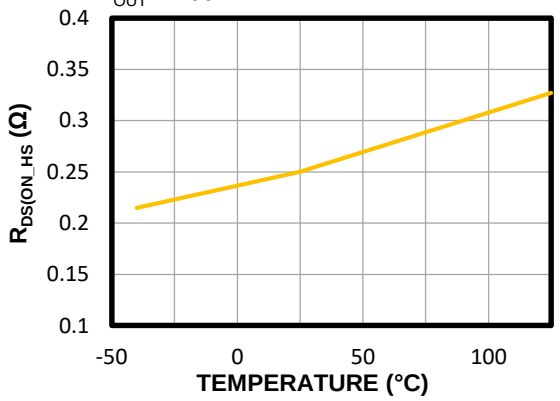


LS-FET On Resistance vs. Load Current



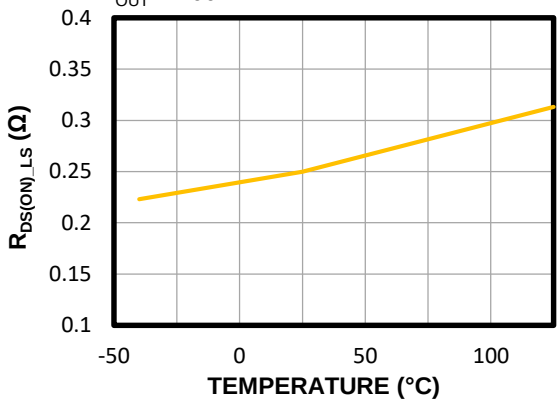
HS-FET On Resistance vs. Temperature

I_{OUT} = 100mA



LS-FET On Resistance vs. Temperature

I_{OUT} = 100mA

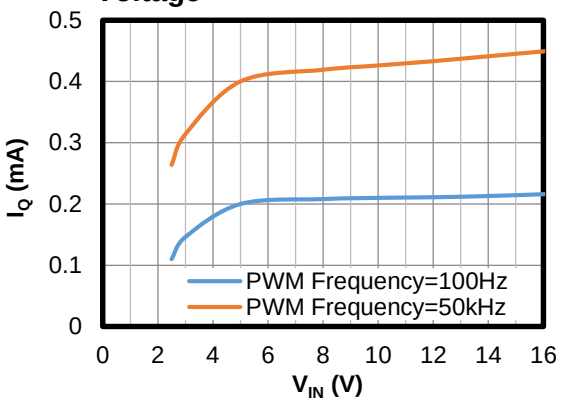


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TYPICAL CHARACTERISTICS *(continued)*

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Quiescent Current vs. Input Voltage



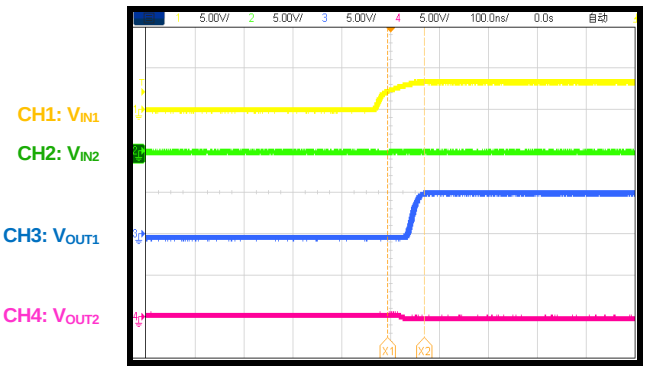
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

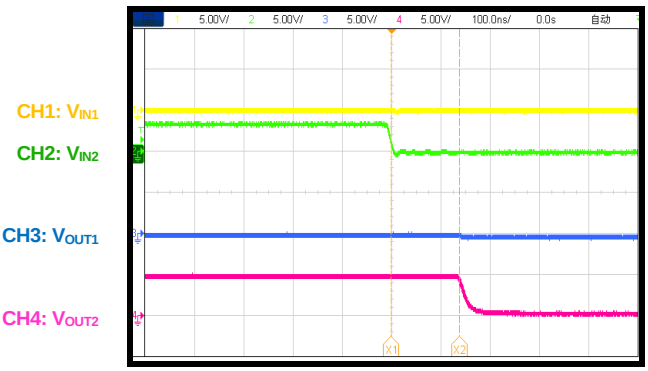
Output Enabled Time (t_1)

No load



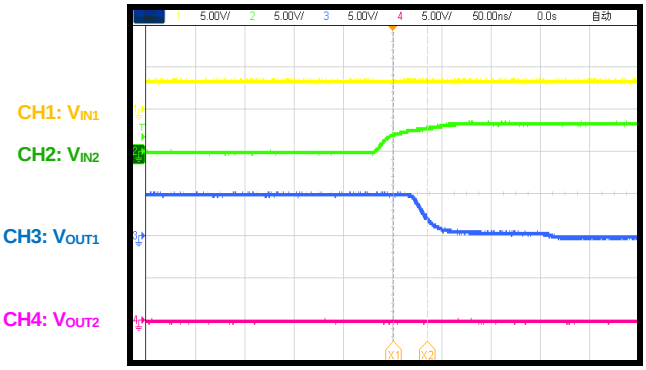
Output Disabled Time (t_2)

No load



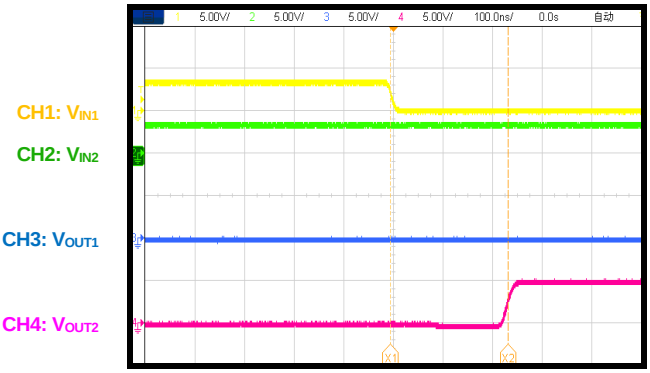
Propagation Delay Time (t_3)

No load



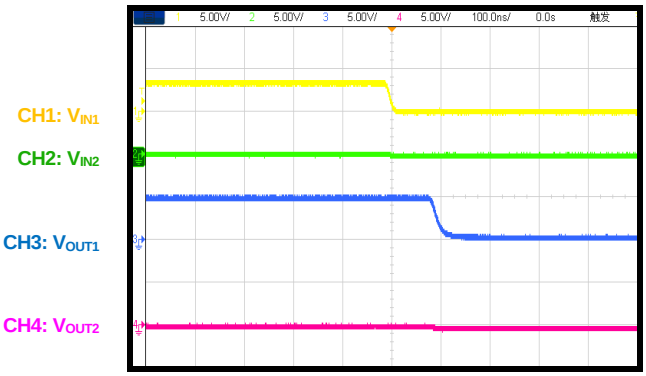
Propagation Delay Time (t_4)

No load



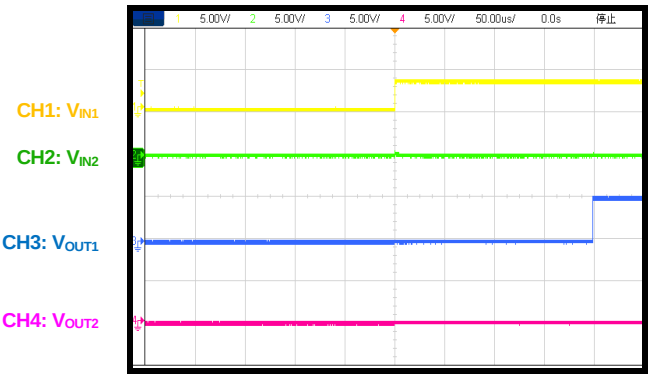
Sleep Mode Entry

No load



Sleep Mode Recovery

No load



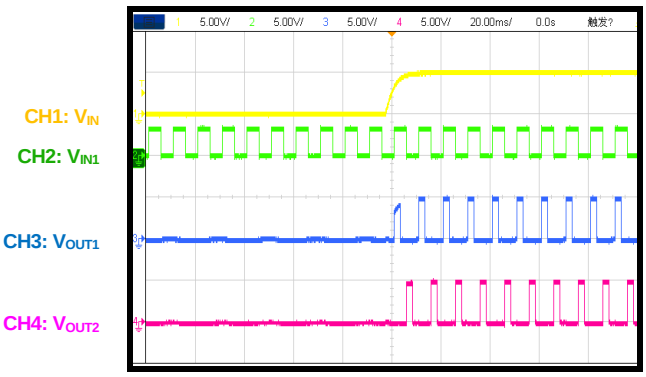
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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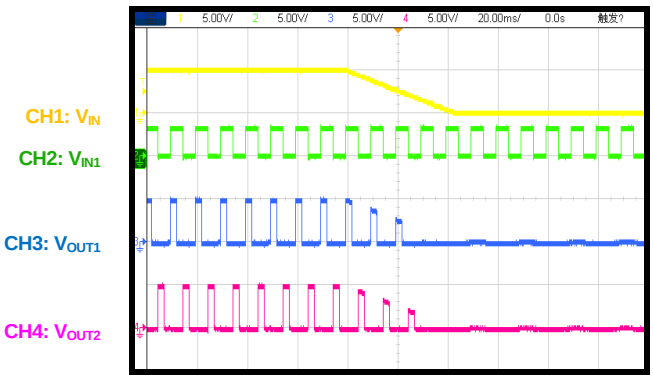
Power Start-Up

IN1 = IN2 = 100Hz, no load



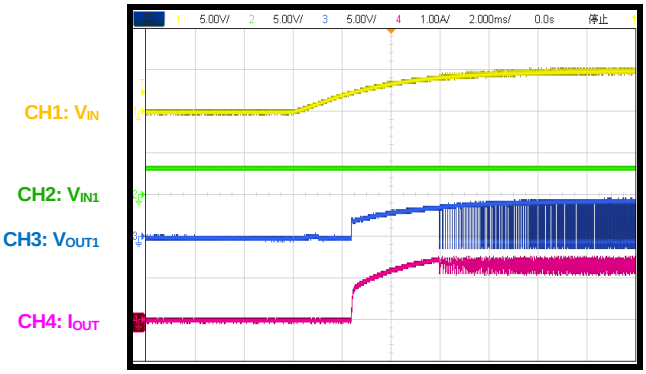
Power Shutdown

IN1 = IN2 = 100Hz, no load



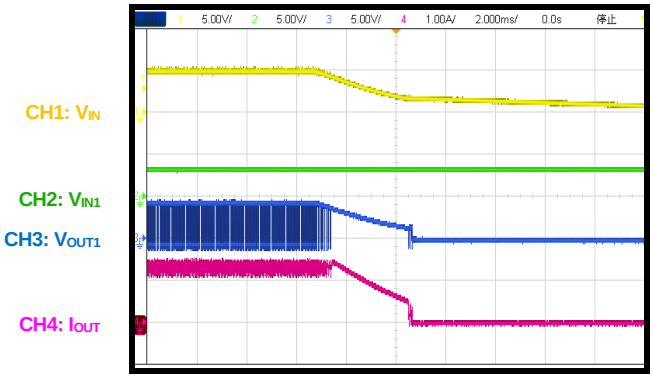
Power Start-Up

IN1 = high, IN2 = low, 2Ω + 100μH load



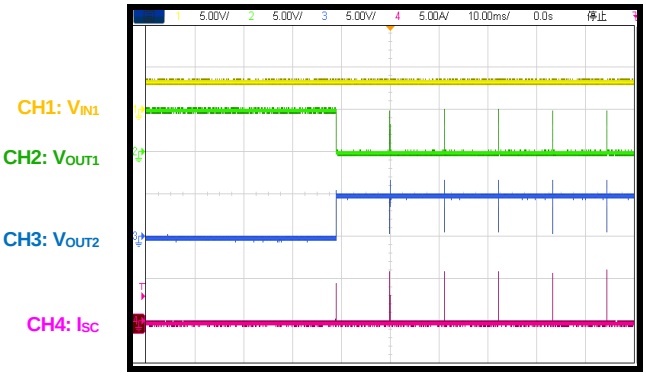
Power Shutdown

IN1 = high, IN2 = low, 2Ω + 100μH load



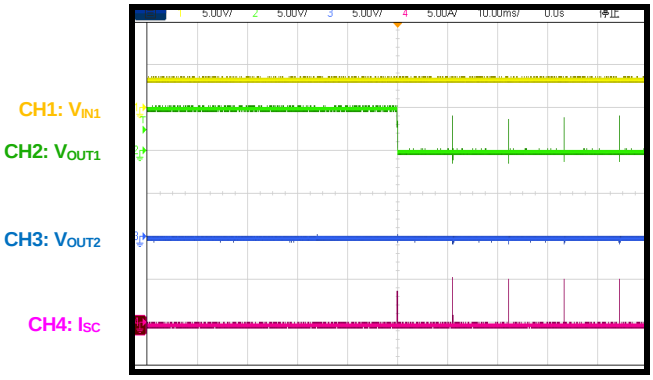
SCP to OUT Short to VIN

IN1 = high, IN2 = low



SCP to OUT Short to GND

IN1 = high, IN2 = low



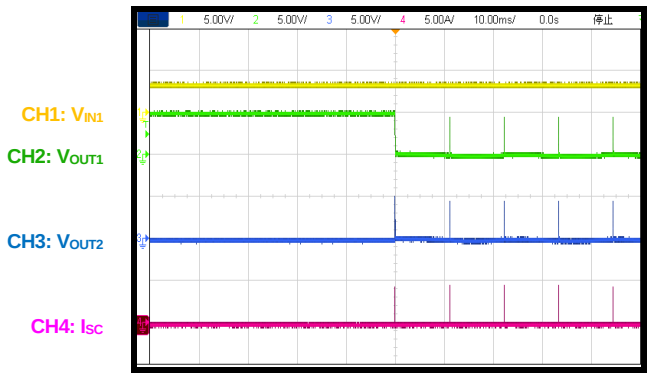
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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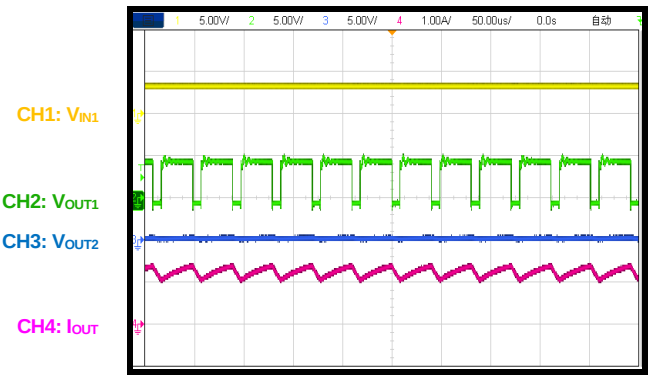
SCP OUT Short to OUT

IN1 = high, IN2 = low



Steady State

IN1 = high, IN2 = low, 2Ω + 100μH load



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FUNCTIONAL BLOCK DIAGRAM

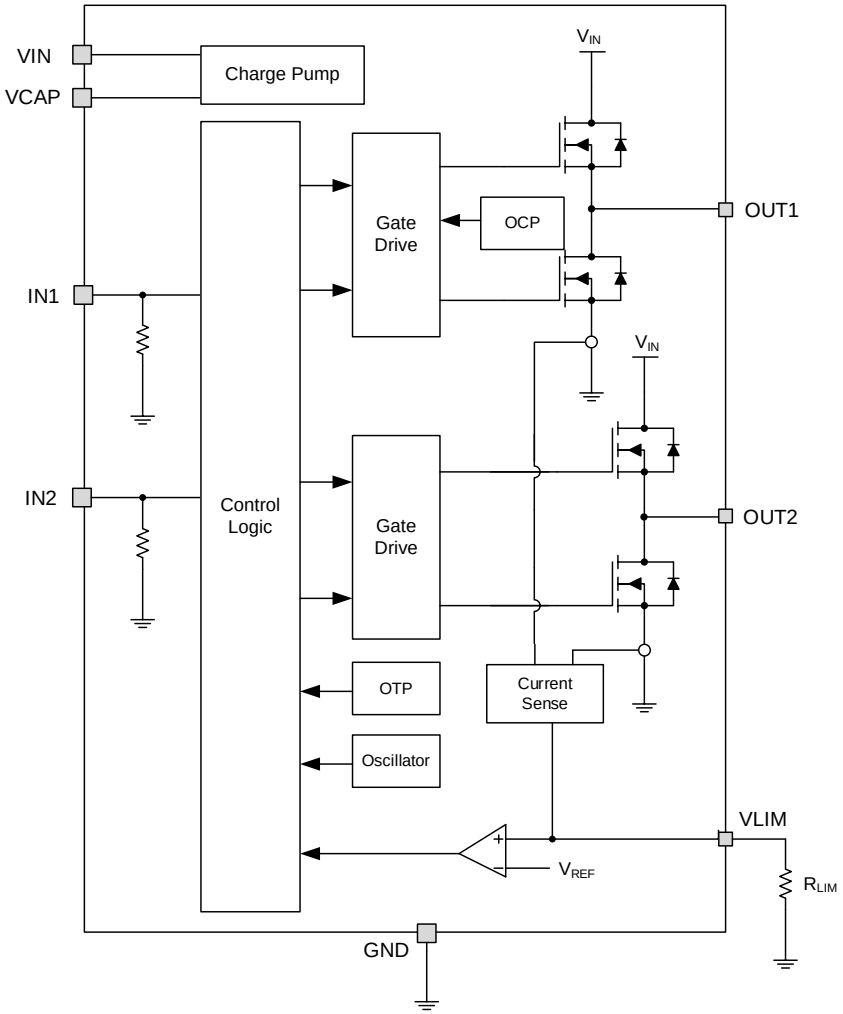


Figure 2: Functional Block Diagram

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OPERATION

The MP1911 is an H-bridge driver. The H-bridge consists of four N-channel power MOSFETs and an internal charge pump to generate the required gate-drive voltages.

Input Logic

The MP1911 is controlled by two input pins, IN1 and IN2. The two on/off inputs control the different output modes: forward, reverse, coast, brake, or sleep. Table 1 shows the MP1911's input logic.

Table 1: Input Logic Truth Table

IN1	IN2	OUT1	OUT2	Function (IR-CUT)
L	L	Hi-Z	Hi-Z	Sleep/coast
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

Sleep Mode

If IN1 and IN2 remain low for more than a set time (typically 1ms), then the MP1911 enters a low-power sleep mode. In this state, all internal circuits, including the gate drive charge pump, are disabled and the H-bridge outputs turn off. If either IN1 or IN2 are pulled high, the IC exits sleep mode.

Current Sense (CS)

An internal current-sense (CS) circuit detects the current flowing into the two low-side MOSFETs (LS-FETs). Connect a resistor from ILIM to ground to set the current limit (I_{TRIP}).

For 1A of output current (I_{OUT}), 80µA of current is sourced into the resistor connected to ILIM. For example, if a 10kΩ resistor is connected between ILIM and ground, then the output voltage (V_{OUT}) on the ILIM voltage (V_{ILIM}) is 0.8V/A of I_{OUT}.

The current is sensed when one of the LS-FETs turns on, including during slow decay (brake) mode.

Current Limit and Regulation

The current in the outputs is limited using constant-off-time pulse-width modulation (PWM) control circuitry. The current limit operation follows:

A diagonal pair of MOSFETs turns on and drives current through the load. The current increases in the load, which is sensed by the internal CS circuit.

If the load current (I_{LOAD}) reaches the current trip threshold, then the H-bridge switches to slow decay mode and the two LS-FETs turn on.

After a fixed minimum off time (t_{ITRIP_MIN}), if I_{LOAD} falls at least 20% below the I_{TRIP} threshold, then the MOSFETs are re-enabled and the cycle repeats. If I_{LOAD} remains above 80% of the I_{TRIP} threshold, then the off time is extended until I_{LOAD} falls to 20% below the threshold.

If I_{LOAD} does not drop below the falling threshold within the maximum off time (t_{ITRIP_MAX}), then the H-bridge exits slow decay mode and resumes normal operation to avoid audible noise.

When V_{ILIM} reaches 1.2V, the I_{TRIP} threshold is triggered. For example, with a 10kΩ resistor from ILIM to ground, V_{ILIM} is 0.8V/A of I_{OUT}. Therefore, when the current reaches 1.5A, V_{ILIM} reaches 1.2V and a current trip occurs.

Figure 3 shows the current limit operation.

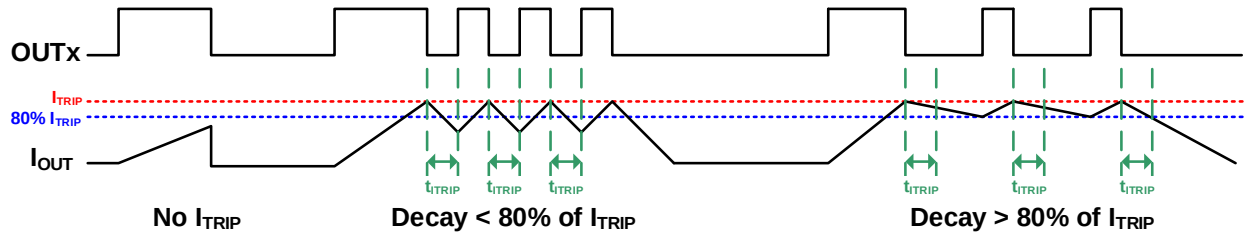


Figure 3: Current Limit Operation

Short-Circuit Protection (SCP)

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If there is a dead short from OUTx to GND or VDD, then the current in the H-bridge high-side MOSFET (HS-FET) or LS-FET increases rapidly to trigger the secondary current limit protection threshold. Under this condition, all MOSFETs turn off for 10ms to prevent damage to the H-bridge MOSFET. After the 10ms off time completes, the IC resumes normal operation. The IC repeats this behavior if the dead-shorted condition is not removed.

Thermal Shutdown

The MP1911 also integrates thermal monitoring. If the die temperature exceeds 150°C, all switches turn off. Once the die temperature drops to a safe level, operation resumes automatically.

Under Voltage Lockout (UVLO)

If V_{IN} falls below the under-voltage lockout (UVLO) threshold, all circuitries in the device are disabled and the internal logic resets. Operation resumes when V_{IN} exceeds the UVLO threshold.

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APPLICATION INFORMATION

External Component Selection

Place a 1µF, ceramic X7R capacitor as close to the IC as possible to bypass the VIN pin to GND. For non-switching applications, the VCAP pin can remain open. For switching applications, a 100nF ceramic capacitor is required from VIN to VCAP. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the input capacitor as close to VIN and GND as possible.
2. Place the capacitor (C2) as close to VIN and VCAP as possible.
3. Maximize the VIN and GND copper plane to minimize the thermal resistance.

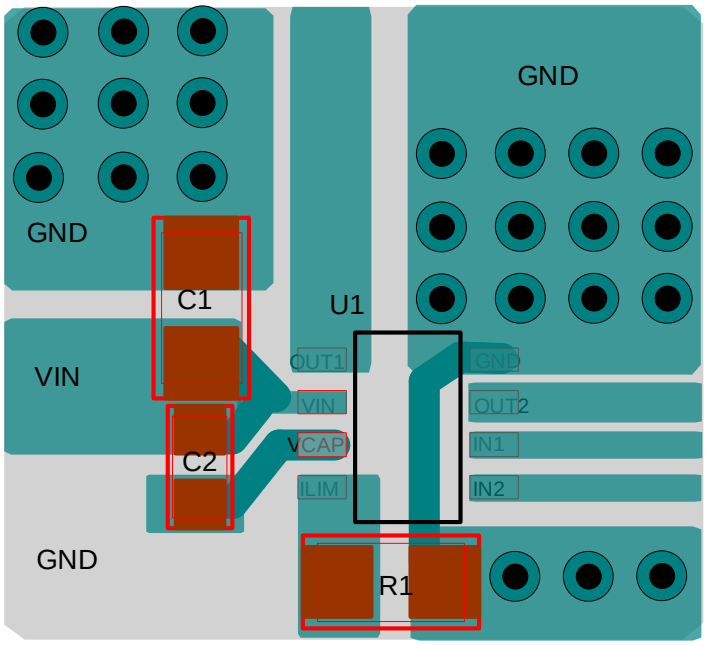


Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

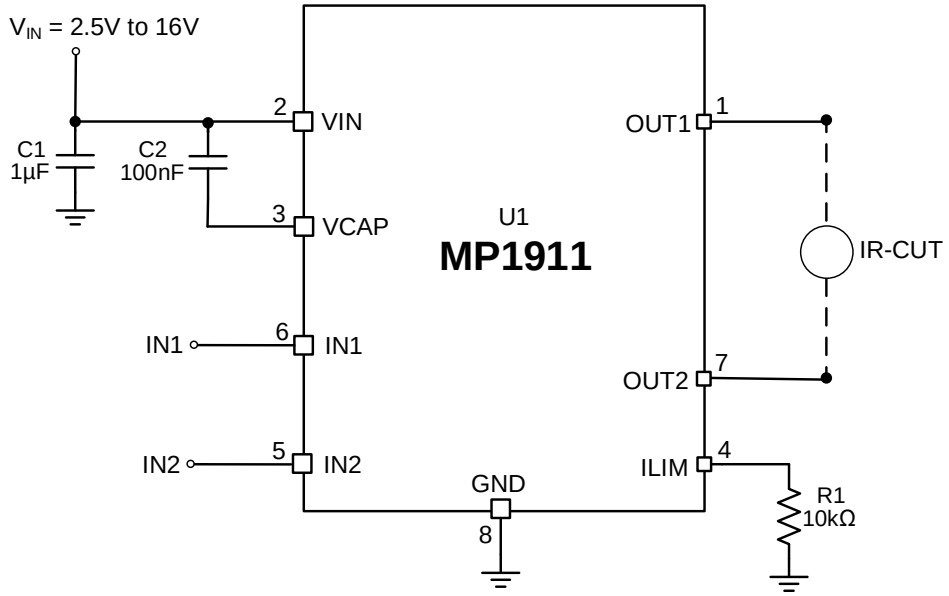
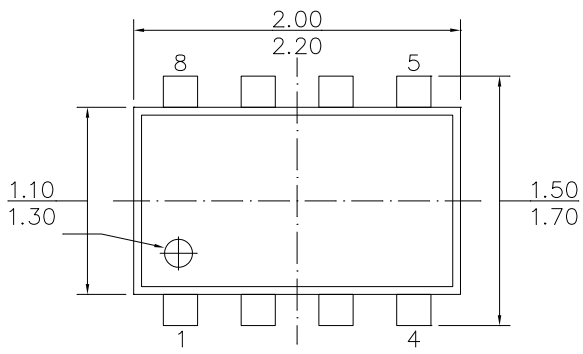


Figure 5: Typical Application Circuit

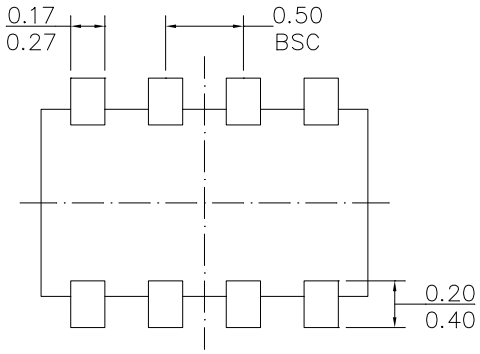
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PACKAGE INFORMATION

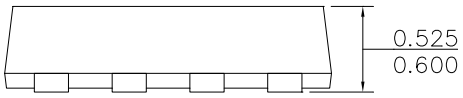
SOT583 (1.6mmx2.1mm)



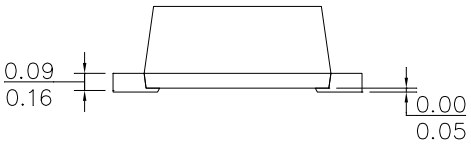
TOP VIEW



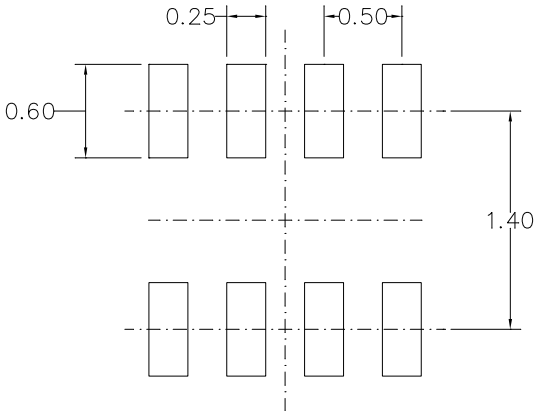
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



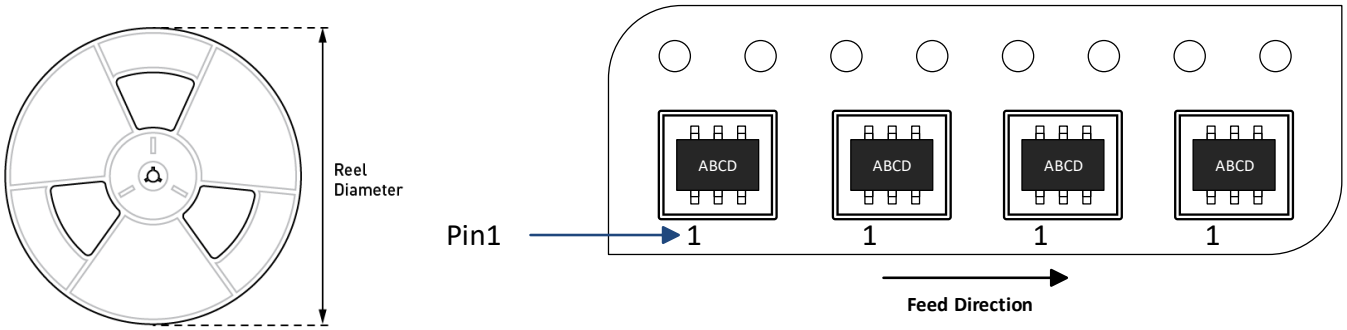
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
3) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
4) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP1911GTL-Z	SOT583 (1.6mmx2.1mm)	5000	N/A	N/A	7in	8mm	4mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/20/2022	Initial Release	-

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