EV8049S-U-00A

24V 5.5A Quad Channel Power Half-Bridge Evaluation Board

The Future of Analog IC Technology

GENERAL DESCRIPTION

The EV8049S-U-00A is the evaluation board for the MP8049S, a high current, quad channel power half-bridge. It accepts PWM modulated inputs for operation that that can be configured as the stereo BTL output stage of a Class-D audio amplifier.

The MP8049S features a low current shutdown mode, standby mode, input under voltage protection, current limit, thermal shutdown and fault flag signal output. All channels of drivers interface with standard logic signals.

The MP8049S is available in a 40 lead QFN 5X5 package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	5 – 26	V
Peak Output Current	I_{PEAK}	5.5	A

FEATURES

- 5V to 26V VDD
- ±5.5A Peak Current Output
- Up to 1MHz Switching Frequency
- Protected Integrated Power 0.14Ω Switches
- 10ns Switch Dead Time
- All Switches Current Limited
- Internal Under Voltage Protection
- Internal Thermal Protection
- Short-circuit Protection
- Fault Output Flag
- Bridge Tied Load Output Power: 37W/Channel at 24V, 8Ω Applications

APPLICATIONS

- Flat TV
- Home Theaters
- DVD Receivers

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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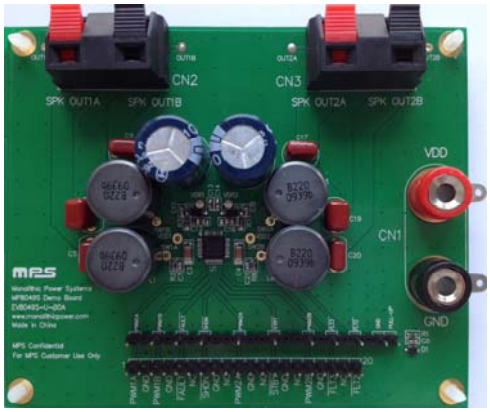
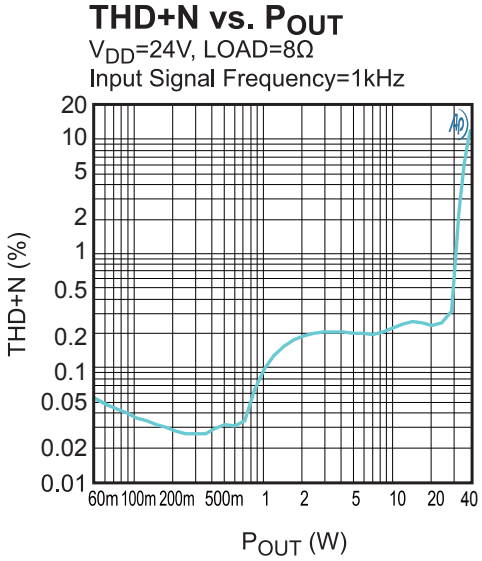
EV8049S-U-00A EVALUATION BOARD



(L x W x H) 4.0" x 3.3" x 1.32"

(10.2cm x 8.4cm x 3.4cm)

Board Number	MPS IC Number
EV8049S-U-00A	MP8049SDU



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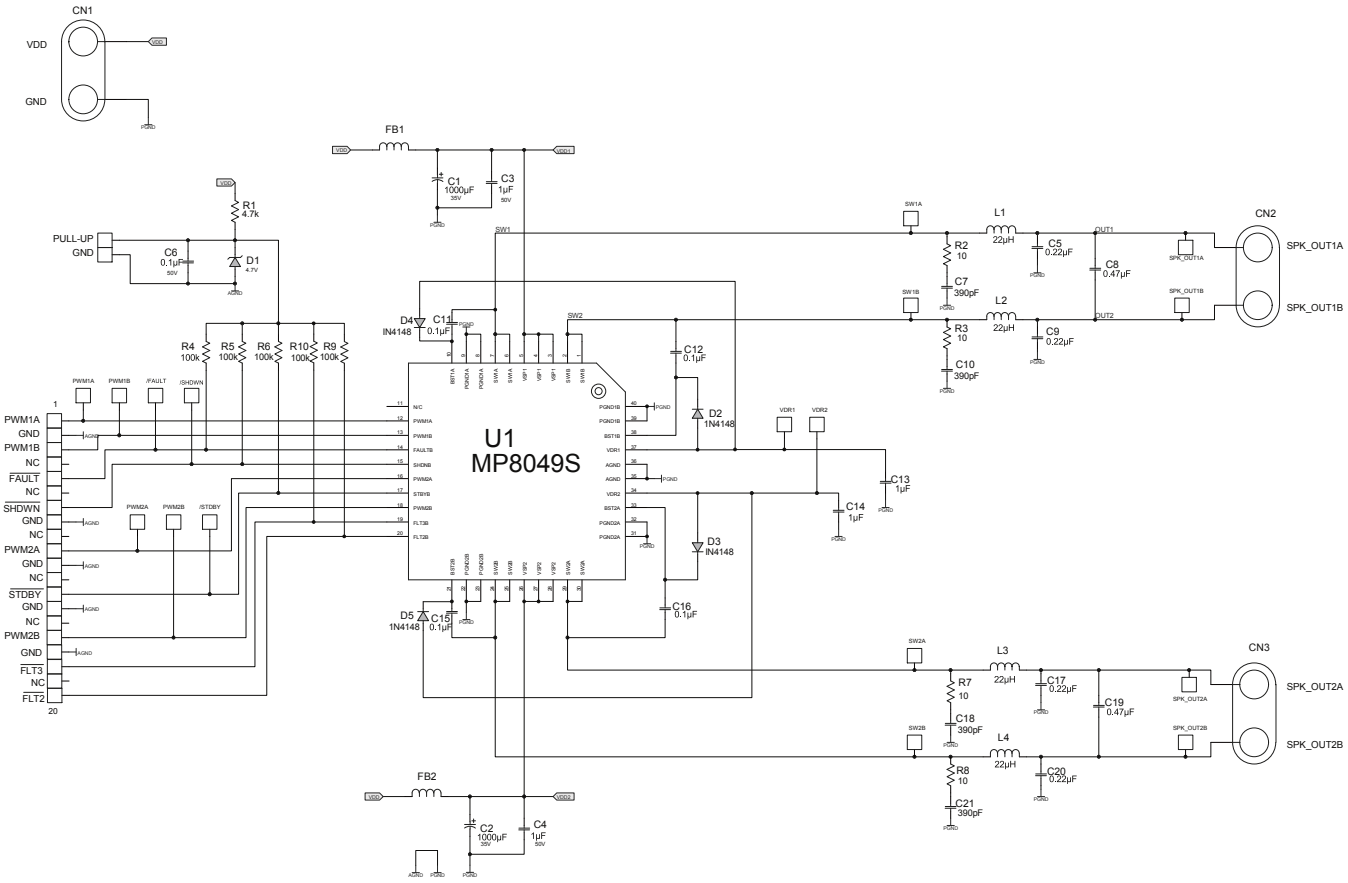
EVALUATION BOARD SCHEMATIC



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EV8049S-U-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Part Number
2	C1, C2	1000uF	CAP/1000UF/RADIAL/35V	Radial	JIANG HAI	CD263-35V1000
2	C3, C4	1μF	CAP/1UF/1206/50V/X7R	1206	TDK	C3216X7R1H105K
4	C5, C9 C17, C20	0.22μF	CAP/0.22UF/FILM/50V	Radial	PANASONIC	ECQV1H224JL
1	C6	0.1μF	CAP/0.1UF/0603/50V/X7R	0603	TDK	C1608X7R1H104K
4	C7, C10 C18, C21	390pF	CAP/390pF/0603/50V/X7R	0603	TDK	C1608COG1H391J
2	C8, C19	0.47μF	CAP/0.47UF/FILM/50V	Radial	PANASONIC	ECQV1H474JL
4	C11, C12 C15, C16	0.1μF	CAP/0.1UF/0805/50V/X7R	0805	TDK	C2012X7R1H104K
2	C13, C14	1μF	CAP/1UF/0603/25V/X7R	0603	muRata	GRM188R7E105KA12 D
1	R1	4.7k	RES/4.7K/0603/5%	0603	YAGEO	RC0603JR-074K7L
4	R2, R3 R7, R8	10	RES/10/0603/1%	0603	YAGEO	RC0603FR-0710RL
5	R4, R5 R6, R9 R10	100k	RES/100K/0603/1%	0603	YAGEO	RC0603FR-07100KL
1	D1	4V7	SOD323/BZT52C4V7S-7	SOD-323	DIODES	BZT52C4V7S
4	D2,D3 D4, D5	IN4148W	1N4148W-7/SOD123	SOD-123	DIODES	1N4148W
2	FB1, FB2	6A	FERRITE/BEAD	1206	muRata	BLM31PG330SH1L
4	L1, L2 L3, L4	22μH	3.26A/22uH/INDUCTOR	Radial	TOKO	13RHBP-A7502BY-220M
2	CN1	VDD	BANANA CONNECTOR	Radial	ANY	
		GND	BANANA CONNECTOR	Radial	ANY	
2	CN2, CN3	CONN	SPEAKER TERMINAL	Radial	ANY	
2	I/O	CONN	SIP 2.54mm * 40 PIN	Radial	ANY	
1	U1	MP8049S	CLASS D POWER STAGE	QFN40_5*5	MPS	MP8049SDU

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PRINTED CIRCUIT BOARD LAYOUT

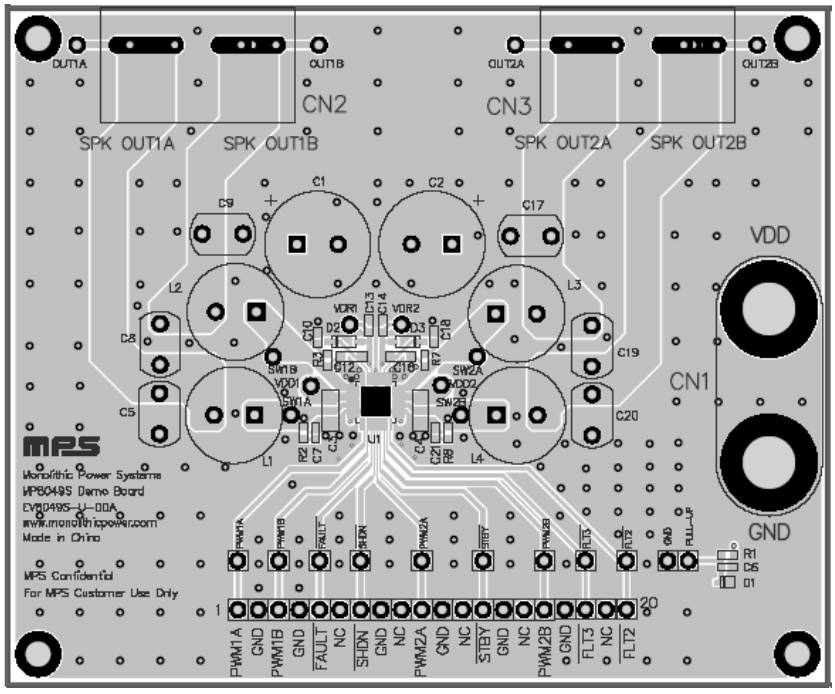

Figure 1—Top and Top Silk Layer

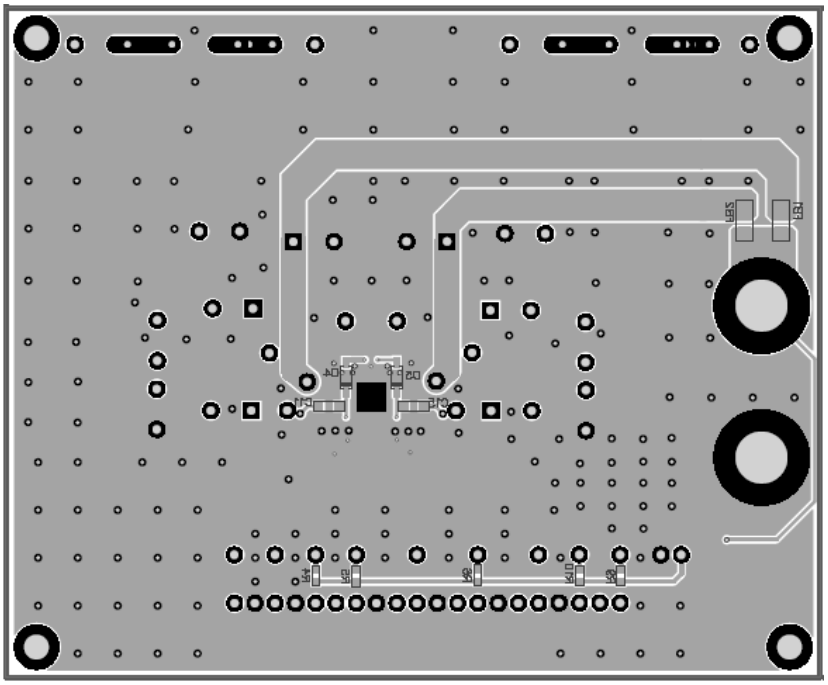

Figure 2— Bottom and Bottom Silk Layer

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QUICK START GUIDE

The EV8049S-U-00A comes pre-configured to operate as a stereo BTL (Bridge-Tied Load) audio power driver, where a complementary PWM modulated audio signal (PWM and $\overline{PWM}$) is used an input, and music is played to speakers connected to the outputs. Please follow the steps in the Quick Start Guide for Stereo BTL Operation section.

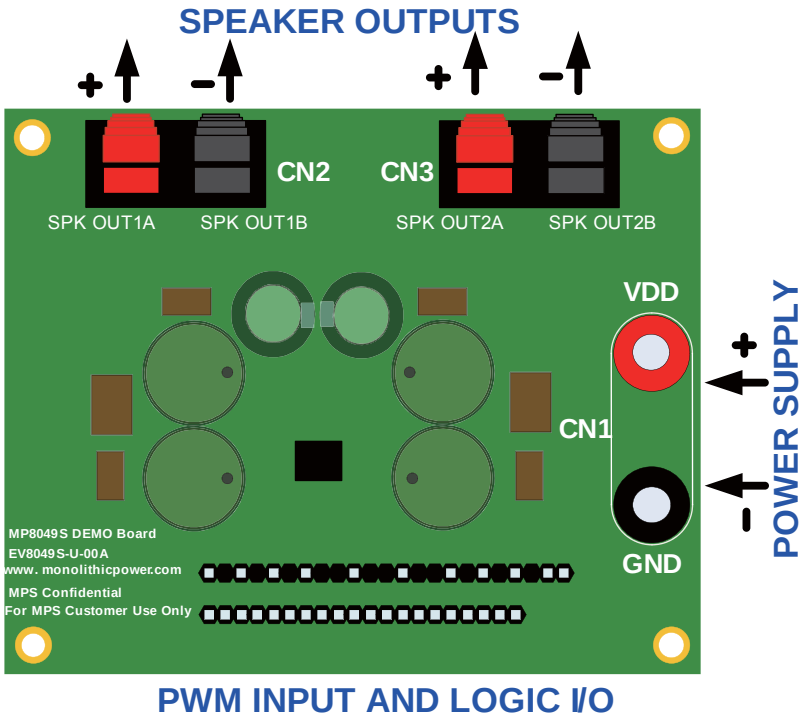

Figure 3 EV8049S-U-00A Connection Diagram

Quick Start Guide for Stereo BTL Operation

Input/Output Requirements

1. Power supply (CN1): 5V to 26V.
2. Complementary PWM Signal Source (PWM, $\overline{PWM}$).
3. Speaker Load (CN2 and CN3): 6Ω to 8Ω.

Setup Condition for Operation

4. Connect the speakers between SPK_OUT1A and SPK_OUT1B, SPK_OUT2A and SPK_OUT2B terminals.
5. Connect a PWM signal source to PWM1A / PWM2A and the complementary signal source $\overline{PWM}$ to PWM1B / PWM2B, respectively. Use the GND terminal between PWM1A and PWM1B / PWM2A and PWM2B as the ground connection for the PWM inputs.
6. Apply power to the board.
7. Audio should be heard through the speakers.

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Instructions for PWM Input and Logic I/O

PIN	I/O	DESCRIPTION				
PWM1A PWM1B PWM2A PWM2B	INPUT	Accept TTL LEVEL PWM signal for driving each of the half bridge				
SHDNB	INPUT	Active low, pull low to shut off the MP8049S				
STBYB	INPUT	Active low, pull low to enter standby mode (turn all the switches to high impedance)				
FAULTB	OUTPUT	FAULTB will be pull low once OCP or OTP is triggered				
FLTB2 FLTB3	OUTPUT	Error reporting, details please refer to the below table				
		FLTB2	FLTB3	OCP	OTP	UVP
		1	1	0	0	0
		0	1	0	0	1
		1	0	0	1	0
		0	0	1	0	0

Note: for more details, please find the datasheet of MP8049S.

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