MP2658

36V, Standalone Switching Charger with Integrated MOSFETs for Multi-Cell Series Battery Pack

DESCRIPTION

The MP2658 is a highly integrated switching charger designed for portable devices with different battery chemistries. The MP2658 supports up to 7-cell series Li-ion, Li-polymer, and $LiFePO_4$ battery packs. It also supports lead-acid, super capacitor, NiMH, and NiCd battery packs from 2V to 31V. The device achieves up to 3A of charge current (I_{CC}) with any battery regulation voltage (V_{BATT_REG}).

The device operates under a maximum 36V DC input voltage and hold-off voltage up to 45V. When an input power supply is present, the MP2658 charges the battery with four phases: trickle charge, pre-charge, constant current (CC) charge, and constant voltage (CV) charge.

The device can be configured to different pre-charge to fast charge thresholds and different charge termination modes via the external pins. This allows the MP2658 to support super capacitor charging, as well as charging for different battery chemistries.

Power management is based on the input current (I_{IN}) and input voltage (V_{IN}). If I_{IN} exceeds the preset input current limit, or if V_{IN} drops to the preset input voltage limit, the MP2658 automatically decreases the charge current to protect the input power supply from an overload.

To guarantee safe operation, the MP2658 offers robust protection features such as battery over-voltage protection (OVP), battery temperature sensing and protection, thermal shutdown, and a charging safety timer.

The MP2658 is available in a QFN-19 (3mmx3mm) package.

FEATURES

- Up to 36V Operating Input Voltage (V_{IN})
- 45V Max Sustainable Voltage when Not Switching
- Up to 3A of Charge Current (I_{CC})
- Supports Any Battery Regulation Voltage (V_{BATT_REG}) from 2V to 31V
- 0.5% V_{BATT_REG} Accuracy
- Integrated Input Current (I_{IN}) Sensing and Reverse Blocking FET
- Internal Loop Compensation
- I_{IN} Limit Regulation
- Minimum V_{IN} Regulation
- Charge Operation Indicator
- Dead Battery Pack Recovery
- Battery Over-Voltage Protection (OVP)
- Charge Safety Timer
- Battery NTC Thermal Monitor
- Available in a QFN-19 (3mmx3mm) Package

APPLICATIONS

- Industrial Medical Equipment
- Power Tools
- Robots and Portable Vacuum Cleaners
- Wireless Speakers
- Walkie Talkies
- Surveillance Systems

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TYPICAL APPLICATION

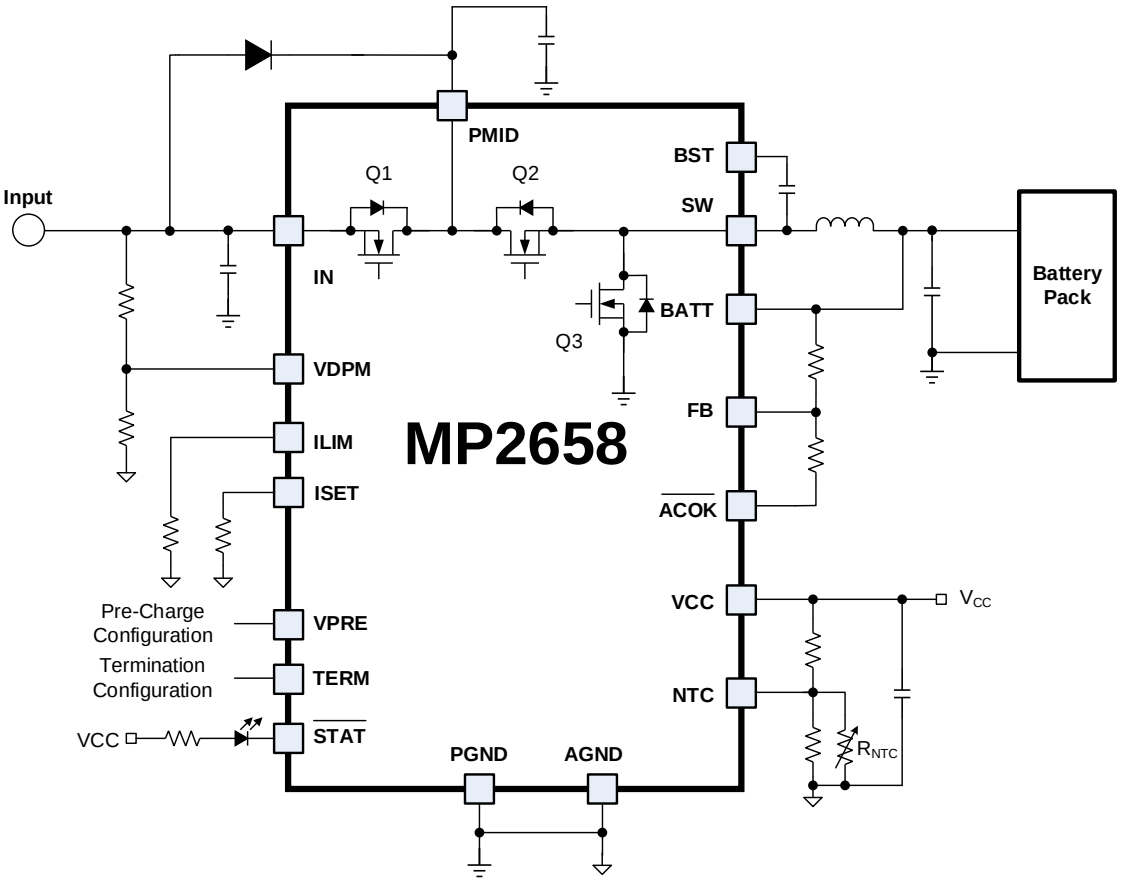

Figure 1: Typical Application

VPRE Pin Connection	Pre-Charge to Fast Charge Threshold (V_{BAT_PRE}) (1)
AGND	70% of V_{BATT_REG}
Float	75% of V_{BATT_REG}
Pull up to VCC	Disable pre-charge
100kΩ resistor to AGND	50% of V_{BATT_REG}

TERM Pin Connection	Termination Current Enable/Disable
AGND	Enable termination
Pull up to VCC	Disable termination
100kΩ resistor to AGND	Disable termination, battery floating voltage is 94% of V_{BATT_REG}

Note:

1) The pre-charge to fast charge threshold (V_{BAT_PRE}) is a percentage of V_{BATT_REG}, and it has the same ratio as $V_{FB_REF_BATPRE}$, which is also a percentage of V_{BATT_REG} in the EC table.

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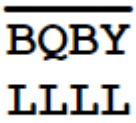
ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2658GQ-xxxx**	QFN-19 (3mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP2658GQ-xxxx-Z).

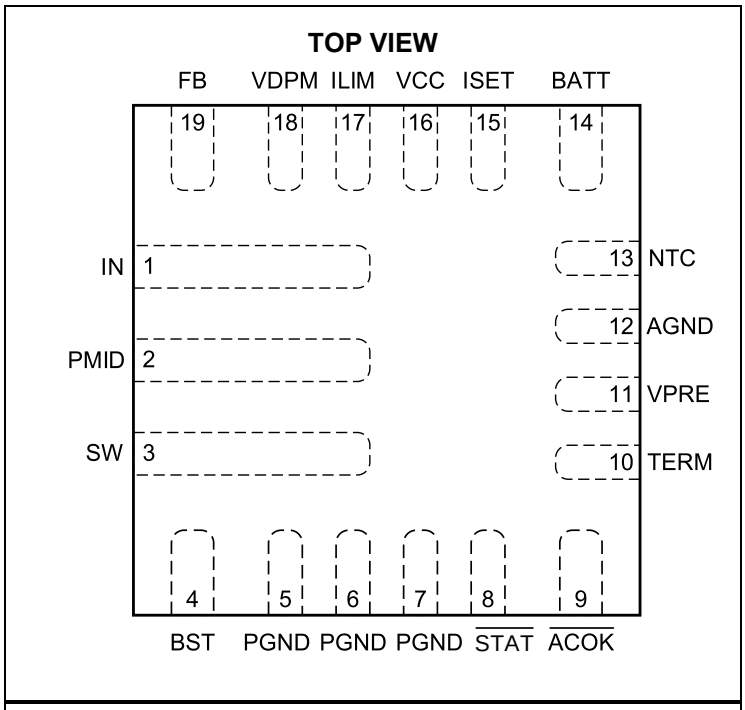
** “xxxx” is the OTP setting option. The factory default is “0000”. This content can be viewed in the one-time programmable (OTP) memory map. Contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING



BQB: Product code of MP2658GQ
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-19 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Type	Description
1	IN	Power	**Power input.** Place a 1µF capacitor from IN to PGND. See the Application Selecting the IN Capacitor (C_{IN}) section on page 17 for more details.
2	PMID	Power	**Decoupling capacitor of the power stage.** Bypass the PMID pin with a ceramic, 2.2µF capacitor connected from PMID to PGND, and placed as close as possible to the IC with the shortest route. Connect a 2A/40V Schottky diode from the IN pin to the PMID pin.
3	SW	Power	**Switching node.**
4	BST	Power	**Bootstrap pin.** Connect a 100nF bootstrap capacitor between the BST and SW pins to form a floating supply to drive the high-side MOSFET (HS-FET) above the supply voltage.
5, 6, 7	PGND	Power	**Power ground.**
8	$\overline{\text{STAT}}$	O	**Status indication.** This pin indicates the charging operation status and fault status with an open-drain output (see Table 4 on page 14).
9	$\overline{\text{ACOK}}$	O	**Battery voltage feedback ground input.** This pin is an open-drain output, active low. Connect the feedback resistor divider's low-side resistor to this pin. The input of this pin is in high impedance when an adapter is unplugged, or when the charger is disabled by the VDPM pin.
10	TERM	I	**Charge termination setting.** Charge termination is disabled if this pin is pulled up to VCC.
11	VPRE	I	**Pre-charge voltage setting.** The pre-charge phase is disabled if this pin is pulled up to VCC.
12	AGND	Power	**Analog ground.** Short AGND to PGND on the PCB.
13	NTC	I	**Temperature-sense input.** Connect a negative temperature coefficient (NTC) thermistor to the NTC pin. The hot and cold temperature windows can be configured with a resistor divider connected from VCC to NTC to AGND. Charging is suspended when the NTC pin's voltage is out of range.
14	BATT	Power	**Battery positive terminal.** Place a minimum 10µF capacitor from BATT to PGND. See the Selecting the BATT Capacitor (C_{BATT}) section on page 17 for more details.
15	ISET	I	**Charging current setting.** Connect a resistor from ISET to AGND.
16	VCC	Power	**Internal circuit power supply.** Bypass VCC to AGND with a 1µF ceramic capacitor. When an input source is present, a 5V output is generated on the VCC pin.
17	ILIM	I	**Input current limit setting.** Connect a resistor from ILIM to AGND.
18	VDPM	I	**Input voltage clamp setting.** Connect a resistor divider from VDPM to IN to AGND. This pin also can be used to disable charging when pulled down to logic low (below 0.2V).
19	FB	I	**Battery voltage feedback input.** Connect this pin to a resistor divider's middle-point to configure the battery charge voltage. When this pin is open by default, the converter stops switching.

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ABSOLUTE MAXIMUM RATINGS (2)

IN, PMID, FB, ACOK, BATT to PGND…….. …… -0.3V to +45V
SW to PGND .....-0.3V (-2V for 20ns) to +45V
BST to PGND…….. ..... SW to SW + 5.5V
All other pins to AGND..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (3) 2.5W
Junction temperature (T_J) ……150°C
Lead temperature (solder) .....260°C
Storage temperature…….. -65°C to +150°C

ESD Ratings

Human body model (HBM) (4).....±2000V
Charged-device model (CDM) (5).....±750V

Recommended Operating Conditions (6)

Supply voltage (V_{IN}) ..... 4.5V to 36V
Input current (I_{IN})..... Up to 3A
Charge current (I_{CHG}) ..... Up to 3A
Battery voltage (V_{BATT}) ..... 2V to 31V
Operating junction temp (T_J) .... -10°C to +125°C

Thermal Resistance (7) θ_{JA} θ_{JC}

QFN-19 (3mmx3mm) .....50.....12.... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per ANSI/ESDA/JEDEC JS-001.
5) Per JESD22-C101.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{BATT} = 14.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Power Characteristic						
IN under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	V_{IN} falling	3.3	3.6	3.9	V
IN UVLO threshold hysteresis		V_{IN} rising		420		mV
IN vs. BATT headroom	V_{HDRM}	V_{IN} rising (VHDRM bit = 0)	0.75	1.0	1.2	V
		V_{IN} falling (VHDRM bit = 0)	0.4	0.6	0.8	V
DC/DC Converter						
Input shutdown current	I_{IN_SHDN}	V_{IN} = 36V, VDPM = AGND,		550		µA
Input quiescent current	I_{IN_Q}	V_{IN} = 36V, charge is enabled, charge termination		1		mA
VCC low-dropout (LDO) output voltage	V_{CC}	V_{IN} = 24V	4.85	5	5.2	V
VCC LDO output current limit			50			mA
Blocking FET on resistance	R_{ON_Q1}			40		mΩ
High-side MOSFET (HS-FET) on resistance	R_{ON_Q2}			40		mΩ
Low-side MOSFET (LS-FET) on resistance	R_{ON_Q3}			56		mΩ
Peak current limit for HS-FET (Q2)	I_{HS_PK}	Constant current (CC) charge mode	4.8	5.4	6	A
		Pre-charge mode		3.4		A
Valley current limit for LS-FET (Q3)	I_{LS_VL}	CC charge mode		3.9		A
Negative current limit for LS-FET (Q3)	I_{LS_ZCD}		-1.6	-1.25	-0.9	A
Switching frequency	f_{SW}	f_{SW} = 680kHz	580	680	790	kHz
		f_{SW} = 350kHz	290	350	420	kHz
Battery Charger						
Trickle-charge to pre-charge threshold	V_{BATT_TC}	V_{BATT} rising	1.65	1.80	1.95	V
Trickle-charge hysteresis		V_{BATT} falling		400		mV
Pre-charge to fast-charge feedback rising threshold	$V_{FB_REF_BATPRE}$	Pre-charge to fast charge rising, as a percentage of $V_{FB_REF_BATREG}$, VPRE pin connected to AGND	68	70	72	%
		As a percentage of $V_{FB_REF_BATREG}$, VPRE pin floating	73	75	77	%
		As a percentage of $V_{FB_REF_BATREG}$, VPRE pin connected to 100kΩ to AGND	48	50	52	%
Pre-charge to fast-charge feedback hysteresis				9		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{BATT} = 14.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Battery feedback regulation voltage	$V_{FB_REF_BATREG}$		1592	1600	1608	V
Battery charge termination current	I_{TERM}	I_{TERM} = 200mA	100	200	300	mA
		I_{TERM} = 100mA	60	110	160	mA
Battery termination deglitch time	t_{TERM_DGL}			50		ms
Recharge feedback threshold	$V_{FB_REF_RECH}$	VRECH bit = 0, VPRE pin connected to AGND, V_{FB} falling, as a percentage of $V_{FB_REF_BATREG}$	92.8	93.8	94.8	%
		VRECH bit = 1, VPRE pin connected to AGND, V_{FB} falling, as a percentage of $V_{FB_REF_BATREG}$	96.0	97.0	98.0	%
		VPRE pin floating, V_{FB} falling, as a percentage of $V_{FB_REF_BATREG}$	87	88.5	90	%
Battery over-voltage protection (OVP) feedback threshold	$V_{FB_BATT_OVP}$	V_{FB} rising, as a percentage of $V_{FB_REF_BATREG}$	102.5	103.75	105.4	%
Battery OVP feedback threshold hysteresis				2		%
BATT leakage current in shutdown mode	I_{BATT_SHDN}	V_{BATT} = 28V, V_{IN} = PGND			10	µA
Charge current (8)	I_{CC}	R_{ISET} = 96kΩ	0.9	1	1.1	A
		R_{ISET} = 48kΩ	1.8	2	2.2	
Pre-charge current	I_{PRE}	V_{IN} = 24V, VPRE pin connected to AGND, V_{FB} = 1V, I_{TERM} = 200mA	100	200	300	mA
		V_{IN} = 24V, VPRE pin connected to AGND, V_{FB} = 1V, I_{TERM} = 100mA	60	110	160	mA
Trickle-charge current	I_{TC}	V_{IN} = 24V, V_{BATT} =1.5V, current in Q1		60		mA
Input Voltage (V_{IN}) and Input Current (I_{IN}) Regulation						
Input current limit	I_{IN_LIM}	R_{ILIM} = 96kΩ	0.9	1	1.1	A
		R_{ILIM} = 48kΩ	1.8	2	2.2	
Input minimum voltage regulation reference	$V_{IN_MIN_REF}$		1.18	1.2	1.22	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{BATT} = 14.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Thermal Regulation and Protection						
Thermal shutdown rising threshold (9)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (9)				20		°C
Battery Temperature Monitoring and Protection						
NTC cold temperature threshold	V_{TH_COLD}	V_{NTC} rising as a percentage of V_{CC}	70.3	71	71.8	%
NTC cold temperature threshold hysteresis		V_{NTC} falling as a percentage of V_{CC}		1.4		%
NTC hot temperature threshold	V_{TH_HOT}	V_{NTC} falling as a percentage of V_{CC}	47.5	48.2	49	%
NTC hot temperature threshold hysteresis		V_{NTC} rising as a percentage of V_{CC}		1.4		%
NTC float threshold	V_{TH_FLOAT}	V_{NTC} rising as a percentage of V_{CC}	90.2	91.1	92	%
Logic I/O Pin Characteristics						
STAT pin output voltage		I_{SINK} = 5mA			0.4	V
ACOK pin output voltage		I_{SINK} = 1mA			0.4	V
Timing Characteristics						
Charge safety timer	t_{TMR}	t_{TMR} = 20hrs		20		hours
LED blinking frequency (9)		V_{NTC} = AGND		2		Hz

Notes:

8) I_{CC} accuracy may exceed ±10% for 3 cells in series (or fewer) for a Li-ion battery, or an equivalent voltage for another chemistry. See Table 3 on page 14 for more details.
9) Guaranteed by design.

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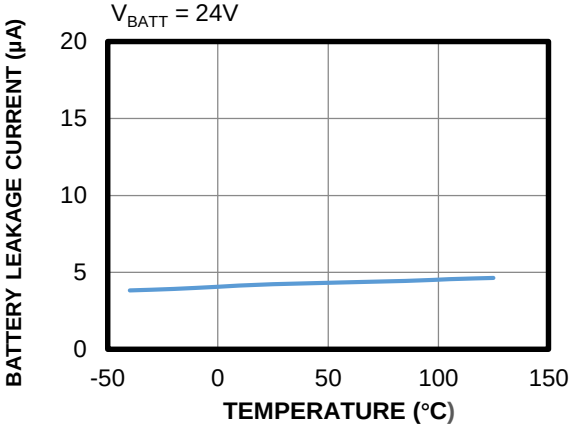
TYPICAL PERFORMANCE CHARACTERISTICS

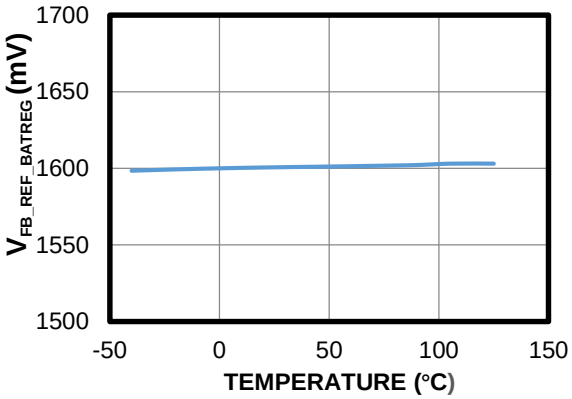
L = 10µH/35mΩ, C_{BATT} = 10µF, T_A = 25°C, unless otherwise noted.

Battery Leakage Current vs. Temperature

V_{BATT} = 24V

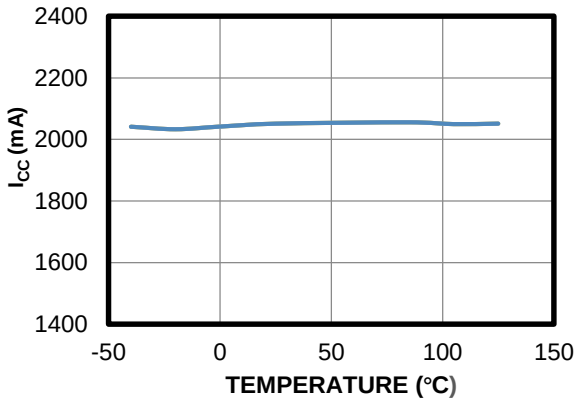


Battery Feedback Reference vs. Temperature

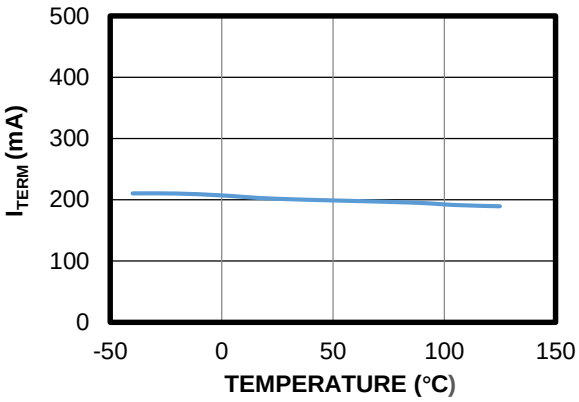


Current Charge vs. Temperature

I_{CC} = 2A

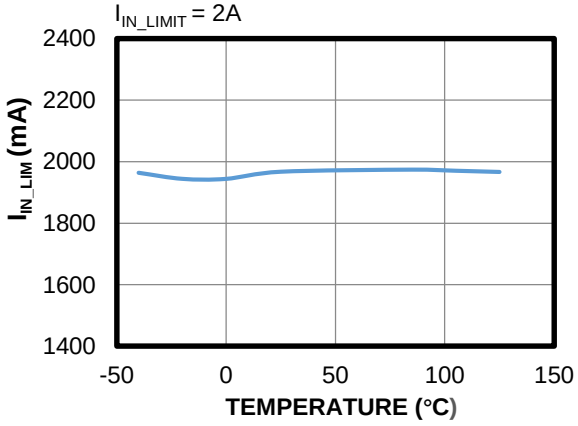


Termination Current vs. Temperature

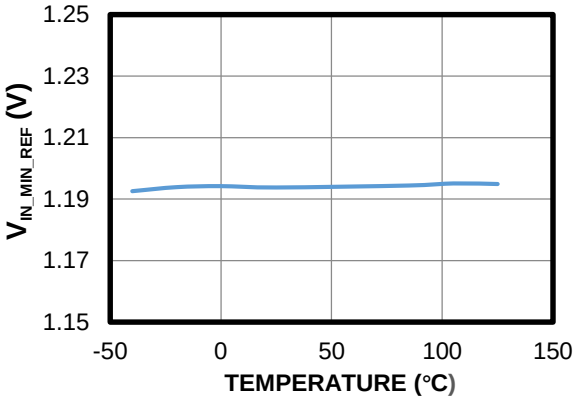


Input Current Limit vs. Temperature

I_{IN_LIMIT} = 2A



$V_{IN_MIN_REF}$ vs. Temperature



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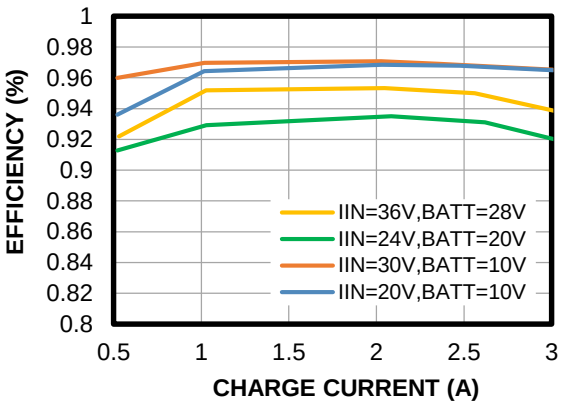
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

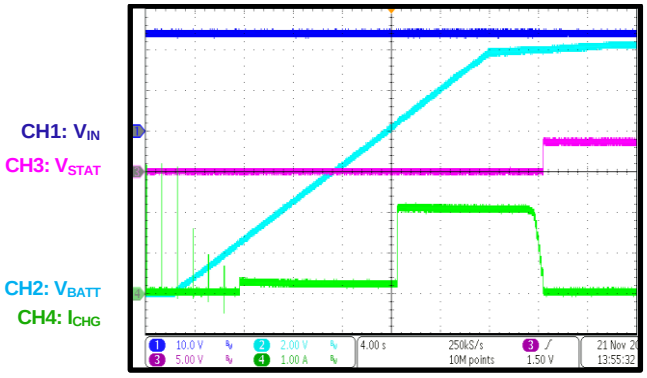
L = 10µH/35mΩ, C_{BATT} = 10µF, T_A = 25°C, unless otherwise noted.

Efficiency vs. Charge Current



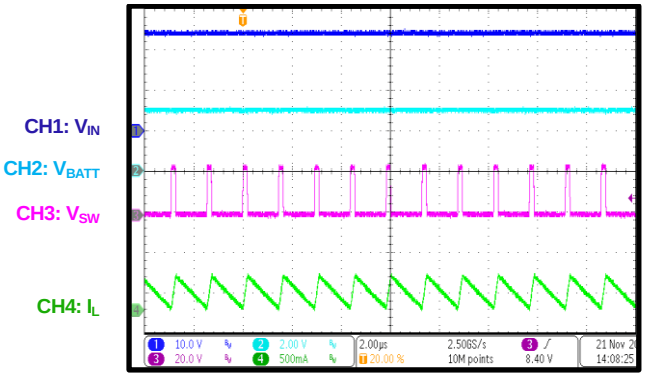
Battery Charge Curve

V_{IN} = 24V, V_{BATT_REG} = 12V, I_{CC} = 2A, I_{IN_LIM} = 2A



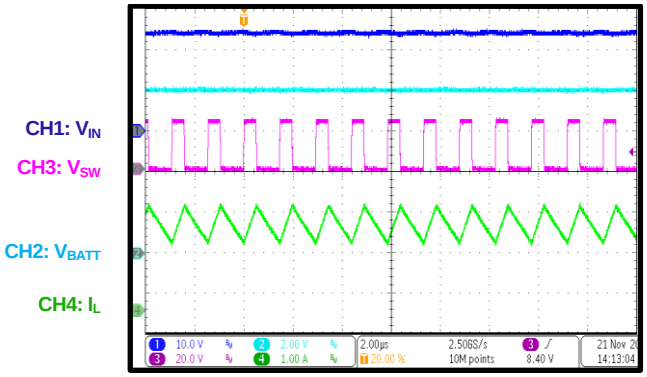
Pre-Charge Steady State

V_{IN} = 24V, V_{BATT_REG} = 12V, V_{BATT} = 3V, I_{PRE} = 200mA



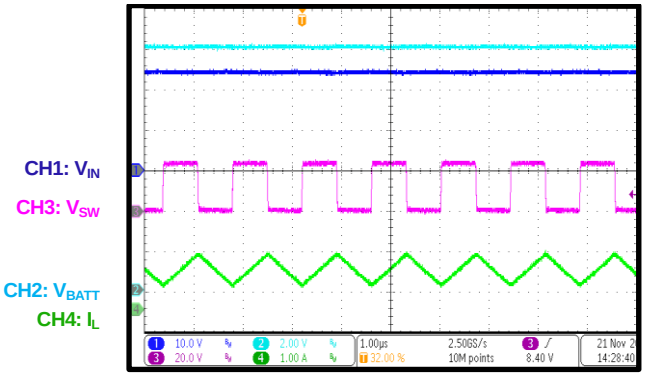
CC Charge Steady State

V_{IN} = 24V, V_{BATT_REG} = 12V, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 2A



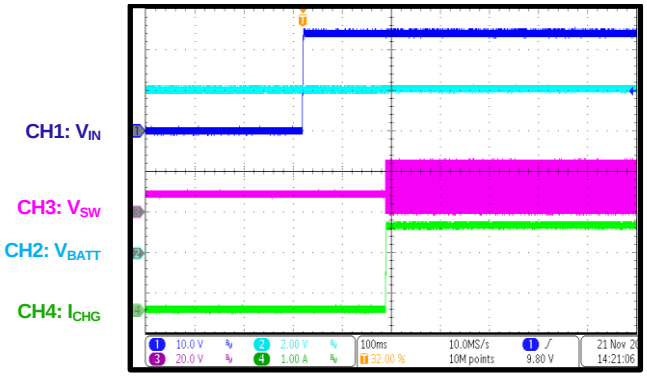
CV Charge Steady State

V_{IN} = 24V, V_{BATT_REG} = 12V, V_{BATT} = 11.95V, I_{CC} = 2A, I_{IN_LIM} = 2A



Start-Up (CC Charge Mode)

V_{IN} = 24V, V_{BATT_REG} = 12V, V_{BATT} = 8V, I_{CC} = 2A, I_{IN_LIM} = 2A



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FUNCTIONAL BLOCK DIAGRAM

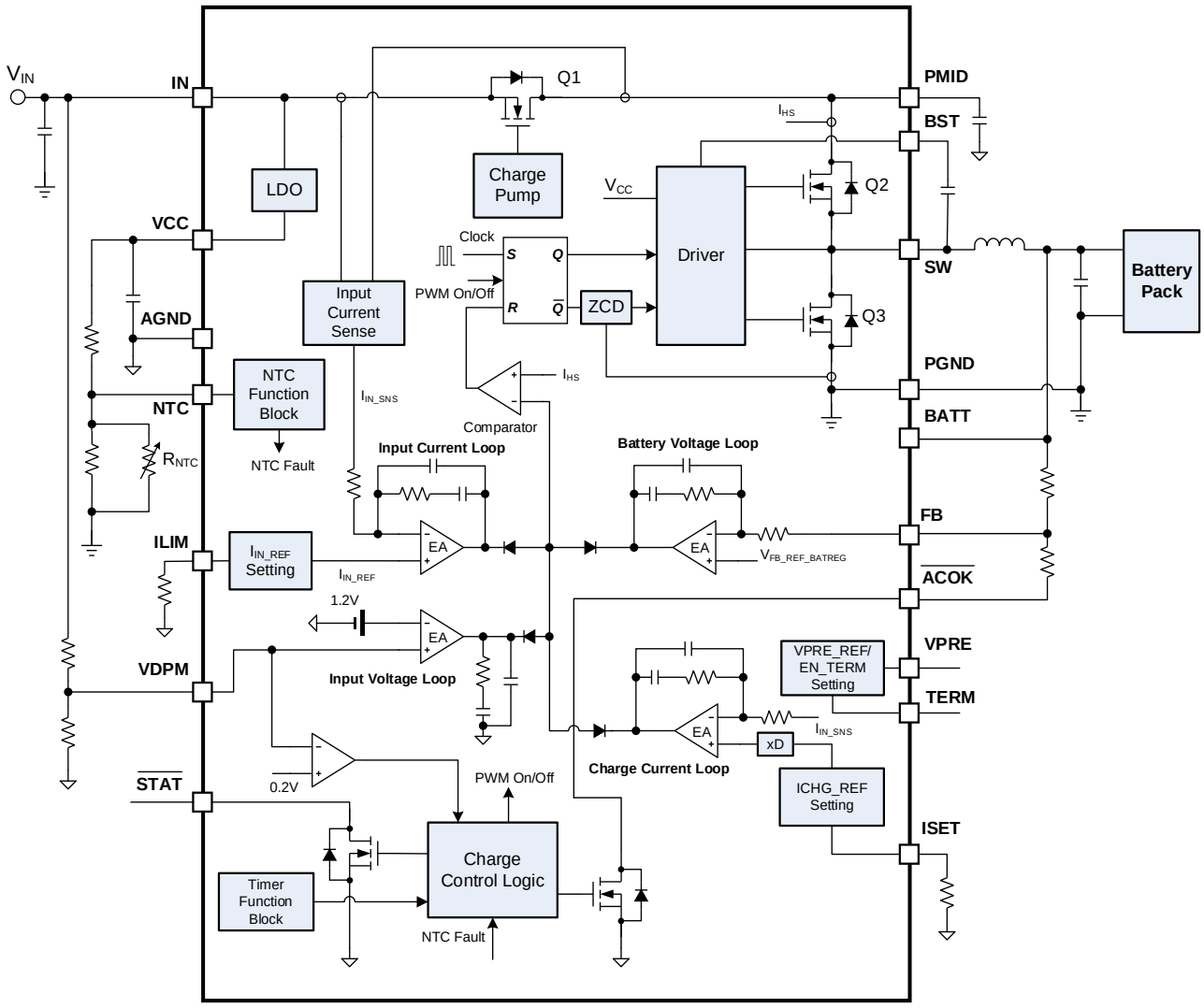

Figure 2: Functional Block Diagram

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OPERATION

Introduction

The MP2658 is a highly integrated switching charger designed for portable devices with Li-ion, Li-polymer, $LiFePO_4$, lead-acid, NiMH, and NiCd batteries, as well as a super capacitor. The device manages battery charging with battery regulation voltages (V_{BATT_REG}) up to 31V.

Power Supply

The VCC pin is powered by the IN pin, and then VCC generates a regulated 5V output with a minimum 50mA current limit. The VCC voltage (V_{CC}) is utilized by the internal bias circuit and the power MOSFET driver. It can also be used for external resistive logic pull-up or an LED driver bias. If a battery is present but the input source is absent, then VCC has no output.

The MP2658 exits sleep mode and is ready to start the charging progress once V_{CC} exceeds the internal under-voltage lockout (UVLO) threshold.

Input Valid Indication

The MP2658 checks the input voltage (V_{IN}) before start-up. The input source has to meet the following requirements:

- $V_{IN} > V_{IN_UVLO}$
- $V_{IN} > V_{BATT} + V_{HDRM}$

After a 170ms delay with a valid input power source, the DC/DC converter is enabled.

Charge Cycle

If the input power is qualified as a good power supply, and if the VPRE pin is not pulled up to VCC, the MP2658 has four main charging phases in the charging cycle: trickle charge, pre-charge, constant-current (CC) charge, and constant-voltage (CV) charge.

Phase 1 (trickle charge): If the battery voltage (V_{BATT}) is below V_{BATT_TC}, a trickle charge is applied on the battery. In this mode, the input current (I_{IN}) is regulated to I_{TC} (60mA) for 20ms, then charging is suspended for 1.4s, which helps reset the protection circuit in the battery pack.

Pre-charge (phase 2): When V_{BATT} exceeds V_{BATT_TC} but is below 70% of battery regulation voltage (when VPRE is connected to AGND. see Table 1 on page 13 for more details), the MP2658 charges the battery with a constant 200mA charge current (if the ITERM bit = 0) or 100mA charge current (if the ITERM bit = 1).

Constant-current (CC) charge (phase 3): When V_{BATT} exceeds 70% of battery regulation voltage (when VPRE is connected to AGND. see Table 1 on page 13 for more details), the MP2658 enters a CC charge phase. The charge current can be set by the ISET pin's resistor.

Constant-voltage (CV) charge (phase 4): When V_{BATT} reaches the charge regulation voltage (V_{BATT_REG}), the charge current (I_{CC}) begins to decrease. When I_{CC} drops to the battery termination threshold (I_{TERM}), the charge cycle is considered complete after a deglitch time (t_{TERM_DGL}). If I_{CC} does not reach I_{TERM} before the charging safety timer expires, the charge cycle ends, and the corresponding timeout fault signal asserts. Charging termination can be enabled or disabled by the TERM pin (see Table 2 on page 13).

Figure 3 shows a typical charge cycle.

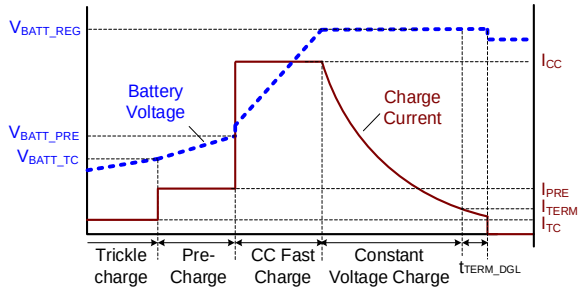

Figure 3: Battery Charging Cycle

If the VPRE pin is pulled up to VCC, the MP2658 has three charging phases in the charging cycle: trickle charge, CC charge, and CV charge. The CC charge starts when V_{BATT} exceeds V_{BATT_TC}.

Auto-Recharge

Once the battery charge cycle completes, the charger remains off. During this time, the external load may consume battery power, or the battery may auto-discharge. A new charge cycle automatically begins if input power is present and the battery voltage falls below the auto-recharge threshold.

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The charging safety timer resets when the auto-recharge cycle begins.

When the VPRE pin is floating, the battery re-charge threshold is fixed to 88.5% of V_{BATT_REG}. This setting is recommended for lead-acid battery charging.

When the VPRE pin is not floating, the battery recharge threshold can be configured by the VRECH bit to be either 93.8% or 97% of V_{BATT_REG}.

Input Voltage and Input Current Limiting

The MP2658 has I_{IN} and V_{IN} limiting to avoid overloading the input power supply. The VDPM pin's voltage is the feedback input for the input voltage regulation loop. When the VDPM voltage falls to 1.2V, I_{CC} is reduced to prevent the input source from being overloaded.

V_{IN} can be regulated by a resistor divider connected to the IN pin, VDPM pin, and AGND. The regulation voltage ($V_{IN_MIN_REF}$) can be calculated with Equation (1):

$$V_{IN_MIN_REF} = V_{IN_MIN} \times \frac{R_2}{R_1 + R_2} (V) \quad (1)$$

Where $V_{IN_MIN_REF}$ is the internal voltage reference (about 1.2V), and R_1 and R_2 are the resistor dividers.

When the VDPM voltage is pulled below 0.2V, the charger is disabled.

The input current limit (I_{IN_LIM}) can be set by the resistor (R_{ILIM}) connected from the ILIM pin to AGND. If the input current of the blocking FET (Q1) reaches the preset limit, the charge current is reduced to regulate the input current. I_{IN_LIM} can be estimated with Equation (2):

$$I_{IN_LIM}(A) = \frac{96(k\Omega)}{R_{ILIM}(k\Omega)} (A) \quad (2)$$

Battery Regulation Voltage (V_{BATT_REG})

The MP2658 supports any battery charge regulation voltage, which is set by a resistor divider connected to the BATT pin, FB pin, and $\overline{ACOK}$ pin. V_{BATT_REG} can be calculated with Equation (3):

$$V_{BATT_REG} = 1.6 \times \left(1 + \frac{R_3}{R_4}\right) (V) \quad (3)$$

Where R3 is a high-side resistor connected from BATT to the FB pin, and R4 is a low-side resistor connected from FB to the $\overline{ACOK}$ pin. The recommended resistance for R4 is 200kΩ or lower.

Pre-Charge Configuration

The MP2658 can configure the pre-charge state via the connection on the VPRE pin (see Table 1)

Table 1: VPRE Pin Selection

VPRE Pin Connection	Pre-Charge to Fast Charge Threshold
AGND	70% of V_{BATT_REG}
Float	75% of V_{BATT_REG}
Pull up to VCC	Disable pre-charge
100kΩ resistor to AGND	50% of V_{BATT_REG}

When the VPRE pin is pulled up to VCC, the pre-charge phase is disabled. When the VPRE pin is not pulled up to VCC, different pre-charge to fast charge thresholds can be set to meet the requirements for different battery chemistries.

Termination Configuration

To accommodate different battery chemistries, the MP2658 can enable and disable charge termination via the TERM pin (see Table 2).

Table 2: Termination Configuration

TERM Pin Connection	Termination Configuration
AGND	Enabled
Pull up to VCC	Disabled
100kΩ resistor to AGND	Disable termination, battery floating voltage is 94% of V_{BATT_REG}

When the TERM pin is pulled up to VCC, the termination feature is disabled, and the MP2658 continues charging the battery until the safety timer expires or the microcontroller (MCU) ceases charging.

When a 100kΩ resistor is connected to the TERM pin and AGND, the termination feature is disabled. After the charging current drops to about 100mA, the battery floating voltage is regulated below 94% of the initial battery regulation voltage. This feature is designed specifically for lead-acid battery charging.

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Charge Current (I_{CC}) Setting

The MP2658 eliminates the external sense resistor and senses I_{CC} internally. I_{CC} can be set by the resistor (R_{ISET}) between the ISET and AGND pins, as estimated with Equation (4):

$$I_{CC}(A) = \frac{96(k\Omega)}{R_{ISET}(k\Omega)}(A) \quad (4)$$

The maximum charge current can be set up to 3A. I_{CC} is related to the PCB thermal dissipation condition and V_{IN}. With a lower V_{IN}, the MP2658's switching loss is smaller, and the maximum deliverable current can be higher. I_{CC} should be set according to the thermal performance for each application.

The I_{CC} accuracy is dependent on the input and battery voltages. With a low battery regulation voltage, the charge current accuracy may exceed ±10%. Table 3 shows the maximum V_{IN} to get ±10% charge current accuracy, with the worst-case scenario for I_{CC} at a 36V V_{IN}.

Table 3: Charge Current Accuracy

V_{BATT_REG}	Max V_{IN} at ±10% I_{CC} Accuracy (I_{CC} = 2A)	I_{CC} Accuracy at 36V V_{IN} (I_{CC} = 1A)
4.2V	15V	±28%
8.4V	20V	±14%
12.2V	25V	≤ ±10%
≥14.4V	36V	< ±10%

Negative Thermal Coefficient (NTC) Input

Connect an appropriate resistor from the VCC pin to the NTC pin, then connect the thermistor from the NTC pin to AGND. The resistor divider determines the NTC pin's voltage. If the NTC pin's voltage falls outside of the NTC window, the MP2658 stops charging. The charger restarts if the temperature goes back into the NTC window range. Figure 4 shows the NTC charging window.

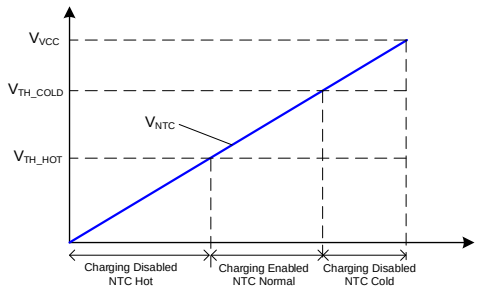

Figure 4: NTC Charging Window

Battery Over-Voltage Protection (OVP)

The MP2658 has battery over-voltage protection (OVP). If V_{BATT} exceeds the battery OV threshold (V_{BATT_OVP}), charging is disabled, the switcher stops, and the fault status is reported on the $\overline{STAT}$ pin.

Charging Safety Timer

The MP2658 provides a safety timer to prevent extended charging cycles due to abnormal battery conditions. If the charging timer finishes before charging completes, charging is terminated.

The safety timer resets at the beginning of a new charge cycle. The following actions restart the safety timer:

- Input voltage removal and reinsertion
- A new charge cycle starts
- The VDPM pin is pulled below 0.2V, then released

Operation Indication

The MP2658 has a $\overline{STAT}$ pin to indicate the operation status. The status of the $\overline{STAT}$ pin changes based on different operating conditions (see Table 4).

Table 4: Operation Indicators

IN	Charging State	$\overline{STAT}$
Absent	N/A	Hi-Z
Present	Charging	Low
Present	Charging complete, charge disabled	Hi-Z
Present	NTC fault, safety timer expiration, battery OVP before termination	Blinking at 2Hz
Present	Regulation mode, battery OVP after termination	Blinking at 1Hz

If there is a 100kΩ resistor is connected to TERM and AGND, termination is disabled, and a new battery regulation voltage is set to 94% of V_{BATT_REG}. The $\overline{STAT}$ pin pulls high before the battery voltage drops below a new threshold, which is V_{RECH} multiplied by 94% of V_{BATT_REG}.

Regulation Mode

If the NTCDET bit is set to 1 and the NTC pin is pulled up to VCC, the MP2658 operates in regulation mode.

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In this mode, battery charge termination is blocked, and the device generates an output voltage that is equal to V_{BATT_REG}.

One-Time Programmable (OTP) Memory

The MP2658 has one-time programmable (OTP) memory to configure the default values of several parameters. The OTP Map section on page 16 shows the configurable parameters.

Multiple Battery Chemistry Charge Configurations

The MP2658 can be configured to charge different battery chemistries. Table 5 shows the recommendations for these battery chemistries, as well as the VPRE pin connection, TERM pin connection, and OTP selections.

Table 5: Multiple Chemistry Battery Charge Configuration

Battery Chemistry	VPRE Pin Connection	Pre-Charge to Fast Charge Threshold	Recharge Threshold	TERM Pin Connection	Termination Configuration
Li-Ion, Li-Polymer, $LiFePO_4$, or Any Other Chemistry	AGND	70% of V_{BATT_REG}	Configured by the VRECH bit	AGND / pull up to VCC	Enable / disable termination
Lead-Acid	Float	75% of V_{BATT_REG}	Fixed to 88.5% of V_{BATT_REG}	100kΩ resistor to AGND	Disable termination, battery floating voltage is 94% of V_{BATT_REG}
Super Capacitor	Pull up to VCC	Disable pre-charge	Configured by the VRECH bit	Pull up to VCC	Disable termination
NiMH/NiCd	100kΩ resistor to AGND	50% of V_{BATT_REG}	Configured by the VRECH bit	AGND / pull up to VCC	Enable / disable termination

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OTP MAP

The MP2658 has a one-time-programmable (OTP) memory function to configure the default values of certain parameters.

Bits	Bit Name	Default	Description
7	RESERVED	N/A	Reserved.
6	VHDRM	0	Sets the IN vs. BATT headroom rising threshold. 0: 1V 1: 0.5V
5	VRECH	0	Sets the recharge threshold. This value is below the battery regulation voltage. 0: 93.8% of battery regulation voltage 1: 97.0% of battery regulation voltage When the VPRE pin is floating, the recharge threshold is fixed at 88.5% of battery regulation voltage, and it is not configured by this bit.
4	ITERM	0	Sets the termination and pre-charge current. 0: 200mA 1: 100mA
3	NTCDET	0	When this bit is set to 1 and NTC is pulled up to VCC, the MP2658 operates in regulation mode, and battery charge termination is blocked. 0: Disabled 1: Enabled
2	FSW	0	Sets the switching frequency (f_{SW}). 0: 680kHz 1: 350kHz
1	TTMR	0	Sets the charging safety timer. 0: 20hrs 1: 10hrs
0	TMR_DIS	0	Enables the safety timer. 0: Enabled 1: Disabled

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APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

Choose an inductor that does not saturate under the worst-case load condition. Estimate the required inductance with Equation (5):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L_MAX}} \times \frac{V_{BATT}}{V_{IN} \times f_{SW}} \quad (5)$$

Where V_{IN} is the input voltage, V_{BATT} is the battery voltage, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current, which is usually designed at 30% to 40% of the CC charge current.

It is recommended to use a 10µH inductor with a 5A saturation current for most applications.

Selecting the PMID Capacitor (C_{PMID})

The PMID pin's capacitor (C_{PMID}) serves as the buck regulator's decoupling capacitor. A ceramic, 2.2µF/50V capacitor with X5R or X7R dielectrics and 1206 size is recommended.

Do not put additional capacitance on the PMID pin. Connect a 2A/40V Schottky diode in an SMA package from IN to PMID.

Selecting the IN Capacitor (C_{IN})

For applications where V_{IN} ≤20V, it is recommended to make the input capacitor (C_{IN}) a 1µF/50V ceramic capacitor in a 0805 or 1206 package.

It is recommended to add a ≥47µF/50V electrolytic capacitor on the IN pin for applications where V_{IN} >20V, especially for those with input hot insertion conditions. During the hot insertion of a high-voltage adapter, the cable's parasitic inductance (together with the IN/PMID node capacitance) can generate an inrush current and voltage spike. The ESR of the electrolytic capacitor can effectively dampen the inrush oscillation magnitude, and a TVS diode can help clamp the voltage spike. (see Table 6 on page 18).

The hot insertion must be tested and verified for real applications. In case of a higher V_{IN} application (e.g. 28V), it is recommended to place a TVS diode across the IN and GND pins.

The following diodes are recommended:

- 1SMA33A from Sunmate in an SMA package
- SMAJ33AQ from Diode, Inc. in an SMA package

Selecting the BATT Capacitor (C_{BATT})

The MP2658 requires a ≥10µF capacitor to stabilize the loop on the BATT node. However, the battery capacitor (C_{BATT}) is generally effective only during hot-plug insertion or short-circuit conditions.

When the battery is plugged in, there might be an overshoot on the BATT pin due to the oscillation caused by C_{BATT} and the battery cable's parasitic inductance. For 5-cell or 6-cell applications, this overshoot may harm the BATT pin. A 47µF/50V electrolytic capacitor can dampen the overshoot with its ESR. Otherwise, use a TVS diode to clamp the BATT node spike. See the Selecting the IN Capacitor (C_{IN}) section for the recommended TVS diodes.

If the BATT node can be shorted to ground, C_{BATT} and the cable inductance can induce a negative voltage spike on the BATT pin, which may harm the IC. An electrolytic capacitor can help dampen the spike, or a unidirectional TVS diode can clamp the spike (see Table 6 on page 18).

Protecting the PMID Pin

When a high-voltage battery is plugged in, there is a current path that flows from the main inductor, high-side MOSFET body diode, then charges up the PMID pin capacitor. An LC resonant circuit may induce a voltage spike on the PMID pin. With a high-voltage battery, the PMID voltage can rise to a dangerous level, so the PMID pin must be protected.

For 5-cell to 7-cell applications, the PMID pin's overshoot due to battery insertion should be tested and verified in a real application. A TVS diode can be added on the PMID node to clamp the overshoot. See the Selecting the IN Capacitor (C_{IN}) section for the recommended TVS diodes. If the PMID pin has a TVS diode, the IN pin does not require a TVS diode (see Table 6 on page 18).

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Table 6: Components Selection Guide

Pin	Condition	Recommendations
IN	≤20V input	1µF/50V ceramic capacitor for adapter applications. Add a ≥47µF capacitance for solar applications.
	>20V input	1µF/50V ceramic capacitor, and add a 47µF/50V electrolytic capacitor. A TVS diode is required if the IN voltage exceeds the pin's maximum voltage rating during a VIN hot insertion test.
BATT	Below 4-cell	10µF/50V ceramic capacitor.
	5-cell or higher	10µF/50V ceramic capacitor. Add a TVS diode or ≥47µF electrolytic capacitor.
PMID	-	2.2µF/50V ceramic capacitor (1206 size recommended). Connect a 2A/40V Schottky diode from IN to PMID. A TVS diode is required if the PMID voltage exceeds the pin's maximum voltage rating during a VBATT hot insertion test.

Setting the VDPM Pin

Multiple functions can be designed with the VDPM pin, described below.

Minimum Input Voltage Limiting

A resistive voltage divider from the IN pin to the VDPM pin sets the minimum input voltage limit (V_{IN_MIN}).

The maximum V_{IN_MIN} regulation voltage should be set below the minimum DC output voltage of the power supply, including the IR voltage drop from the DC input current and series resistance on the PCB, connector, and cable.

The minimum V_{IN_MIN} regulation voltage should be set to exceed V_{BATT_REG} + V_{HDRM}.

Enable (EN) Control

Pull the VDPM pin below 0.2V to disable the charger and reset the safety timer. Figure 5 shows a recommended application circuit for this function.

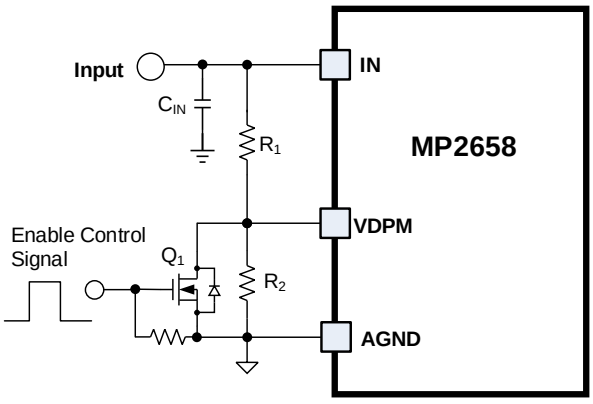

Figure 5: Enable Control

Where R2 is recommended to be 10kΩ.

Disable Input Voltage Limiting

If the input voltage limit function is not required, the VDPM pin can be tied to the VCC pin.

Direct Enable (EN) Control

If input voltage limiting is not used, the VDPM pin can be directly driven by the host to enable/disable charging. It is recommended to use a 100kΩ resistor to pull up the VDPM pin to VCC. The logic high level should exceed 1.3V, and the logic low level should be below 0.2V.

Resistor Selection for the NTC Sensor

The battery temperature-sensing NTC thermistor can be connected in series or parallel. Figure 6 shows an NTC connection in parallel.

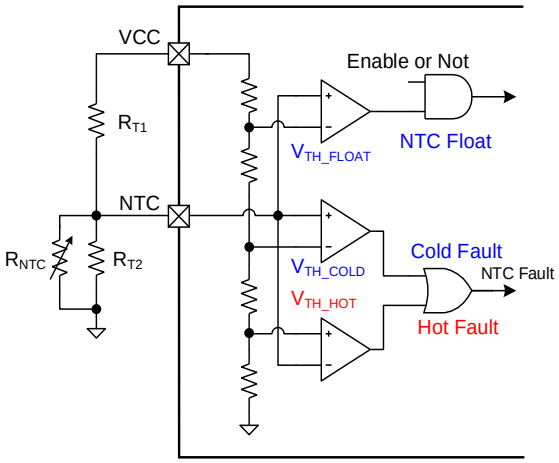

Figure 6: NTC Parallel Connection

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Calculate the appropriate R_{T1} and R_{T2} values to set the NTC window with Equation (6) and Equation (7), respectively:

$$R_{T1} = \frac{R_{NTC_HOT} \times R_{NTC_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC_COLD} - R_{NTC_HOT})} \quad (6)$$

$$R_{T2} = \frac{R_{NTC_HOT} \times R_{NTC_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC_HOT}} \quad (7)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the upper bound of its operating temperature range, R_{NTC_COLD} is its lower bound, V_{HOT} is the hot temperature threshold, and V_{COLD} is the cold temperature threshold.

For example, for a 103AT-2 thermistor, the thermistor has the following electrical characteristics:

- At 0°C, $R_{NTC_COLD} = R_{0°C} = 27.28k\Omega$
- At 60°C, $R_{NTC_HOT} = R_{60°C} = 3.02k\Omega$

Put the above resistor values into Equation (6) and Equation (7) to determine that $R_{T1} = 2.26k\Omega$, and $R_{T2} = 6.95k\Omega$.

Figure 7 shows an NTC connected in series.

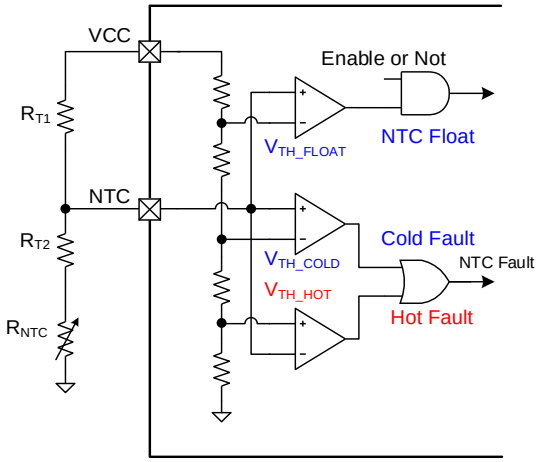

Figure 7: NTC Series Connection

With an NTC connection in series, R_{T1} and R_{T2} can be estimated with Equation (8) and Equation (9), respectively:

$$R_{T1} = \frac{(R_{NTC_COLD} - R_{NTC_HOT}) \times (1 - V_{COLD}) \times (1 - V_{HOT})}{(1 - V_{HOT}) \times V_{COLD} - (1 - V_{COLD}) \times V_{HOT}} \quad (8)$$

$$R_{T2} = \frac{V_{COLD} \times R_{T1}}{1 - V_{COLD}} - R_{NTC_COLD} \quad (9)$$

Put the R_{NTC_COLD} and R_{NTC_HOT} resistor values into the equations above to determine that $R_{T1} = 15.98k\Omega$, and $R_{T2} = 11.85k\Omega$.

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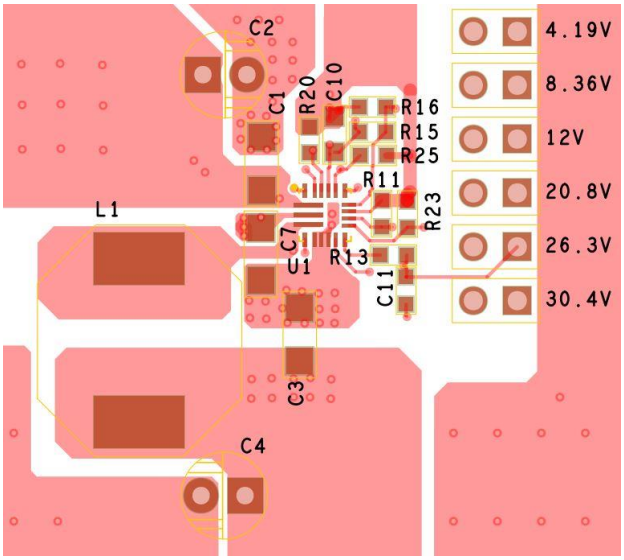
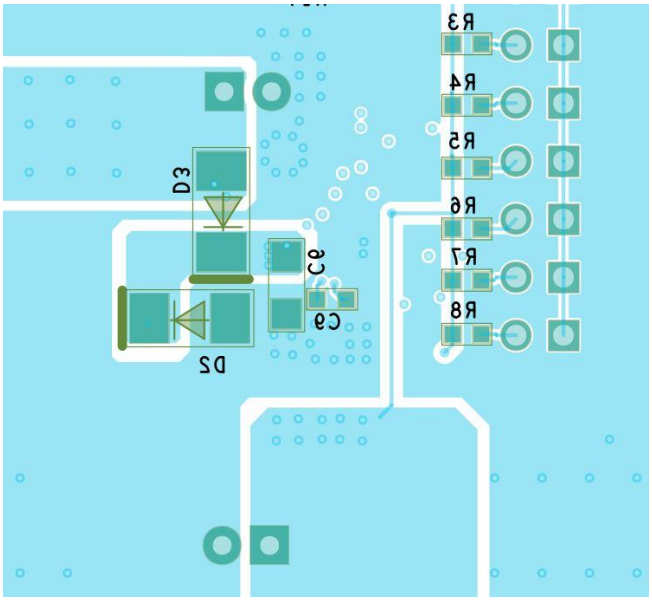
PCB Layout Guidelines

PCB layout is critical to meet specified noise, efficiency, and stability requirements. For the best results, follow the guidelines below:

1. Place the PMID capacitor as close as possible to the PMID and PGND pins using a short copper plane connection.
2. Place the PMID capacitor on the same layer as the IC.
3. Minimize the high-frequency current path loop between the PMID capacitor and the buck converter's power MOSFETs (PMID pin to capacitor, PGND to capacitor).
4. Place the inductor's input terminal as close as possible to the SW pin.
5. Minimize the copper area of the inductor's input terminal trace to reduce electrical and magnetic field radiation, but ensure the trace is wide enough to carry the charging current.
6. Minimize parasitic capacitance from the inductor input terminal to any other trace or plane.
7. If possible, choose a PMID capacitor with 1206 dimensions.
8. Route the SW traces beneath the PMID capacitor.
9. Connect the AGND pin to the ground of the battery capacitor, such as C_{BATT} or PCB ground.
10. Place decoupling capacitors (e.g. the VCC pin's capacitor) as close as possible to the IC pins, and make the connection as short as possible.
11. Connect the IC's power pin to as many copper planes as possible to conduct heat away from the IC.
12. Ensure that the number and physical size of the vias is sufficient for a current path



Top Layer



Bottom Layer

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

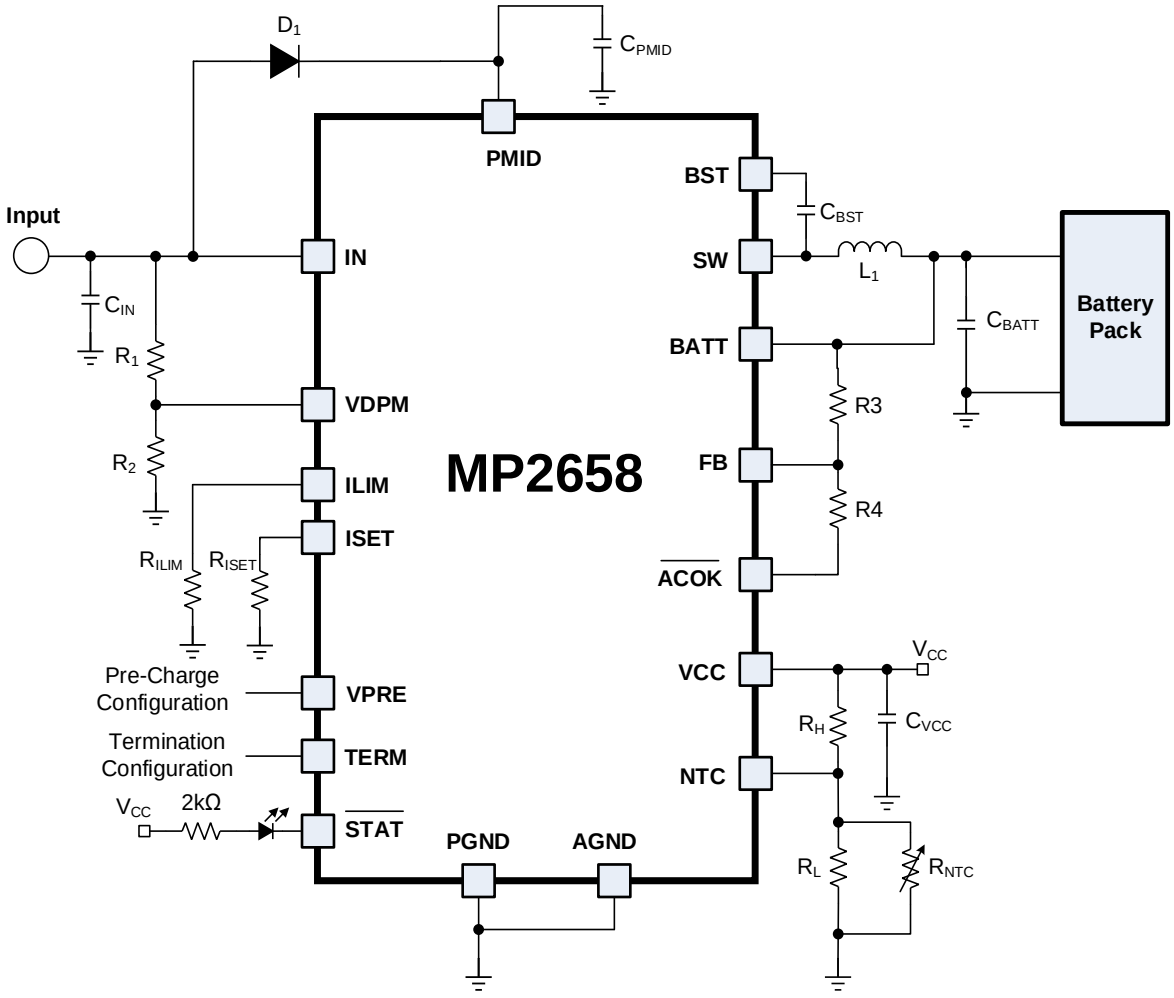

Figure 8: Typical Application Circuit for 16V Input (3-Cell Li-Ion Battery)

Table 7: Key BOM

Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	1µF	Ceramic capacitor, 50V, X5R or X7R	0805	Any
1	C_{BATT}	10µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{PMID}	2.2µF	Ceramic capacitor, 50V, X5R or X7R	1206	Any
1	C_{VCC}	1µF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	L1	10µH	Inductor, I_{SAT} > 4A	SMD	Any
1	D1	2A/40V	Schottky diode 2A/40V	SMA	Any

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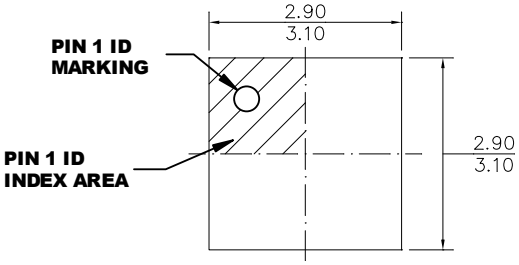
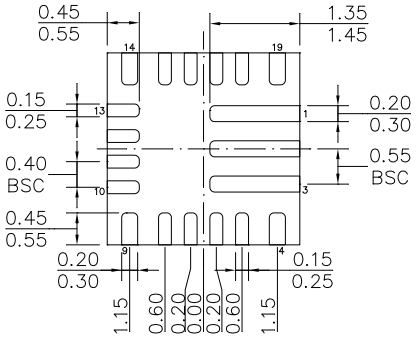
PACKAGE INFORMATION

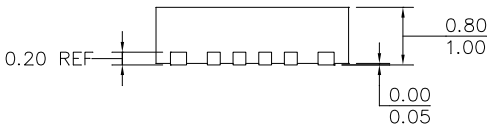
QFN-19 (3mmx3mm)



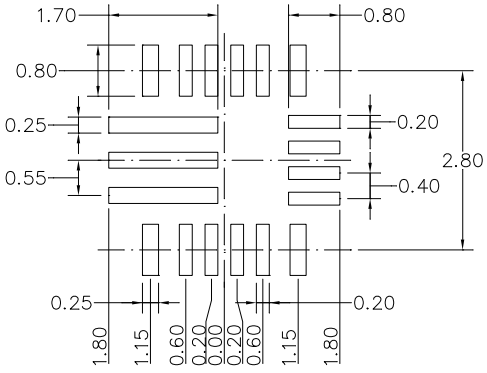
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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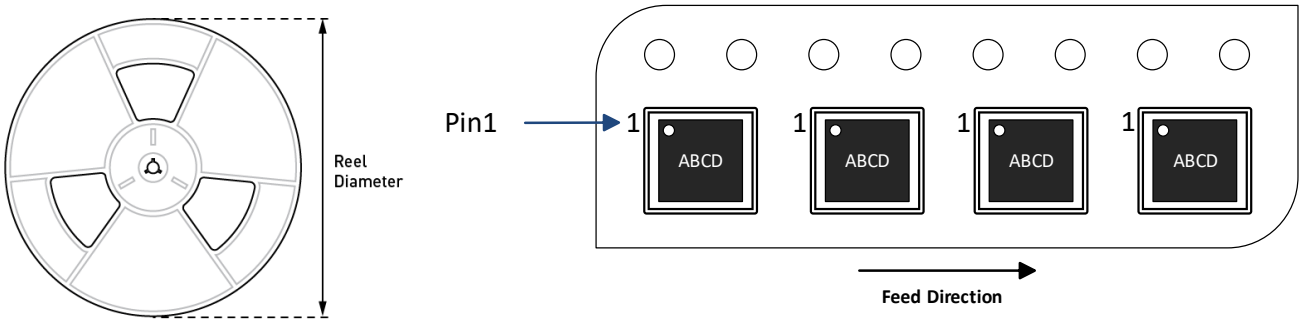
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2658GQ-xxxx-Z	QFN-19 (3mmx3mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/5/2024	Initial Release	-

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