MPQ4242

5A, 36V, Fully Integrated USB PD Solution with Integrated Buck-Boost Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4242 is a fully integrated power delivery (PD) solution for USB Type-C sourcing ports. It integrates a buck-boost converter with four power switches and a USB PD controller. The device supports up to 5A of continuous output current (I_{OUT}) under a certain input supply range.

The MPQ4242's USB Type-C port supports USB PD revision 3.0 with PPS. It is backward compatible with DCP schemes for battery charging specification (BC1.2), 3A divider mode, and 1.2V/1.2V mode. The MPQ4242 also supports QC 2.0/3.0 and Huawei FCP mode.

The MPQ4242 provides a configurable PD power management state machine when the battery voltage (V_{BATT}) is low, or if an over-temperature condition occurs. When two MPQ4242s are used as dual PD ports, the internal power sharing logic can effectively distribute the total power.

Fault condition protections include I/O pin short for the BUS and VIN pins, CC over-current protection (OCP), current limiting with hiccup mode, output over-voltage protection (OVP), and thermal shutdown.

The MPQ4242 requires a minimal number of readily available, standard external components. It is available in a QFN-22 (4mmx5mm) package.

FEATURES

- All-In-One USB PD Solution for Automotive Sourcing Ports
- Integrated 4-Switch Buck-Boost Converter
- Integrated PD 3.0 Controller
- Wide 4.8V to 36V Operating Input Voltage (V_{IN}) Range
- 3.3V to 22.5V Output Voltage (V_{OUT}) Range
- Accurate Output CC Current Limit: ±5%
- External High-Side MOSFET (HS-FET) can be Paralleled
- Low I_Q when USB Type-C is Disconnected
- 250kHz / 420kHz Configurable Frequency with Spread Spectrum
- Supports USB Type-C V2.0
- Supports USB PD R3.0, V2.0, and PPS with 7 PDO List
- Supports QC 3.0 Specification, Huawei FCP
- Supports DCP Schemes for BC1.2, 3A Divider Mode, and 1.2V/1.2V Mode
- CCx, DP, and DM Short to V_{BUS} / V_{BATT} Protection
- Battery Short to Ground Protection Driver
- I^2C Slave Interface
- Output Line Drop Compensation
- Configurable PD Power Management during Low Battery Voltages or High Temperatures
- Supports Dual-Port PD Power Sharing
- PWM Duty Cycle Configurable LED Driver
- Up to 120 Minutes for EN Off Delay
- Available in a QFN-22 (4mmx5mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

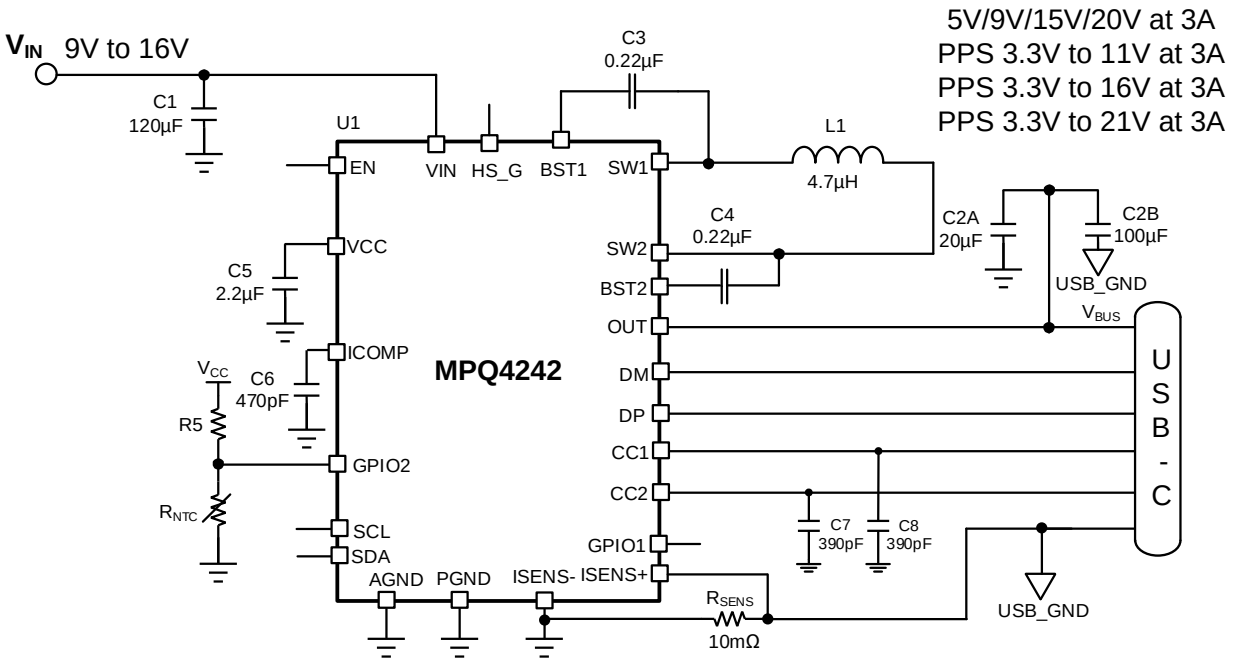
APPLICATIONS

- USB Power Delivery Charging Ports
- USB Power Supplies

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MPQ4242GVE-0000-AEC1	QFN-22 (4mmx5mm)	*See Below*	1
MPQ4242GVE-0001-AEC1			
MPQ4242GVE-0015-AEC1			
MPQ4242GVE-xxxx-AEC1**			
EVKT-MPQ4242	-	-	-

* For Tape & Reel, add suffix -Z (e.g. MPQ4242GVE-xxxx-AEC1-Z).

** "-xxxx" is the configuration code identifier for the register setting stored in the OTP. Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

*** The MPQ4242GVE-0000-AEC1 is the default 60W PD version, which can be configured once by the one-time programmable (OTP) memory. The MPQ4242GVE-0001-AEC1 is the standard version for a 45W PD application, and it cannot be written with the OTP again.

TOP MARKING

MPSYWW
MP4242
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4242: Part number
LLLLLL: Lot number
E: Wettable flank

EVALUATION KIT EVKT-MPQ4242

EVKT-MPQ4242 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EVQ4242-VE-00B	The MPQ4242 evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I^2C communication interface device, one USB cable, and one ribbon cable	1
3	MPQ4242GVE-0000-AEC1	The MPQ4242 IC, which can be used for OTP configurations	2

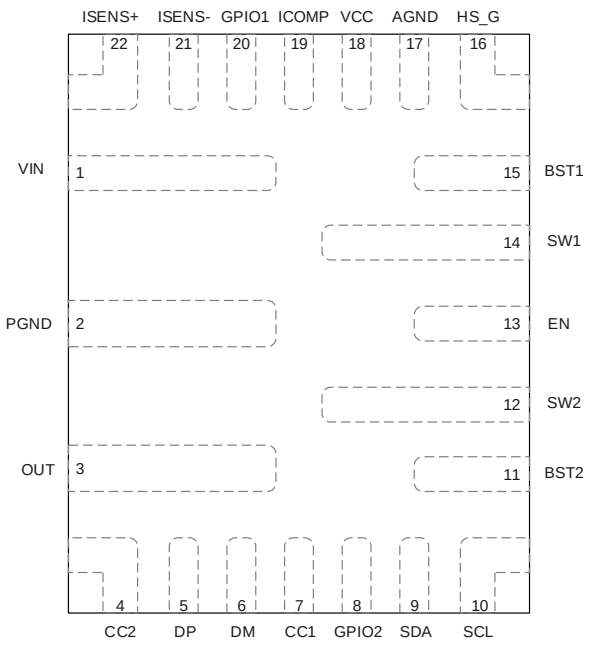
Order directly from MonolithicPower.com or our distributors.



Figure 1: EVKT-MPQ4242 Evaluation Kit Set-Up

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PACKAGE REFERENCE



QFN-22 (4mmx5mm) with Wettable Flanks

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PIN FUNCTIONS

Pin #	Name	Description	
1	VIN	**Supply voltage.** The MPQ4242 operates from a 4.8V to 36V unregulated input. An input capacitor (C_{IN}) is required to prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible. The VIN pin is the drain of the internal power device, and it is the power supply for the whole chip.	
2	PGND	**Power ground.** Place the PGND pin outside of the C_{IN} and output capacitor (C_{OUT}) ground path to prevent switching current spikes. PGND requires extra consideration during the PCB layout. Make the PGND connection with copper traces and vias.	
3	OUT	**Buck-boost output pin.** C_{OUT} is required to prevent large voltage spikes from appearing at the output in buck-boost and boost mode. Place C_{OUT} as close to the IC as possible.	
4	CC2	**Configuration channel (CC).** The CC2 pin discovers, configures, and manages connections across a USB Type-C cable.	
5	DP	**D+ data line to USB connector.** The DP pin is the input/output used for handshaking with portable devices.	
6	DM	**D- data line to USB connector.** The DM pin is the input/output used for handshaking with portable devices.	
7	CC1	**Configuration Channel (CC).** The CC1 pin discovers, configures, and manages connections across a USB Type-C cable.	
8	GPIO2	POL	**USB Type-C polarity indication.** The POL pin is an open drain. When CC1 is selected as the CC line, POL is pulled low; when CC2 is selected as the CC line, POL is an open drain.
		NTC	**NTC thermal-sense input.**
		VCONN_IN	**1W VCONN power supply input.**
		LED_PWM	**Output for the PWM driver to the LED.**
		ATTACH	**Output to indicate if the device is attached.** The ATTACH pin is active low.
		POWER_SHARE2	**Power sharing 2 input.** The POWER_SHARE2 pin is active high. When this pin's voltage exceeds 1.87V, the PD power drops to the PS_PDP_THD setting.
9	SDA	**I^2C data line.**	
10	SCL	**I^2C clock signal input.**	
11	BST2	**Bootstrap 2**. Connect a 0.22µF capacitor between the SW2 and BST2 pins to form a floating supply across the high-side switch driver.	
12	SW2	**Switch 2 output.** Use a wide PCB trace to make the SW2 connection.	
13	EN	**Enable control pin.** Apply a logic high voltage on the EN pin to enable the IC. Pull EN to logic low to disable the IC. The EN pin has an internal 6µA pull-up.	
14	SW1	**Switch 1 output.** Use a wide PCB trace to make the SW1 connection.	
15	BST1	**Bootstrap 1**. Place a 0.22µF capacitor between the SW1 and BST1 pins to form a floating supply across the high-side switch driver.	
16	HS_G	**High-side gate driver signal for an external N-channel MOSFET.**	
17	AGND	**Analog ground.** Connect the AGND pin to PGND.	
18	VCC	**Internal 5V LDO regulator output.** Decouple the VCC pin with a 2.2µF capacitor.	
19	ICOMP	**Compensation pin for the CC current limit loop.** Decouple the ICOMP pin with a 470pF capacitor.	

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PIN FUNCTIONS *(continued)*

<table>
<tr><th>Pin #</th><th>Name</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">20</td><td rowspan="6">GPIO1</td><td>GATE</td><td>Gate drive for the external low-side N-channel power MOSFET. The GATE pin is an open-drain structure. GATE pulls low to turn off the power MOSFET when the secondary current limit is triggered. If GATE is not selected, the GND short to V_{BATT} detection function is disabled.</td></tr>
<tr><td>POWER_SHARE1</td><td>Power sharing 1 input. The POWER_SHARE1 pin is active low. When this pin’s voltage is low, the PD power drops to the value set by PS_PDP_THD.</td></tr>
<tr><td>FAULT</td><td>Fault indication. Open-drain output. If a fault occurs, the FAULT pin pulls low.</td></tr>
<tr><td>NTC2</td><td>Second NTC detection input. If the NTC2 pin is triggered, PDP reduces its power to the set power share value.</td></tr>
<tr><td>ATTACH_FLT_ALT</td><td>Attach and fault indicator. The ATTACH_FLT_ALT pin is an open-drain output. If no fault event has occurred, this pin pulls low for 12µs when a sink plug-in is detected. If a fault occurs, it pulls low. See the truth table below for more details.
<table>
<tr><td>Device Plug In</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Fault Event</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>ATTACH_FLT_ALT</td><td>Open drain</td><td>12µs pull-down pulse</td><td>Low</td><td>Low</td></tr>
</table></td></tr>
<tr><td>IMON</td><td>Current monitor output. The IMON pin represents the signal between the ISENS+ and ISENS- pins.</td></tr>
<tr><td>21</td><td>ISENS-</td><td colspan="2">Negative node of current-sense signal input. Place a current-sense resistor between the PGND pin and the USB port’s GND. Connect the ISENS- pin to the PGND side.</td></tr>
<tr><td>22</td><td>ISENS+</td><td colspan="2">Positive node of current-sense signal input. Place a current-sense resistor between the PGND pin and the USB port’s GND. Connect the ISENS+ pin to the USB port’s GND side.</td></tr>
</table>

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
V_{HS_G} .....-0.3V to V_{IN} + 12V
V_{EN} .....-0.3V to +40V
V_{OUT}, V_{CC1}, V_{CC2}, V_{DP}, V_{DM}.....-0.3V to +26V
V_{SW1}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{SW2}.....-0.3V (-5V for <10ns) to V_{OUT} + 0.3V (29V for <10ns)
V_{BST1}.....V_{SW1} + 6.5V
V_{BST2}.....V_{SW2} + 6.5V
All other pins .....-0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-22 (4mmx5mm) 4.55W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings (3)

CC1/CC2/DP/DM (HBM) (4) ..... ±8kV
Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (5)

Supply voltage (V_{IN}) .....4.8V to 36V
Output voltage (V_{OUT}).....3.3V to 22.5V
Output current.....5A or 100W peak
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance	θ_{JA}	θ_{JC}
EVQ4242-VE-00B (6)	27.5	5.2 °C/W
QFN-22 (4mmx5mm) (7)	44	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AECQ100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on MPQ4242 test board, 43mmx5mm, 4-layer PCB.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	EN = 0V, T_J = 25°C		12	20	μA
		EN = 0V, T_J = -40°C ~125°C		12	80	μA
Supply current (standby)	I_{Q_STB}	No device attached, set EN to 1b via the I^2C, T_J = 25°C		150	200	μA
Supply current (quiescent)	I_{Q_BB}	Buck-boost non-switching, CC attached		4		mA
EN rising threshold	V_{EN_RISING}		-4%	1.3	+4%	V
EN hysteresis	V_{EN_HYS}			100		mV
EN pull-up current	I_{EN}	V_{EN} = 2V	3	6	9	μA
Thermal shutdown (8)	T_{TSD}			175		°C
Thermal hysteresis (8)	T_{TSD_HYS}			20		°C
V_{IN} under-voltage lockout threshold rising	$V_{IN_UVLO_RISING}$		-4%	4.3	+4%	V
V_{IN} under-voltage lockout threshold hysteresis	$V_{IN_UVLO_HYS}$			400		mV
VCC regulator	V_{CC}		4.75	5	5.25	V
VCC load regulation	V_{CC_REG}	I_{CC} = 70mA		3		%
VBUS_UV falling threshold 1	V_{BUS_UV1}		2.9	3	3.1	V
VBUS_UV falling threshold 2	V_{BUS_UV2}		-3%	4.5	+3%	V
Buck-boost Converter						
Switch A on resistance	$R_{DS_ON_A}$			16.3		mΩ
Switch B on resistance	$R_{DS_ON_B}$			41.5		mΩ
Switch C on resistance	$R_{DS_ON_C}$			15		mΩ
Switch D on resistance	$R_{DS_ON_D}$			15.3		mΩ
VHS_G voltage	V_{HSG}			V_{IN} + 10		V
VHS_G source current (8)	I_{HSG}			100		μA
VHS_G pull-down	R_{HS_DN}			3	6.5	Ω
Output voltage	V_{OUT0}		-3%	3.3	+3%	V
	V_{OUT1}		-2%	5	+2%	V
	V_{OUT2}		-1.5%	9	+1.5%	V
	V_{OUT3}		-1.5%	20	+1.5%	V
Output over-voltage protection (OVP)	V_{OVP}		112	117	122	%
Output absolute OVP	V_{OVP_ABS}		24	25	26	V
OVP recovery hysteresis	V_{OVP_HYS}			10		%
Input over-voltage protection	V_{IN_OVP}	OTP trim option	21.4	22.4	23.4	V
Input OVP recovery hysteresis	V_{OVP_HYS}	OTP trim option		2		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Switch leakage	SWLKG	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1000	nA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C~125°C			80	μA
Line drop compensation	VLDC	Set LINE_DROP_COMP to 01b via the I²C, V_{OUT} = 5V, I_{OUT} = 3A (only enabled when V_{OUT} > 4.9V)		150		mV
ISENS OC Threshold	I_{OC1}	OC threshold = 1A, R_{SENS} = 10mΩ	9	10	11	mV
	I_{OC2}	OC threshold = 3A, R_{SENS} = 10mΩ	28.5	30	31.5	mV
Switch A current limit	I_{LIMIT1}	Switch A, boost mode		20		A
Switch B valley limit	I_{LIMIT2}	Switch B, buck mode		6.7		A
Oscillator frequency	f_{SW1}	Set FREQ to 00b via the I²C	200	250	300	kHz
	f_{SW2}	Set FREQ to 01b via the I²C	350	420	490	kHz
Frequency dithering span	f_{DITH_SPAN}	Set FREQ to 01b via the I²C		±11		%
Minimum on time (8)	t_{ON_MIN}	Buck SWC		80		ns
Minimum off time (8)	t_{OFF_MIN}	Buck SWB		60		ns
Soft-start time	t_{SS}	5V output from 10% to 90%, Constant slew rate for other V_{OUT}	0.5	1.1	1.7	ms
Output discharge resistance	R_{DIS_OUT}			320		Ω
Ground NMOSFET Gate Driver						
GND short to battery threshold	V_{RGND}	R_{SENS} = 10mΩ		135		mV
Short to battery retry delay (8)	t_{SBP}			1		s
Gate pull-down resistance	R_{PD}			20	45	Ω
NTC, NTC2						
External thermal sense triggering voltage	V_{NTC_ETY}	R_P = 43.2kΩ, R_{NTC} = 4.79kΩ (100°C)	8%	10%	12%	V_{CC}
External thermal sense recovery voltage 1	V_{NTC_RCY1}	Set NTC_HYSTERESIS to 0b via the I²C		20%		V_{CC}
External thermal sense recovery voltage 2	V_{NTC_RCY2}	Set NTC_HYSTERESIS to 1b via the I²C		30%		V_{CC}
GPIO1						
Power share input high	V_{IH_PS}		2			V
Power share input low	V_{IL_PS}				0.8	V
Power share pull-up resistance	I_{LKG_PS}	5V pull-up		1		MΩ
Fault pull-down resistance	R_{PD_FAULT}			20	45	Ω
Fault leakage	I_{LKG_FAULT}				3	μA
GPIO2						
POL pull-down resistance	R_{PD_POL}	Connect CC1 to GND with a 5.1kΩ resistor			45	Ω
POL leakage	I_{LKG_POL}	Connect CC2 to GND with a 5.1kΩ resistor			3	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LED PWM output FREQ	f_{LED}		21	24	27	kHz
LED_PWM output duty	D_{LED}			50		%
Connected output	V_{ATTO}	USB Type-C connected, force 50μA			0.4	V
Power share input threshold	V_{TH_PS}		1.52	1.87	2.22	V
USB Charging Mode Identification						
BC1.2 DCP Mode						
DP and DM short resistance	$R_{DP_DM_SHORT}$	V_{DP} = 0.8V, I_{DM} = 1mA		30	70	Ω
Divider Mode						
DP output voltage	$V_{DIVIDER_DP}$	V_{OUT} = 5V	2.5	2.7	2.9	V
DM output voltage	$V_{DIVIDER_DM}$	V_{OUT} = 5V	3.05	3.3	3.55	V
DP output impedance	$R_{DIVIDER_DP}$			23		kΩ
DM output impedance	$R_{DIVIDER_DM}$			17		kΩ
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP_DM_1.2V}$	V_{OUT} = 5V	1.15	1.25	1.35	V
DP/DM output impedance	$R_{DP_DM_1.2V}$			75		kΩ
Quick Charge 3.0 Mode						
DP/DM low voltage	V_{QC_LOW}		0.2	0.3	0.4	V
DP/DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
QC mode entry voltage glitch time (QC identify) (8)	t_{QC_GLITCH}			1000		ms
DP output impendence	R_{DP_QC}			350		kΩ
DM output impendence	R_{DM_QC}			20		kΩ
Request voltage time (8)	$t_{V_NEW_REQUEST}$		200			ms
Output voltage change glitch time (8)	$t_{GLITCH_V_CHANGE}$		20		60	ms
Unplug V_{BUS} discharge time (8)	$t_{VBUS_DISC_QC}$				500	ms
CDP Mode						
DM CDP output voltage	V_{DM_SRC}	V_{DP} = 0.6V, DM sink = 250μA	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC} EN	V_{DAT_REF}		0.25	0.35	0.45	V
DP rising lower window threshold hysteresis	$V_{DAT_REF_HYS}$			30		mV
DP rising upper window threshold for V_{DM_SRC}	V_{LGC_SRC}		0.8	0.9	1	V
DP rising upper window threshold hysteresis	$V_{LGC_SRC_HYS}$			50		mV
FCP Mode						
DM Tx high voltage(8)	V_{FCPT_H}	R_{LOAD} = 15kΩ	2.55		5	V
DM Tx low voltage(8)	V_{FCPT_L}	R_{LOAD} = 15kΩ			0.4	V
DM Rx high voltage	V_{FCPR_H}		1.5		5	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DM Rx low voltage	V_{FCPR_L}				1	V
DM pull-low resistance	R_{LD_D-}			15		kΩ
Unit interval of PHY(8)	UI		144	160	176	µs
USB Type-C - CC1 and CC2 pins						
CC pull-up current 1	I_{RP1}	V_{BUS} = 5V @ 3A, T_J = 0°C to 85°C	-8%	330	+8%	µA
CC pull-up current 2	I_{RP2}	V_{BUS} = 5V @ 1.5A, T_J = 0°C to 85°C	-8%	180	+8%	µA
CC voltage to enable VCONN for 3A USB Type-C mode	V_{RA1}				0.75	V
CC voltage to enable VBUS for 3A USB Type-C mode	V_{RD1}		0.85		2.45	V
CC disconnect threshold for 3A USB Type-C mode	V_{OPEN1}		2.75			V
CC voltage to enable VCONN for 1.5A USB Type-C mode	V_{RA2}				0.35	V
CC voltage to enable VBUS for 1.5A USB Type-C mode	V_{RD2}		0.45		1.5	V
CC disconnect threshold for 1.5A USB Type-C mode	V_{OPEN2}		1.7			V
CC voltage falling de-bounce timer	$t_{CC_DEBOUNCE}$	VBUS enable deglitch	100	150	200	ms
CC voltage rising de-bounce timer	$t_{PD_DEBOUNCE}$	VBUS disable deglitch	5	10	15	ms
100mW VCONN output power	P_{VCONN_100mW}	Default	100			mW
1W VCONN output power	P_{VCONN_1W}	Set GPIO2 to 011b via the I^2C	1			W
USB PD						
Unit interval time (8)	t_{UI}		3.03		3.7	µs
Transmitter						
End drive BMC time (8)	t_{EDBMC}				23	µs
Falling time (8)	t_{FALL}		300	400		ns
Rising time (8)	t_{RISE}		300	400		ns
Hold low BMC time (8)	t_{HLBMC}		1			µs
Logic high voltage	V_{LH}		1.05		1.2	V
Logic low voltage	V_{LL}				70	mV
Output impedance	Z_{TX}			45		Ω
Receiver (8)						
CC receiver capacitance	$C_{RECEIVER}$				600	pF
Transitions for signal detection	$N_{TRANSITION}$		3			Edges
Rx bandwidth limiting filter	t_{RX_FILTER}		100			ns
Time window for detecting non-idle	$t_{TRANSITION_WINDOW}$		12		20	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = floating, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Receiver input impedance	Z_{BMC_RX}		1			MΩ
I²C Interface Specifications (8)						
Input logic high	V_{IH}	I²C pull-up VDD can be to 1.8V to 5V	1.26			V
Input logic low	V_{IL}				0.54	V
Output voltage logic low	V_{OUT_L}				0.45	V
SCL clock frequency	f_{SCL}			400		kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Set-up time for repeated start condition	t_{SU_STA}		160			ns
Hold time for repeated start condition	t_{HD_STA}		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	t_{SU_STO}		160			ns
Rising time of SCL and SDA	t_R		10		300	ns
Falling time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF
SCL low time	t_{LOW}		160			ns

Note:

8) Guaranteed by characterization sample test.

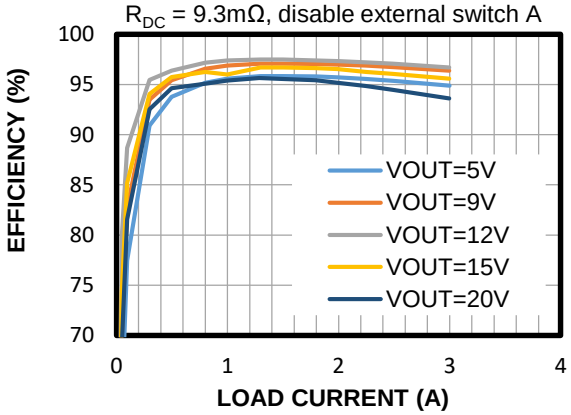
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TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

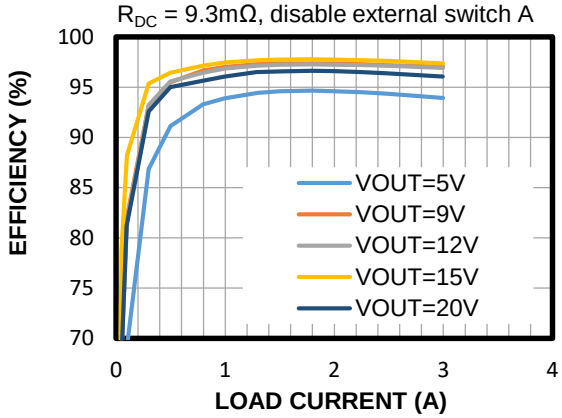
Efficiency vs. Load Current

V_{IN} = 9V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, disable external switch A



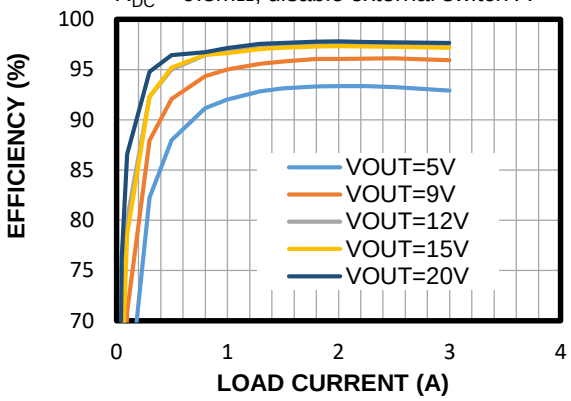
Efficiency vs. Load Current

V_{IN} = 12V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, disable external switch A

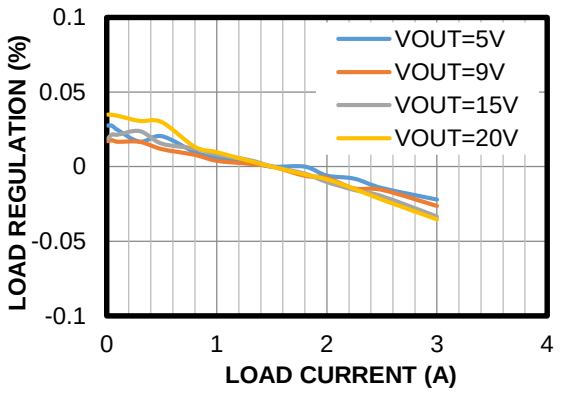


Efficiency vs. Load Current

V_{IN} = 16V, FCCM, L = 4.7µH,
R_{DC} = 9.3mΩ, disable external switch A

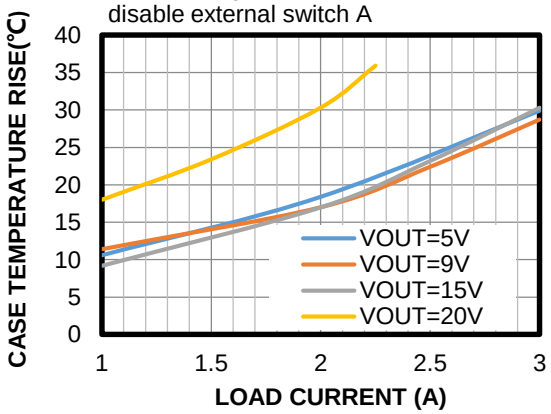


Load Regulation vs. Load Current



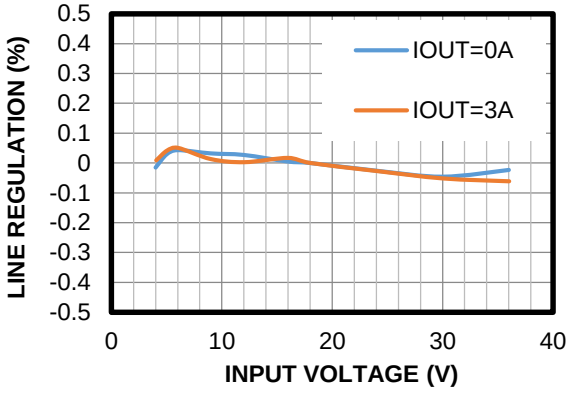
Case Temperature Rise

V_{IN} = 12V, f_{SW} = 420kHz, 4.3cmx5cm PCB,
disable external switch A



Line Regulation vs. Input Voltage

V_{OUT} = 5V, measured between VOUT and PGND

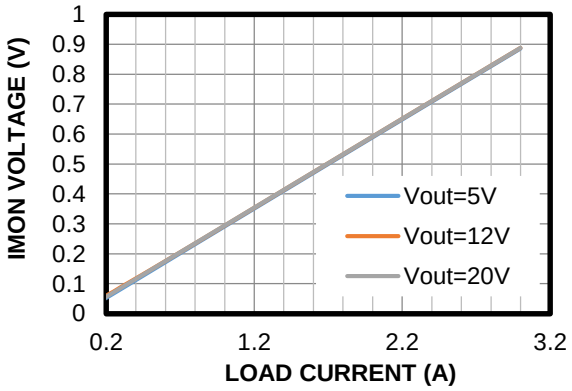


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TYPICAL CHARACTERISTICS *(continued)*

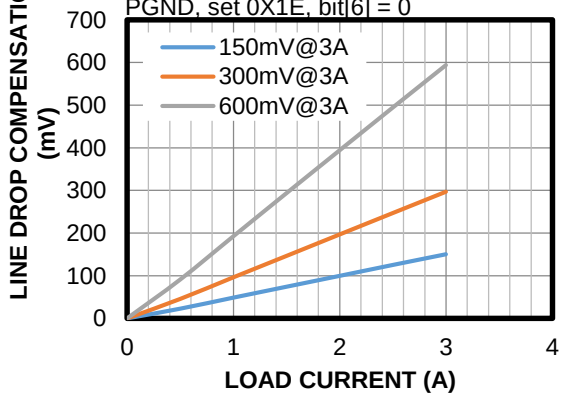
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

IMON Voltage vs. Load Current



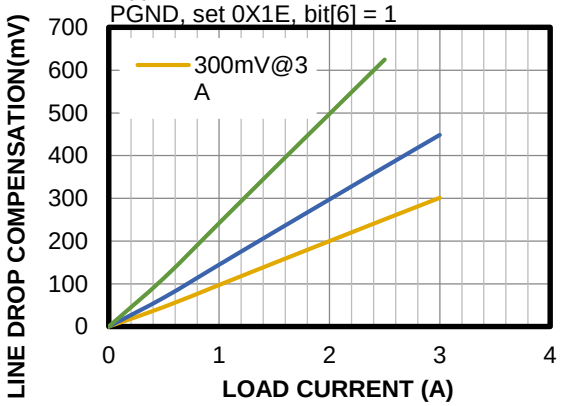
Line Drop Compensaton vs. Load Current

V_{OUT} = 5V, measured between VOUT and PGND, set 0X1E, bit[6] = 0

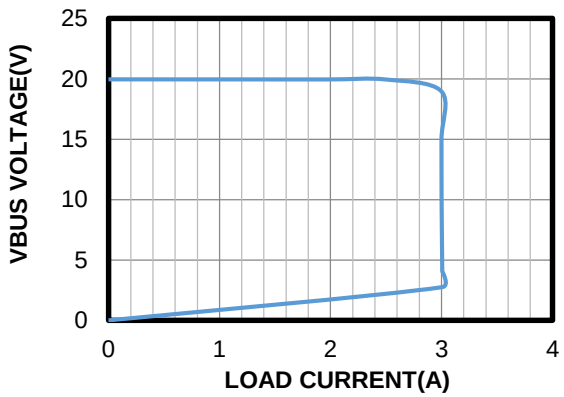


Line Drop Compensaton vs. Load Current

V_{OUT} = 5V,measured between VOUT and PGND, set 0X1E, bit[6] = 1



VBUS Voltage vs. Load Current

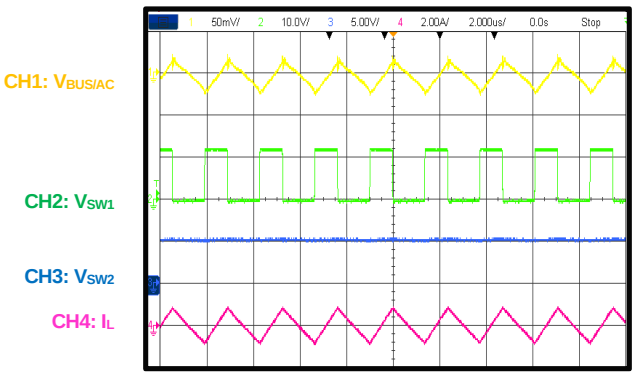


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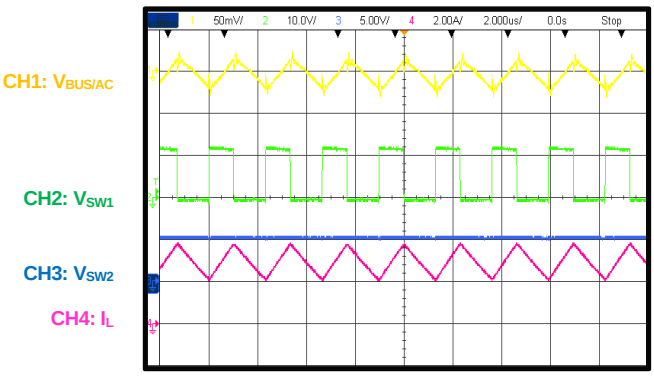
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

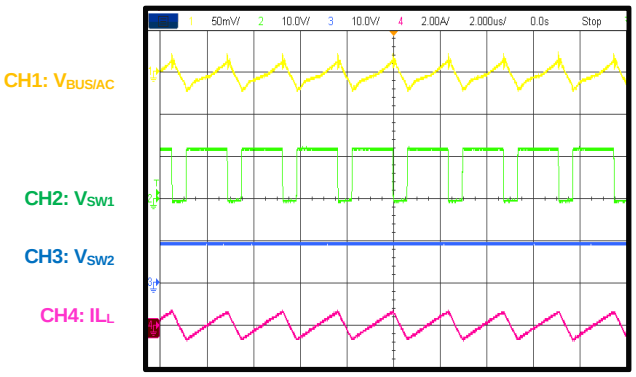
Output Voltage Ripple
V_{BUS} = 5V, load = 0A



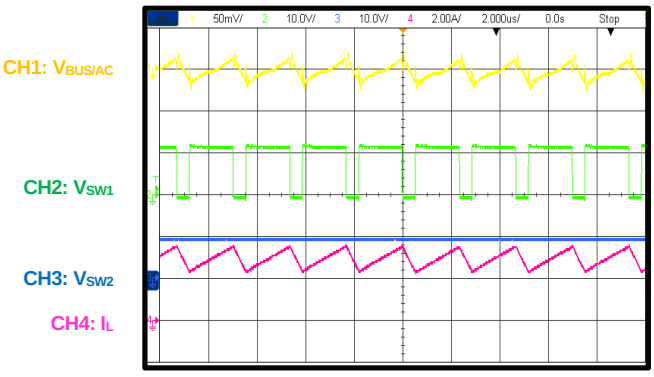
Output Voltage Ripple
V_{BUS} = 5V, load = 3A



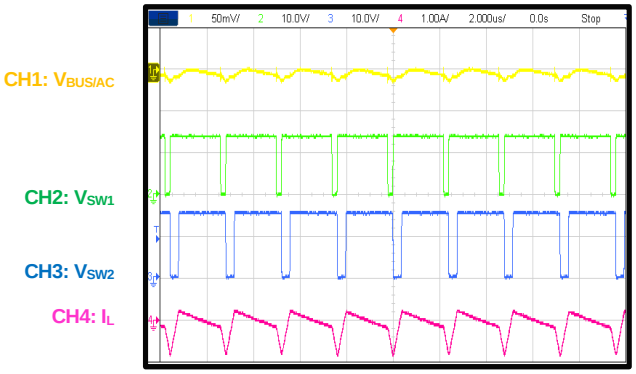
Output Voltage Ripple
V_{BUS} = 9V, load = 0A,



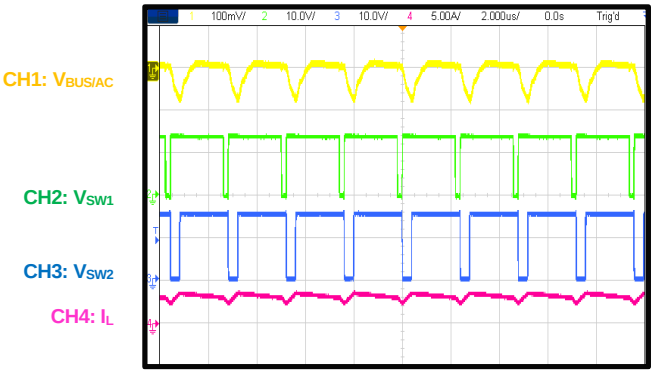
Output Voltage Ripple
V_{BUS} = 9V, load = 3A,



Output Voltage Ripple
V_{IN} = 14V, V_{BUS} = 15V, load = 0A



Output Voltage Ripple
V_{IN} = 14V, V_{BUS} = 15V, load = 3A



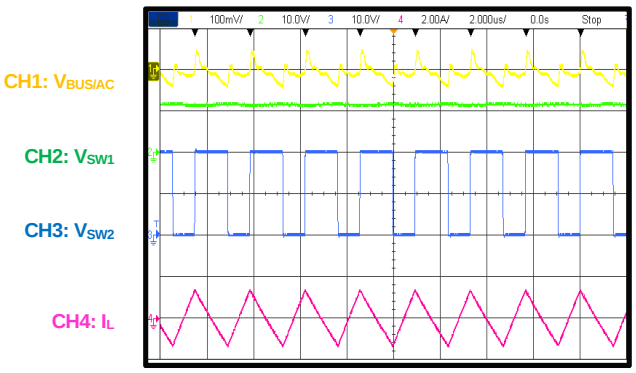
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

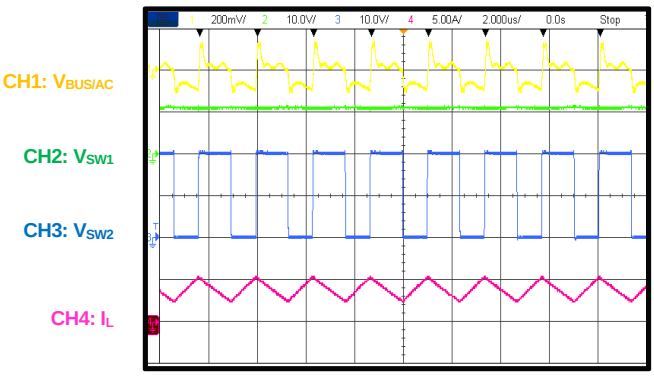
Output Voltage Ripple

V_{BUS} = 20V, load = 0A



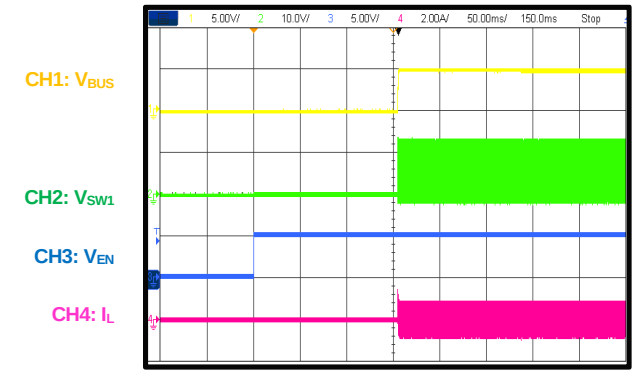
Output Voltage Ripple

V_{BUS} = 20V, load = 2.25A



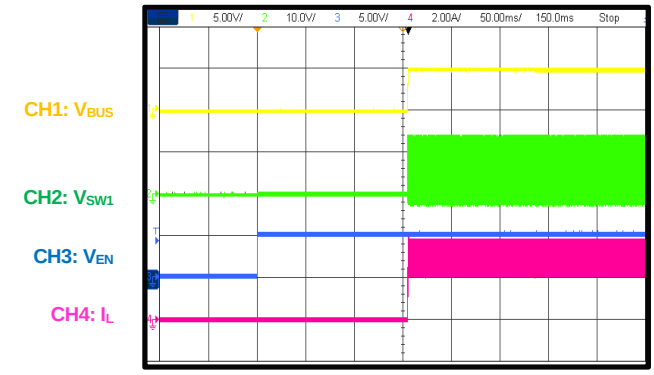
EN Pin Enabled

CC1 connected to a 5.1kΩ R_d resistor, load = 0A



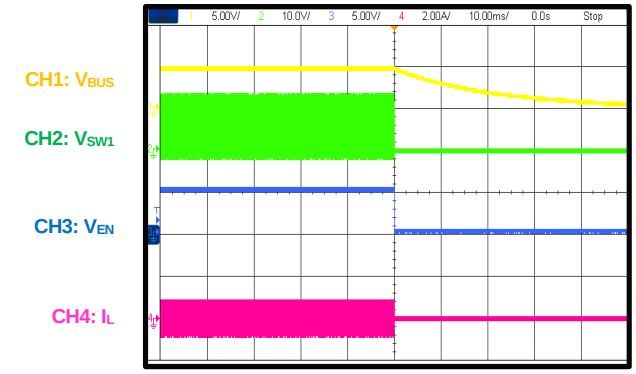
EN Pin Enabled

CC1 connected to a 5.1kΩ R_d resistor, load = 3A



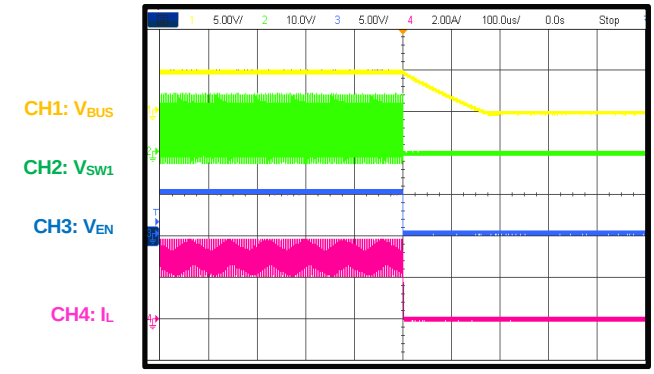
EN Pin Disabled

CC1 connected to a 5.1kΩ R_d resistor, load = 0A



EN Pin Disabled

CC1 connected to a 5.1kΩ R_d resistor, load = 3A



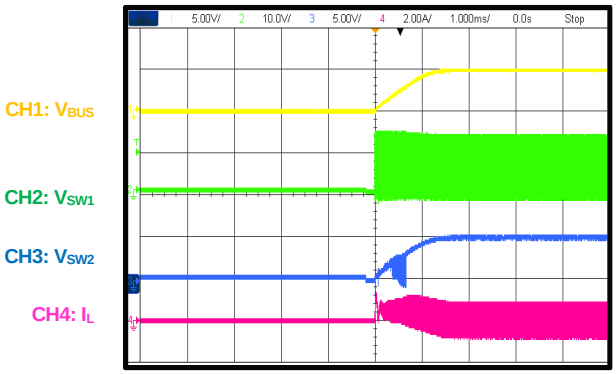
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

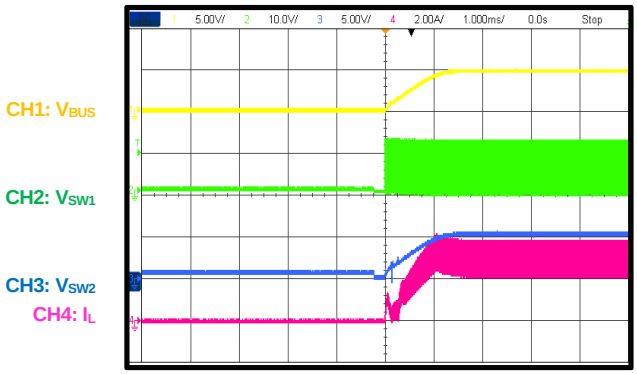
Input Start-Up

Load = 0A, CC1 connected to a 5.1kΩ R_d resistor



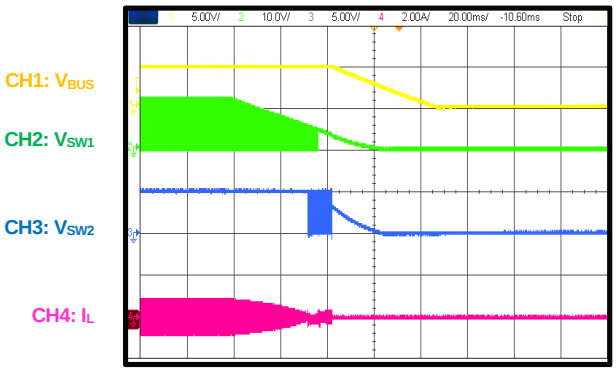
Input Start-Up

Load = 3A, CC1 connected to a 5.1kΩ R_d resistor



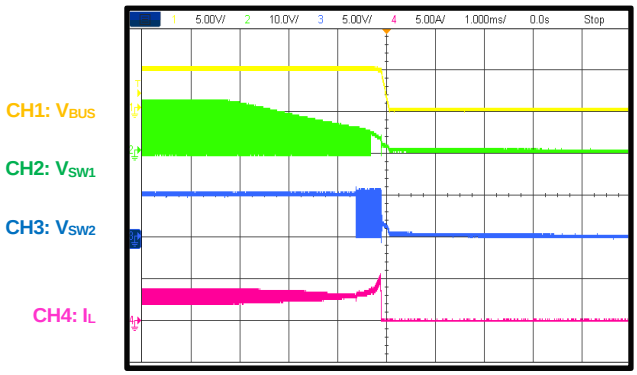
Input Shutdown

Load = 10mA

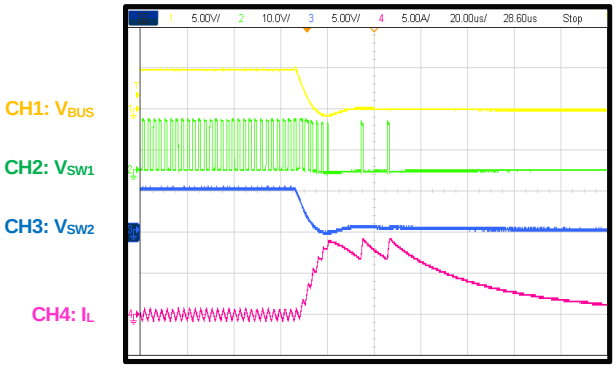


Input Shutdown

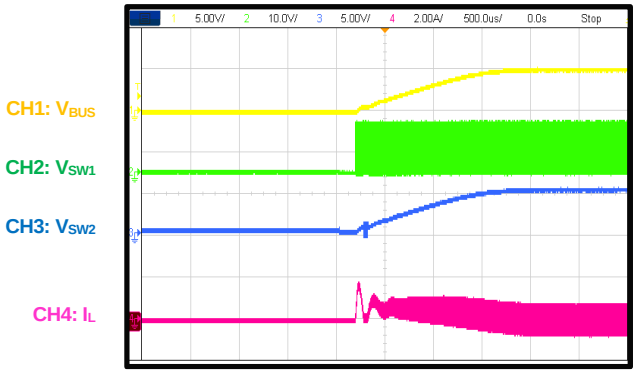
Load = 3A



SCP Entry



SCP Recovery

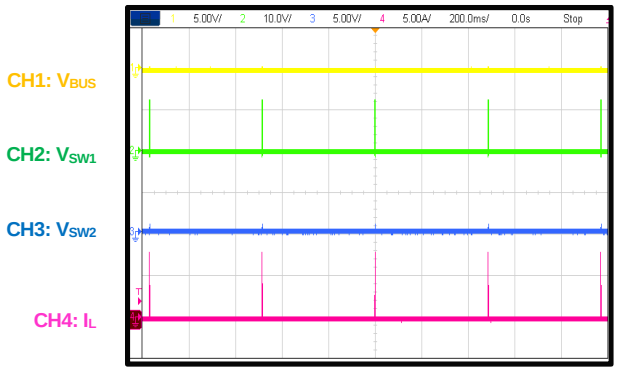


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

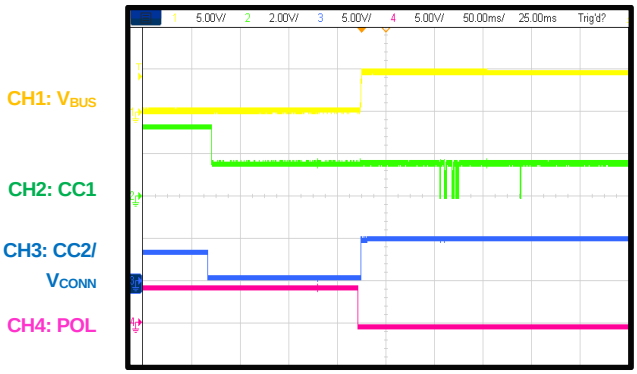
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

SCP Steady State



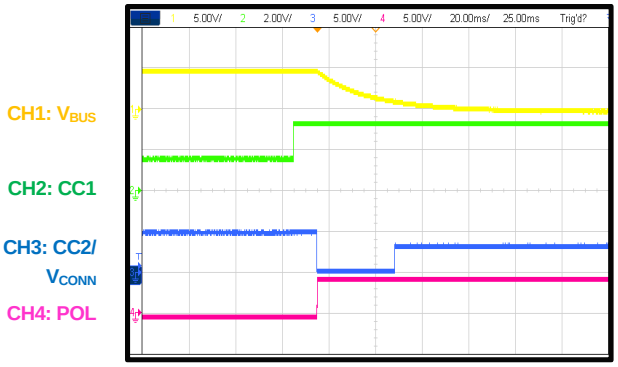
CC1 Connected to R_d to Enable VBUS

I_{OUT} = 0A, CC2 connected to a 1kΩ R_a resistor



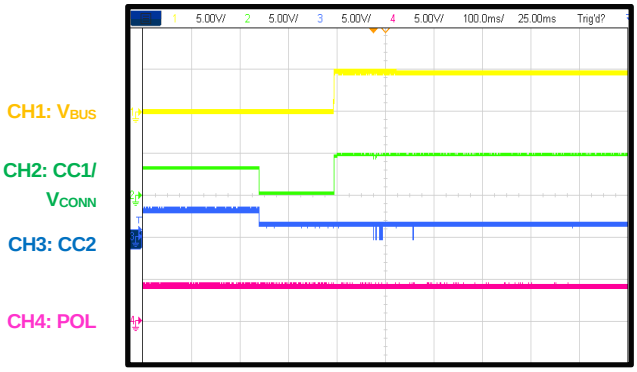
CC1 Disconnected from R_d to Disable VBUS

I_{OUT} = 0A, CC2 connected to a 1kΩ R_A resistor



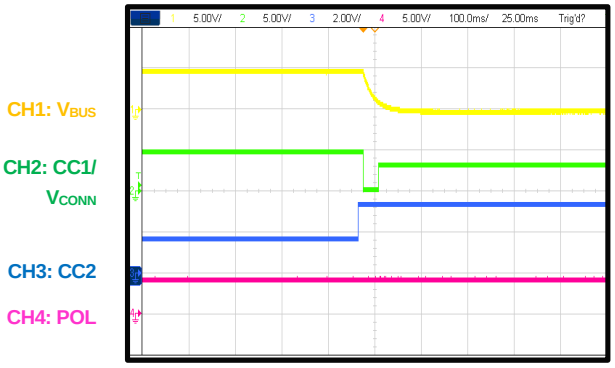
CC2 Connected to R_d to Enable VBUS

I_{OUT} = 0A, CC1 connected to a 1kΩ R_A resistor



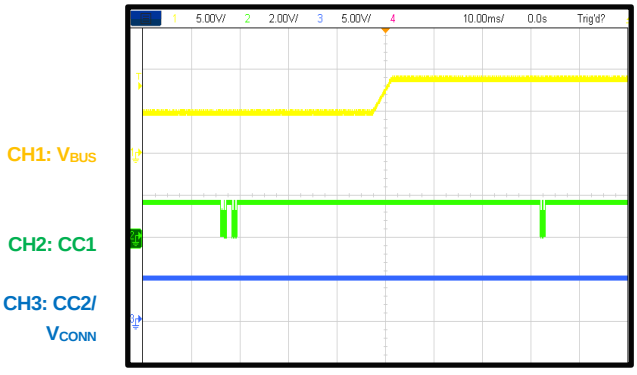
CC2 Disconnected from R_d to Disable VBUS

I_{OUT} = 0A, CC1 connected to1kΩ Ra resistor



PDO Transition

5V PDO to 9V PDO

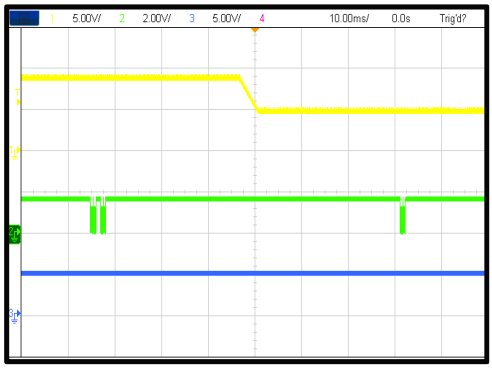


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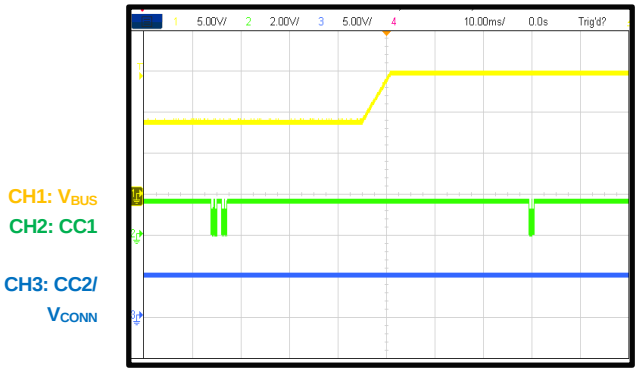
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

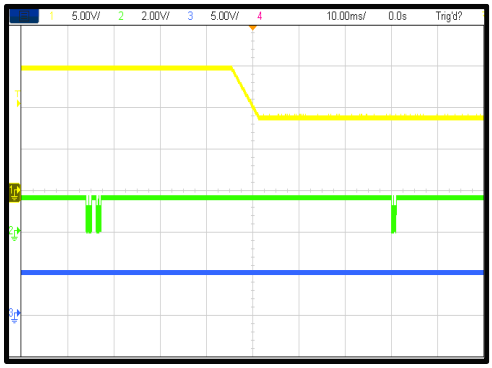
PDO Transition
9V PDO to 5V PDO



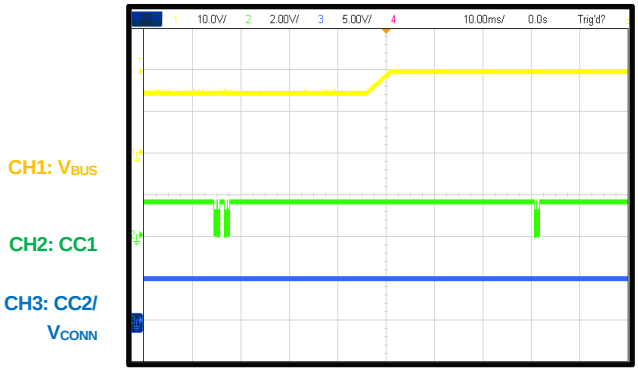
PDO Transition
9V PDO to 15V PDO



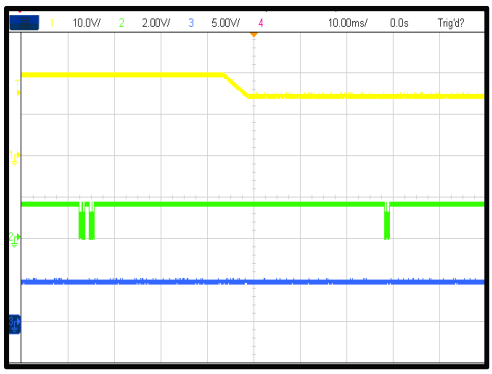
PDO Transition
15V PDO to 9V PDO



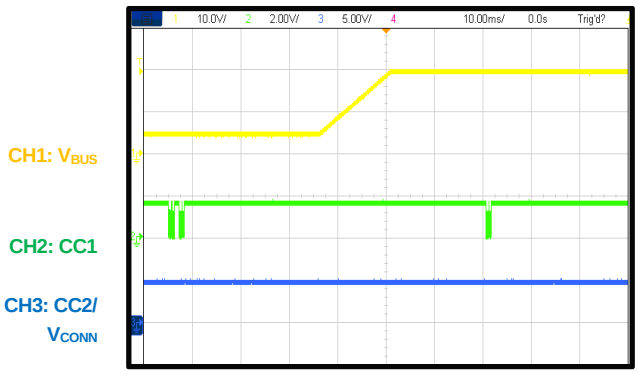
PDO Transition
15V PDO to 20V PDO



PDO Transition
20V PDO to 15V PDO



PDO Transition
5V PDO to 20V PDO



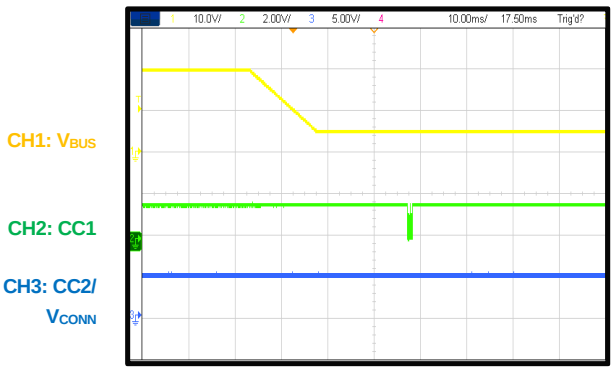
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

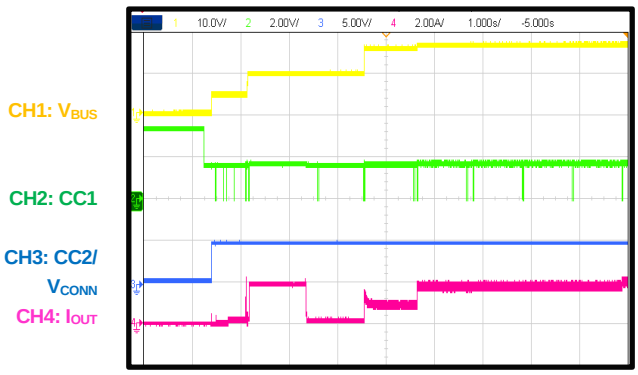
PDO Transition

20V PDO to 5V PDO



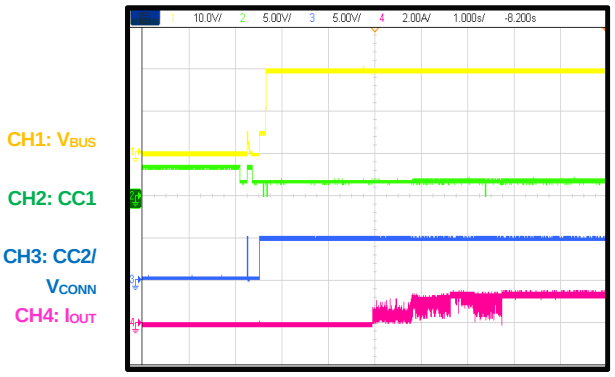
Mobile Phone Charging Test

Phone requests 3.3V to 21V APDO



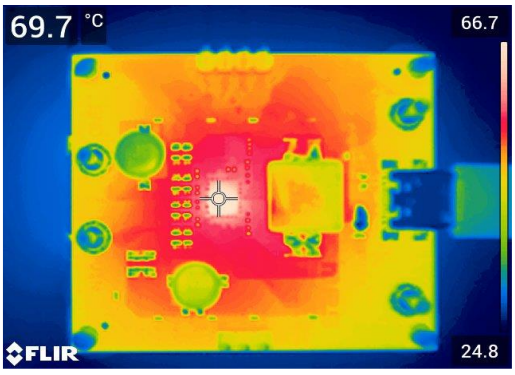
Laptop Charging Test

Laptop requests 20V PDO



Thermal Image

V_{IN} = 13.5V, V_{OUT} = 20V, I_{OUT} = 3A,
f_{SW} = 420kHz, 4.3cmx5cm PCB,
top/bottom layer: 2oz; mid-layer 1 and 2: 1oz,
enable external switch A



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FUNCTIONAL BLOCK DIAGRAM

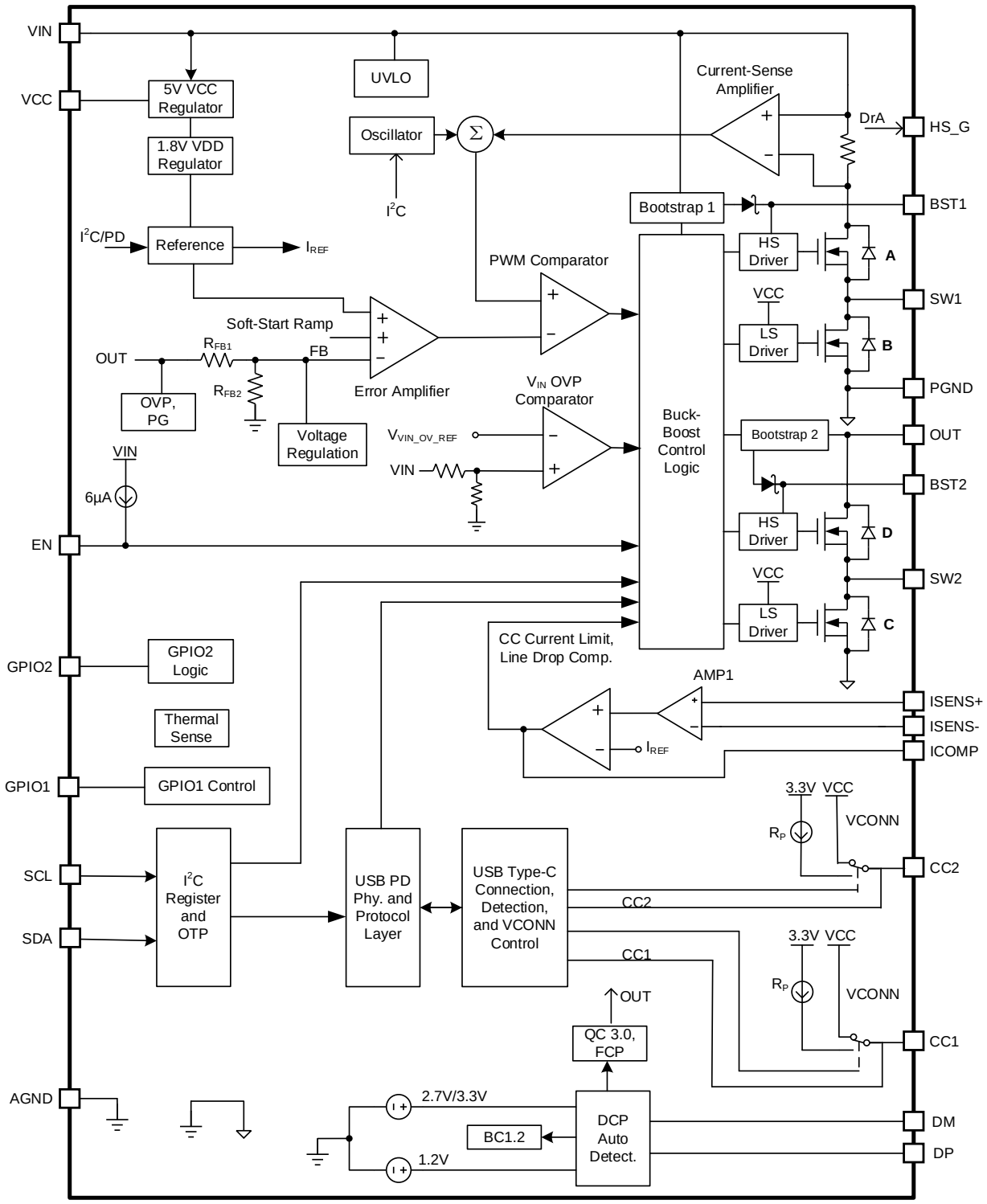


Figure 2: Functional Block Diagram

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OPERATION

The MPQ4242 is a buck-boost converter with four integrated switches and USB charging protocols. The buck-boost converter works in current mode, which provides a fast transient response for buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency across the full input range and smooths transitions between different modes. Figure 2 on page 21 shows the internal block diagram.

Pulse-Width Modulation (PWM) Operation

The MPQ4242 operates in a fixed-frequency peak current mode control to regulate the output voltage (V_{OUT}). The internal clock initiates the PWM cycle and turns on the related power switch. The switch remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle starts. The switching frequency (f_{SW}) can be configured to 250kHz or 420kHz via the I^2C.

Buck-Boost Operation

The MPQ4242 can regulate V_{OUT} to be above, below, or equal to the input voltage (V_{IN}). Figure 3 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

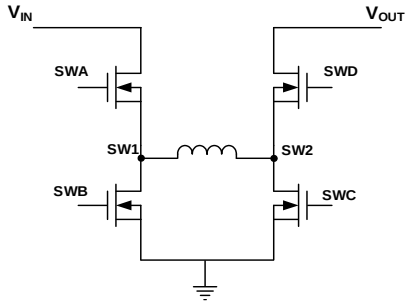


Figure 3: Buck-Boost Topology

Buck mode, boost mode, and buck-boost mode can have different V_{IN} inputs (see Figure 4).

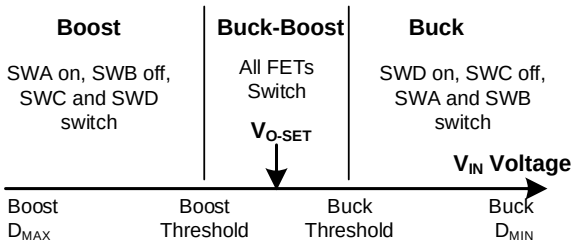


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} exceeds V_{OUT}, the MPQ4242 works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current (I_L).

SWA works with a peak current mode control logic, and SWB turns on until the t_{CLK} times out. In each buck mode cycle, SWA turns on to charge I_L. When I_L reaches the value set by V_{COMP}, SWA turns off and SWB turns on. SWB stays on until the next clock begins. Then SWA turns on and the cycle repeats. The COMP signal is the error amplifier (EA) output from the V_{OUT} feedback and the internal FB reference voltage. Figure 5 shows the buck mode waveform.

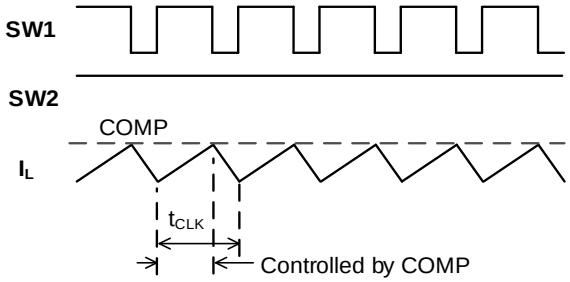


Figure 5: Buck Mode Waveform

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is below V_{OUT}, the MPQ4242 works in boost mode. In boost mode, SWC and SWD switch for boost regulation. Meanwhile, SWB is off and SWA stays on to conduct I_L

SWC turns on at the beginning of each clock cycle. SWC turns off when I_L reaches the value set by V_{COMP}. SWD turns on until t_{CLK} times out to boost I_L to the output. Figure 6 shows the boost work waveform.

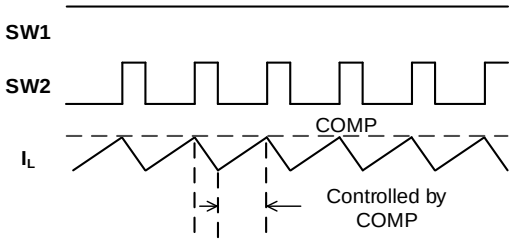


Figure 6: Boost Waveform

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Buck-Boost Mode (V_{IN} ≈ V_{OUT})

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MPQ4242 adopts buck-boost control to regulate the output (see Figure 7).

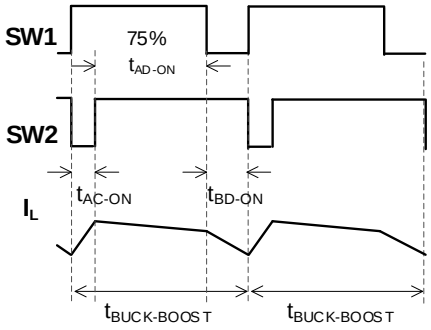


Figure 7: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, buck-boost mode activates. The MOSFET turn-on sequence is as follows:

1. SWA and SWC
2. SWA and SWD
3. SWB and SWD

Throughout this process, I_L can reach the V_{COMP} requirement, and supply enough current to the output.

The SWA and SWD turn-on time is fixed to 75% of the buck-boost operation frequency.

If the buck mode minimum off time is almost reached, the IC enters buck-boost mode. If V_{IN} is about 10% above V_{OUT} in buck-boost mode, the IC changes to buck mode. If V_{IN} is about 10% below V_{OUT}, the IC enters boost mode. If the boost mode minimum on time is almost reached, the IC enters buck-boost mode.

External High-Side MOSFET Gate Driver

An external N-channel MOSFET can be added to improve system efficiency, especially for PD applications exceeding 45W. For applications below 45W, an external MOSFET is not required, and EXT_HS_FET_RON should be set to 000b.

The external MOSFET is paralleled with the internal SWA. To accurately sense the input current, a 5mΩ to 12mΩ $R_{DS(ON)}$ MOSFET is recommended. The EXT_HS_FET_RON configuration value should match (or be close to) the MOSFET's real $R_{DS(ON)}$ under a $10V_{GS}$ condition. The external MOSFET only turns on in boost mode when V_{IN} is significantly below V_{OUT}.

5V Internal VCC Regulator

The 5V internal regulator powers the CC pin's pull-up, VCONN, and most of the internal logic circuitries. The regulator takes the VIN input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, the regulator's output is in full regulation. If V_{IN} is below 5V, the output decreases with V_{IN}.

The VCC pin can support 0.1W of output power (P_{OUT}). The VCC pin requires a 2.2µF ceramic decoupling capacitor.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ4242's UVLO comparator monitors V_{IN}.

Internal Soft-Start

Soft start prevents the converter's V_{OUT} from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 5V. When SS is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference. The SS time is internally set to 1ms for a 5V V_{OUT}.

If the output of the MPQ4242 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal soft-start capacitor exceeds the internal feedback voltage.

Constant Current (CC) Mode Over-Current-Protection (OCP)

The MPQ4242 senses the ground current via an external current-sense resistor. The device uses this information to limit the output current (I_{OUT}). This is a highly accurate current limit. If I_{OUT} exceeds the current-limit threshold, the MPQ4242 enters constant current (CC) limit mode, and the current amplitude is limited.

If the MPQ4242 works in fixed PDO mode, it sends a hard reset message once I_{OUT} exceeds the constant current limit. If the MPQ4242 works

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in APDO mode and continues to reduce the load resistance, V_{OUT} drops until reaches its under-voltage (UV) threshold (about 3V). If a UV condition is triggered, the MPQ4242 sends a hard reset message. If I_{OUT} still exceeds the over-current protection (OCP) threshold, the MPQ4242 enters hiccup mode to periodically restart the part.

This protection is especially useful when the output is dead-shorted to ground. This operation greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4242 exits hiccup mode once the OC condition is removed.

The current limit threshold can be set from 1A to 6.35A (with a 50mA resolution) via the I^2C.

Peak and Valley Current Limit.

In addition to the output CC limit, the MPQ4242 also has SWA peak current and SWB valley current limits.

In buck mode and buck-boost mode, both the SWA peak current limit and the SWB valley current limit work as thresholds. The SWB's valley current limit has a 6.7A falling threshold. In boost mode, only the SWA peak current limit threshold operates. The peak current limit can be configured via the I^2C or one-time-programmable (OTP) memory.

Output Over-Voltage Protection (OVP)

The MPQ4242 has output over-voltage protection (OVP). If V_{OUT} exceeds 117% of V_{REF}, SWA, SWB, SWC, and SWD turn off. The resistor discharge path from the OUT pin to ground turns on. When V_{OUT} drops to 107% of V_{REF}, the chip returns to normal operation.

The absolute output OVP threshold is about 25V. The discharge resistor turns on when absolute OVP is triggered.

Input Over-Voltage Protection (V_{IN} OVP)

The MPQ4242 has input OVP. If V_{IN} exceeds its OVP rising threshold (about 22V), SWA, SWB, SWC, and SWD turn off. The chip returns to normal operation when V_{IN} drops to its OVP falling threshold (about 20V).

V_{IN} OVP if disabled by default, and it is controlled by OTP trimming. The MPQ4242-0000 does not have V_{IN} OVP. The MPQ4242-0001 provides V_{IN} OVP.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. Its UVLO rising threshold is 2.2V, with a hysteresis of 150mV. The BST1 capacitor's voltage is regulated internally by VCC through D2, M1, and C4. The BST2 capacitor's voltage is regulated internally by VCC through D3, M2, and C5 (see Figure 8).

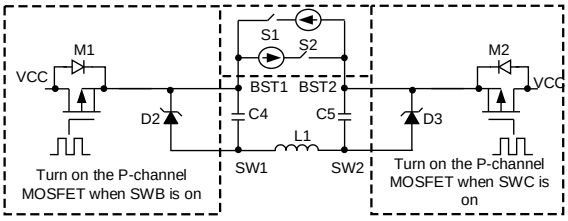


Figure 8: Internal Bootstrap Charging Circuit

In buck mode, S2 is always on, and BST2 is charged by BST1. In boost mode, S1 is always on, and BST1 is charged by BST2.

Output Line Drop Compensation

The MPQ4242 is capable of compensating for a V_{OUT} drop.

If I_{OUT} is 0A, there is no compensation. If I_{OUT} is 3A, the line drop compensation voltage is 150mV. For example, if the USB output current exceeds 3A, the line drop compensation voltage stays at 150mV and does not rise. The line drop compensation value can be set to 150mV, 300mV, or 600mV via 0x18, bits[2:1]. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Then the line drop compensation value can be set to 300mV, 450mV, or 750mV when the load is 3A.

Line drop compensation can be configured via the I^2C or OTP. The compensated voltage is the same for all voltages.

For the default IC, line drop compensation is disabled in PPS mode. Line drop compensation can be enabled in PPS mode through factory OTP trimming.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures.

If the silicon die temperature exceeds 175°C, the whole chip shuts down. When the temperature

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falls below its lower threshold (about 155°C), the chip is enabled again.

CHARGING MODE AUTO-DETECTION

Legacy USB 2.0 Mode

The MPQ4242 integrates a USB-dedicated charging port automatic detection function that recognizes most mainstream portable devices. The device supports the following charging schemes:

- USB battery charging specification (BC1.2) / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple 3A Divider Mode
- 1.2V/1.2V Mode
- QC 3.0
- Huawei FCP Class A

The automatic detection function is a state machine that supports all of the above DCP charging schemes. This function starts in 3A divider mode. If a device compliant to divider mode is connected, the MPQ4242 stays in divider mode. Meanwhile, 3.3V is applied to the DM pin, while 2.7V is applied to the DP pin.

If a BC1.2 or YD/T 1591-2009 compliant device is connected, the MPQ4242 operates in 1.2V/1.2V and BC1.2 DCP mode. In this scenario, DM and DP are shorted together with a resistance. The device then stays in this mode until the data line is released. If this occurs, the MPQ4242 returns to 3A divider mode.

When a QC 3.0 or FCP device (without PD protocol) is connected, the MPQ4242 can automatically enter high-voltage, quick charge mode.

The MPQ4242 supports BC1.2 charging downstream port (CDP) handshaking as well. This can be enabled by setting CDP_EN to 1b via the I^2C.

If a USB PD contract is established after the sink is connected, the QC 3.0 and FCP functions are disabled.

USB Type-C Port

The USB Type-C receptacle, plug, and cable solution incorporates a configuration process to detect a downstream facing port (DFP) to upstream facing port (UFP) connection. This detection function is used for V_{BUS} management and can determine the host-to-device connection.

Initially, a DFP-to-UFP connection is detected by a host (DFP) when one of the CC pins at its USB Type-C receptacle senses a specified resistance at GND. Subsequently, DFP-to-UFP disconnect is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer connected to GND via a specified resistance.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the DFP detects the presence of a connected device (UFP) port. When a DFP-to-UFP connection is detected, the DFP is expected to enable power to the receptacle and proceed to normal USB operation with the connected device. When a DFP-to-UFP disconnect is detected, the port sourcing V_{BUS} removes power.

The MPQ4242's power supply capability is rated for 5V @ 3A by default. V_{CONN} is provided by the DFP to power cables with electronics that are plugged in. V_{CONN} is provided power over the CC pin that is not connected to the cable's CC wire. The maximum output power of V_{CONN} is 1W.

VCONN is disabled until R_A is detected. R_A is a pull-down resistor connected from the CC pin to GND. It resistance must be below 1.2kΩ.

USB Power Delivery (PD) 3.0

In USB power delivery (PD), pairs of directly connected ports negotiate the voltage, current, and/or the direction of power flow over the USB cable, using VBUS or the CC wire as the communication channel. The mechanisms used operate independently of other USB methods that negotiate power. USB Type-C connectors can support the CC wire as the communication channel.

The USB PD engine can disable the clock and enter sleep mode if no PD command is detected. The input current is typically 150μA in sleep mode. Figure 9 on page 26 shows the USB PD communication stack.

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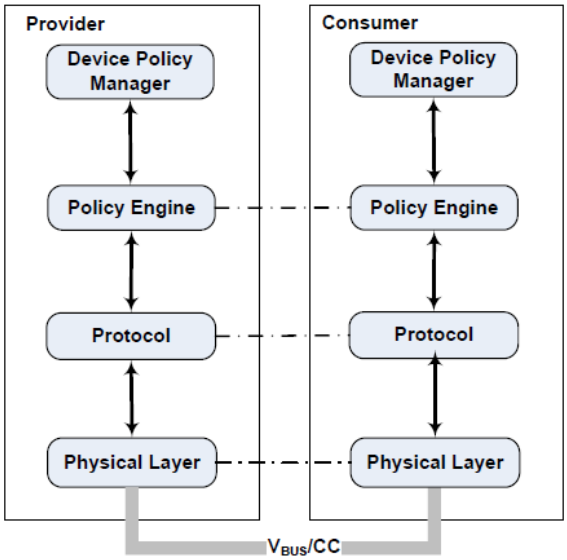


Figure 9: USB PD Communication Stack

Table 1 shows the functions and DFP commands supported by the MPQ4242.

Table 1: Control Message

Transmitted Message	Received Message
ACCEPT	GET_PPS_STATUS
GET_STATUS	GET_STATUS
GOODCRC	GOODCRC
NOT_SUPPORTED	NOT_SUPPORTED
PS_RDY	REJECT
REJECT	SOFT_RESET
SOFT_RESET	HARD_RESET
HARD_RESET	VCONN_SWAP
-	GET_SOURCE_CAP
-	GET_SOURCE_CAP_ EXTENDED

Table 2 shows the data messages.

Table 2: Data Message

Transmitted Message	Received Message
SOURCE_CAPABILITIES	SINK_CAPABILITIES
BIST	REQUEST
ALERT	BIST
-	ALERT

Table 3 shows the extended messages.

Table 3: Extended Message

Transmitted Message	Received Message
STATUS	-
PPS_STATUS	-
SOURCE_ CAPABILITIES_ EXTENDED	-

FIgure 10 shows the MPQ4242's device policy manager function block.

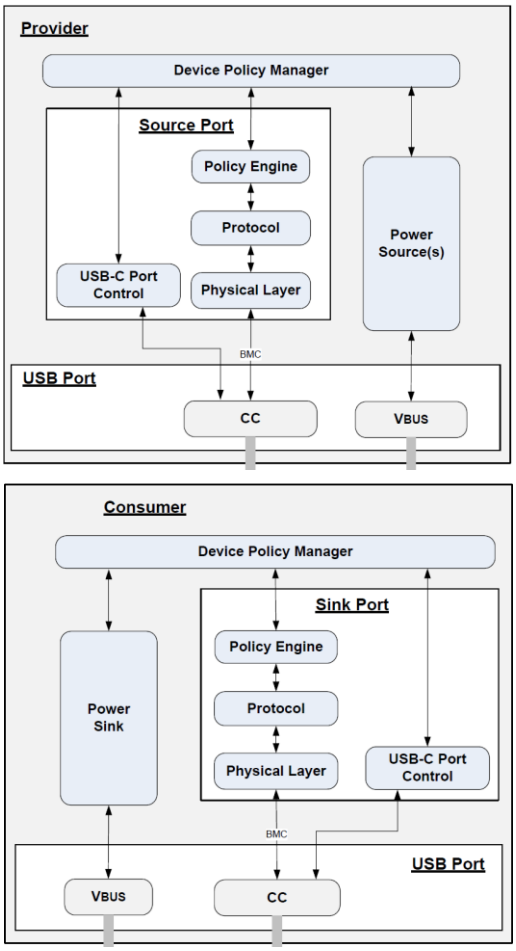


Figure 10: Device Policy Manager

Figure 11 shows a PD contract handshake sequence for the MPQ4242.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 11: PD Contract Handshake

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VCONN Power Supply

The integrated VCONN power supply has a maximum of 100mW. The power switch connected from VCC to VCONN has a current limit. During a VCONN short to ground event, the MPQ4242 turns off VCONN.

For a 1W VCONN application, an external VCONN supply should be applied to GPIO2.

LED PWM Driver

The GPIO2 pin can be configured as a PWM output to drive an LED. By default, it is 25kHz, with a 50% duty cycle PWM and a maximum 15mA capability.

The PWM duty cycle can be set between 5% and 100% (with a 1% resolution) via the I^2C.

EN Off Time

The MPQ4242 has a configurable EN off time. When the EN pin is pulled low, the device operates at full functionality until the timer elapses. The maximum EN off delay is 120 minutes. If the EN pin is pull high within this time, the counter is reset.

Current Monitor Output

When the GPIO1 pin is set as IMON, the MPQ4242 senses the average load current through a current-sense resistor. The IMON amplifier outputs a voltage signal on the GPIO1 pin. This signal is amplified from the voltage difference between the ISEN+ and ISEN- pins. It is recommended to place a 4.7nF + 4.7kΩ filter on the GPIO1 pin (see Figure 12). The minimum load that IMON can recognize is 0.2A.

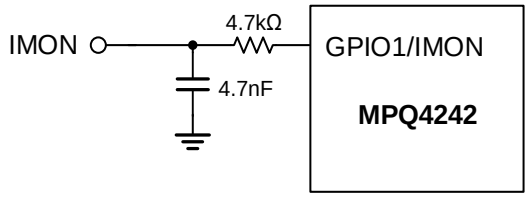


Figure 12: IMON Connection

The relationship between the IMON voltage and the load current can be calculated with Equation (1):

$$V_{IMON} = Gain \times I_{OUT} \times R_{SENS} \quad (1)$$

Where Gain is 27.5V/V, and R_{SENS} = 10mΩ.

When automatic PFM/PWM mode is set up, the IMON function can only work normally when the part enters continuous conduction mode (CCM).

NTC Function

When the GPIO2 pin is set to the NTC function, the device compares the NTC voltage to V_{REF}. If the NTC voltage is below the threshold, the MPQ4242 initiates thermal shutdown protection. In this scenario, the device will either shut down or reduce the PD power. The response can be selected via NTC_MODE.

If NTC_MODE is set to 1, OTW2_NTC_PDP determines the value to which PD power should be reduced. OTW2_NTC_PDO_SELECT sets which PDO voltage is enabled after entering NTC mode. See Table 4 on page 29 for more details.

It the NTC voltage rises above the recovery threshold, the device recovers to a normal state. The I^2C can set one of two NTC recovery hysteresis values. There is no 16s recover delay.

NTC2 Function

When the GPIO1 pin is set to the NTC2 function, the device compares the NTC2 voltage to V_{REF}. If the NTC2 voltage drops below this threshold, the MPQ4242 triggers power sharing. When the power share function is triggered, PD power rating drops to the value set by PS_PDP_THD. Table 4 on page 29 shows the PDO / APDO voltage and current.

If the NTC2 voltage rises above the recovery threshold, the MPQ4242 exits power sharing. NTC_HYSTERESIS sets the hysteresis, which is also sets the hysteresis for the GPIO1 pin's NTC function.

The NTC_MODE, OTW2_NTC_PDO_SELECT, and OTW2_NTC_PDP bits do not control the NTC2 pin's behavior.

If GPIO2 is set to the power share function while GPIO1 is set for the NTC2 function, the MPQ4242 enters power sharing when either NTC2 or GPIO2_POWER_SHARE is triggered.

Battery to Ground Short Protection Driver

The GPIO1 pin can be set to the GATE function for GND to battery short protection. If a battery to output ground (GND2) short occurs, the GATE pin pulls low and Q2 turns off. Figure 13 on page 28 shows the battery to ground short driver.

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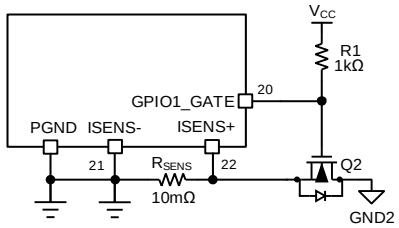


Figure 13: Battery Short-to-Ground Driver

Over Temperature Warning (OTW) Function

The MPQ4242 senses its die temperature internally. If the chip's temperature exceeds the OTW1 threshold, the MPQ4242 reduces the PD power state to the value set by OTW1_PDP. OTW1_PDO_SELECT sets which PDO voltage is enabled after entering OTW1 mode. Table 4 on page 29 shows the OTW_PDO_SELECT function.

If the die temperature continues increasing and triggers the second threshold set by OTW2, the MPQ4242 reduces the PD power to the level set by OTW2_NTC_PDP.

OTW2_NTC_PDO_SELECT sets which PDO voltage is enabled. The MPQ4242 waits 16 seconds after the OTW condition is removed before recovering to a normal PD rating.

Low-Battery Operation

During the first V_{IN} start-up, the MPQ4242 is delayed for 1s before detecting V_{IN}.

If the MPQ4242 detects that the battery voltage (its VIN voltage) is lower than the VBATT_LOW_THLD1 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW1_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT_L1_PDO_SELECT.

If the MPQ4242 detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD2 falling threshold for the VBATT_LOW_BLK deglitch time, it reduces the PD power rating according to the set value. Meanwhile, VBATT_LOW2_FLAG is set. If there is a PD contract, the PD engine resends the updated PDO with a reduced PDP. The PDO list is determined by VBATT_L2_PDO_SELECT.

If the MPQ4242 detects that the battery voltage (its VIN voltage) is below the VBATT_LOW_THLD3 falling threshold for the VBATT_LOW_BLK deglitch time, it shuts down.

When the battery voltage recovers and exceeds the VBATT_LOW_THLD rising threshold with a 1s digital deglitch time, the PDO recovers to normal PDP.

There are three battery voltage (V_{BATT}) low thresholds: VBATT_LOW_THLD1, VBATT_LOW_THLD2, and VBATT_LOW_THLD3. Accordingly, VBATT_LOW1_PDP and VBATT_LOW2_PDP define the MPQ4242's reduced PDP level. During the MPQ4242's first start-up, the internal VBATT_LOW_FLAG default state is 0. The VBATT_LOW detection circuitry starts to work when a USB Type-C receptacle is attached; it is reset by UVLO or an EN shutdown.

POWER SHARE FUNCTION

GPIO1_POWER_SHARE

The GPIO1_POWER_SHARE pin can accept an external input voltage. If the second MPQ4242 (MPQ4242-B) detects that a valid sink is attached in, the first MPQ4242's (MPQ4242-A) GPIO1_POWER_SHARE pin is pulled down by the MPQ4242-B's GPIO2_ATTACH pin (see Figure 14).

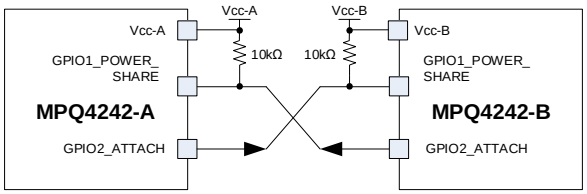


Figure 14: Power Share Connection Between Two MPQ4242s (e.g. Cut Total Power to 50% / 50%)

When the power share function is triggered, the PDO list and current are determined by PS_PDP_THD and PS_PDP_THD_PDO_SELECT (see Table 4 on page 29). For example, a 3.3V to 21V APDO current rating is can be calculated as 45W / 21V = 2.1A.

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Table 4: PDO Voltage and Current Set Table based on the PS_PDP_THD and PS_PDP_THD_PDO_SEL

PDO List	5V (Fixed)	9V (Fixed)	12V (Fixed)	15V (Fixed)	20V (Fixed)	5V (Prog.)	9V (Prog.)	15V (Prog.)	20V (Prog.)
Output Current	PDP / 5 (9)	PDP / 9	PDP / 12	PDP / 15	PDP / 20 (10)	PDP / 5.9	PDP / 11	PDP / 16	PDP / 21 (10)
PS_PDP_THD_ PDO_SEL Register Selection Bit (13)	x	1	0	1	1	1	1	0	0
PS_PDP_THD = 22.5W	5V, 3A (11)	9V, 2.5A	-	15V, 1.5A	20V, 1.13A	3.3V to 5.9V, 3A (12)	3.3V to 11V, 2A	-	-

Notes:

9) A fixed 5V PDO is always enabled after enter power sharing.
10) The fixed PDO current is equal to PDP / Voltage. The maximum current is 3A for <20V fixed PDOs. The maximum current can be 5A for 20V PDO and all APDOs.
11) The minimum PDP is 5V x 1.5A = 7.5W. R_P changes to 5V / 1.5A when PDP <15W.
12) The PPS current is calculated with PDP / 5.9V for 5V PPS; PDP / 11V for 9V PPS; PDP / 16V for 15V PPS; PDP / 21V for 20V PPS.
13) The registers PS_PDP_THD, PS_PDO_SELECT, VBATT_L1_PDO_SELECT, VBATT_L2_PDO_SELECT, OTW1_PDO_SELECT, and OTW2_NTC_PDO_SELECT share the same format. The gray cells are set by 8-bit register values.

GPIO2_POWER_SHARE

The GPIO2_POWER_SHARE threshold is V_{TH_PS} (typically 1.87V). When the GPIO2 pin is set for the power share function, and the MPQ4242-A detects that its GPIO2 voltage exceeds V_{TH_PS}, the power share function is triggered. In this scenario, the PDO list and current is determined by PS_PDP_THD and PS_PDP_THD_PDO_SELECT (see Table 5).

Table 5: PDO Voltage and Current Set Table based on PS_PDP_THD and PS_PDP_THD_PDO_SEL

PDO List	5V Fixed	9V Fixed	12V Fixed	15V Fixed	20V Fixed	5V Prog.	9V Prog.	15V Prog.	20V Prog.
Output Current	PDP / 5 (9)	PDP / 9	PDP / 12	PDP / 15	PDP / 20 (10)	PDP / 5.9	PDP / 11	PDP / 16	PDP / 21 (10)
PS_PDP_THD_ PDO_SEL Register Selection Bit (13)	x	1	0	0	0	1	1	0	0
PS_PDP_THD = 15W	5V, 3A (11)	9V, 1.6A	-	-	x	3.3V to 5.9V, 3A (12)	3.3V to 11V, 1.35A	-	-

The MPQ4242 exits the power sharing status after the GPIO2 voltage drops below V_{TH_PS}. Figure 15 shows the GPIO2_POWER_SHARE connection block.

When V_{BUS} exceeds 11.2V, the power share function is triggered.

Table 6 on page 30 shows the PDP of the MPQ4242-A and MPQ4242-B in the GPIO2_POWER_SHARE function.

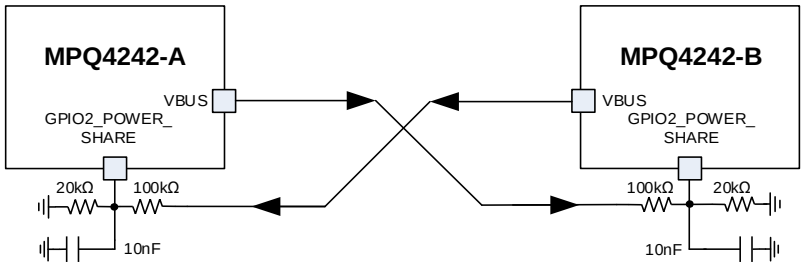


Figure 15: GPIO2 Power Share Connection Between Two MPQ4242s

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Table 6: GPIO2 Power Share PDP Management In Dual-Channel Application (14)

Column Format = <PD Contract W> (<Advertised Power W>)
Total Shared Power = 60W
Each Port PDP = 45W

Condition	USB Type-C Port 1	USB Type-C Port 2	Total Power
1	-- (45W) (15)	-- (45W) (15)	-
2	15W (45W)	-- (45W) (15)	15W
3	27W (45W)	-- (45W) (15)	27W
4	45W (45W)	15W (15W)	60W
5	27W (45W)	15W (45W)	42W
6	27W (45W)	27W (45W)	54W
7	15W (15W)	45W (45W)	60W
8	-- (15W) (16)	45W (45W)	45W
9	-- (45W) (15)	27W (45W)	27W

Notes:

14) The PDP table is based on the GPIO2_POWER_SHARE set-up in Figure 15 on page 29. The MPQ4242-A triggers power sharing when the MPQ4242-B's V_{BUS} >11.2V.
15) The port is not connected and there is no valid PD contract, but the maximum PDP (45W) is still advertised.
16) Power sharing has been triggered because another port has made a PD contract with a high PDP. To limit the total shared power to 60W or less, the advertised power drops to 15W.

Figure 16 shows the PDP state machine. Figure 17 on page 31 shows the PDP foldback scheme.

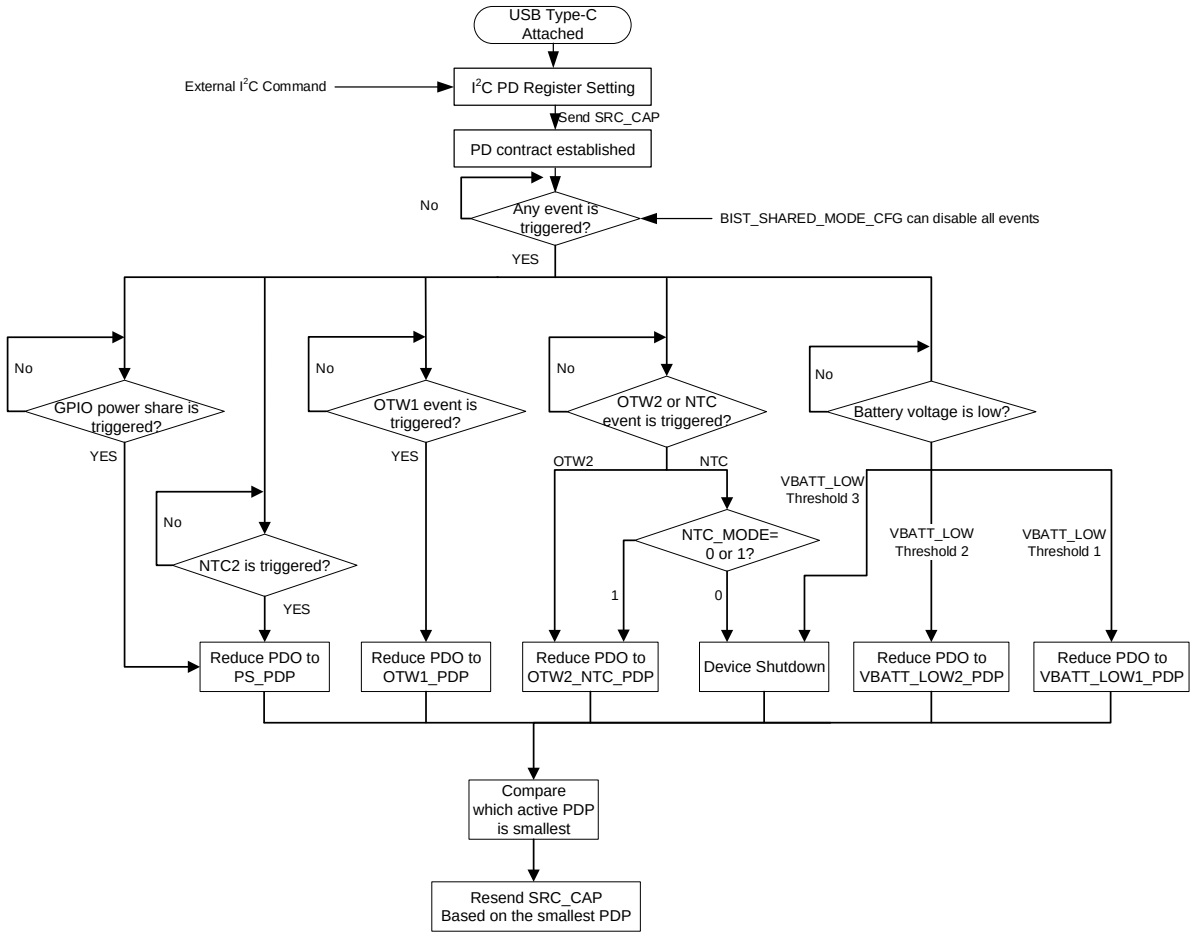


Figure 16: PDP State Machine (I²C Still Operates during NTC Shutdown)

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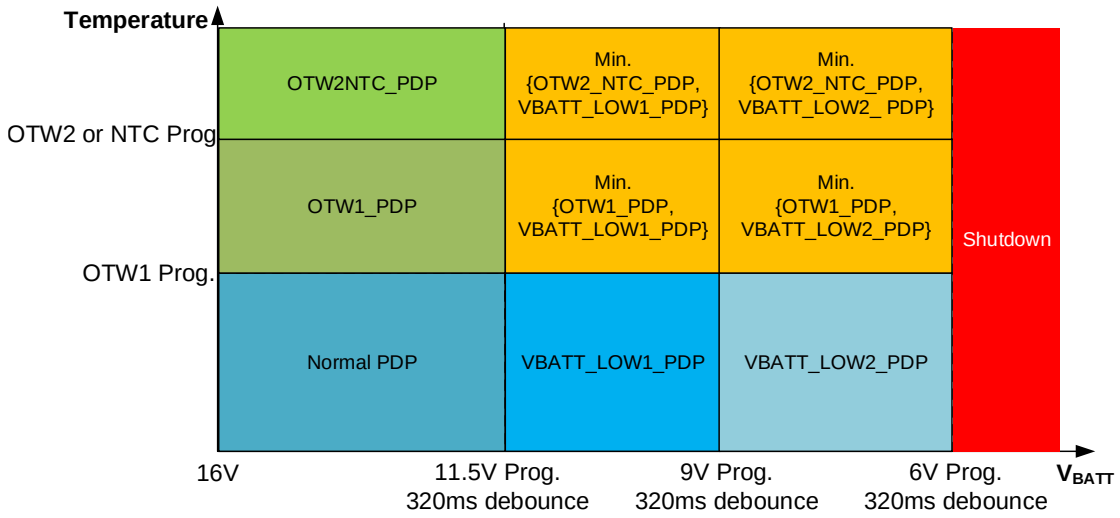


Figure 17: PDP Foldback Scheme

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I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence.

The MPQ4242 interface is an I²C slave that supports fast mode (400kHz). The I²C interface adds flexibility to the power supply solution. The output voltage (V_{OUT}), transition slew rate, and additional parameters can be instantaneously controlled by the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Conditions

The start (S) condition and stop (P) condition are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 18).

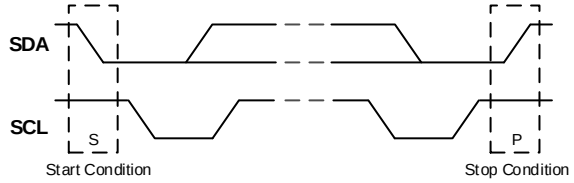


Figure 18: Start and Stop Conditions

The master then generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data should be followed by an acknowledge bit.

I²C Start-Up Timing

The I²C function is enabled once VIN exceeds its UVLO threshold and EN is active.

I²C Update Sequence

The MPQ4242 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ4242 acknowledges by pulling SDA low during the high period of a single clock pulse. A valid I²C address selects the MPQ4242. The MPQ4242 performs an update on the falling edge of the LSB. Figure 19 shows an I²C write example for a single register. Figure 20 on page 33 shows an I²C write example for multiple registers. Figure 21 on page 33 shows an I²C read example for a single register.

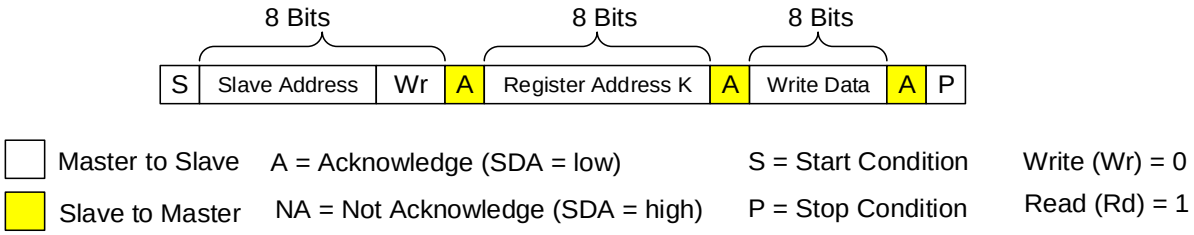


Figure 19: I²C Write Example (Write Single Register)

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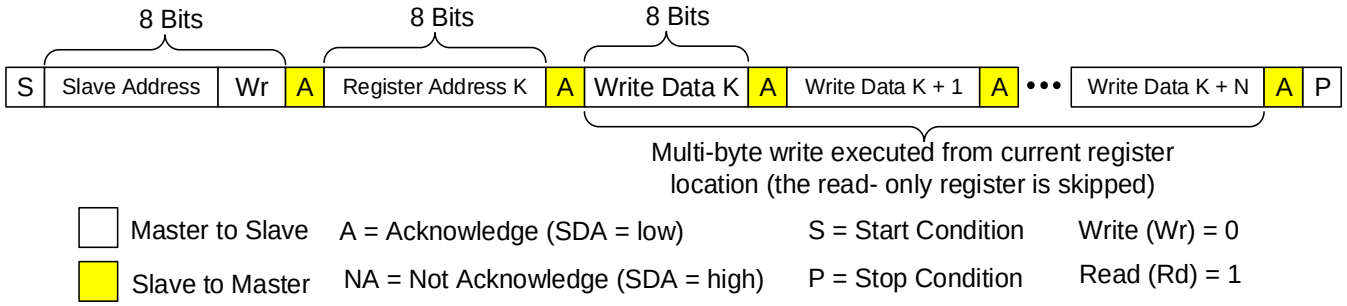


Figure 20: I²C Write Example (Write Multiple Registers)

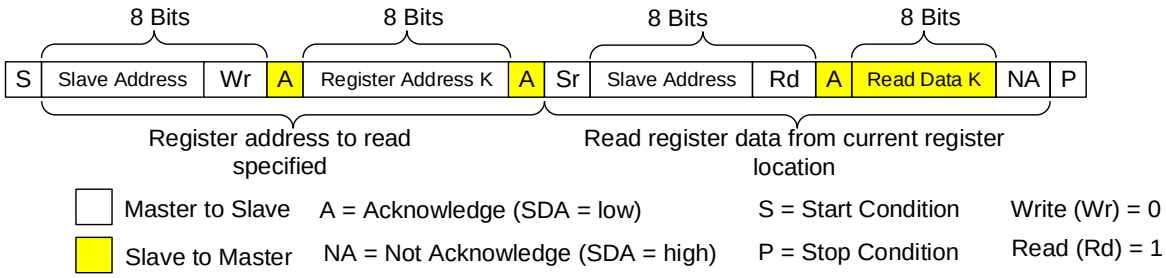


Figure 21: I²C Read Example (Read Single Register)

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I²C REGISTER MAP

Addr. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	PDO_SET1	R/W	-	-	PDO7_EN (17)	PDO6_EN (17)	PDO5_EN (17)	PDO4_EN (17)	PDO3_EN (17)	PDO2_EN (17)
01	PDO_SET2	R/W	-	-	PDO7_TYPE (17)	PDO6_TYPE (17)	PDO5_TYPE (17)	PDO4_TYPE (17)	PDO3_TYPE (17)	PDO2_TYPE (17)
02	HOST_SET	R/W	COMMUNICA_CAPAB_HOST (17)	PRODUCT_TYPE_DFP (17)		HOST_CAPABILITY(000B) (17)			PORT_NUMBER (17)	
03	PDO_I1	R/W	PDO1_CURRENT_SETTING (17) (3A default)							
04	PDO_V2_L	R/W	PDO2_VOLTAGE_SETTING (low byte) (17) (9V default)							
05	PDO_V2_H	R/W	PDO2_VOLTAGE_SETTING (high byte) (17) (0x00)							
06	PDO_I2	R/W	PDO2_CURRENT_SETTING (17) (3A default)							
07	PDO_V3_L	R/W	PDO3_VOLTAGE_SETTING (low byte) (17) (15V default)							
08	PDO_V3_H	R/W	PDO3_VOLTAGE_SETTING (high byte) (17) (0x00)							
09	PDO_I3	R/W	PDO3_CURRENT_SETTING (17) (3A)							
0A	PDO_V4_L	R/W	PDO4_VOLTAGE_SETTING (low byte) (17) (20V default)							
0B	PDO_V4_H	R/W	PDO4_VOLTAGE_SETTING (high byte) (17) (0x00)							
0C	PDO_I4	R/W	PDO4_CURRENT_SETTING (17) (3A)							
0D	PDO_V5_L	R/W	PDO5_VOLTAGE_SETTING (low byte) (17) (3.3V)							
0E	PDO_V5_H	R/W	PDO5_VOLTAGE_SETTING (high byte) (17) (11V)							
0F	PDO_I5	R/W	PDO5_CURRENT_SETTING (17) (3A)							
10	PDO_V6_L	R/W	PDO6_VOLTAGE_SETTING (low byte) (17) (3.3V)							
11	PDO_V6_H	R/W	PDO6_VOLTAGE_SETTING (high byte) (17) (16V)							
12	PDO_I6	R/W	PDO6_CURRENT_SETTING (17) (3A)							
13	PDO_V7_L	R/W	PDO7_VOLTAGE_SETTING (low byte) (17) (3.3V)							
14	PDO_V7_H	R/W	PDO7_VOLTAGE_SETTING (high byte) (17) (21V)							
15	PDO_I7	R/W	PDO7_CURRENT_SETTING (17) (3A)							
16	PD_CTL1	R/W	CDP_EN (17)	LEGACY_CHARGING_MODE_SEL (17)		USBCOMMUNICATE (17)	NTC_CTL_RP (17)	TOUCH_TEMP (17)		TYPE-C_MODE (17)
17	PD_CTL2	R/W	HDRST	USBSUSPEND (17)	TOUCH CURRENT (17)			COMPLIANCE (17)		
18	PWR_CLT1	R/W	EN (17)	MODE (17)	FREQ (17)		DITHER (17)	LINE_DROP_COMP (17)		SLEW_RATE (17)
19	PWR_CLT2	R/W	EN_VBUS (17)	PPS_MIN_SEL (17)	OTW1_THRESHOLD (17)			OTP_THRESHOLD (17)		
1A	VOUT_L	R/W	RESERVED_ALL: 0					VOUT_DATA_BIT_LOW[2:0] (17)		
1B	VOUT_H	R/W	VOUT_DATA_BIT_HIGH[10:3] (17) (use this as default DAC V_{REF})							
1C	IOUT_LIM	R/W	-	OUTPUT_CURRENT_LIMIT_THRESHOLD (17) (1A to 6.35A/50mA step)						
1D	CTL_SYS0	R/W	-			-		-		GO_BIT
1E	CTL_SYS1	R/W	SEND_SRC_CAP	ADDITIONAL_LINE_DROP_COMPENSATION (17)	EN_OFF_TIMER (17)		I2C_SLAVE_ADDRESS (A4~A1) (17)			
1F	CTL_SYS2	R/W	GPIO1 (17)			GPIO2 (17)			I2C_CTL_VOUT_EN (17)	
20	CTL_SYS3	R/W	PS_PDP_THD (17) (PDP is reduced to this value after power sharing)							
21	CTL_SYS4	R/W	PS_PDP_THD_PDO_SELECT (17)							
22	CTL_SYS5	R/W	-	PPS_3A_5A (17)	CC_BLANK_TIMER (17)		-		PD_CAP_PEAK_CURRENT (17)	

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I²C REGISTER MAP *(continued)*

Addr. (Hex)	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
23	CTL_SYS6	R/W	VBATT_LOW1_PDP (17)							
24	CTL_SYS7	R/W	VBATT_L1_PDO_SELECT (17)							
25	CTL_SYS8	R/W	VBATT_LOW2_PDP (17)							
26	CTL_SYS9	R/W	VBATT_L2_PDO_SELECT (17)							
27	CTL_SYS10	R/W	OTW1_PDP (17)							
28	CTL_SYS11	R/W	OTW1_PDO_SELECT (17)							
29	CTL_SYS12	R/W	OTW2_NTC_PDP (17)							
2A	CTL_SYS13	R/W	OTW2_NTC_PDO_SELECT (17)							
2B	CTL_SYS14	R/W	VBATT_LOW_THLD1 (17)				VBATT_LOW_THLD2 (17)			
2C	CTL_SYS15	R/W	VBATT_LOW_THLD3 (17)				VBATT_LOW_BLK (17)		-	-
2D	CTL_SYS16	R/W	-	EXT_HS_FET_RON (17)			OTW2_THRESHOLD (17)			-
2E	CTL_SYS17	R/W	PEAK_CL (17)		-	NTC_HYSTERESIS (17)	NTC_MODE (17)	-	VBUS_VOLTAGE (17)	
2F	CTL_SYS18	R/W	OTP_PROGRAM	LED_PWM_DUTY (17)						
30	STATUS1	R	ATTACHED	NTC2_ENTER	POL	SHORT_VBATT	FAULT	OTP_PAGE	CC_CV	NTC_ENTER
31	STATUS2	R	VBATT_LOW1_FLAG	VBATT_LOW2_FLAG	OTW1	OTW2	SELECTED_PDO_INDEX			PDO_TYPE
32	STATUS3	R	CONTRACT_POWER (CP)							
33	ID1	R	OTP_SUFFIX_CODE (17)							
34	ID2	R	OTP_SOFTWARE_REVISION_NO (17)							
35	FW_REV	R	MISMATCH	GIVEBACK_FLAG	CABLE_CAP	FIRMWARE_REVISION				
36	MAX_REQ_CUR	R	Max requested operation current (MISMATCH = 1) in a 20mA unit; only valid when GIVEBACK_FLAG = 0; fixed PDO							
37	MFR_ID	R	MANUFACTURER_ID (17): 0000 1001b							
38	DEV_ID	R	DEVICE_ID (17): 0101 1000b							
39	CLK_ON	W	Write 1b to enable clock							

Note:

17) This register can be configured via the one-time programmable (OTP) memory.

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REGISTER MAP

The default register value is based on MPQ4242-0000.

PDO_SET1

Address: 0x00
Type: Read/Write

Bits	Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	PDO7_EN	Enables the PDO7's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[4]	PDO6_EN	Enables the PDO6's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[3]	PDO5_EN	Enables the PDO5's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[2]	PDO4_EN	Enables the PDO4's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[1]	PDO3_EN	Enables the PDO3's power object setting. The default is 1b. 0b: Disabled 1b: Enabled
D[0]	PDO2_EN	Enables the PDO2's power object setting. The default is 1b. 0b: Disabled 1b: Enabled

PDO1 is fixed as a 5V power data object, and it is always enabled. Its voltage can be changed by VBUS_VOLTAGE.

PDO_SET2

Address: 0x01
Type: Read/Write

Bits	Name	Description
D[7:6]	RESERVED	Reserved.
D[5]	PDO7_TYPE	Sets the PDO7's power object. The default is 1b. 0b: Fixed PDO 1b: APDO
D[4]	PDO6_TYPE	Sets the PDO6's power object. The default is 1b. 0b: Fixed PDO 1b: APDO
D[3]	PDO5_TYPE	Sets the PDO5's power object. The default is 1b. 0b: Fixed PDO 1b: APDO

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D[2]	PDO4_TYPE	Sets the PDO4's power object. The default is 0b. 0b: Fixed PDO 1b: APDO
D[1]	PDO3_TYPE	Sets the PDO3's power object. The default is 0b. 0b: Fixed PDO 1b: APDO
D[0]	PDO2_TYPE	Sets the PDO2's power object. The default is 0b. 0b: Fixed PDO 1b: APDO

HOST_SET

Address: 0x02
Type: Read/Write

Bits	Name	Description
D[7]	COMMUNICA_ CAPAB_HOST	Sets the USB communication capabilities for the USB host. The default is 0b. 0b: Other 1b: The product can enumerate USB devices
D[6:5]	PRODUCT_TYPE_ DFP	Sets the product type (DFP). The default is 11b. 00b: Undefined 01b: PDUSB hub 10b: PDUSB host 11b: Power Brick
D[4:2]	HOST_CAPABILITY	Sets the DFP VDO message's B26…24 bits. The default is 000b.
D[1:0]	PORT_NUMBER	Sets the unique port number to identify a specific port on a multi-port device.

PDO_I1

Address: 0x03
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO1_CURRENT_ SETTING	Sets PDO1's maximum output current setting in 20mA units. The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V2_L and PDO_V2_H

Address: 0x04, 0x05
Type: Read/Write

If PDO2_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V2_L, Bits D[7:0]	PDO2_VOLTAGE_ SETTING	Sets the PDO2's output voltage in 100mV units. The default is 0x5A (9V). The maximum voltage that can be set is 22.97V.

If PDO2_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V2_H, Bits D[7:0]	PDO2_MAXIMUM_ VOLTAGE	Sets the maximum PDO2 voltage in 100mV increments.
PDO_V2_L, Bits D[7:0]	PDO2_MINIMUM_ VOLTAGE	Sets the minimum PDO2 voltage in 100mV increments.

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PDO_I2

Address: 0x06
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO2_CURRENT_ SETTING	Sets PDO2's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V3_L and PDO_V3_H

Address: 0x07, 0x08
Type: Read/Write

If PDO3_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V3_L, Bits D[7:0]	PDO3_VOLTAGE_ SETTING	Sets the PDO3's output voltage in 100mV units. The default is 0x96 (15V). The maximum voltage that can be set is 22.97V.

If PDO3_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V3_H, Bits D[7:0]	PDO3_MAXIMUM_ VOLTAGE	Sets the maximum PDO3 voltage in 100mV increments.
PDO_V3_L, Bits D[7:0]	PDO3_MINIMUM_ VOLTAGE	Sets the minimum PDO3 voltage in 100mV increments.

PDO_I3

Address: 0x09
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO3_CURRENT_ SETTING	Sets PDO3's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V4_L and PDO_V4_H

Address: 0x0A, 0x0B
Type: Read/Write

If PDO4_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V4_L, Bits D[7:0]	PDO4_VOLTAGE_ SETTING	Sets the PDO4's output voltage in 100mV units. The default is 0xC8 (20V). The maximum voltage that can be set is 22.97V.

If PDO4_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V4_H, Bits D[7:0]	PDO4_MAXIMUM_ VOLTAGE	Sets the maximum PDO4 voltage in 100mV increments.
PDO_V4_L, Bits D[7:0]	PDO4_MINIMUM_ VOLTAGE	Sets the minimum PDO4 voltage in 100mV increments.

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PDO_I4

Address: 0x0C
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO4_CURRENT_ SETTING	Sets PDO4's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x96 (3A and fixed PDO). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V5_L and PDO_V5_H

Address: 0x0D, 0x0E
Type: Read/Write

If PDO5_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V5_L, Bits D[7:0]	PDO5_VOLTAGE_ SETTING	Sets the PDO5's output voltage in 100mV units.

If PDO5_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V5_H, Bits D[7:0]	PDO5_MAXIMUM_ VOLTAGE	Sets the maximum PDO5 voltage in 100mV increments. The default is 0x6E (11V).
PDO_V5_L, Bits D[7:0]	PDO5_MINIMUM_ VOLTAGE	Sets the minimum PDO5 voltage in 100mV increments. The default is 0x21 (3.3V).

PDO_I5

Address: 0x0F
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO5_CURRENT_ SETTING	Sets PDO5's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 0x3C (3A). When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V6_L and PDO_V6_H

Address: 0x10, 0x11
Type: Read/Write

If PDO6_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V6_L, Bits D[7:0]	PDO6_VOLTAGE_ SETTING	Sets the PDO6's output voltage in 100mV units.

If PDO6_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V6_H, Bits D[7:0]	PDO6_MAXIMUM_ VOLTAGE	Sets the maximum PDO6 voltage in 100mV increments. The default is 0xA0 (16V).
PDO_V6_L, Bits D[7:0]	PDO6_MINIMUM_ VOLTAGE	Sets the minimum PDO6 voltage in 100mV increments. The default is 0x21 (3.3V).

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PDO_I6

Address: 0x12
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO6_CURRENT_ SETTING	Sets PDO6's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 3A and APDO. When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PDO_V7_L and PDO_V7_H

Address: 0x13, 0x14
Type: Read/Write

If PDO7_TYPE is set to 0b (fixed PDO).

Register	Name	Description
PDO_V7_L, Bits D[7:0]	PDO7_VOLTAGE_ SETTING	Sets the PDO7's output voltage in 100mV units.

If PDO7_TYPE is set to 1b (APDO).

Register	Name	Description
PDO_V7_H, Bits D[7:0]	PDO7_MAXIMUM_ VOLTAGE	Sets the maximum PDO7 voltage in 100mV increments. The default is 0xD2 (21V).
PDO_V7_L, Bits D[7:0]	PDO7_MINIMUM_ VOLTAGE	Sets the minimum PDO7 voltage in 100mV increments. The default is 0x21 (3.3V).

PDO_I7

Address: 0x15
Type: Read/Write

Bits	Name	Description
D[7:0]	PDO7_CURRENT_ SETTING	Sets PDO7's maximum output current setting in 20mA units for fixed PDO, or 50mA units for APDO (PPS). The default is 3A and APDO. When this bit is set to exceed 3A, the MPQ4242 checks the cable current rating first. If it is 5A, then send the >3A setting; if the cable is 3A, only send a 3A maximum current capability.

PD_CTL1

Address: 0x16
Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7]</td><td>CDP_EN</td><td>0b</td><td>Selects the CDP mode. If this bit is set to 1, all the DCP, QC, and Apple modes are disabled. The device only works in CDP handshaking mode. The default is 0.</td></tr>
<tr><td>D[6:5]</td><td>LEGACY_ CHARGING_ MODE_SEL</td><td>00b</td><td>Sets certain values based on the truth table below.
<table>
<tr><td>CDP_EN</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>LEGACY_ CHARGING_ MODE_SEL</td><td>X</td><td>00</td><td>01</td><td>10/11</td></tr>
<tr><td>Mode</td><td>CDP mode</td><td>All DCP modes are active</td><td>Apple mode and BC1.2 mode are active</td><td>Only BC1.2 is active; Apple mode and QC mode are disabled</td></tr>
</table></td></tr>
<tr><td>D[4]</td><td>USBCOMMUN ICATE</td><td>0b</td><td>Sets whether USB communication is supported. The default is 0b.
0b: USB communication is not supported
1b: USB communication is supported</td></tr>
</table>

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D[3]	NTC_CTL_RP	0b	Selects whether the device enters USB Type-C 3A or 1.5A mode if an NTC or over-temperature warning (OTW) event occurs. In 5V @ 3A USB Type-C mode, the R_P pull-up current is 330µA and the R_D detection range is between 0.8V and 2.6V. The default is 0. 0b: PDP <15W, and R_P = 1.5A,otherwise, R_P = 3A 1b: The device enters 1.5A USB Type-C mode if an NTC or OTW1/OTW2 condition occurs
D[2:1]	TOUCH_TEMP	00b	Sets the touch temperature default value to 0, 1 or 2. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 20, bits[1:0]. These bits are set to 00b by default
D[0]	TYPE-C_ MODE	0b	Selects 3A or 1.5A Type-C mode. In 5V @ 3A USB Type-C mode, the R_P pull-up current is 330µA and the R_D detection range is between 0.85V and 2.45V. The default is 0. 0b: 3A Type-C mode 1b: 1.5A Type-C mode

PD_CTL2

Address: 0x17
Type: Read/Write

Bits	Name	Default	Description
D[7]	HDRST	0b	Sends a hard reset command. The default is 0b. 0b: Normal state. 1b: Send a hard reset command to the sink. After the HDRST message is sent, this bit automatically resets to 0b
D[6]	USB_ SUSPEND	0b	Sets whether the USB suspend function is supported. The default is 0b. 0b: Not supported 1b: Supported
D[5:3]	TOUCH_ CURRENT	000b	Sets the TOUCH_CURRENT, bits[2:0]. These bits are defined in SOURCE_CAPABILITIES_EXTENDED Message byte 13, bits[2:0]. These bits are set to 000b by default. Bit D[5] indicates TOUCH_CURRENT, bit 2
D[2:0]	COMPLIANCE	101b	Sets the values of bits[2:0] of the Compliance byte, defined in SOURCE_CAPABILITIES_EXTENDED Message byte 12, bits[2:0]. Bit D[2] sets the compliance value for bit 2.

PWR_CTL1

Address: 0x18
Type: Read/Write

Bits	Name	Default	Description
D[7]	EN	1b	Determines the I^2C control to turn the part on or off. When the external EN pin is low, the converter is off and the I^2C shuts down. When the EN pin is high, the EN bit takes over. The default is 1. 0b: The part is off but the I^2C register does not reset. In addition, the USB Type-C logic is off, and the system clock turns off to save quiescent current (I_Q) 1b: If the USB Type-C receptacle is disconnected, the system clock remains off to save I_Q
D[6]	MODE	1b	Sets the PWM mode. The default is 1. 0b: Enables auto-PFM/PWM mode 1b: Forced PWM mode

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D[5:4]	FREQ	01b	Sets the switching frequency (f_{SW}). The default is 01. 00b: 250kHz 01b: 420kHz 10b/11b: Reserved
D[3]	DITHER	0b	Enables the frequency spread spectrum function. The default is 0. 0b: Disabled 1b: Enabled
D[2:1]	LINE_DROP_COMP	00b	Sets the output voltage compensation vs. the load feature. The compensation amplitude is fixed for any output voltage. Set 0x1E, bit[6] = 1 to enable an additional compensation voltage. Line drop compensation has a maximum clamp at 800mV, regardless of the output current. Line drop compensation is disabled once the MPQ4242 enters PPS mode. Line drop compensation can be enabled in PPS mode through the factory OTP trim. The default is 00. 00b: No compensation 01b: V_{OUT} compensates 150mV at a 3A Iout 10b: V_{OUT} compensates 300mV at a3A Iout 11b: V_{OUT} compensates 600mV at a3A Iout
D[0]	SLEW_RATE	1b	Sets the output slew rate to adjust V_{OUT}. The default is 1. The slew rate can be calculated with the following equation: V_{OUT} slew rate = V_{REF} slew rate x Feedback resistor ratio (12.5) 0b: 0.4mV/μs V_{REF} rising slew rate; 0.08mV/μs V_{REF} falling slew rate 1b: 0.08mV/μs V_{REF} rising slew rate; 0.08mV/μs V_{REF} falling slew rate

PWR_CTL2

Address: 0x19
Type: Read/Write

Bits	Name	Default	Description
D[7]	EN_VBUS	0b	Enables the power converter's output directly, even there is no USB Type-C sink device. The default is 0b. 0b: The power converter's on/off status is controlled by the USB Type-C controller 1b: The power converter is enabled
D[6]	PPS_MIN_SEL	1b	Sets the V_{BUS} under-voltage (UV) threshold: This bit also controls the 3.3V or 5V minimum PPS voltage. The default is 1. 0b: The V_{BUS} UV falling threshold is 4.5V with 5% accuracy for 5V minimum PPS voltage applications 1b: The V_{BUS} UV falling threshold is 2.97V (3.135V maximum) with 4.5% accuracy for 3.3V minimum PPS voltage applications
D[5:3]	OTW1_THRESHOLD	100b	Sets the over-temperature warning (OTW1) threshold. The default is 100. The OTW threshold has a 20°C hysteresis for recovery. 000: Disable the OTW function 001b: 105°C 010b:115°C 011b: 125°C 100b: 135°C 101b: 145°C 110b: 155°C 111b: 165°C

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D[2:0]	OTP_ THRESHOLD	010b	Sets the OT shutdown threshold. The default is 010. OTP has a 20°C hysteresis for recovery. 000b: 155°C 001b: 165°C 010b:175°C 011b: 185°C 100b~111b: Reserved

VOUT_L and VOUT_H

Address: 0x1A, 0x1B
Type: Read/Write

The VOUT_L and VOUT_H registers set V_{OUT} following an 11-bit direct format.

Name	VOUT															
Format	Direct, unsigned binary integer															
Register Name	N/A					VOUT_H D[7:0]								VOUT_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high			Data bit low							
Default value (5V)	N/A					250 Integer										

The real-world V_{OUT} (in V) can be calculated with Equation (2):

$$V_{OUT}\ (V) = V / 100 + 2.5 \quad (2)$$

Where V is an 11-bit, unsigned binary integer from VOUT[10:0] (ranging between 0 and 2047). The V_{OUT} resolution (or minimum step) is 10mV. The MPQ4242 has a feedback network from the OUT pin to internal FB reference voltage. The feedback resistor ratio is V_{OUT} / V_{REF} = 12.5.

See the CTL_SYS0 section below when changing V_{OUT}.

IOUT_LIM

Address: 0x1C
Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[6:0]	IOUT_LIM	0x48	Sets the CC current limit for the buck-boost output CC, in 50mA units. The default is 0x48 (3.6A). When changing IOUT_LIM, the internal I_{REF} should have some slew rate control. The ramping slew rate is 1mA/µs.

CTL_SYS0

Address: 0x1D
Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[0]	GO_BIT	0b	Controls when the MPQ4242 starts to change V_{OUT} / I_{OUT_LIM}. Set GO_BIT to 1 to start the output / CC limit change based on VOUT / IOUT_LIM registers. When V_{OUT} / I_{OUT_LIM} finishes changing (the internal V_{REF} steps to the target V_{REF}), GO_BIT automatically resets to 0. This prevents false operation of the VOUT/IOUT_LIM scaling. The default is 0. 0b: V_{OUT} / I_{OUT_LIM} do not change 1b: V_{OUT} / I_{OUT_LIM} changes based on the VOUT / IOUT_LIM register settings

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CTL_SYS1

Address: 0x1E
Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7]</td><td>SEND_SRC_CAP</td><td>0b</td><td>Sends the source capability message. Write 1 to this bit to force the MPQ4242 to send a Src_Cap message. This bit automatically resets to 0 after the Src_Cap message is sent out. The default is 0b.</td></tr>
<tr><td>D[6]</td><td>ADDITIONAL_ LINE_DROP_ COMPENSATION</td><td>0b</td><td>Enables an additional 150mV for line drop compensation based on the 0x18, bits[2:1] set-up. This bit is active only when line drop compensation is active.

0b: Disabled
1b: Enabled</td></tr>
<tr><td>D[5:4]</td><td>EN_OFF_TIMER</td><td>000b</td><td>Sets the EN off time. There is a shutdown delay time after the EN pin goes low. If EN pulls high while the counter increases, the counter is reset. The default is 00.

00b: No delay
01b: 20 minutes
10b: 40 minutes
11b: 120 minutes</td></tr>
<tr><td>D[3:0]</td><td>I2C_SLAVE_ ADDRESS</td><td>0001b</td><td>Set the I²C slave address A4 to A1 bit.
<table>
<tr><th colspan="2">I²C Address (A7:A1)</th></tr>
<tr><th>Binary</th><th>Hex</th></tr>
<tr><td>1100 001 (Default)</td><td>61h</td></tr>
<tr><td>I²C adjustable for A4~A1</td><td>Set by I2C_SLAVE_ADDRESS, bits D[3:0]</td></tr>
</table>
</td></tr>
</table>

CTL_SYS2

Address: 0x1F
Type: Read and Write

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7:5]</td><td>GPIO1</td><td>000b</td><td>Sets the GPIO1 pin function. The default is 000.

000b: POWER_SHARE1. See the GPIO1_POWER_SHARE section on page 28 for more details
001b: GATE. Provides a GND to battery short protection drive
010b: FAULT, open-drain output. Pulls low to indicate if a fault has occurred, such as OCP, OTP, and GND/DP/DM/CCx to battery short
011b: NTC2. When this function is selected, the power share input is controlled by NTC2. The NTC_MODE bit does not control the NTC2 behavior. NTC_HYSTERESIS sets the hysteresis
100/101b: ATTACH_FLT_ALT, open-drain output. This pin pulls low for 12µs at the connection rising edge if no fault event has occurred. Pulls low if a fault occurs
111b: Current monitor output. Represents the signal between ISENS+ and ISENS-</td></tr>
</table>

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D[4:2]	GPIO2	000b	Sets the GPIO2 pin function. The default is 000. 000b: Reserved 001b: POL, open-drain output. Indicates the USB Type-C plug's polarity. When CC1 is selected as the CC line, POL pulls low; when CC2 is selected as the CC line or disconnected, POL is an open drain 010b: NTC. Functions as an input pin to sense the external thermal. See the NTC Function section on page 27 for more details 011b: VCONN_IN. Apply a 5V / 1.5W power supply on this pin 100b: LED_PWM output. It is a 25kHz PWM signal output with an adjustable duty cycle. See the CTL_SYS18 section on page 49 for more details 101b: ATTACH. Indicates if the USB Type-C port is connected. Only high or low for two states 110b: POWER_SHARE2. GPIO2 power sharing is triggered when the GPIO2 voltage exceeds 1.87V. See the GPIO2_POWER_SHARE section on page 29 for more details
D[1]	I2C_CTL_VOUT_EN	0b	Enables the I^2C registers 0x1A, 0x1B, 0x1C, and 0x1D. The default is 0. 0b: V_{OUT} and I_{OUT_LIM} do not change, even after sending commands to VOUT_L, VOUT_H, GO_BIT, and ILIMIT. V_{OUT} is controlled by the USB PD engine 1b: V_{OUT} changes based on the VOUT/IOUT_CC register setting
D[0]	RESERVED	-	Reserved.

CTL_SYS3 and CTL_SYS4

Address: 0x20 to 0x21
Type: Read and Write

Bits	Name	Default	Description
D[7:0]	PS_PDP_THD	0x5A	Sets the threshold to which the PDO power rating is reduced. When the GPIOx pin (if set to the POWER_SHARE function) pulls low, the MPQ4242's PD power drops to the values set by PS_PDP_THD. The default is 45W. 0x01: 0.5W 0xFF: 127.5W
D[7:0]	PS_PDP_THD_PDO_SELECT	0xBE	Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PS_PDP_THD. The default means 4 fixed PDOs:5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.

CTL_SYS5

Address: 0x22
Type: Read/Write

Bits	Name	Default	Description
D[7]	RESERVED	-	Reserved.
D[6]	PPS_3A_5A	0b	Sets the maximum current for APDO after entering a power sharing, V_{BATT} low, OTW, or NTC state. The default is 0b. 0b: 3A 1b: 5A (requires 5A cable)
D[5:4]	CC_BLANK_TIMER	10b	Sets the blank time when the output CC over-current condition is reached. The default is 10b. 00b: No additional CC blank timer 01b: 2ms 10b: 16ms 11b: 32ms

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D[1:0]	PD_CAP_ PEAK_CURRENT	11b	Enables the peak current 1, 2, and 3 capability in the SOURCE_CAP_EXTEND message. The default is 11. 00b: Not support 01b: Support peak current 1 10b: Support peak currents 1 and 2 11b: Support peak currents 1, 2 and 3

CTL_SYS6~CTL_SYS13

Address: 0x23~0x2A
Type: Read/Write

Bits	Name	Default	Description
D[7:0]	VBATT_LOW1_ PDP	0x5A	Sets the maximum power rating when V_{BATT} drops below its first threshold. PDP is reduced to the value set by these bits. The default is 45W. 0x01: 0.5W 0xFF: 127.5W
D[7:0]	VBATT_L1_ PDO_SELECT	0xBE	Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs:5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.
D[7:0]	VBATT_LOW2_ PDP	0x1E	Sets the maximum power rating when V_{BATT} drops below its second threshold. PDP is reduced to the value set by these bits. The default is 15W. 0x01: 0.5W 0xFF: 127.5W
D[7:0]	VBATT_L2_ PDO_SELECT	0xBE	Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs:5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.
D[7:0]	OTW1_PDP	0x5A	Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 45W. 0x01: 0.5W 0xFF: 127.5W
D[7:0]	OTW1_PDO_ SELECT	0xBE	Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs:5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.
D[7:0]	OTW2_NTC_ PDP	0x3C	Sets the maximum power rating when the die temperature drops below its threshold. PDP is reduced to the value set by these bits. The default is 30W. 0x01: 0.5W 0xFF: 127.5W
D[7:0]	OTW2_NTC_ PDO_SELECT	0xBE	Selects which voltage is enabled in the PDO list. See Table 4 on page 29 for more details. The final PDO current is determined by PDP_L. The default means 4 fixed PDOs:5V/9V/15V/20V and 3 APDOs: 3.3V to 5.9V/3.3V to 11V/3.3V to 16V.

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CTL_SYS14 and CTL_SYS15

Address: 0x2B, 0x2C
Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7:4]</td><td>VBATT_LOW_THLD1</td><td>0100b</td><td>Sets the threshold for input voltage detection. The default is 0100b. See the Low Battery Operation section on page 28 for more details.
<table>
<tr><th>D[3:0]</th><th>Input Voltage Falling</th><th>Hysteresis</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>12.6V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>12.2V</td></tr>
<tr><td>0011</td><td>11.8V</td></tr>
<tr><td>0100</td><td>11.4V</td></tr>
<tr><td>0101</td><td>11V</td></tr>
<tr><td>0110</td><td>10.6V</td></tr>
<tr><td>0111</td><td>10.2V</td></tr>
<tr><td>1000</td><td>9.8V</td></tr>
<tr><td>1001</td><td>9.4V</td></tr>
<tr><td>1010</td><td>9V</td></tr>
<tr><td>1011</td><td>8.6V</td></tr>
<tr><td>1100</td><td>8.2V</td></tr>
<tr><td>1101</td><td>7.8V</td></tr>
<tr><td>1110</td><td>7.4V</td></tr>
<tr><td>1111</td><td>7V</td></tr>
</table></td></tr>
<tr><td>D[3:0]</td><td>VBATT_LOW_THLD2</td><td>1000b</td><td>Sets the threshold for input voltage detection. The default is 1000b. See the Low Battery Operation section on page 28 for more details.
<table>
<tr><th>D[3:0]</th><th>Input Voltage Falling</th><th>Input Voltage Rising</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>11.8V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>11.4V</td></tr>
<tr><td>0011</td><td>11V</td></tr>
<tr><td>0100</td><td>10.6V</td></tr>
<tr><td>0101</td><td>10.2V</td></tr>
<tr><td>0110</td><td>9.8V</td></tr>
<tr><td>0111</td><td>9.4V</td></tr>
<tr><td>1000</td><td>9V</td></tr>
<tr><td>1001</td><td>8.6V</td></tr>
<tr><td>1010</td><td>8.2V</td></tr>
<tr><td>1011</td><td>7.8V</td></tr>
<tr><td>1100</td><td>7.4V</td></tr>
<tr><td>1101</td><td>7V</td></tr>
<tr><td>1110</td><td>6.6V</td></tr>
<tr><td>1111</td><td>6.2V</td></tr>
</table></td></tr>
</table>

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<table>
<tr><td>D[7:4]</td><td>VBATT_LOW_
THLD3</td><td>1010b</td><td>Those bits set the threshold of input voltage detection. The default is 1010b. See the Low Battery Operation section on page 28 for more details.
<table>
<tr><th>D[3:0]</th><th>Input Voltage Falling</th><th>Input Voltage Rising</th></tr>
<tr><td>0000</td><td>This function is disabled</td><td>This function is disabled</td></tr>
<tr><td>0001</td><td>9.8V</td><td rowspan="16">800mV</td></tr>
<tr><td>0010</td><td>9.4V</td></tr>
<tr><td>0011</td><td>9V</td></tr>
<tr><td>0100</td><td>8.6V</td></tr>
<tr><td>0101</td><td>8.2V</td></tr>
<tr><td>0110</td><td>7.8V</td></tr>
<tr><td>0111</td><td>7.4V</td></tr>
<tr><td>1000</td><td>7V</td></tr>
<tr><td>1001</td><td>6.6V</td></tr>
<tr><td>1010</td><td>6.2V</td></tr>
<tr><td>1011</td><td>5.8V</td></tr>
<tr><td>1100</td><td>5.4V</td></tr>
<tr><td>1101</td><td>5V</td></tr>
<tr><td>1110</td><td>4.6V</td></tr>
<tr><td>1111</td><td>4.2V</td></tr>
</table></td></tr>
<tr><td>D[3:2]</td><td>VBATT_LOW_
BLK</td><td>10b</td><td>Sets the V_{BATT} low 1, and V_{BATT} low 2, and V_{BATT} low 3 blank times. The default is 10b.

00b: 10ms
01b: 160ms
10b: 320ms
11b: 640ms</td></tr>
<tr><td>D[1:0]</td><td>RESERVED</td><td>-</td><td>Reserved.</td></tr>
</table>

CTL_SYS16

Address: 0x2D
Type: Read/Write

<table>
<tr><th>Bits</th><th>Name</th><th>Default</th><th>Description</th></tr>
<tr><td>D[7]</td><td>RESERVED</td><td>-</td><td>Reserved.</td></tr>
<tr><td>D[6:4]</td><td>EXT_HS_
FET_RON</td><td>000b</td><td>Sets the $R_{(DS)ON}$ for external N-channel MOSFET at 10V V_{GS}. Select $R_{(DS)ON}$ such that is matches MOSFET's actual $R_{(DS)ON}$ at 10V_{GS}. The default is 000b.
<table>
<tr><th>D[6:4]</th><th>$R_{(DS)ON}$ (mΩ)</th></tr>
<tr><td>000</td><td>This function is disabled</td></tr>
<tr><td>001</td><td>5</td></tr>
<tr><td>010</td><td>7.5</td></tr>
<tr><td>011</td><td>10</td></tr>
<tr><td>100</td><td>12.5</td></tr>
</table></td></tr>
<tr><td>D[3:1]</td><td>OTW2_
THRESHOLD</td><td>110b</td><td>Sets the over-temperature warning (OTW) threshold. The default is 110b. OTW has a 20°C hysteresis for recovery.

000b: Disable OTW
001b: 105°C
010b:115°C
011b: 125°C
100b: 135°C
101b: 145°C
110b: 155°C
111b: 165°C</td></tr>
<tr><td>D[0]</td><td>RESERVED</td><td>-</td><td>Reserved.</td></tr>
</table>

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CTL_SYS17

Address: 0x2E
Type: Read/Write

Bits	Name	Default	Description
D[7:6]	PEAK_CL	11b	Sets the high-side peak current limit in boost mode. The default is 11b. D[7:6] / Peak Limit 00 / 8A 01 / 12A 10 / 16A 11 / 20A
D[4]	NTC_ HYSTERESIS	1b	Sets the NTC thermal recovery hysteresis. This bit controls both NTC and NTC2. The default is 1b. 0b: 10% 1b: 20%
D[3]	NTC_MODE	0b	Sets the behavior if the NTC function is triggered. The default is 0b. 0b: Shut down the MPQ4242 1b: Reduce the PD power to the value set by OTW2_NTC_PDP
D[1:0]	VBUS_ VOLTAGE	10b	Sets the default VBUS voltage. The default is 10b. 00b: 5V 01b: 5.05V 10b: 5.1V 11b: 5.15V

CTL_SYS18

Address: 0x2F
Type: Read/Write

Bits	Name	Default	Description
D[7]	OTP_PROGRAM	0x0	Configures the I^2C register value into the OTP memory cell. A password is required before using the OTP. The OTP can be configured once. Only the MPQ4242-0000 and OTP_PAGE = 0 can be used to configure the OTP. Write 1 to this bit to implement OTP configurations. After configuring is complete, this bit automatically resets to 0. Apply a 12V V_{IN} while configuring the OTP.
D[6:0]	LED_PWM_DUTY	0x32	Sets the LED_PWM output duty cycle. The minimum value is 5%; the maximum is 100%. 0x05: 5% 0x64: 100%

STATUS1

Address: 0x30
Type: Read-Only

This register is latch-off, and it is cleared when it is read.

Bits	Name	Description
D[7]	ATTACHED	Returns whether the sink is connected. 0b: Disconnected 1b: Connected
D[6]	NTC2_ENTER	Returns whether an NTC2 event has occurred. 0b: No NTC2 event has occurred 1b: An NTC2 event has occurred

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D[5]	POL	Indicates the USB Type-C polarity. 0b: CC1 is selected as the CC line 1b: CC2 is selected as the CC line
D[4]	SHORT_VBATT	Indicates the output bus voltage status. 0b: Normal state 1b: DP, DM, CC1, CC2 or USB_GND is shorted with the battery voltage
D[3]	FAULT	FAULT function indicates a fault has happened. Fault conditions include OCP, OTP, and GND/DP/DM/CCx to battery shorts. 0b: No fault has occurred 1b: One or more fault events have occurred
D[2]	OTP_PAGE	Indicates the current OTP page index. 0b: Page 0. No OTP configurations 1b: Page 1
D[1]	CC_CV	Indicates the output power status. 0b: The output is in a CV state 1b: The output is in a CC current limit state
D[0]	NTC_ENTER	Returns whether an NTC event has occurred. 0b: No NTC event has occurred 1b: An NTC event has occurred

STATUS2

Address: 0x31
Type: Read-Only

This register is latch-off, and it is cleared when it is read.

Bits	Name	Description
D[7]	VBATT_LOW1_ FLAG	Indicates if V_{IN} is below its first lower threshold. 0b: V_{IN} is not below its threshold 1b: V_{IN} is below its threshold
D[6]	VBATT_LOW2_ FLAG	Indicates if V_{IN} is below its second lower threshold. 0b: V_{IN} is not below its threshold 1b: V_{IN} is below its threshold
D[5]	OTW1	Indicates if the device is in an over-temperature warning (OTW1) state. 0b: No OTW1 state has been detected 1b: The device is in an OTW1 state
D[4]	OTW2	Indicates if the device is in an over-temperature warning (OTW2) state. 0b: No OTW2 state has been detected 1b: The device is in an OTW2 state
D[3:1]	SELECTED_ PDO_INDEX	Returns the sink's selected PDO index. 0: No PD contract 1~7: PDO1~ 7 has been selected
D[0]	PDO_TYPE	Indicates if the sink's selected PDO is fixed PDO or APDO (PPS). 0b: Fixed PDO 1b: APDO

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STATUS3

Address: 0x32
Type: Read-Only

This register reflects an instantaneous value. It is a non-latch register.

Bits	Name	Description
D[7:0]	CONTRACT_ POWER	Returns the PD contracted power in 0.5W units. Calculate the fixed PDO value with the following equation: Fixed PDO = Voltage x Maximum Current; Calculate the PPS with the following equation: PPS: Max Voltage x Max Current. If there is no PD contract, the value is 7.5W or 15W depending on R_P.

ID1

Address: 0x33
Type: Read-Only

Bits	Name	Description
D[7:0]	OTP_SUFFIX_ CODE	“0x00” represents the MPQ4242-0000. “0x01” represents the MPQ4242-0001.

ID2

Address: 0x34
Type: Read-Only

Bits	Name	Description
D[7:0]	OTP_SOFTWARE_ REVISION_NO	Stores the revision number, which is the OTP value.

FW_REV

Address: 0x35
Type: Read-Only

Bits	Name	Description
D[7]	MISMATCH	Indicates if the sink request sets a mismatch bit. Defined in the PD specification. 0b: The MISMATCH bit is set to 0 1b: The MISMATCH bit is set to 1
D[6]	GIVEBACK_FLAG	This bit is set if the sink requests a GIVEBACK flag.
D[5]	CABLE_CAP	0b: The cable can handle 3A only 1b: 5A cable
D[4:0]	FIRMWARE_REVISION	Returns the PD firmware revision number.

MAX_REQ_CUR

Address: 0x36
Type: Read-Only

Bits	Name	Description
D[7:0]	MAX_REQ_CUR	Sink requested maximal operation current (MISMATCH bit = 1) in 20mA unit, only valid when GIVEBACK_FLAG = 0 and fixed PDO is selected.

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MFR_ID

Address: 0x37
Type: Read-Only

Bits	Name	Description
D[7:0]	MANUFACTURER_ID	Returns the manufacturer ID. The default is 0000 1001b.

DEV_ID

Address: 0x38
Type: Read-Only

Bits	Name	Description
D[7:0]	DEVICE_ID	Returns the device ID. The default is 0101 1000b.

CLK_ON

Address: 0x39
Type: Write-Only

Bits	Name	Description
D[7:0]	CLOCK_ON	Enables the digital clock. Write 0x01 to enable the digital clock. No I^2C registers can be modified before the digital clock is enabled. This bit automatically resets to 0 after the clock is enabled. The digital clock is enabled when a USB Type-C device is connected. Write 0 to 0x39, set the EN bit to 0, or pull down the EN pin and VIN pin below their UVLO thresholds to disable the digital clock again.

GPIO1 and GPIO2 Options

GPIO1 Options	GATE	POWER_SHARE1	FAULT	NTC2	ATTACH_FLT_ALT	IMON
GPIO2 Options	POL	NTC	VCONN_IN (max 5.25V)	LED_PWM	ATTACH	POWER_SHARE2

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APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

In a buck-boost topology, the inductor must support buck applications with the maximum input voltage (V_{IN}) and boost applications with the minimum V_{IN}. Two critical inductance values can be determined according to the buck mode and boost mode current ripple. The first inductance value (L_{MIN_BUCK}) can be calculated with Equation (3):

$$L_{MIN_BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{REQ} \times \Delta I_L} \quad (3)$$

The second inductance value (L_{MIN_BOOST}) can be calculated with Equation (4):

$$L_{MIN_BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (4)$$

Where f_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple.

Typically, the peak-to-peak ripple can be set at 1A to 3A of the inductor current. In addition to the inductance value, the inductor must support the peak current in buck and boost applications to avoid saturation. The peak current in buck mode can be calculated with Equation (5):

$$I_{PEAK_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (5)$$

The peak current in boost mode can be calculated with Equation (6):

$$I_{PEAK_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (6)$$

Where η is the estimated efficiency of the MPQ4242

Selecting the Input Capacitor

It is recommended to use ceramic capacitors plus an electrolytic capacitor for the input and output capacitors. This filters the input and output ripple current and helps achieve stable operation. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100µF electrolytic capacitor and two 10µF + 0.1µF ceramic capacitors are recommended.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to VIN as possible.

Selecting the Output Capacitor

The device requires an output capacitor (C_{OUT}) to maintain the DC output voltage. Typically, a 100µF polymer or hybrid electric capacitor and two 10µF + 0.1µF ceramic output capacitors are recommended for excellent loop stability and transient response.

The E-capacitor's ESR must be smaller than 50mΩ for excellent loop stability, transient response, and efficiency.

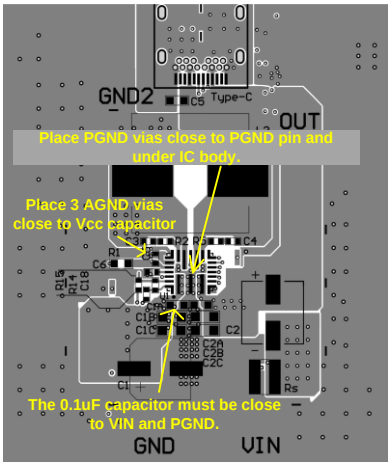
In GND to battery short applications, the output E-capacitor's negative node must be connected to the current-sense resistor (see Figure 24 on page 55).

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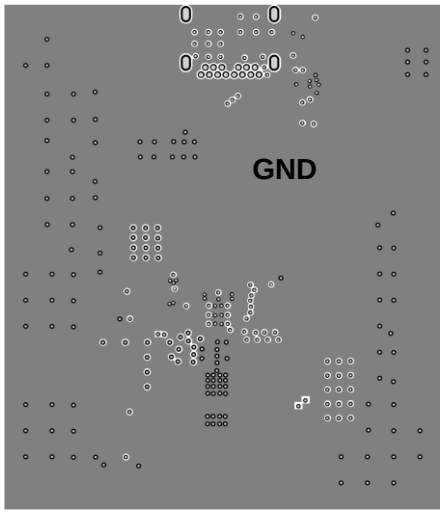
PCB Layout Guidelines

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 23 and follow the guidelines below:

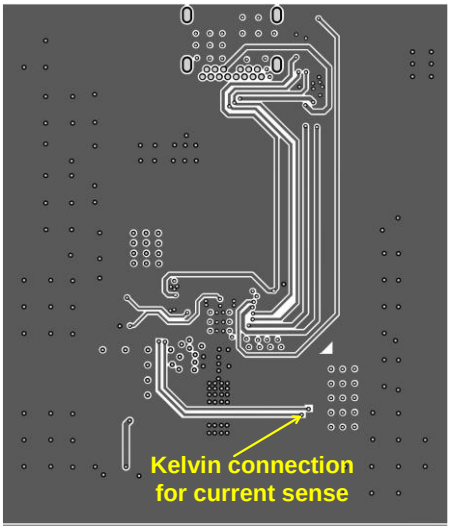
1. Use short, direct, and wide traces to connect OUT. Adding vias under the IC, then route the OUT trace on both PCB layers.
2. Place a large copper plane for PGND. Add multiple vias to improve thermal dissipation. Connect AGND to PGND.
3. Place PGND vias close to PGND pin and under the IC's body.
4. Place the VCC decoupling capacitor as close as possible to the VCC pin. Place 3 vias close to the VCC decoupling capacitor's AGND terminal.
5. Place a large copper plane for SW .
6. Place two ceramic input decoupling capacitors as close as possible to VIN, VOUT, and PGND to improve EMI performance.
7. Place an input filter at the bottom layer to improve EMI performance.
8. Use Kelvin connections for the output current sense traces (ISENS+ and ISENS-).
9. Place the input capacitor also close to the VIN pin as possible. Especially the 0.1µF capacitor should be placed close to the VIN pin and PGND.
10. Make the HS_G trace wide and short.



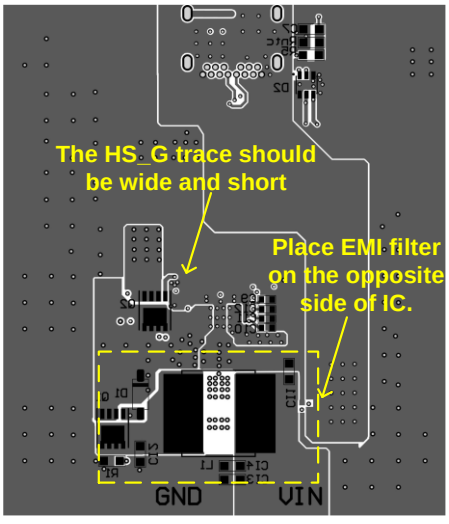
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 23: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

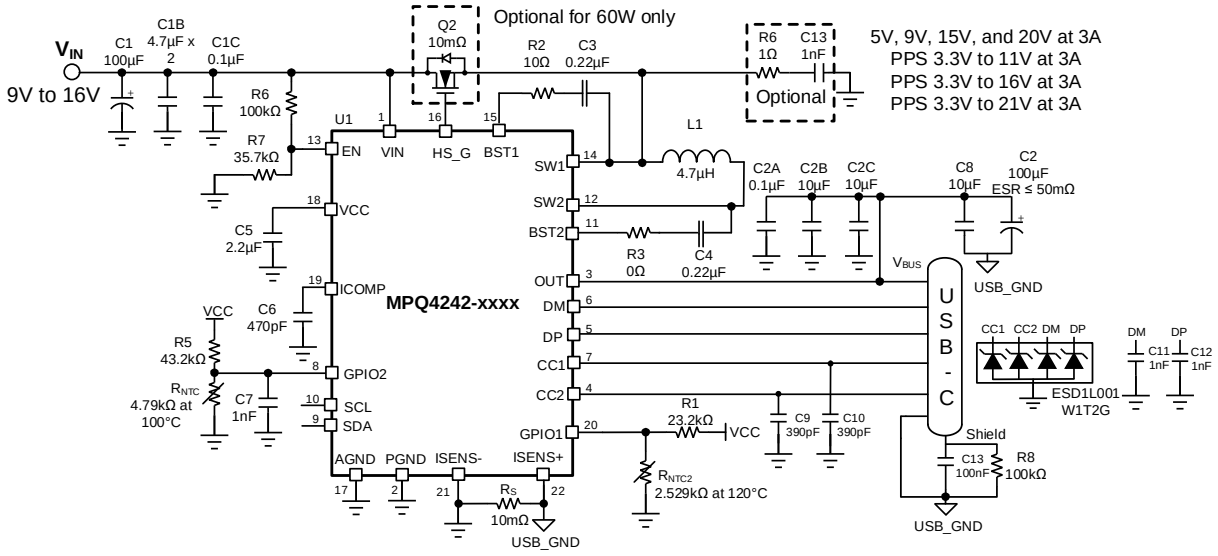


Figure 24: MPQ4242 60W PD Application

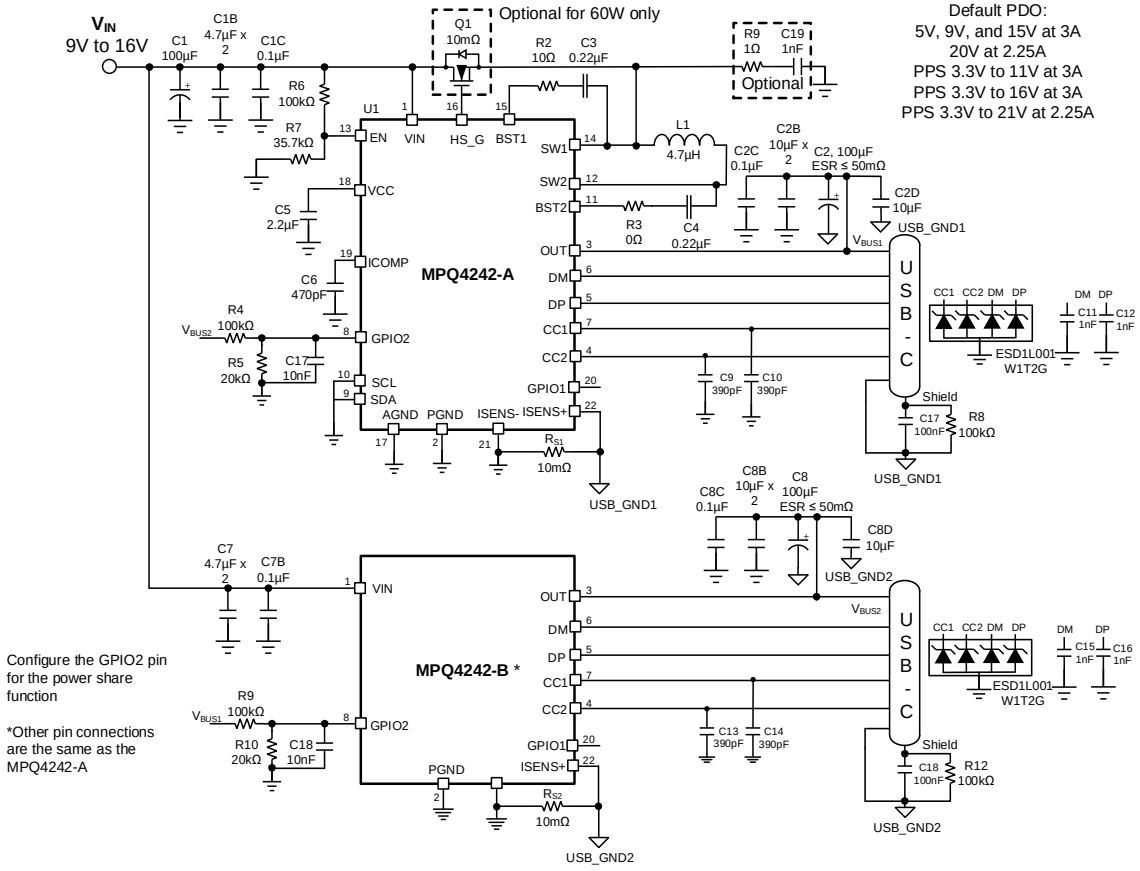


Figure 25: MPQ4242 Dual-Channel 45W PD Application with GPIO2_POWER_SHARE (18) (19) (20)

Notes:

18) See Table 5 on page 29 for the GPIO2 power share PDP management. V_{BUS} exceeds 11.2V to trigger power share function (GPIO2 input voltage > 1.87V).
19) GPIO1 can be configured as a gate drive for the external low-side N-channel power MOSFET used for USB_GND short to battery protection.
20) TVS diodes are required to pass the ±8kV contact =/ ±15kV air discharge per IEC ESD specifications.

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MPQ4242GQV-0000 CONFIGURATION TABLE

OTP Items(PDO)	Enabled/Disabled	PDO Type	Voltage Setting	Current Setting
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled (default)	0b: Fixed PDO (default)	9V (default)	3A
PDO3	1b: Enabled (default)	0b: Fixed PDO (default)	15V (default)	3A
PDO4	1b: Enabled (default)	0b: Fixed PDO (default)	20V (default)	3A
PDO5	1b: Enabled (default)	1b: APDO (default)	3.3V to 11V	3A
PDO6	1b: Enabled (default)	1b: APDO (default)	3.3V to 16V	3A
PDO7	1b: Enabled (default)	1b: APDO (default)	3.3V to 21V	3A

Table 7: OTP Descriptions

OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's function.	000b: POWER_SHARE function (default)
GPIO2	Configures the GPIO2 pin's function.	000b: Reserved
OTP_THRESHOLD	Sets the over-temperature shutdown threshold.	010b: 175°C (default)
OTW1_THRESHOLD	Sets-the over temperature warning threshold.	100b: 135°C (default)
OTW1_PDP	Sets the maximum power rating when the die temp drops below its threshold.	45W (default)
OTW1_PDO_SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
OTW2_THRESHOLD	Sets the over-temperature warning threshold.	110b: 155°C (default)
OTW2_NTC_PDP	Set the maximum power rating when the die temperature drops below its threshold.	30W (default)
OTW2_NTC_PDO_ SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
NTC_HYSTERESIS	Sets the NTC thermal recovery hysteresis.	1b: 20%(default)
NTC_MODE	Sets the MPQ4242 behavior when the NTC is triggered.	1b: Reduce PD power to the value set by OTW2_NTC_PDP
VBATT_LOW_THLD1	Sets the first threshold for V_{IN} detection.	0100b: 11.4V (default)
VBATT_LOW_THLD2	Sets the second threshold for V_{IN} detection.	1000b: 9V (default)
VBATT_LOW_THLD3	Sets the third threshold for V_{IN} detection. The device shuts down after this threshold is triggered.	1010b: 6.2V (default)
VBATT_LOW_BLK	Sets the V_{BATT} low 1 and V_{BATT} low 2 blank times.	10b: 320ms (default)
VBATT_LOW1_PDP	Sets the maximum power rating when V_{BATT} falls below its first threshold.	45W (default)
VBATT_L1_PDO_ SELECT	Select s the voltage that is enabled in the PDO list.	0xBE (default)
VBATT_LOW2_PDP	Sets the maximum power rating when V_{BATT} falls below its second threshold.	15W (default)
VBATT_L2_PDO_SELECT	Selects the voltage that is enabled in the PDO list.	0xBE (default)
PS_PDP_THD	Set the thresholds to which the PDO power rating is reduced.	45W (default)
PS_PDP_THD_PDO_ SELECT	Selects which voltage is enabled in the PDO list.	0xBE (default)
VBUS_VOLTAGE	Sets the default VBUS voltage.	10b: 5.1V (default)

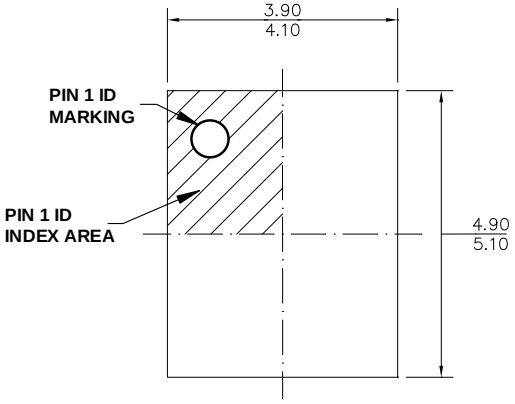
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MODE	Sets the PFM/PWM mode.	1b: Forced PWM mode (default)
FREQ	Sets the switching frequency	01b: 420kHz (default)
DITHER	Sets the spread spectrum feature	0b: No frequency spread spectrum (default)
EN_OFF_TIMER	Sets the EN off timer.	000b: No delay (default)
LINE_DROP_COMP	Sets the output voltage compensation vs load feature.	00b: No compensation (default)
SLEW_RATE	Sets the output slew rate to adjust V_{OUT}.	1b: 0.08mV/μs V_{REF} rising slew rate, 0.08mV/μs V_{REF} falling slew rate (default)
PEAK_CL	Sets the high-side peak current limit in boost mode.	11b: 20A (default)
RSENS	Sets the external CC limit R_{SENS} resistor value.	1b: 10mΩ
EXT_HS_FET_RON	Sets the $R_{DS(ON)}$ of the external N-channel MOSFET at $10V_{GS}$.	000b: This function is disabled (default)
CC_BLANK_TIMER	Sets the blank time when the output CC over-current condition is reached.	01b: 2ms (default)
LEGACY_CHARGING_MODE_SEL	Selects QC 3.0/DCP short mode / Divider mode.	00b: All DCP modes are active (default)
I2C_SLAVE_ADDRESS	Sets the MPQ4242's I^2C slave address.	61h (default)
VIN_OVP	Enables the VIN_OVP function. When V_{IN} > 22V, the MPQ4242 shuts down.	0b: Disable VIN_OVP function

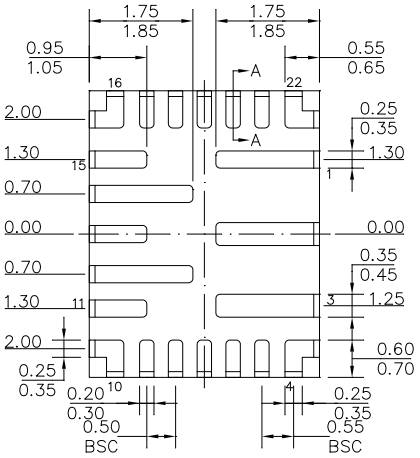
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PACKAGE INFORMATION

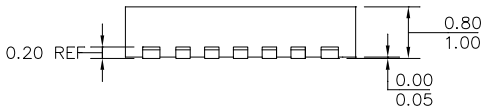
QFN-22 (4mmx5mm)



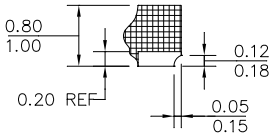
TOP VIEW



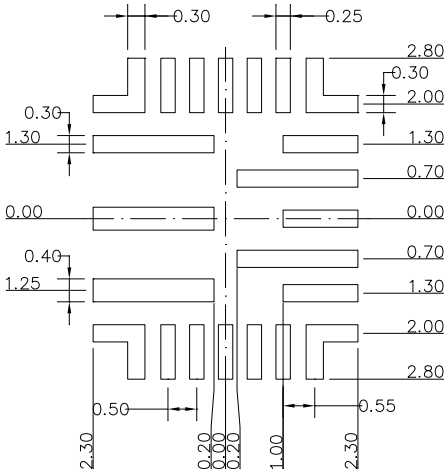
BOTTOM VIEW



SIDE VIEW



SECTION A-A



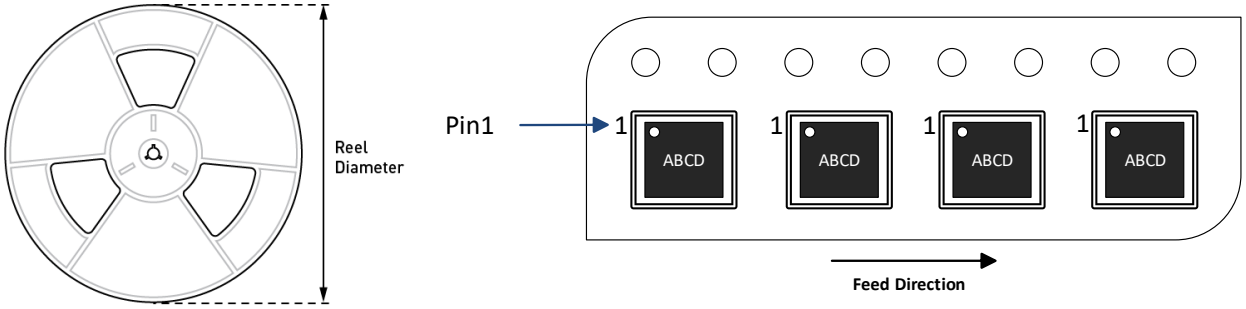
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4242GVE-0000-AEC1-Z	QFN-22 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4242GVE-0001-AEC1-Z	QFN-22 (4mmx5mm)						
MPQ4242GVE-0015-AEC1-Z	QFN-22 (4mmx5mm)						
MPQ4242GVE-xxxx-AEC1-Z	QFN-22 (4mmx5mm)						

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/10/2022	Initial Release	-

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