

NTD5414N, NVD5414N

Power MOSFET

24 A, 60 V Single N-Channel DPAK

Features

- Low $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- LED Lighting and LED Backlight Drivers
- DC-DC Converters
- DC Motor Drivers
- Power Supplies Secondary Side Synchronous Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	60	V
Gate-to-Source Voltage – Continuous			V _{GS}	± 20	V
Gate-to-Source Voltage – Nonrepetitive (T _P < 10 μs)			V _{GS}	± 30	V
Continuous Drain Current R _{θJC} (Note 1)	Steady State	T _C = 25°C	I _D	24	A
		T _C = 100°C		16	
Power Dissipation R _{θJC} (Note 1)	Steady State	T _C = 25°C	P _D	55	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	75	A
Operating and Storage Temperature Range			T _J , T _{stg}	–55 to +175	°C
Source Current (Body Diode)			I _S	24	A
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 50 V _{dc} , V _{GS} = 10 V, I _{L(pk)} = 24 A, L = 0.3 mH, R _G = 25 Ω)			E _{AS}	86.4	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	2.7	$^\circ\text{C/W}$
	$R_{\theta JA}$	58.6	

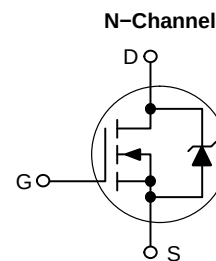
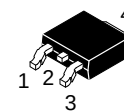
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).



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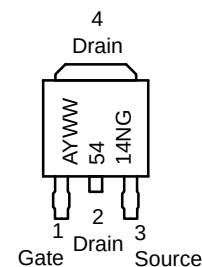
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
60 V	37 m Ω @ 10 V	24 A



DPAK
CASE 369AA
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
5414N = Specific Device Code
G = Pb-Free Device

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD5414N, NVD5414N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			67.3		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 150^\circ\text{C}$		50	
Gate-Body Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0	3.2	4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(th)}/T_J$			0.74		mV/ $^\circ\text{C}$
Drain-to-Source On-Voltage	$V_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		0.7	1.16	V
		$V_{GS} = 10\text{ V}, I_D = 12\text{ A}, 150^\circ\text{C}$		0.7		
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}$		28.4	37	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		24		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		800	1200	pF
Output Capacitance	C_{oss}			165		
Transfer Capacitance	C_{rss}			75		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V},$ $I_D = 24\text{ A}$		25	48	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.1		
Gate-to-Source Charge	Q_{GS}			4.8		
Gate-to-Drain Charge	Q_{GD}			11.3		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10\text{ V}, V_{DD} = 48\text{ V},$ $I_D = 24\text{ A}, R_G = 9.1\text{ }\Omega$		12		ns
Rise Time	t_r			58		
Turn-Off Delay Time	$t_{d(off)}$			47		
Fall Time	t_f			69		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 2)	V_{SD}	$V_{GS} = 0\text{ V}$ $I_S = 24\text{ A}$	$T_J = 25^\circ\text{C}$		0.92	1.15	V
			$T_J = 125^\circ\text{C}$		0.8		
Reverse Recovery Time	t_{rr}	$I_S = 24\text{ A}_{dc}, V_{GS} = 0\text{ V}_{dc},$ $dI_S/dt = 100\text{ A}/\mu\text{s}$			45.7		ns
Charge Time	t_a				31.7		
Discharge Time	t_b				14		
Reverse Recovery Stored Charge	Q_{RR}				76		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

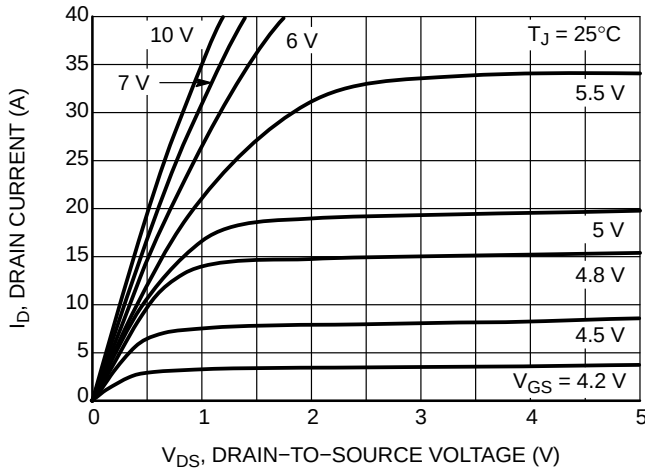


Figure 1. On-Region Characteristics

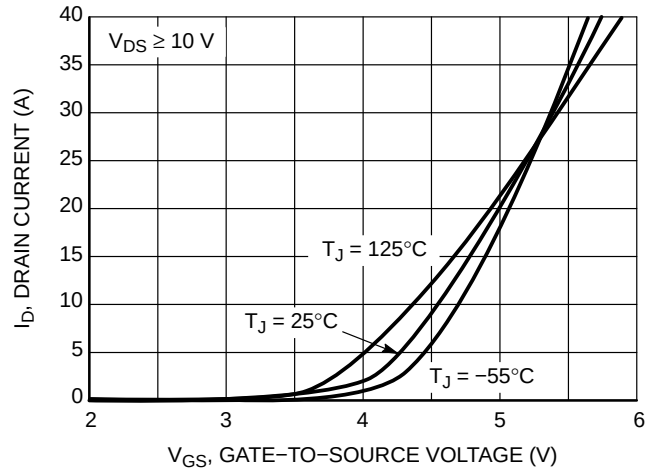


Figure 2. Transfer Characteristics

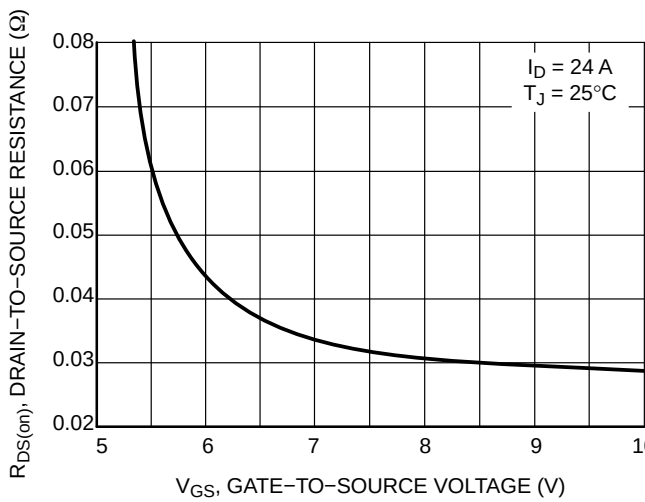


Figure 3. On-Resistance vs. Gate-to-Source Voltage

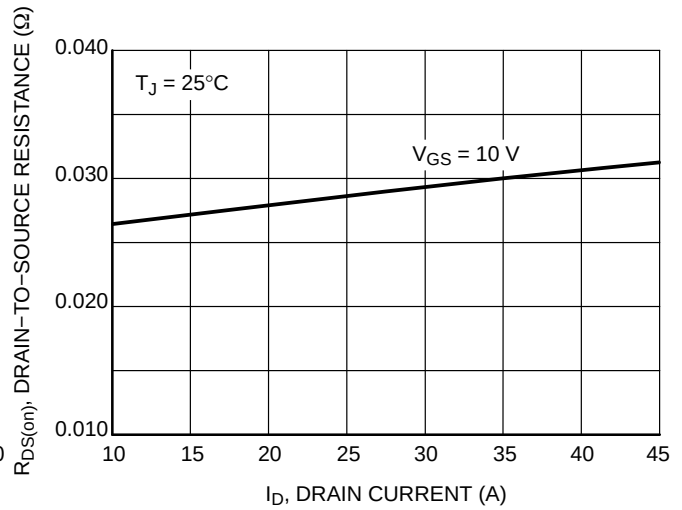


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

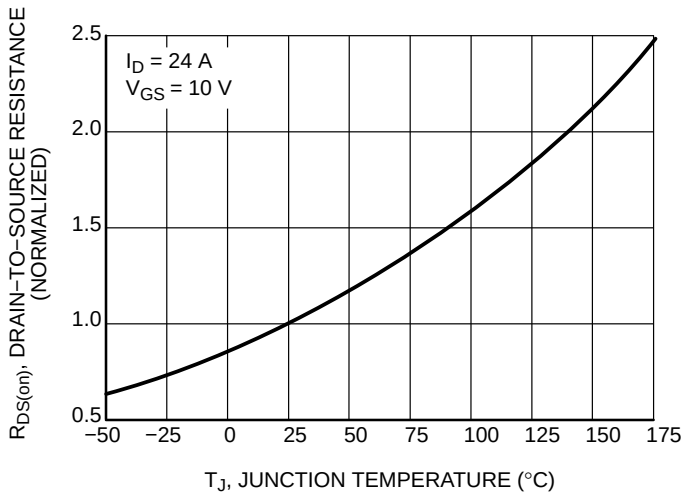


Figure 5. On-Resistance Variation with Temperature

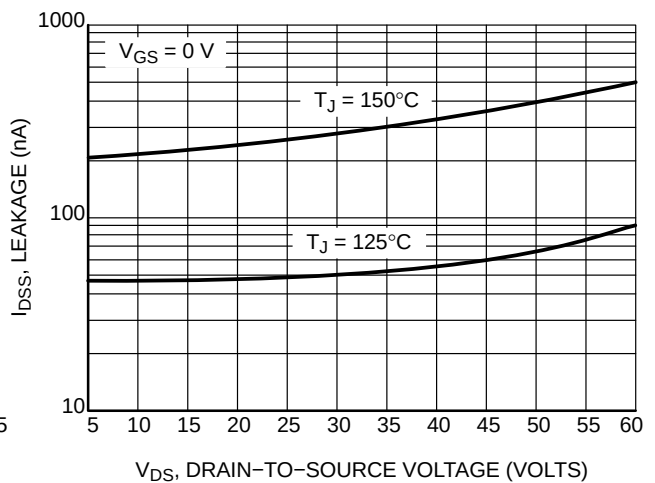


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

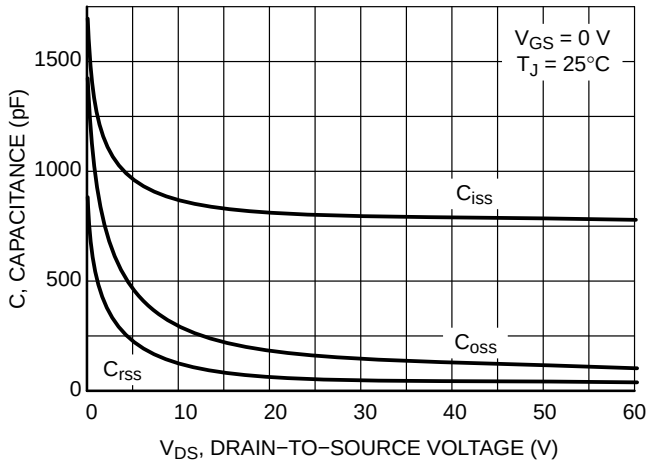


Figure 7. Capacitance Variation

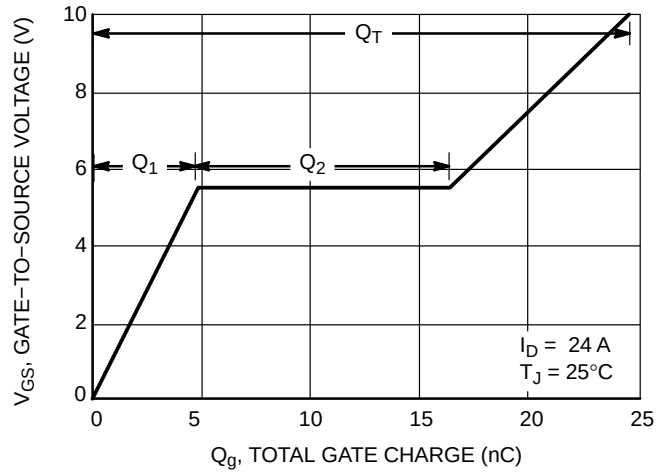


Figure 8. Gate-to-Source Voltage vs. Total Charge

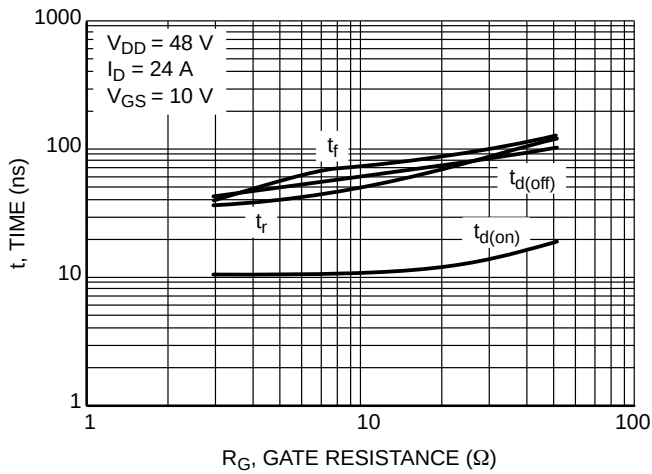


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

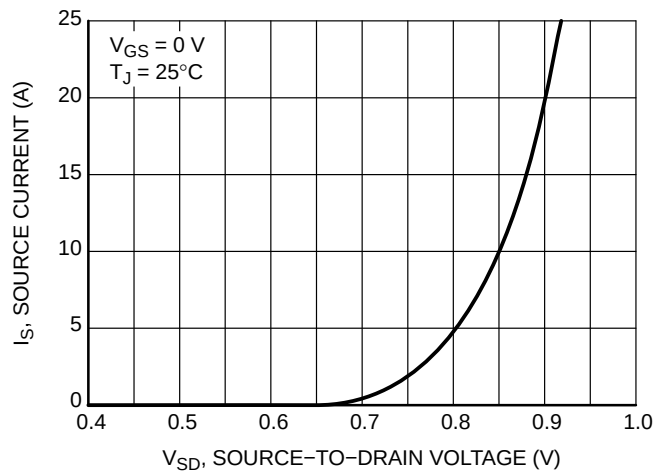


Figure 10. Diode Forward Voltage vs. Current

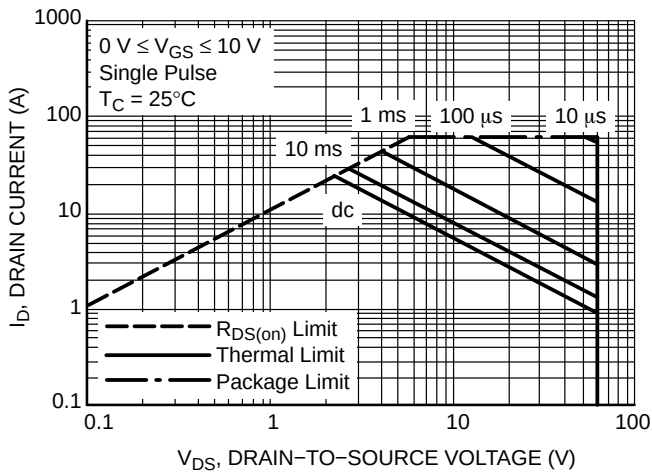


Figure 11. Maximum Rated Forward Biased Safe Operating Area

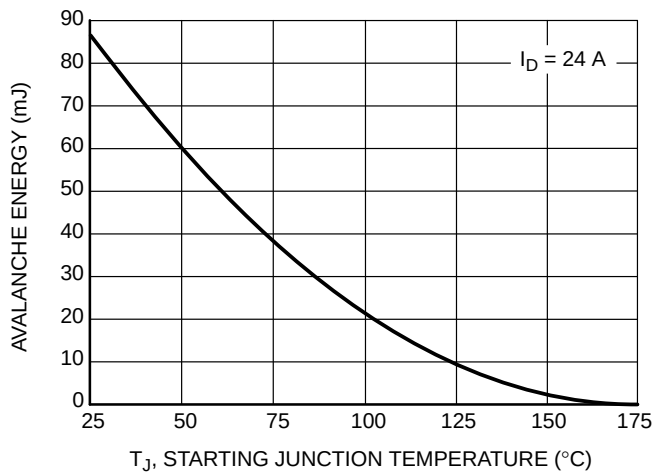


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD5414N, NVD5414N

TYPICAL PERFORMANCE CURVES

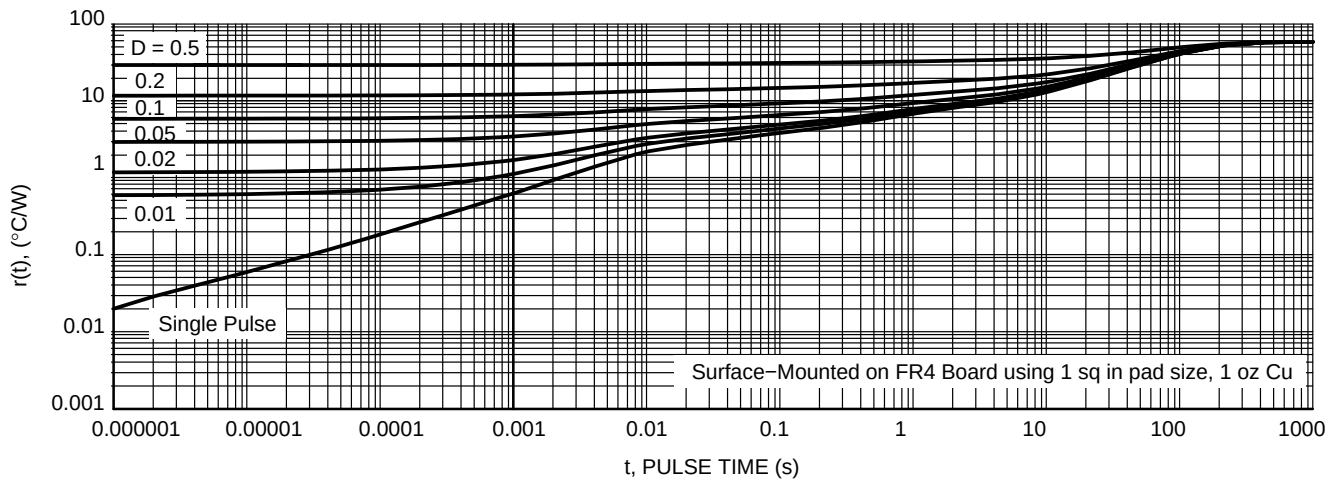


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD5414NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD5414NT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

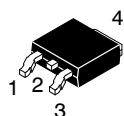
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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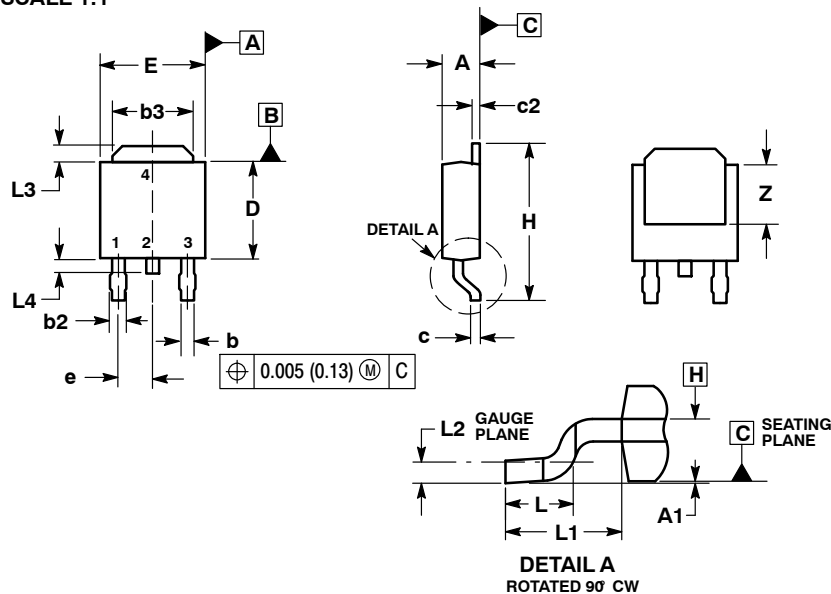
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



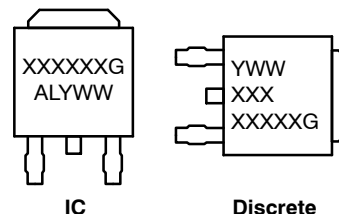
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

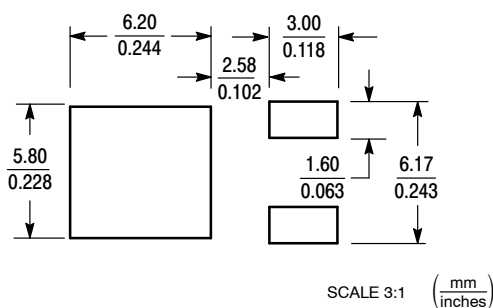
GENERIC MARKING DIAGRAM*



- XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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