LogiCORE PCI Interface v3.0

DS 208 (v.1.2) June 28, 2002 **Data Sheet, v3.0.99**

Introduction

With the Xilinx LogiCORE PCI-X Interface, a designer can build a customized PCI-X 1.0a-compliant core with high sustained performance, 800 Mbytes/sec.

Features

- Fully PCI-X 1.0a-compliant core, 64-bit, 100/66/33 MHz interface with 3.3 V operation
- Customizable, programmable, single-chip solution
- Predefined implementation for predictable timing
- Incorporates Xilinx Smart-IP Technology
- Fully verified design tested with Xilinx proprietary test-bench and hardware
- Available for configuration and download on the web:
  - Web-based Configuration and Download Tool
  - Web-based User Constraint File Generator Tool
- Instant Access to New Releases
- Integrated extended capabilities:
  - PCI-X Capability Item
  - Power Management Capability Item
  - Message Signalled Interrupt Capability Item
- Supported PCI-X only functions:
  - Split Completion
  - Memory Read Dword
  - Memory Read Block
  - Memory Write Block
- Supported PCI only functions:
  - Memory Read
  - Memory Read Multiple
  - Memory Read Line
  - Memory Write and Invalidate

LogiCORE Facts

PCI-X64 / PCI64 Resource Utilization[1]	
Slice Four Input LUTs	2646
Slice Flip Flops	1605
IOB Flip Flops	257
IOBs	90
BUFGs / DCMs	2 / 1
PCI-X64 Mode Only Resource Utilization[1]	
Slice Four Input LUTs	2126
Slice Flip Flops	1461
IOB Flip Flops	257
IOBs	90
BUFGs / DCMs	1 / 1
PCI64 Mode Only Resource Utilization[1]	
Slice Four Input LUTs	1915
Slice Flip Flops	1350
IOB Flip Flops	253
IOBs	90
BUFGs / DCMs	1 / 0
Provided with Core	
Documentation	*PCI-X Design Guide* *PCI-X Implementation Guide*
Design File Formats	Verilog/VHDL Simulation Model NGO Netlist
Constraint Files	User Constraint Files (UCF)
Example Design	Verilog/VHDL Example Design
Design Tool Requirements	
Xilinx Tools	v4.2i, Service Pack 3
Tested Entry and Verification Tools[2]	Synplicity Synplify Synopsys FPGA Express Exemplar Leonardo Spectrum Xilinx XST[3] Cadence Verilog XL Model Technology ModelSim

1. The resource utilization depends on configuration of the interface and the user design. Unused resources are trimmed by the Xilinx technology mapper. The utilization figures reported in this table are representative of a maximum configuration.
2. See the implementation guide or product release notes for current supported versions.
3. XST is command line option only. See Implementation Guide for details.

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LogiCORE Facts (Cont)		
PCI-X 64 Supported Devices		
PCI64/33 Only	Virtex-E V300EBG432-8C Virtex-II 2V1000FG456-5C	3.3v only 3.3v only
PCI-X64/66 Only	Virtex-E V300EBG432-8C Virtex-II 2V1000FG456-5C	3.3v only 3.3v only
PCI-X64/100 Only	Virtex-II 2V1000FG456-5C	3.3v only
PCI-X64/66 PCI64/33	Virtex-II 2V1000FG456-5C	3.3v only
Xilinx provides technical support for this LogiCORE product when used as described in the Design Guide and the Implementation Guide. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices not listed, or if customized beyond that allowed in the product documentation.		

Note: Fully compliant designs over 66 MHz require two bitstreams.
Note: Universal card implementations not supported.
Note: Commercial devices only; 0 C < T_j < 85 C.

More Features

- Supported PCI and PCI-X functions:
  - Memory Write
  - I/O Read
  - I/O Write
  - Configuration Read
  - Configuration Write
  - Interrupt Acknowledge
  - Bus Parking
  - Type 0 Configuration Space Header
  - Full 64-bit Addressing Support
  - Up to 6 Base Address Registers
  - Expansion ROM Base Address Register
  - Instant-On Base Address Registers
  - Parity Generation, Parity Error Detection
  - Full Command/Status Registers

Applications

- Embedded applications in networking, industrial, and telecommunication systems
- PCI-X add-in boards such as frame buffers, network adapters, and data acquisition boards
- Hot swap CompactPCI-X boards
- Any applications that need a PCI-X interface

General Description

The LogiCORE PCI-X Interface is a preimplemented and fully tested module for Xilinx FPGAs. Critical paths are controlled by constraint and guide files to ensure predictable timing. This significantly reduces the engineering time required to implement the PCI-X portion of your design. Resources can instead be focused on your unique user application logic in the FPGA and on the system level design. As a result, LogiCORE PCI-X products minimize your product development time.

The core meets the setup, hold, and clock to timing requirements as specified in the PCI-X specification. The interface is verified through extensive simulation.

Other features that enable efficient implementation of a PCI-X system include:

- Block SelectRAM™ memory. Blocks of on-chip ultra-fast RAM with synchronous write and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.
- SelectRAM memory. Distributed on-chip ultra-fast RAM with synchronous write option and dual-port RAM capabilities. Used in PCI-X designs to implement FIFOs.

The interface is carefully optimized for best possible performance and utilization in Xilinx FPGA devices.

Smart-IP Technology

Drawing on the architectural advantages of Xilinx FPGAs, Xilinx Smart-IP technology ensures the highest performance, predictability, repeatability, and flexibility in PCI-X designs. The Smart-IP technology is incorporated in every LogiCORE PCI-X Interface.

Xilinx Smart-IP technology leverages the Xilinx architectural advantages, such as look-up tables and segmented routing, as well as floorplanning information, such as logic mapping and location constraints. This technology provides the best physical layout, predictability, and performance. Additionally, these features allow for significantly reduced compile times over competing architectures.

To guarantee the critical setup, hold, minimum clock to out, and maximum clock to out timing, the PCI-X interface is delivered with Smart-IP constraint files that are unique for a device and package combination. These constraint files guide the implementation tools so that the critical paths always are within specification.

Xilinx provides Smart-IP constraint files for many device and package combinations. Constraint files for unsupported device and package combinations may be generated using the web-based constraint file generator.

Functional Description

The LogiCORE PCI-X Interface is partitioned into six major blocks and a user application as shown in Figure 1.

Datapath

There are four datapaths, in and out for both target and initiator. To improve timing and ease of design, the four unidirectional datapaths are multiplexed inside the interface. All data transfers are register-to-register. Since fewer registers are on each datapath, loading is reduced and false timing paths are eliminated.

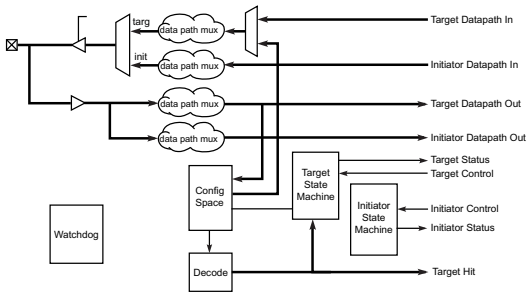


Figure 1: **LogiCORE PCI-X Interface Block Diagram**

Decode

When an address is broadcast on the bus, the decode module compares it to the base address registers for a match. If one occurs, the target state machine is activated.

PCI-X Configuration Space

This block provides the first 64 bytes of Type 0, version 2.3 Configuration Space Header, and an additional 64 bytes reserved for extended capabilities, as shown in Table 1. The remaining 128 bytes of configuration space are available to the user for application specific registers. Together, these support software-driven “Plug-and Play” initialization and configuration. This includes information for Command, Status, Base Address Registers, and the extended capabilities required for PCI-X.

Three extended capabilities are provided in the interface:

- PCI-X Capability Item
- Power Management Capability Item
- Message Signalled Interrupt Capability Item

These capability items may be linked or delinked from the capabilities list as required, and user functions can be integrated into the capabilities list.

Table 1: **PCI-X Configuration Space Header**

31	24	23	16	15	8	7	0	
Device ID				Vendor ID				00h
Status				Command				04h
Class Code							Rev ID	08h
BIST		Header Type		Latency Timer			Cache Line Size	0Ch
Base Address Register 0 (BAR0)								10h
Base Address Register 1 (BAR1)								14h
Base Address Register 2 (BAR2)								18h
Base Address Register 3 (BAR3)								1Ch
Base Address Register 4 (BAR5)								20h
Base Address Register 5 (BAR5)								24h
Cardbus CIS Pointer								28h
Subsystem ID				Subsystem Vendor ID				2Ch
Expansion ROM Base Address								30h
Reserved							CapPtr	34h
Reserved								38h
Max Lat		Min Gnt		Interrupt Pin			Interrupt Line	3Ch
Power Management Capability				NxtCap			PM Cap	40h
Data		PMCSR BSE		PMCSR				44h
Message Control				NxtCap			MSI Cap	48h
Message Address								4Ch
Message Upper Address								50h
Reserved				Message Data				54h
PCI-X Command				NxtCap			PCI-X Cap	58h
PCI-X Status								5Ch
Reserved								60h-7Fh
Available User Configuration Space								80h-FFh

Note:
Shaded areas are not implemented and return zero.

Watchdog

The watchdog monitors various system conditions, including bus mode and bus width. This module also indicates if run-time reconfiguration is required for loading different bitstreams.

Target State Machine

This block controls the PCI-X and PCI interface for target functions. The controller is a high-performance state machine using one-hot encoding for maximum performance.

Initiator State Machine

This block controls the PCI-X and PCI interface for initiator functions. The initiator control logic also uses one-hot encoding for maximum performance.

User Interface

The PCI-X interface provides a simplified user application interface which allows a user to create one design that handles both PCI-X and PCI transactions without design changes, and both 32-bit and 64-bit data transfers without external data width conversion. This eliminates the need for multiple designs to support PCI-X and PCI and varying bus widths.

This streamlined interface also simplifies the amount of work needed to create a user application. The user interface can be designed as either a 32-bit or 64-bit interface and the PCI-X interface will automatically handle data conversions regardless of the width of the PCI-X or PCI bus.

Interface Configuration

The LogiCORE PCI-X Interface can easily be configured to fit unique system requirements by using the Xilinx Web-based Configuration and Download Tool or by changing the HDL configuration file. The following customization options, among many others, are supported by the interface and are described in the product design guide.

- Base Address Registers (number, size, and mode)
- Expansion ROM BAR
- Cardbus CIS pointer
- Configuration Space Header ROM
- Interrupt Connectivity
- Extended Command Use
- Capability Configuration

Burst Transfer

The PCI-X bus derives its performance from its ability to support burst transfers. The performance of any PCI-X application depends largely on the size of the burst transfer. Buffers to support PCI-X burst transfer can efficiently be implemented using on-chip RAM resources.

Supported PCI Commands

Table 2 lists the PCI bus commands supported by the LogiCORE PCI-X Interface, and Table 3 lists the supported PCI-X bus commands.

Table 2: **PCI Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read[1]	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	Ignore	Ignore
1001	Reserved	Ignore	Ignore
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Memory Read Multiple[2]	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line[2]	Yes	Yes
1111	Memory Write Invalidate[2]	Yes	Yes

1. This command can only be used for a single dword transfer.
2. These commands have fixed byte enables of 0h.

Table 3: **PCI-X Bus Commands**

CBE [3:0]	Command	Initiator	Target
0000	Interrupt Acknowledge	Yes	Yes
0001	Special Cycle	Yes	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	Ignore	Ignore
0101	Reserved	Ignore	Ignore
0110	Memory Read Dword	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Alias to Memory Read Block	Yes	Yes
1001	Alias to Memory Write Block	Yes	Yes
1010	Configuration Read	Yes	Yes
1011	Configuration Write	Yes	Yes
1100	Split Completion	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Block	Yes	Yes
1111	Memory Write Block	Yes	Yes

Bandwidth

The LogiCORE PCI-X Interface supports fully compliant zero wait-state burst operations for both sourcing and receiving data. This interface supports a sustained bandwidth of up to 800 MBytes/sec. The design can be configured to take advantage of the ability of the LogiCORE PCI-X Interface to do very long bursts.

The flexible user application interface, combined with support for many different PCI-X features, gives users a solution that lends itself to use in many high-performance applications. The user is not locked into one DMA engine, hence, an optimized design that fits a specific application can be designed.

Recommended Design Experience

The LogiCORE PCI-X Interface is pre-implemented allowing engineering focus on the unique user application functions of a PCI-X design. Regardless, PCI-X is a high-performance design that is challenging to implement in any technology. Therefore, previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, constraint files, and guide files is recommended. The challenge to implement a complete PCI-X design including user application functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Timing Specifications

The maximum speed at which your user design is capable of running can be affected by the size and quality of the design. The following tables show the key timing parameters for the LogiCORE PCI-X Interface. Timing Parameters in the 66MHz PCI-x are listed in Table 4. Timing Parameters in the 33MHz PCI are listed in Table 5.

Ordering Information

This core may be downloaded from the Xilinx IP Center for use with the Xilinx CORE Generator System V4.1 and later. The Xilinx CORE Generator System tool is bundled with all Alliance and Foundation Series Software packages, at no additional charge.

Part Numbers

DO-DI-PCIX64-VE

-PCI-X 64-bit 66/100 MHz IP only Core

DX-DI-64IP-XVE

- Upgrade from DO-DI-PCI64/DO-DI-PCI-AL/DO-DI-PCI64DK to DO-DI-PCIX64-VE

To order Xilinx's PCI Core, please visit the Xilinx Silicon Xpresso Cafe or contact your local Xilinx sales representative.

Information on additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

Table 4: **Timing Parameters, 66MHz PCI-X**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	15[1]	20
T_{high}	CLK High Time	6	-
T_{low}	CLK Low Time	6	-
T_{val}	CLK to Signal Valid Delay (bussed signals)	0.7[2]	3.8[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	0.7[2]	3.8[2]
T_{on}	Float to Active Delay	0[2]	-
T_{off}	Active to Float Delay	-	7[2]
T_{su}	Input Setup Time to CLK (bussed signals)	1.7[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	1.7[2]	-
T_{h}	Input Hold Time from CLK	0.5[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCIX.
3. Operation at 100 MHz requires T_{su} of 1.2 and T_{cyc} of 10.

Table 5: **Timing Parameters, 33MHz PCI**

Symbol	Parameter	Min	Max
T_{cyc}	CLK Cycle Time	30[1]	-
T_{high}	CLK High Time	11	-
T_{low}	CLK Low Time	11	-
T_{val}	CLK to Signal Valid Delay (bussed signals)	2[2]	11[2]
T_{val}	CLK to Signal Valid Delay (point to point signals)	2[2]	11[2]
T_{on}	Float to Active Delay	2[2]	-
T_{off}	Active to Float Delay	-	28[1]
T_{su}	Input Setup Time to CLK (bussed signals)	7[2]	-
T_{su}	Input Setup Time to CLK (point to point signals)	10[2]	-
T_{h}	Input Hold Time from CLK	0[2]	-
T_{rstoff}	Reset Active to Output Float	-	40

Notes:
1. Controlled by timespec constraints, included in product.
2. Controlled by SelectIO configured for PCI33_3 or PCIX.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/28/02	1.0	New template