32-Bit

Microcontroller

TC37xEXT

32-Bit Single-Chip Microcontroller
AB-Step

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1, 2021-03

Microcontroller

OPEN MARKET VERSION

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1 Summary of Features

The TC37xEXT product family has the following features:

- High Performance Microcontroller with three CPU cores
- Three 32-bit super-scalar TriCore CPUs (TC1.6.2P), each having the following features:
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - up to 300 MHz operation at full temperature range
  - up to 240/96 Kbyte Data Scratch-Pad RAM (DSPR)
  - up to 64 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 32 Kbyte Instruction Cache (ICACHE)
  - 16 Kbyte Data Cache (DCACHE)
- Lockstepped shadow cores for up to three TC1.6.2P
- Multiple on-chip memories
  - All embedded NVM and SRAM are ECC protected
  - up to 6 Mbyte Program Flash Memory (PFLASH)
  - up to 256 Kbyte Data Flash Memory (DFLASH 0) usable for EEPROM emulation
  - BootROM (BROM)
- 128-Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
  - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - SRI to SPB bus bridges (SFI Bridge)
- Optional Hardware Security Module (HSM) on some variants
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
  - 12 Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
  - 5 Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
  - 1 High Speed Serial Link (HSSL) for serial inter-processor communication up to 320 Mbit/s
  - 2 serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - 3 MCMCAN Modules with 4 CAN nodes for high efficiency data handling via FIFO buffering
  - 15 Single Edge Nibble Transmission (SENT) channels for connection to sensors
  - 1 FlexRay™ module with 2 channels (E-Ray) supporting V2.1
  - One Generic Timer Module (GTM) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)

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  - One General Purpose 12 Timer Unit (GPT120)
  - 2 channel Peripheral Sensor Interface conforming to V1.3 (PSI5)
  - 1 Peripheral Sensor Interface with Serial PHY (PSI5-S)
  - 1 Inter-Integrated Circuit Bus Interface (I2C) conforming to V2.1
  - 2 IEEE802.3 Ethernet MAC with RMII and MII interfaces (ETH)
- Versatile Successive Approximation ADC (VADC)
  - Cluster of 12 independent ADC kernels
  - Input voltage range from 0 V to 5.5V (ADC supply)
- Delta-Sigma ADC (DSADC)
  - 6 channels
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- multi-core debugging, real time tracing, and calibration
- four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Peripheral PLL
- Embedded Voltage Regulator
- Qualified for automotive application according to AEC-Q100 (only applicable after delivery release of the corresponding sales codes)
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL D (only applicable for sales codes listed within a released Safety Package Release Note from IFX)

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Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

Table 1-1 Platform Feature Overview

Feature		TC37xEXT
CPUs	Type	TC1.6.2
	Cores / Checker Cores	3 / 3
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	64 KB
	DSPR	240 KB for CPU0,1/ 96 KB else
	DLMU	64 KB
SRAM global	DAM	32 KB
Extension Memory	TCM	2 MB
	XCM	1 MB
	XTM	16 KB
Program Flash	Size	6 MB
	Banks	2 x 3 MB
Data Flash	Size (single-ended)	256 KB (DF0) + 128 KB (DF1)
DMA	Channels	128
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	4 / 32
	Secondary Groups/Channels	4 / 64
	Fast Compare Channels	4
EDSADC	Channels	6

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Table 1-1 Platform Feature Overview (cont'd)

Feature		TC37xEXT
GTM	Clusters	6 (5 @ 200 MHz, 1 @ 100 MHz)
	TIM (8 ch)	6
	TOM (16 ch)	3
	ATOM (8 ch)	6
	MCS (8 ch)	5
	CMU / ICM	1 / 1
	PSM	1
	TBU channels[1)]	4 (TBU0-3)
	SPE	2
	CMP / MON	1 / 1
	BRC / DPLL	1 / 1
	CDTM modules	5
	DTM modules	16 (6 on TOM, 10 on ATOM)
Timer	GPT12	1
	CCU6	1
STM	Modules	3
FlexRay	Modules	1
	Channels	2
CAN	Modules	3
	Nodes	3 x 4
	of which support TT-CAN	1
QSPI	Modules	5
	HSCI Channels	0
ASCLIN	Modules	12
I2C	Interfaces	1
SENT	Channels	15
PSI5	Modules	2
PSI5-S	Modules	1
HSSL	Channels	1
MSC	Channels	2
SDMMC	eMMC/SD Interface	1
CIF	Camera Interface	1
Ethernet (10/100Mbit/1Gbit)	Modules	2
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
Security	HSM+	1

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Table 1-1 Platform Feature Overview (cont'd)

Feature		TC37xEXT
Debug	OCDS	yes
	MCDS	yes
	miniMCDS	-
	miniMCDS TRAM	-
	AGBT 2)	yes
Low Power Features	Standby RAM	2
	SCR	yes
Packages	Type	Pad Position Configuration / LFBGA-292 / LQFP-176 / LFQP-144
I/O	Type	5 V CMOS / 3.3 V CMOS / LVDS
$T_{ambient}$	Range	−40 … +150°C

1) TBU3 has special purpose as angle clock.

2) The Aurora Gigabit Trace Module (AGBT) is a trace interface intended for development use only (not to be used in series production). It is only available on the specific emulation devices with feature package E, T, and on ADAS devices with feature package A, H of the TC39x, TC37xEXT, TC35x, TC33xEXT. AGBT I/O functions are only available for packages with 292 or more pins. For details on AGBT parameters see the "TC3xx Emulation Devices" Data Sheet.

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2 TC37xEXT Pin Definition and Functions

The following figures show the TC37xEXT package variants:

- LFBGA-292 for feature package TE (**Figure 2-1**)
- LFBGA-292 for feature package TX (**Figure 2-2**)
- LQFP-176 for feature package (**Figure 2-3**)
- LQFP-144 for feature package (**Figure 2-4**)
- Sequence of Pads in Pad Frame (**Chapter 2.5**)

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2.1 LFBGA-292 Package Pinning of TC37xEXT TE

Note: In the following LFBGA package the VFLEX2 supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC1	VEXT	P10.7	P10.6	P10.2	P10.3	P10.0	P11.11	P11.9	P11.2	P13.3	P13.1	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A
B	P02.0	VSS	VEXT	P10.8	P10.5	P10.4	P10.1	P11.12	P11.10	P11.3	P13.2	P13.0	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B
C	P02.2	P02.1																	P15.2	P20.14	C
D	P02.4	P02.3		VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS		P20.12	P20.13	D
E	P02.6	P02.5		P02.9	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9		P20.10	P20.11	E
F	P02.8	P02.7		P02.11	P02.10											$\overline{\text{ESR0}}$	P20.6		P20.7	P20.8	F
G	P00.0	P00.1		P01.4	P01.3			VDDSB (VDD)	VSS	DAPE2	DAPE1	VSS	VDD			$\overline{\text{ESR1}}$	$\overline{\text{PORST}}$		P20.1	P20.3	G
H	P00.2	P00.3		P01.6	P01.5		VDDSB (VDD)		VSS	VSS	VSS	VSS		VDD		P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H
J	P00.4	P00.5		P00.6	P01.7		VSS	VSS		VSS	VSS		VSS	VSS		TCK	P21.1		P21.3	P21.5	J
K	P00.7	P00.9		P00.8	P00.10		AGBTC LKP (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	DAPE0		TMS	P21.0		P21.2	P21.4	K
L	P00.11	P00.12		AN43	AN42		AGBTC LKN (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	AGBTE RR (VSS)		P22.10	P22.11		$\overline{\text{TRST}}$	VSS	L
M	AN46	AN47		AN41	AN40		VSS	VSS		VSS	VSS		VSS	VSS		P22.8	P22.9		XTAL2	XTAL1	M
N	AN44	AN45		AN36 / P40.6	AN38 / P40.8		VDD		VSS	VSS	VSS	VSS		VDD		P22.6	P22.7		VDD	VEXT	N
P	AN39 / P40.9	AN37 / P40.7		AN32 / P40.4	AN34			VDD	VSS	AGBTT XN (VSS)	AGBTT XP (VSS)	VSS	VDD			P22.4	P22.5		P22.1	P22.0	P
R	AN33 / P40.5	AN35		AN31	AN23											P23.7	P23.6		P22.3	P22.2	R
T	VAREF 2	VAGND 2		AN30	AN22	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	P34.4	P33.14	P32.5	VSS	P23.5		P23.3	P23.4	T
U	AN29 / P40.14	AN28 / P40.13		NC1	AN17 / P40.10	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	P34.5	P33.15	P32.6	P32.7	VSS		P23.1	P23.2	U
V	AN27 / P40.3	AN26 / P40.2																	VEXT	P23.0	V
W	AN25 / P40.1	AN24 / P40.0	AN19 / P40.12	AN18 / P40.11	AN16	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE 1P	P32.4	VSS	VEXT	W
Y	NC1	AN21	AN20	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE 1N	P32.2	P32.3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

TC37xed - (top view)

Figure 2-1 TC37xEXT TE package variant LFBGA-292

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Table 2-1 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	CIF_D9			**sensor pixel data input**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CIF_D10			**sensor pixel data input**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	CIF_D11			**sensor pixel data input**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CIF_D12			**sensor pixel data input**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	CIF_D13			**sensor pixel data input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CIF_D14			**sensor pixel data input**
	CAN11_RXDB			**CAN receive input node 1**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	CIF_D15			**sensor pixel data input**
	ASCLIN5_ARXA			**Receive input**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	CIF_PCLK			**Sensor Pixel Clock input**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CIF_VSYNC			**vertical synchronization signal input**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CIF_HSYNC			**horizontal synchronization signal input**
	CCU60_T12HRC			**External timer start 12**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN1_11			**Mux input channel 1 of TIM module 4**
	GTM_TIM1_IN1_1			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_1			**Mux input channel 1 of TIM module 0**
	SENT_SENT9B			**Receive input channel 9**
	EDSADC_DSDIN1A			**Digital datastream input, channel 1**
	EVADC_G9CH2	AI		**Analog input channel 2, group 9**
	EDSADC_EDS4PB			**Positive analog input channel 4, pin B**
	P00.10	O0		**General-purpose output**
	GTM_TOUT19	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC9	O6		**Transmit output**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN2_11			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	SENT_SENT10B			**Receive input channel 10**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	EVADC_FC3CH0			**Analog input FC channel 3**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

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Table 2-2 Port 01 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P01.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_2			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_14			**Mux input channel 0 of TIM module 2**
	GTM_TIM0_IN5_8			**Mux input channel 5 of TIM module 0**
	QSPI3_SLSIB			**Slave select input**
	EVADC_G9CH14	AI		**Analog input channel 14, group 9**
	P01.3	O0		**General-purpose output**
	GTM_TOUT111	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_SLSO9	O4		**Master slave select output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
G4	P01.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_2			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_14			**Mux input channel 1 of TIM module 2**
	GTM_TIM0_IN6_8			**Mux input channel 6 of TIM module 0**
	CAN01_RXDC			**CAN receive input node 1**
	EVADC_G9CH13	AI		**Analog input channel 13, group 9**
	P01.4	O0		**General-purpose output**
	GTM_TOUT112	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASLSO	O3		**Slave select signal output**
	QSPI3_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P01.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_2			**Mux input channel 3 of TIM module 5**
	GTM_TIM2_IN3_7			**Mux input channel 3 of TIM module 2**
	GTM_TIM2_IN2_7			**Mux input channel 2 of TIM module 2**
	QSPI3_MRSTC			**Master SPI data input**
	ASCLIN9_ARXA			**Receive input**
	EVADC_G9CH12	AI		**Analog input channel 12, group 9**
	P01.5	O0		**General-purpose output**
	GTM_TOUT113	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_MRST	O4		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
H4	P01.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_2			**Mux input channel 6 of TIM module 5**
	GTM_TIM5_IN5_3			**Mux input channel 5 of TIM module 5**
	GTM_TIM2_IN5_7			**Mux input channel 5 of TIM module 2**
	QSPI3_MTSRC			**Slave SPI data input**
	P01.6	O0		**General-purpose output**
	GTM_TOUT114	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASCLK	O3		**Shift clock output**
	QSPI3_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-2 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P01.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_2			**Mux input channel 7 of TIM module 5**
	GTM_TIM2_IN7_7			**Mux input channel 7 of TIM module 2**
	QSPI3_SCLKC			**Slave SPI clock inputs**
	ASCLIN9_ARXB			**Receive input**
	P01.7	O0		**General-purpose output**
	GTM_TOUT115	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ATX	O3		**Transmit output**
	QSPI3_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D0			**sensor pixel data input**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D1			**sensor pixel data input**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	CIF_D2			**sensor pixel data input**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	CIF_D3			**sensor pixel data input**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	CIF_D4			**sensor pixel data input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	CIF_D5			**sensor pixel data input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	CIF_D6			**sensor pixel data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	CIF_D7			**sensor pixel data input**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CIF_D8			**sensor pixel data input**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P02.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_2			**Mux input channel 2 of TIM module 4**
	GTM_TIM3_IN3_10			**Mux input channel 3 of TIM module 3**
	GTM_TIM0_IN2_10			**Mux input channel 2 of TIM module 0**
	ASCLIN8_ARXA			**Receive input**
	P02.9	O0		**General-purpose output**
	GTM_TOUT116	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	ASCLIN8_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
F5	P02.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_2			**Mux input channel 3 of TIM module 4**
	GTM_TIM3_IN4_11			**Mux input channel 4 of TIM module 3**
	GTM_TIM0_IN3_10			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXC			**Receive input**
	CAN01_RXDE			**CAN receive input node 1**
	ASCLIN8_ARXB			**Receive input**
	P02.10	O0		**General-purpose output**
	GTM_TOUT117	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-3 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P02.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_3			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN5_12			**Mux input channel 5 of TIM module 3**
	GTM_TIM0_IN7_7			**Mux input channel 7 of TIM module 0**
	EVADC_G9CH15	AI		**Analog input channel 15, group 9**
	P02.11	O0		**General-purpose output**
	GTM_TOUT118	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN8_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-4 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_12			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN4_2			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_2			**Mux input channel 4 of TIM module 0**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	ASCLIN11_ARXA			**Receive input**
	GETH_RXERC			**Receive Error MII**
	P10.0	O0		**General-purpose output**
	GTM_TOUT102	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
A5	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
B6	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_3			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**
A4	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

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Table 2-4 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_13			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	CAN20_RXDB			**CAN receive input node 0**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-5 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_4			**Mux input channel 0 of TIM module 4**
	GTM_TIM2_IN0_7			**Mux input channel 0 of TIM module 2**
	ASCLIN3_ARXB			**Receive input**
	GTM_DTMA2_1			**CDTM2_DTM4**
	P11.0	O0		**General-purpose output**
	GTM_TOUT119	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_5			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN1_6			**Mux input channel 1 of TIM module 2**
	P11.1	O0		**General-purpose output**
	GTM_TOUT120	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN2_5			**Mux input channel 2 of TIM module 4**
	GTM_TIM2_IN2_6			**Mux input channel 2 of TIM module 2**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	GTM_TOUT121	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D8	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN3_5			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN3_8			**Mux input channel 3 of TIM module 2**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	GTM_TOUT122	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E8	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN4_5			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN4_7			**Mux input channel 4 of TIM module 2**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	GTM_TOUT123	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E7	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN5_5			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
B8	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN6_5			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN6_7			**Mux input channel 6 of TIM module 2**
	GETH_RXERA			**Receive Error MII**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	GTM_TOUT125	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_4			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_8			**Mux input channel 7 of TIM module 2**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	CAN20_RXDF			**CAN receive input node 0**
	P11.14	O0		**General-purpose output**
	GTM_TOUT126	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-5 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_5			**Mux input channel 7 of TIM module 4**
	GTM_TIM0_IN7_8			**Mux input channel 7 of TIM module 0**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	GTM_TOUT127	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-6 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_5			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN0_7			**Mux input channel 0 of TIM module 3**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	GTM_DTMA4_0			**CDTM4_DTM4**
	P12.0	O0		**General-purpose output**
	GTM_TOUT128	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**

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Table 2-6 Port 12 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_6			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN1_6			**Mux input channel 1 of TIM module 3**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	GTM_TOUT129	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-7 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**

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Table 2-7 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-8 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
E13	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
B15	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
B13	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D13	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_10			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A13	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_3			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-8 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_3			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_3			**Mux input channel 3 of TIM module 2**
	ASCLIN0_ACTSA			**Clear to send input**
	QSPI2_MRSTFN			**Master SPI data input (LVDS N line)**
	ASCLIN9_ARXD			**Receive input**
	P14.9	O0		**General-purpose output**
	GTM_TOUT89	O1		**GTM muxed output**
	CAN23_TXD	O2		**CAN transmit output node 3**
	MSC0_EN1	O3		**Chip Select**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	—	O7		**Reserved**
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_3			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_3			**Mux input channel 4 of TIM module 2**
	CAN23_RXDA			**CAN receive input node 3**
	QSPI2_MRSTFP			**Master SPI data input (LVDS P line)**
	P14.10	O0		**General-purpose output**
	GTM_TOUT90	O1		**GTM muxed output**
	—	O2		**Reserved**
	MSC0_EN0	O3		**Chip Select**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	—	O7		**Reserved**

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Table 2-9 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	SDMMC0_DAT7_IN			**read data in**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
	SDMMC0_DAT7	O		**write data out**
A18	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	SDMMC0_CLK	O7		**card clock**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
B17	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	SDMMC0_CMD_IN			**command in**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_CMD	O		**command out**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
A16	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-9 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
D14	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-10 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G19	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_11			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN3_5			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
G20	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
F17	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	SDMMC0_DAT0_IN			**read data in**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
	SDMMC0_DAT0	O		**write data out**
F20	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	SDMMC0_DAT1_IN			**read data in**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
	SDMMC0_DAT1	O		**write data out**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
E19	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	SDMMC0_DAT2_IN			**read data in**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
	SDMMC0_DAT2	O		**write data out**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	SDMMC0_DAT3_IN			**read data in**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
	SDMMC0_DAT3	O		**write data out**
D19	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	SDMMC0_DAT4_IN			**read data in**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SDMMC0_DAT4	O		**write data out**

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Table 2-10 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	SDMMC0_DAT5_IN			**read data in**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SDMMC0_DAT5	O		**write data out**
C20	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	SDMMC0_DAT6_IN			**read data in**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_DAT6	O		**write data out**

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Table 2-11 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_11			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN4_6			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	QSPI4_MRSTDN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXC			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_13			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_6			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	QSPI4_MRSTDP			**Master SPI data input (LVDS P line)**
	ASCLIN11_ARXD			**Receive input**
	GTM_DTMA4_1			**CDTM4_DTM4**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**

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Table 2-11 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input** DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

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Table 2-12 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	GETH1_CRSDVB			Carrier Sense / Data Valid combi-signal for RMII
	GETH1_RXDVB			Receive Data Valid MII
	GETH1_CRSA			Carrier Sense MII
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
P19	P22.1	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	QSPI4_MRSTB			Master SPI data input
	ASCLIN7_ARXE			Receive input
	GETH1_RXERA			Receive Error MII
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI4_SCLKP	O4		Master SPI clock output (LVDS P line)
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	GETH1_COLA			**Collision MII**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P16	P22.4	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN0_8			**Mux input channel 0 of TIM module 3**
	ASCLIN7_ARXF			**Receive input**
	GETH1_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	GTM_DTMA3_0			**CDTM3_DTM4**
	P22.4	O0		**General-purpose output**
	GTM_TOUT130	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	CAN13_TXD	O6		**CAN transmit output node 3**
	—	O7		**Reserved**
P17	P22.5	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN1_7			**Mux input channel 1 of TIM module 3**
	QSPI0_MTSRC			**Slave SPI data input**
	CAN13_RXDC			**CAN receive input node 3**
	GETH1_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH1_TXCLKB			**Transmit Clock Input for MII**
	GETH1_RXCLKA			**Receive Clock MII**
	P22.5	O0		**General-purpose output**
	GTM_TOUT131	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N16	P22.6	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN2_6			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_14			**Mux input channel 6 of TIM module 2**
	QSPI0_MRSTC			**Master SPI data input**
	ASCLIN4_ARXC			**Receive input**
	GETH1_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH1_RXDVA			**Receive Data Valid MII**
	GETH1_CRSB			**Carrier Sense MII**
	GETH1_RCTLA			**Receive Control for RGMII**
	P22.6	O0		**General-purpose output**
	GTM_TOUT132	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	CAN21_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
N17	P22.7	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN3_7			**Mux input channel 3 of TIM module 3**
	QSPI0_SCLKC			**Slave SPI clock inputs**
	CAN21_RXDF			**CAN receive input node 1**
	GETH1_TXCLKA			**Transmit Clock Input for MII**
	GETH1_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P22.7	O0		**General-purpose output**
	GTM_TOUT133	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN0_4			**Mux input channel 0 of TIM module 5**
	GTM_TIM3_IN4_7			**Mux input channel 4 of TIM module 3**
	QSPI0_SCLKB			**Slave SPI clock inputs**
	GETH1_RXCLKC			**Receive Clock MII**
	P22.8	O0		**General-purpose output**
	GTM_TOUT134	O1		**GTM muxed output**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	GETH1_MDC	O6		**MDIO clock**
	—	O7		**Reserved**
M17	P22.9	I	SLOW / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN1_10			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN5_7			**Mux input channel 5 of TIM module 3**
	QSPI0_MRSTB			**Master SPI data input**
	ASCLIN4_ARXD			**Receive input**
	CAN22_RXDE			**CAN receive input node 2**
	GETH1_MDIOC			**MDIO Input**
	GTM_DTMA3_1			**CDTM3_DTM4**
	P22.9	O0		**General-purpose output**
	GTM_TOUT135	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH1_MDIO	O		**MDIO Output**

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Table 2-12 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.10	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN2_8			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN6_7			**Mux input channel 6 of TIM module 3**
	QSPI0_MTSRB			**Slave SPI data input**
	P22.10	O0		**General-purpose output**
	GTM_TOUT136	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	CAN23_TXD	O5		**CAN transmit output node 3**
	GETH1_TXD0	O6		**Transmit Data**
	—	O7		**Reserved**
L17	P22.11	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN3_10			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN7_7			**Mux input channel 7 of TIM module 3**
	CAN23_RXDE			**CAN receive input node 3**
	P22.11	O0		**General-purpose output**
	GTM_TOUT137	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	GETH1_TXEN	O6		**Transmit Enable MII and RMII**
	GETH1_TCTL			**Transmit Control for RGMII**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
V20	P23.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_4			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_4			**Mux input channel 5 of TIM module 0**
	CAN10_RXDC			**CAN receive input node 0**
	P23.0	O0		**General-purpose output**
	GTM_TOUT41	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
U19	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**
U20	P23.2	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN6_5			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_5			**Mux input channel 6 of TIM module 0**
	ASCLIN7_ARXC			**Receive input**
	P23.2	O0		**General-purpose output**
	GTM_TOUT43	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN23_TXD	O4		**CAN transmit output node 3**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH1_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T19	P23.3	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	MSC1_INJ0			**Injection signal from port**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	CAN23_RXDB			**CAN receive input node 3**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
T20	P23.4	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	QSPI4_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN0	O5		**Chip Select**
	GETH1_TXD1	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T17	P23.5	I	FAST / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	GETH1_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	QSPI4_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN1	O5		**Chip Select**
	CAN22_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**
R17	P23.6	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM4_IN2_7			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_10			**Mux input channel 2 of TIM module 1**
	CAN22_RXDC			**CAN receive input node 2**
	GETH1_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	P23.6	O0		**General-purpose output**
	GTM_TOUT138	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_SLSO11	O4		**Master slave select output**
	CAN11_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-13 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R16	P23.7	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM4_IN3_7			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_10			**Mux input channel 3 of TIM module 1**
	CAN11_RXDC			**CAN receive input node 1**
	GETH1_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P23.7	O0		**General-purpose output**
	GTM_TOUT139	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-14 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-14 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	CAN21_RXDD			**CAN receive input node 1**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

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Table 2-14 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
W18	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

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Table 2-14 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T15	P32.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_9			**Mux input channel 5 of TIM module 5**
	GTM_TIM4_IN1_14			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_8			**Mux input channel 5 of TIM module 3**
	SENT_SENT10C			**Receive input channel 10**
	P32.5	O0		**General-purpose output**
	GTM_TOUT140	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
U15	P32.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_9			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN4_15			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN6_8			**Mux input channel 6 of TIM module 3**
	CAN02_RXDC			**CAN receive input node 2**
	CBS_TGI4			**Trigger input**
	ASCLIN2_ARXF			**Receive input**
	ASCLIN6_ARXC			**Receive input**
	SENT_SENT11C			**Receive input channel 11**
	P32.6	O0		**General-purpose output**
	GTM_TOUT141	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO12	O4		**Master slave select output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO4	O		**Trigger output**

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Table 2-14 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U16	P32.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_8			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN0_15			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN7_8			**Mux input channel 7 of TIM module 3**
	CBS_TGI5			**Trigger input**
	CAN22_RXDB			**CAN receive input node 2**
	SENT_SENT12C			**Receive input channel 12**
	P32.7	O0		**General-purpose output**
	GTM_TOUT142	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO5	O		**Trigger output**

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Table 2-15 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_13			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN4_6			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_6			**Mux input channel 4 of TIM module 0**
	EDSADC_ITR0E			**Trigger/Gate input, channel 0**
	SENT_SENT13C			**Receive input channel 13**
	IOM_PIN_0			**GPIO pad input to FPC**
	GTM_DTMT1_2			**CDTM1_DTM0**
	EVADC_G10CH7	AI		**Analog input channel 7, group 10**
	P33.0	O0		**General-purpose output**
	GTM_TOUT22	O1		**GTM muxed output**
	IOM_MON0_0			**Monitor input 0**
	IOM_GTM_0			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	—	O7		**Reserved**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_15			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN5_6			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_6			**Mux input channel 5 of TIM module 0**
	EDSADC_ITR1E			**Trigger/Gate input, channel 1**
	PSI5_RX0C			**RXD inputs (receive data) channel 0**
	EDSADC_DSCIN2B			**Modulator clock input, channel 2**
	SENT_SENT9C			**Receive input channel 9**
	ASCLIN8_ARXC			**Receive input**
	IOM_PIN_1			**GPIO pad input to FPC**
	EVADC_G10CH6	AI		**Analog input channel 6, group 10**
	P33.1	O0		**General-purpose output**
	GTM_TOUT23	O1		**GTM muxed output**
	IOM_MON0_1			**Monitor input 0**
	IOM_GTM_1			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN2_14			**Mux input channel 2 of TIM module 3**
	GTM_TIM1_IN6_6			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_6			**Mux input channel 6 of TIM module 0**
	EDSADC_ITR2E			**Trigger/Gate input, channel 2**
	SENT_SENT8C			**Receive input channel 8**
	EDSADC_DSDIN2B			**Digital datastream input, channel 2**
	IOM_PIN_2			**GPIO pad input to FPC**
	EVADC_G10CH5	AI		**Analog input channel 5, group 10**
	P33.2	O0		**General-purpose output**
	GTM_TOUT24	O1		**GTM muxed output**
	IOM_MON0_2			**Monitor input 0**
	IOM_GTM_2			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN3_12			**Mux input channel 3 of TIM module 3**
	GTM_TIM1_IN7_6			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_6			**Mux input channel 7 of TIM module 0**
	PSI5_RX1C			**RXD inputs (receive data) channel 1**
	SENT_SENT7C			**Receive input channel 7**
	EDSADC_DSCIN1B			**Modulator clock input, channel 1**
	IOM_PIN_3			**GPIO pad input to FPC**
	EVADC_G10CH4	AI		**Analog input channel 4, group 10**
	P33.3	O0		**General-purpose output**
	GTM_TOUT25	O1		**GTM muxed output**
	IOM_MON0_3			**Monitor input 0**
	IOM_GTM_3			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO2	O3		**Master slave select output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM4_IN4_14			Mux input channel 4 of TIM module 4
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI4_SLSIA			Slave select input
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	QSPI4_SLSO0	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	PSI5S_CLK	O5		PSI5S CLK is a clock that can be used on a pin to drive the external PHY.
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1
	SMU_FSP1	O		FSP[1..0] Output Signals - Generated by SMU_core
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	QSPI4_SCLKA			Slave SPI clock inputs
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	QSPI4_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	EDSADC_CGPWMN	O6		Negative carrier generator output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
	IOM_REF1_12			Reference input 1

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-15 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN0_8			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN5_14			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_8			**Mux input channel 0 of TIM module 2**
	QSPI2_SCLKD			**Slave SPI clock inputs**
	CBS_TGI6			**Trigger input**
	P33.14	O0		**General-purpose output**
	GTM_TOUT143	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
	CBS_TGO6	O		**Trigger output**
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN1_9			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN6_12			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_7			**Mux input channel 1 of TIM module 2**
	CBS_TGI7			**Trigger input**
	P33.15	O0		**General-purpose output**
	GTM_TOUT144	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
	CBS_TGO7	O		**Trigger output**

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Table 2-16 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN3_9			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN4_12			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN3_9			**Mux input channel 3 of TIM module 2**
	EVADC_G10CH11	AI		**Analog input channel 11, group 10**
	P34.1	O0		**General-purpose output**
	GTM_TOUT146	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN4_9			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN5_13			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN4_8			**Mux input channel 4 of TIM module 2**
	ASCLIN4_ARXB			**Receive input**
	CAN00_RXDG			**CAN receive input node 0**
	CAN20_RXDC			**CAN receive input node 0**
	EVADC_G10CH10	AI		**Analog input channel 10, group 10**
	P34.2	O0		**General-purpose output**
	GTM_TOUT147	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-16 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN5_10			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN6_13			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN5_9			**Mux input channel 5 of TIM module 2**
	EVADC_G10CH9	AI		**Analog input channel 9, group 10**
	P34.3	O0		**General-purpose output**
	GTM_TOUT148	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN6_10			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN7_12			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN6_8			**Mux input channel 6 of TIM module 2**
	QSPI2_MRSTD			**Master SPI data input**
	EVADC_G10CH8	AI		**Analog input channel 8, group 10**
	P34.4	O0		**General-purpose output**
	GTM_TOUT149	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI2_MRST	O4		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-16 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN7_9			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN7_12			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_9			**Mux input channel 7 of TIM module 2**
	QSPI2_MTSRD			**Slave SPI data input**
	ASCLIN8_ARXE			**Receive input**
	P34.5	O0		**General-purpose output**
	GTM_TOUT150	O1		**GTM muxed output**
	ASCLIN8_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI2_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-17 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
U10	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
W9	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
U9	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
T9	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
Y9	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**

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Table 2-17 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T8	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
U8	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
W8	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
U7	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G11CH5			**Analog input channel 5, group 11**
	EVADC_G1CH1			**Analog input channel 1, group 1**
Y8	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
W7	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
T7	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
W6	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
U6	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**
T6	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
W5	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
U5	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-17 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W4	AN18/P40.11	I	S / HighZ / VDDM	**Analog Input 18**
	SENT_SENT11A			**Receive input channel 11**
	EVADC_G11CH8			**Analog input channel 8, group 11**
	EVADC_G2CH2			**Analog input channel 2, group 2**
W3	AN19/P40.12	I	S / HighZ / VDDM	**Analog Input 19**
	SENT_SENT12A			**Receive input channel 12**
	EVADC_G11CH9			**Analog input channel 9, group 11**
	EVADC_G2CH3			**Analog input channel 3, group 2**
Y3	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
Y2	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
T5	AN22	I	D / HighZ / VDDM	**Analog Input 22**
	EVADC_G2CH6			**Analog input channel 6, group 2**
R5	AN23	I	D / HighZ / VDDM	**Analog Input 23**
	EVADC_G2CH7			**Analog input channel 7, group 2**
W2	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
W1	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
V2	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
	EVADC_G11CH10			**Analog input channel 10, group 11**
V1	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
	EVADC_G11CH11			**Analog input channel 11, group 11**

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Table 2-17 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN28/P40.13	I	S / HighZ / VDDM	**Analog Input 28**
	SENT_SENT13A			**Receive input channel 13**
	EVADC_G3CH4			**Analog input channel 4, group 3**
U1	AN29/P40.14	I	S / HighZ / VDDM	**Analog Input 29**
	SENT_SENT14A			**Receive input channel 14**
	EVADC_G3CH5			**Analog input channel 5, group 3**
T4	AN30	I	D / HighZ / VDDM	**Analog Input 30**
	EVADC_G3CH6			**Analog input channel 6, group 3**
R4	AN31	I	D / HighZ / VDDM	**Analog Input 31**
	EVADC_G3CH7			**Analog input channel 7, group 3**
P4	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
	EVADC_G11CH12			**Analog input channel 12, group 11**
R1	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
	EVADC_G11CH13			**Analog input channel 13, group 11**
P5	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
	EVADC_G11CH14			**Analog input channel 14, group 11**
R2	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
N4	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
P2	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**

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Table 2-17 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N5	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
P1	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
M5	AN40	I	D / HighZ / VDDM	**Analog Input 40**
	EVADC_G8CH8			**Analog input channel 8, group 8**
M4	AN41	I	D / HighZ / VDDM	**Analog Input 41**
	EVADC_G8CH9			**Analog input channel 9, group 8**
L5	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
L4	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
N1	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
N2	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
M1	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
M2	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

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Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

1. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
2. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-18 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AGBTCLKN (VSS)	I	AGBT_CLK / VEXT	**Input PAD (negative pole) for the external 100 MHz differential clock.** AGBT Input; (TC3xx devices without AGBT: VSS)
K7	AGBTCLKP (VSS)	I	AGBT_CLK / VEXT	**Input PAD (positive pole) for the external 100 MHz differential clock.** AGBT Input; (TC3xx devices without AGBT: VSS)
P10	AGBTTXN (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole** AGBT Output; (TC3xx devices without AGBT: VSS)
P11	AGBTTXP (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole** AGBT Output; (TC3xx devices without AGBT: VSS)
L14	AGBTERR (VSS)	I	FAST / PD / VEXT	**Input PAD for CRC error from FPGA.** AGBT Input; (TC3xx devices without AGBT: VSS)
Y17	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
W17	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
G10	DAPE2	I/O	FAST / PD2 / VEXT	**DAPE: DAPE2 Data I/O** DAPE: DAPE2 Data I/O (TC3xx devices without DAPE: VSS)
G11	DAPE1	I/O	FAST / PD2 / VEXT	**DAPE: DAPE1 Data I/O** DAPE: DAPE1 Data I/O (TC3xx devices without DAPE: VSS)
K16	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input** TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		**DAP: DAP1 Data I/O**

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Table 2-18 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K14	DAPE0	I	FAST / PD2 / VEXT	**DAPE: DAPE0 Clock Input** DAPE: DAPE0 clock input (TC3xx devices without DAPE: NC)
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input** TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
	DAPE0	I		**DAPE: DAPE0 Clock Input**
J16	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input** TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		**DAP: DAP0 Clock Input**
G16	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
F16	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

Table 2-19 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13	VDD	I	—	**Digital Core Power Supply (1.25V)**
A2, B3, V19, W20	VEXT	I	—	**External Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**

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Table 2-19 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y5	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
B18, A19	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	**Digital Ground**
Y4	VSSM	I	—	**Analog Ground for VDDM**
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G12	VSS	I	—	**Digital Ground**
L20	VSS	I	—	**Oscillator Ground, VSS(OSC)**
Y6	VAREF1	I	—	**Positive Analog Reference Voltage 1**
Y7	VAGND1	I	—	**Negative Analog Reference Voltage 1**
T1	VAREF2	I	—	**Positive Analog Reference Voltage 2**
T2	VAGND2	I	—	**Negative Analog Reference Voltage 2**
A1, Y1, U4	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
G8, H7	VDDSB (VDD)	I	—	**Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)**
T11	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
N19	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
N20	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

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2.2 LFBGA-292 Package Pinning of TC37xEXT TX

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC1	VEXT	P10.7	P10.6	P10.2	P10.3	P10.0	P11.11	P11.9	P11.2	P13.3	P13.1	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A
B	P02.0	VSS	VEXT	P10.8	P10.5	P10.4	P10.1	P11.12	P11.10	P11.3	P13.2	P13.0	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B
C	P02.2	P02.1																	P15.2	P20.14	C
D	P02.4	P02.3		VSS	VFLEX	P11.15	P11.14	P11.5	P11.6	P11.4	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS		P20.12	P20.13	D
E	P02.6	P02.5		P02.9	VSS	P11.13	P11.8	P11.7	P11.1	P11.0	P12.1	P12.0	P14.2	P15.5	VDD	VSS	P20.9		P20.10	P20.11	E
F	P02.8	P02.7		P02.11	P02.10											$\overline{\text{ESR0}}$	P20.6		P20.7	P20.8	F
G	P00.0	P00.1		P01.4	P01.3			VDDSB (VDD)	VSS	DAPE2	DAPE1	VSS	VDD			$\overline{\text{ESR1}}$	$\overline{\text{PORST}}$		P20.1	P20.3	G
H	P00.2	P00.3		P01.6	P01.5		VDDSB (VDD)		VSS	VSS	VSS	VSS		VDD		P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H
J	P00.4	P00.5		P00.6	P01.7		VSS	VSS		VSS	VSS		VSS	VSS		TCK	P21.1		P21.3	P21.5	J
K	P00.7	P00.9		P00.8	P00.10		AGBTC LKP (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	DAPE0		TMS	P21.0		P21.2	P21.4	K
L	P00.11	P00.12		AN43	AN42		AGBTC LKN (VSS)	VSS	VSS	VSS	VSS	VSS	VSS	AGBTE RR (VSS)		P22.0	P22.1		$\overline{\text{TRST}}$	VSS	L
M	AN46	AN47		AN41	AN40		VSS	VSS		VSS	VSS		VSS	VSS		P22.8	P22.9		XTAL2	XTAL1	M
N	AN44	AN45		AN36 / P40.6	AN38 / P40.8		VDD		VSS	VSS	VSS	VSS		VDD		P22.6	P22.7		VDD	VEXT	N
P	AN39 / P40.9	AN37 / P40.7		AN32 / P40.4	AN34			VDD	VSS	AGBTT XN (VSS)	AGBTT XP (VSS)	VSS	VDD			P22.4	P22.5		P22.11	P22.10	P
R	AN33 / P40.5	AN35		AN31	AN23											P23.7	P23.6		P22.3	P22.2	R
T	VAREF 2	VAGND 2		AN30	AN22	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	P34.4	P33.14	P32.5	VSS	P23.5		P22.12	P23.4	T
U	AN29 / P40.14	AN28 / P40.13		NC1	AN17 / P40.10	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	P34.5	P33.15	P32.6	P32.7	VSS		P23.1	P23.3	U
V	AN27 / P40.3	AN26 / P40.2																	VFLEX 2	P23.2	V
W	AN25 / P40.1	AN24 / P40.0	AN19 / P40.12	AN18 / P40.11	AN16	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	P32.1 / VGATE 1P	P32.4	VSS	VEXT	W
Y	NC1	AN21	AN20	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	P33.13	P32.0 / VGATE 1N	P32.2	P32.3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

TC37xed_geth - (top view)

Figure 2-2 TC37xEXT TX package variant LFBGA-292

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Table 2-20 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	CIF_D9			**sensor pixel data input**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CIF_D10			**sensor pixel data input**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	CIF_D11			**sensor pixel data input**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CIF_D12			**sensor pixel data input**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	CIF_D13			**sensor pixel data input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CIF_D14			**sensor pixel data input**
	CAN11_RXDB			**CAN receive input node 1**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	CIF_D15			**sensor pixel data input**
	ASCLIN5_ARXA			**Receive input**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	CIF_PCLK			**Sensor Pixel Clock input**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CIF_VSYNC			**vertical synchronization signal input**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CIF_HSYNC			**horizontal synchronization signal input**
	CCU60_T12HRC			**External timer start 12**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN1_11			**Mux input channel 1 of TIM module 4**
	GTM_TIM1_IN1_1			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_1			**Mux input channel 1 of TIM module 0**
	SENT_SENT9B			**Receive input channel 9**
	EDSADC_DSDIN1A			**Digital datastream input, channel 1**
	EVADC_G9CH2	AI		**Analog input channel 2, group 9**
	EDSADC_EDS4PB			**Positive analog input channel 4, pin B**
	P00.10	O0		**General-purpose output**
	GTM_TOUT19	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC9	O6		**Transmit output**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN2_11			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	SENT_SENT10B			**Receive input channel 10**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	EVADC_FC3CH0			**Analog input FC channel 3**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-20 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

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Table 2-21 Port 01 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G5	P01.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_2			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_14			**Mux input channel 0 of TIM module 2**
	GTM_TIM0_IN5_8			**Mux input channel 5 of TIM module 0**
	QSPI3_SLSIB			**Slave select input**
	EVADC_G9CH14	AI		**Analog input channel 14, group 9**
	P01.3	O0		**General-purpose output**
	GTM_TOUT111	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_SLSO9	O4		**Master slave select output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
G4	P01.4	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_2			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_14			**Mux input channel 1 of TIM module 2**
	GTM_TIM0_IN6_8			**Mux input channel 6 of TIM module 0**
	CAN01_RXDC			**CAN receive input node 1**
	EVADC_G9CH13	AI		**Analog input channel 13, group 9**
	P01.4	O0		**General-purpose output**
	GTM_TOUT112	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASLSO	O3		**Slave select signal output**
	QSPI3_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-21 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H5	P01.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN3_2			**Mux input channel 3 of TIM module 5**
	GTM_TIM2_IN3_7			**Mux input channel 3 of TIM module 2**
	GTM_TIM2_IN2_7			**Mux input channel 2 of TIM module 2**
	QSPI3_MRSTC			**Master SPI data input**
	ASCLIN9_ARXA			**Receive input**
	EVADC_G9CH12	AI		**Analog input channel 12, group 9**
	P01.5	O0		**General-purpose output**
	GTM_TOUT113	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI3_MRST	O4		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
H4	P01.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_2			**Mux input channel 6 of TIM module 5**
	GTM_TIM5_IN5_3			**Mux input channel 5 of TIM module 5**
	GTM_TIM2_IN5_7			**Mux input channel 5 of TIM module 2**
	QSPI3_MTSRC			**Slave SPI data input**
	P01.6	O0		**General-purpose output**
	GTM_TOUT114	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ASCLK	O3		**Shift clock output**
	QSPI3_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-21 Port 01 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J5	P01.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_2			**Mux input channel 7 of TIM module 5**
	GTM_TIM2_IN7_7			**Mux input channel 7 of TIM module 2**
	QSPI3_SCLKC			**Slave SPI clock inputs**
	ASCLIN9_ARXB			**Receive input**
	P01.7	O0		**General-purpose output**
	GTM_TOUT115	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN9_ATX	O3		**Transmit output**
	QSPI3_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-22 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D0			**sensor pixel data input**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D1			**sensor pixel data input**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	CIF_D2			**sensor pixel data input**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D2	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	CIF_D3			**sensor pixel data input**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D1	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	CIF_D4			**sensor pixel data input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	CIF_D5			**sensor pixel data input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	CIF_D6			**sensor pixel data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	CIF_D7			**sensor pixel data input**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F1	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CIF_D8			**sensor pixel data input**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E4	P02.9	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_2			**Mux input channel 2 of TIM module 4**
	GTM_TIM3_IN3_10			**Mux input channel 3 of TIM module 3**
	GTM_TIM0_IN2_10			**Mux input channel 2 of TIM module 0**
	ASCLIN8_ARXA			**Receive input**
	P02.9	O0		**General-purpose output**
	GTM_TOUT116	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	ASCLIN8_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
F5	P02.10	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_2			**Mux input channel 3 of TIM module 4**
	GTM_TIM3_IN4_11			**Mux input channel 4 of TIM module 3**
	GTM_TIM0_IN3_10			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXC			**Receive input**
	CAN01_RXDE			**CAN receive input node 1**
	ASCLIN8_ARXB			**Receive input**
	P02.10	O0		**General-purpose output**
	GTM_TOUT117	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-22 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P02.11	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_3			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN5_12			**Mux input channel 5 of TIM module 3**
	GTM_TIM0_IN7_7			**Mux input channel 7 of TIM module 0**
	EVADC_G9CH15	AI		**Analog input channel 15, group 9**
	P02.11	O0		**General-purpose output**
	GTM_TOUT118	O1		**GTM muxed output**
	—	O2		**Reserved**
	ASCLIN8_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-23 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_12			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN4_2			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_2			**Mux input channel 4 of TIM module 0**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	ASCLIN11_ARXA			**Receive input**
	GETH_RXERC			**Receive Error MII**
	P10.0	O0		**General-purpose output**
	GTM_TOUT102	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-23 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
A5	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-23 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
B6	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_3			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-23 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**
A4	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

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Table 2-23 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A3	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

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Table 2-23 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_13			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	CAN20_RXDB			**CAN receive input node 0**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-24 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E10	P11.0	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_4			**Mux input channel 0 of TIM module 4**
	GTM_TIM2_IN0_7			**Mux input channel 0 of TIM module 2**
	ASCLIN3_ARXB			**Receive input**
	GTM_DTMA2_1			**CDTM2_DTM4**
	P11.0	O0		**General-purpose output**
	GTM_TOUT119	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN11_TXD	O5		**CAN transmit output node 1**
	GETH_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E9	P11.1	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_5			**Mux input channel 1 of TIM module 4**
	GTM_TIM2_IN1_6			**Mux input channel 1 of TIM module 2**
	P11.1	O0		**General-purpose output**
	GTM_TOUT120	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
A10	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
D10	P11.4	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN2_5			**Mux input channel 2 of TIM module 4**
	GTM_TIM2_IN2_6			**Mux input channel 2 of TIM module 2**
	GETH_RXCLKB			**Receive Clock MII**
	P11.4	O0		**General-purpose output**
	GTM_TOUT121	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN13_TXD	O5		**CAN transmit output node 3**
	GETH_TXER	O6		**Transmit Error MII**
	GETH_TXCLK	O7		**Transmit Clock Output for RGMII**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D8	P11.5	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN3_5			**Mux input channel 3 of TIM module 4**
	GTM_TIM2_IN3_8			**Mux input channel 3 of TIM module 2**
	GETH_TXCLKA			**Transmit Clock Input for MII**
	GETH_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P11.5	O0		**General-purpose output**
	GTM_TOUT122	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	—	O7		**Reserved**
D9	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E8	P11.7	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN4_5			**Mux input channel 4 of TIM module 4**
	GTM_TIM2_IN4_7			**Mux input channel 4 of TIM module 2**
	GETH_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	CAN11_RXDD			**CAN receive input node 1**
	P11.7	O0		**General-purpose output**
	GTM_TOUT123	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
E7	P11.8	I	SLOW / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN5_5			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN5_8			**Mux input channel 5 of TIM module 2**
	GETH_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	CAN12_RXDD			**CAN receive input node 2**
	P11.8	O0		**General-purpose output**
	GTM_TOUT124	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
B8	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E6	P11.13	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN6_5			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN6_7			**Mux input channel 6 of TIM module 2**
	GETH_RXERA			**Receive Error MII**
	CAN13_RXDD			**CAN receive input node 3**
	P11.13	O0		**General-purpose output**
	GTM_TOUT125	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
D7	P11.14	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_4			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_8			**Mux input channel 7 of TIM module 2**
	GETH_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVB			**Receive Data Valid MII**
	GETH_CRSA			**Carrier Sense MII**
	CAN20_RXDF			**CAN receive input node 0**
	P11.14	O0		**General-purpose output**
	GTM_TOUT126	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-24 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.15	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN7_5			**Mux input channel 7 of TIM module 4**
	GTM_TIM0_IN7_8			**Mux input channel 7 of TIM module 0**
	GETH_COLA			**Collision MII**
	P11.15	O0		**General-purpose output**
	GTM_TOUT127	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-25 Port 12 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P12.0	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN0_5			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN0_7			**Mux input channel 0 of TIM module 3**
	CAN00_RXDC			**CAN receive input node 0**
	GETH_RXCLKC			**Receive Clock MII**
	GTM_DTMA4_0			**CDTM4_DTM4**
	P12.0	O0		**General-purpose output**
	GTM_TOUT128	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_MDC	O6		**MDIO clock**
	—	O7		**Reserved**

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Table 2-25 Port 12 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E11	P12.1	I	SLOW / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM4_IN1_6			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN1_6			**Mux input channel 1 of TIM module 3**
	GETH_MDIOC			**MDIO Input**
	P12.1	O0		**General-purpose output**
	GTM_TOUT129	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

Table 2-26 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**

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Table 2-26 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A12	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**
B11	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**

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Table 2-26 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-27 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-27 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
E13	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-27 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
B15	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-27 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
B13	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

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Table 2-27 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D13	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_10			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
A13	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_3			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-27 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D12	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_3			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_3			**Mux input channel 3 of TIM module 2**
	ASCLIN0_ACTSA			**Clear to send input**
	QSPI2_MRSTFN			**Master SPI data input (LVDS N line)**
	ASCLIN9_ARXD			**Receive input**
	P14.9	O0		**General-purpose output**
	GTM_TOUT89	O1		**GTM muxed output**
	CAN23_TXD	O2		**CAN transmit output node 3**
	MSC0_EN1	O3		**Chip Select**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	—	O7		**Reserved**
D11	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_3			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_3			**Mux input channel 4 of TIM module 2**
	CAN23_RXDA			**CAN receive input node 3**
	QSPI2_MRSTFP			**Master SPI data input (LVDS P line)**
	P14.10	O0		**General-purpose output**
	GTM_TOUT90	O1		**GTM muxed output**
	—	O2		**Reserved**
	MSC0_EN0	O3		**Chip Select**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	—	O7		**Reserved**

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Table 2-28 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	SDMMC0_DAT7_IN			**read data in**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
	SDMMC0_DAT7	O		**write data out**
A18	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	SDMMC0_CLK	O7		**card clock**

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Table 2-28 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
B17	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	SDMMC0_CMD_IN			**command in**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_CMD	O		**command out**

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Table 2-28 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A17	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-28 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E14	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
A16	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-28 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D15	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
D14	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-29 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
G19	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_11			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN3_5			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**

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Table 2-29 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H19	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
G20	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
F17	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-29 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	SDMMC0_DAT0_IN			**read data in**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
	SDMMC0_DAT0	O		**write data out**
F20	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	SDMMC0_DAT1_IN			**read data in**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
	SDMMC0_DAT1	O		**write data out**

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Table 2-29 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E17	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
E19	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	SDMMC0_DAT2_IN			**read data in**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
	SDMMC0_DAT2	O		**write data out**

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Table 2-29 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	SDMMC0_DAT3_IN			**read data in**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
	SDMMC0_DAT3	O		**write data out**
D19	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	SDMMC0_DAT4_IN			**read data in**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SDMMC0_DAT4	O		**write data out**

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Table 2-29 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	SDMMC0_DAT5_IN			**read data in**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SDMMC0_DAT5	O		**write data out**
C20	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	SDMMC0_DAT6_IN			**read data in**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_DAT6	O		**write data out**

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Table 2-30 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_11			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN4_6			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	QSPI4_MRSTDN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXC			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
J17	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_13			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_6			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	QSPI4_MRSTDP			**Master SPI data input (LVDS P line)**
	ASCLIN11_ARXD			**Receive input**
	GTM_DTMA4_1			**CDTM4_DTM4**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

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Table 2-30 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K19	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
J19	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

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Table 2-30 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K20	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
J20	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

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Table 2-30 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**

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Table 2-30 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input** DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

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Table 2-31 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
L16	P22.0	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	QSPI4_MTSRB			Slave SPI data input
	ASCLIN6_ARXE			Receive input
	GETH1_CRSDVB			Carrier Sense / Data Valid combi-signal for RMII
	GETH1_RXDVB			Receive Data Valid MII
	GETH1_CRSA			Carrier Sense MII
	P22.0	O0		General-purpose output
	GTM_TOUT47	O1		GTM muxed output
	ASCLIN3_ATXN	O2		Differential Transmit output (low active)
	QSPI4_MTSR	O3		Master SPI data output
	QSPI4_SCLKN	O4		Master SPI clock output (LVDS N line)
	MSC1_FCLN	O5		Shift-clock inverted part of the differential signal
	—	O6		Reserved
	ASCLIN6_ATX	O7		Transmit output
L17	P22.1	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	General-purpose input
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0
	QSPI4_MRSTB			Master SPI data input
	ASCLIN7_ARXE			Receive input
	GETH1_RXERA			Receive Error MII
	P22.1	O0		General-purpose output
	GTM_TOUT48	O1		GTM muxed output
	ASCLIN3_ATXP	O2		Differential Transmit output (high active)
	QSPI4_MRST	O3		Slave SPI data output
	IOM_MON2_4			Monitor input 2
	IOM_REF2_4			Reference input 2
	QSPI4_SCLKP	O4		Master SPI clock output (LVDS P line)
	MSC1_FCLP	O5		Shift-clock direct part of the differential signal
	—	O6		Reserved
	ASCLIN7_ATX	O7		Transmit output

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Table 2-31 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R20	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	GETH1_COLA			**Collision MII**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
R19	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-31 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P16	P22.4	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN0_8			**Mux input channel 0 of TIM module 3**
	ASCLIN7_ARXF			**Receive input**
	GETH1_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	GTM_DTMA3_0			**CDTM3_DTM4**
	P22.4	O0		**General-purpose output**
	GTM_TOUT130	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO12	O4		**Master slave select output**
	—	O5		**Reserved**
	CAN13_TXD	O6		**CAN transmit output node 3**
	—	O7		**Reserved**
P17	P22.5	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN1_7			**Mux input channel 1 of TIM module 3**
	QSPI0_MTSRC			**Slave SPI data input**
	CAN13_RXDC			**CAN receive input node 3**
	GETH1_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH1_TXCLKB			**Transmit Clock Input for MII**
	GETH1_RXCLKA			**Receive Clock MII**
	P22.5	O0		**General-purpose output**
	GTM_TOUT131	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-31 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N16	P22.6	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN2_6			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_14			**Mux input channel 6 of TIM module 2**
	QSPI0_MRSTC			**Master SPI data input**
	ASCLIN4_ARXC			**Receive input**
	GETH1_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH1_RXDVA			**Receive Data Valid MII**
	GETH1_CRSB			**Carrier Sense MII**
	GETH1_RCTLA			**Receive Control for RGMII**
	P22.6	O0		**General-purpose output**
	GTM_TOUT132	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	CAN21_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
N17	P22.7	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM3_IN3_7			**Mux input channel 3 of TIM module 3**
	QSPI0_SCLKC			**Slave SPI clock inputs**
	CAN21_RXDF			**CAN receive input node 1**
	GETH1_TXCLKA			**Transmit Clock Input for MII**
	GETH1_GREFCLK			**Gigabit Reference Clock input for RGMII (125 MHz high precission)**
	P22.7	O0		**General-purpose output**
	GTM_TOUT133	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-31 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M16	P22.8	I	SLOW / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN0_4			**Mux input channel 0 of TIM module 5**
	GTM_TIM3_IN4_7			**Mux input channel 4 of TIM module 3**
	QSPI0_SCLKB			**Slave SPI clock inputs**
	GETH1_RXCLKC			**Receive Clock MII**
	P22.8	O0		**General-purpose output**
	GTM_TOUT134	O1		**GTM muxed output**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI0_SCLK	O4		**Master SPI clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	GETH1_MDC	O6		**MDIO clock**
	—	O7		**Reserved**
M17	P22.9	I	SLOW / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN1_10			**Mux input channel 1 of TIM module 5**
	GTM_TIM3_IN5_7			**Mux input channel 5 of TIM module 3**
	QSPI0_MRSTB			**Master SPI data input**
	ASCLIN4_ARXD			**Receive input**
	CAN22_RXDE			**CAN receive input node 2**
	GETH1_MDIOC			**MDIO Input**
	GTM_DTMA3_1			**CDTM3_DTM4**
	P22.9	O0		**General-purpose output**
	GTM_TOUT135	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_MRST	O4		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH1_MDIO	O		**MDIO Output**

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Table 2-31 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.10	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN2_8			**Mux input channel 2 of TIM module 5**
	GTM_TIM3_IN6_7			**Mux input channel 6 of TIM module 3**
	QSPI0_MTSRB			**Slave SPI data input**
	P22.10	O0		**General-purpose output**
	GTM_TOUT136	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI0_MTSR	O4		**Master SPI data output**
	CAN23_TXD	O5		**CAN transmit output node 3**
	GETH1_TXD0	O6		**Transmit Data**
	—	O7		**Reserved**
P19	P22.11	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM5_IN3_10			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN7_7			**Mux input channel 7 of TIM module 3**
	CAN23_RXDE			**CAN receive input node 3**
	P22.11	O0		**General-purpose output**
	GTM_TOUT137	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI0_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	GETH1_TXEN	O6		**Transmit Enable MII and RMII**
	GETH1_TCTL			**Transmit Control for RGMII**
	—	O7		**Reserved**
T19	P22.12	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GETH1_RXCLKB			**Receive Clock MII**
	P22.12	O0		**General-purpose output**
	—	O1		**Reserved**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_TXER	O6		**Transmit Error MII**
	GETH1_TXCLK	O7		**Transmit Clock Output for RGMII**

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Table 2-32 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U19	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**
V20	P23.2	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN6_5			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_5			**Mux input channel 6 of TIM module 0**
	ASCLIN7_ARXC			**Receive input**
	P23.2	O0		**General-purpose output**
	GTM_TOUT43	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN23_TXD	O4		**CAN transmit output node 3**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH1_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-32 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U20	P23.3	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	MSC1_INJ0			**Injection signal from port**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	CAN23_RXDB			**CAN receive input node 3**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
T20	P23.4	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	QSPI4_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN0	O5		**Chip Select**
	GETH1_TXD1	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-32 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T17	P23.5	I	FAST / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	GETH1_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	QSPI4_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN1	O5		**Chip Select**
	CAN22_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**
R17	P23.6	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM4_IN2_7			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_10			**Mux input channel 2 of TIM module 1**
	CAN22_RXDC			**CAN receive input node 2**
	GETH1_RXD2A			**Receive Data 2 MII and RGMII (RGMII can use RXD2A only)**
	P23.6	O0		**General-purpose output**
	GTM_TOUT138	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI0_SLSO11	O4		**Master slave select output**
	CAN11_TXD	O5		**CAN transmit output node 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-32 Port 23 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R16	P23.7	I	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM4_IN3_7			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_10			**Mux input channel 3 of TIM module 1**
	CAN11_RXDC			**CAN receive input node 1**
	GETH1_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P23.7	O0		**General-purpose output**
	GTM_TOUT139	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-33 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
Y17	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-33 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
Y18	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	CAN21_RXDD			**CAN receive input node 1**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

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Table 2-33 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y19	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
W18	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

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Table 2-33 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T15	P32.5	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_9			**Mux input channel 5 of TIM module 5**
	GTM_TIM4_IN1_14			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_8			**Mux input channel 5 of TIM module 3**
	SENT_SENT10C			**Receive input channel 10**
	P32.5	O0		**General-purpose output**
	GTM_TOUT140	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
U15	P32.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN6_9			**Mux input channel 6 of TIM module 5**
	GTM_TIM4_IN4_15			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN6_8			**Mux input channel 6 of TIM module 3**
	CAN02_RXDC			**CAN receive input node 2**
	CBS_TGI4			**Trigger input**
	ASCLIN2_ARXF			**Receive input**
	ASCLIN6_ARXC			**Receive input**
	SENT_SENT11C			**Receive input channel 11**
	P32.6	O0		**General-purpose output**
	GTM_TOUT141	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	QSPI2_SLSO12	O4		**Master slave select output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO4	O		**Trigger output**

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Table 2-33 Port 32 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U16	P32.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN7_8			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN0_15			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN7_8			**Mux input channel 7 of TIM module 3**
	CBS_TGI5			**Trigger input**
	CAN22_RXDB			**CAN receive input node 2**
	SENT_SENT12C			**Receive input channel 12**
	P32.7	O0		**General-purpose output**
	GTM_TOUT142	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO5	O		**Trigger output**

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Table 2-34 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_13			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN4_6			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_6			**Mux input channel 4 of TIM module 0**
	EDSADC_ITR0E			**Trigger/Gate input, channel 0**
	SENT_SENT13C			**Receive input channel 13**
	IOM_PIN_0			**GPIO pad input to FPC**
	GTM_DTMT1_2			**CDTM1_DTM0**
	EVADC_G10CH7	AI		**Analog input channel 7, group 10**
	P33.0	O0		**General-purpose output**
	GTM_TOUT22	O1		**GTM muxed output**
	IOM_MON0_0			**Monitor input 0**
	IOM_GTM_0			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	—	O7		**Reserved**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_15			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN5_6			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_6			**Mux input channel 5 of TIM module 0**
	EDSADC_ITR1E			**Trigger/Gate input, channel 1**
	PSI5_RX0C			**RXD inputs (receive data) channel 0**
	EDSADC_DSCIN2B			**Modulator clock input, channel 2**
	SENT_SENT9C			**Receive input channel 9**
	ASCLIN8_ARXC			**Receive input**
	IOM_PIN_1			**GPIO pad input to FPC**
	EVADC_G10CH6	AI		**Analog input channel 6, group 10**
	P33.1	O0		**General-purpose output**
	GTM_TOUT23	O1		**GTM muxed output**
	IOM_MON0_1			**Monitor input 0**
	IOM_GTM_1			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN2_14			**Mux input channel 2 of TIM module 3**
	GTM_TIM1_IN6_6			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_6			**Mux input channel 6 of TIM module 0**
	EDSADC_ITR2E			**Trigger/Gate input, channel 2**
	SENT_SENT8C			**Receive input channel 8**
	EDSADC_DSDIN2B			**Digital datastream input, channel 2**
	IOM_PIN_2			**GPIO pad input to FPC**
	EVADC_G10CH5	AI		**Analog input channel 5, group 10**
	P33.2	O0		**General-purpose output**
	GTM_TOUT24	O1		**GTM muxed output**
	IOM_MON0_2			**Monitor input 0**
	IOM_GTM_2			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN3_12			**Mux input channel 3 of TIM module 3**
	GTM_TIM1_IN7_6			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_6			**Mux input channel 7 of TIM module 0**
	PSI5_RX1C			**RXD inputs (receive data) channel 1**
	SENT_SENT7C			**Receive input channel 7**
	EDSADC_DSCIN1B			**Modulator clock input, channel 1**
	IOM_PIN_3			**GPIO pad input to FPC**
	EVADC_G10CH4	AI		**Analog input channel 4, group 10**
	P33.3	O0		**General-purpose output**
	GTM_TOUT25	O1		**GTM muxed output**
	IOM_MON0_3			**Monitor input 0**
	IOM_GTM_3			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO2	O3		**Master slave select output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_14			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_9			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_9			**Mux input channel 0 of TIM module 0**
	QSPI4_SLSIA			**Slave select input**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	GTM_TOUT32	O1		**GTM muxed output**
	IOM_MON0_10			**Monitor input 0**
	QSPI1_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO0	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	PSI5S_CLK	O5		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_8			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_8			**Mux input channel 2 of TIM module 0**
	QSPI4_SCLKA			**Slave SPI clock inputs**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	GTM_TOUT33	O1		**GTM muxed output**
	IOM_MON0_11			**Monitor input 0**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	QSPI4_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_CGPWMN	O6		**Negative carrier generator output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y16	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-34 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T14	P33.14	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN0_8			**Mux input channel 0 of TIM module 5**
	GTM_TIM4_IN5_14			**Mux input channel 5 of TIM module 4**
	GTM_TIM2_IN0_8			**Mux input channel 0 of TIM module 2**
	QSPI2_SCLKD			**Slave SPI clock inputs**
	CBS_TGI6			**Trigger input**
	P33.14	O0		**General-purpose output**
	GTM_TOUT143	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**
	CBS_TGO6	O		**Trigger output**
U14	P33.15	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN1_9			**Mux input channel 1 of TIM module 5**
	GTM_TIM4_IN6_12			**Mux input channel 6 of TIM module 4**
	GTM_TIM2_IN1_7			**Mux input channel 1 of TIM module 2**
	CBS_TGI7			**Trigger input**
	P33.15	O0		**General-purpose output**
	GTM_TOUT144	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
	CBS_TGO7	O		**Trigger output**

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Table 2-35 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM5_IN3_9			**Mux input channel 3 of TIM module 5**
	GTM_TIM3_IN4_12			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN3_9			**Mux input channel 3 of TIM module 2**
	EVADC_G10CH11	AI		**Analog input channel 11, group 10**
	P34.1	O0		**General-purpose output**
	GTM_TOUT146	O1		**GTM muxed output**
	ASCLIN4_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	CAN00_TXD	O4		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	CAN20_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN4_9			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN5_13			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN4_8			**Mux input channel 4 of TIM module 2**
	ASCLIN4_ARXB			**Receive input**
	CAN00_RXDG			**CAN receive input node 0**
	CAN20_RXDC			**CAN receive input node 0**
	EVADC_G10CH10	AI		**Analog input channel 10, group 10**
	P34.2	O0		**General-purpose output**
	GTM_TOUT147	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-35 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN5_10			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN6_13			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN5_9			**Mux input channel 5 of TIM module 2**
	EVADC_G10CH9	AI		**Analog input channel 9, group 10**
	P34.3	O0		**General-purpose output**
	GTM_TOUT148	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	QSPI2_SLSO10	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
T13	P34.4	I	SLOW / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN6_10			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN7_12			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN6_8			**Mux input channel 6 of TIM module 2**
	QSPI2_MRSTD			**Master SPI data input**
	EVADC_G10CH8	AI		**Analog input channel 8, group 10**
	P34.4	O0		**General-purpose output**
	GTM_TOUT149	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	QSPI2_MRST	O4		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-35 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U13	P34.5	I	FAST / PU1 / VEVRSB / ES	**General-purpose input**
	GTM_TIM5_IN7_9			**Mux input channel 7 of TIM module 5**
	GTM_TIM4_IN7_12			**Mux input channel 7 of TIM module 4**
	GTM_TIM2_IN7_9			**Mux input channel 7 of TIM module 2**
	QSPI2_MTSRD			**Slave SPI data input**
	ASCLIN8_ARXE			**Receive input**
	P34.5	O0		**General-purpose output**
	GTM_TOUT150	O1		**GTM muxed output**
	ASCLIN8_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	QSPI2_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

Table 2-36 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
U10	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
W9	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**
U9	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
T9	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
Y9	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**

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Table 2-36 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T8	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
U8	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
W8	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
U7	AN9	I	D / HighZ / VDDM	**Analog Input 9**
	EVADC_G11CH5			**Analog input channel 5, group 11**
	EVADC_G1CH1			**Analog input channel 1, group 1**
Y8	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
W7	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
T7	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
W6	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
U6	AN14	I	D / HighZ / VDDM	**Analog Input 14**
	EVADC_G1CH6			**Analog input channel 6, group 1**
	EDSADC_EDS3PB			**Positive analog input channel 3, pin B**
T6	AN15	I	D / HighZ / VDDM	**Analog Input 15**
	EVADC_G1CH7			**Analog input channel 7, group 1**
	EDSADC_EDS3NB			**Negative analog input channel 3, pin N**
W5	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
U5	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-36 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W4	AN18/P40.11	I	S / HighZ / VDDM	**Analog Input 18**
	SENT_SENT11A			**Receive input channel 11**
	EVADC_G11CH8			**Analog input channel 8, group 11**
	EVADC_G2CH2			**Analog input channel 2, group 2**
W3	AN19/P40.12	I	S / HighZ / VDDM	**Analog Input 19**
	SENT_SENT12A			**Receive input channel 12**
	EVADC_G11CH9			**Analog input channel 9, group 11**
	EVADC_G2CH3			**Analog input channel 3, group 2**
Y3	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
Y2	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
T5	AN22	I	D / HighZ / VDDM	**Analog Input 22**
	EVADC_G2CH6			**Analog input channel 6, group 2**
R5	AN23	I	D / HighZ / VDDM	**Analog Input 23**
	EVADC_G2CH7			**Analog input channel 7, group 2**
W2	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
W1	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
V2	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
	EVADC_G11CH10			**Analog input channel 10, group 11**
V1	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
	EVADC_G11CH11			**Analog input channel 11, group 11**

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Table 2-36 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
U2	AN28/P40.13	I	S / HighZ / VDDM	**Analog Input 28**
	SENT_SENT13A			**Receive input channel 13**
	EVADC_G3CH4			**Analog input channel 4, group 3**
U1	AN29/P40.14	I	S / HighZ / VDDM	**Analog Input 29**
	SENT_SENT14A			**Receive input channel 14**
	EVADC_G3CH5			**Analog input channel 5, group 3**
T4	AN30	I	D / HighZ / VDDM	**Analog Input 30**
	EVADC_G3CH6			**Analog input channel 6, group 3**
R4	AN31	I	D / HighZ / VDDM	**Analog Input 31**
	EVADC_G3CH7			**Analog input channel 7, group 3**
P4	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
	EVADC_G11CH12			**Analog input channel 12, group 11**
R1	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
	EVADC_G11CH13			**Analog input channel 13, group 11**
P5	AN34	I	D / HighZ / VDDM	**Analog Input 34**
	EVADC_G8CH2			**Analog input channel 2, group 8**
	EVADC_G11CH14			**Analog input channel 14, group 11**
R2	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
N4	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
P2	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**

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Table 2-36 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N5	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
P1	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
M5	AN40	I	D / HighZ / VDDM	**Analog Input 40**
	EVADC_G8CH8			**Analog input channel 8, group 8**
M4	AN41	I	D / HighZ / VDDM	**Analog Input 41**
	EVADC_G8CH9			**Analog input channel 9, group 8**
L5	AN42	I	D / HighZ / VDDM	**Analog Input 42**
	EVADC_G8CH10			**Analog input channel 10, group 8**
L4	AN43	I	D / HighZ / VDDM	**Analog Input 43**
	EVADC_G8CH11			**Analog input channel 11, group 8**
N1	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
N2	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
M1	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
M2	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

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Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

3. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
4. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-37 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AGBTCLKN (VSS)	I	AGBT_CLK / VEXT	**Input PAD (negative pole) for the external 100 MHz differential clock.** AGBT Input; (TC3xx devices without AGBT: VSS)
K7	AGBTCLKP (VSS)	I	AGBT_CLK / VEXT	**Input PAD (positive pole) for the external 100 MHz differential clock.** AGBT Input; (TC3xx devices without AGBT: VSS)
P10	AGBTTXN (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole** AGBT Output; (TC3xx devices without AGBT: VSS)
P11	AGBTTXP (VSS)	O	AGBT_TX / VEXT	**Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole** AGBT Output; (TC3xx devices without AGBT: VSS)
L14	AGBTERR (VSS)	I	FAST / PD / VEXT	**Input PAD for CRC error from FPGA.** AGBT Input; (TC3xx devices without AGBT: VSS)
Y17	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
W17	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
M20	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
G10	DAPE2	I/O	FAST / PD2 / VEXT	**DAPE: DAPE2 Data I/O** DAPE: DAPE2 Data I/O (TC3xx devices without DAPE: VSS)
G11	DAPE1	I/O	FAST / PD2 / VEXT	**DAPE: DAPE1 Data I/O** DAPE: DAPE1 Data I/O (TC3xx devices without DAPE: VSS)
K16	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input** TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		**DAP: DAP1 Data I/O**

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Table 2-37 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K14	DAPE0	I	FAST / PD2 / VEXT	**DAPE: DAPE0 Clock Input** DAPE: DAPE0 clock input (TC3xx devices without DAPE: NC)
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input** TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
	DAPE0	I		**DAPE: DAPE0 Clock Input**
J16	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input** TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		**DAP: DAP0 Clock Input**
G16	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
F16	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

Table 2-38 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
P8, P13, N7, N14, E15, H14, D16, G13	VDD	I	—	**Digital Core Power Supply (1.25V)**
A2, B3, W20	VEXT	I	—	**External Power Supply (5V / 3.3V)**
D5	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
V19	VFLEX2	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**

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Table 2-38 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y5	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
B18, A19	VDDP3	I	—	**Flash Power Supply (3.3V)**
B2, D4, E5, T16, U17, W19, Y20, E16, D17, B19, A20	VSS	I	—	**Digital Ground**
Y4	VSSM	I	—	**Analog Ground for VDDM**
P9, P12, N9, N10, N11, N12, M7, M8, M10, M11, M13, M14, L8, L9, L10, L11, L12, L13, K8, K9, K10, K11, K12, K13, J7, J8, J10, J11, J13, J14, H9, H10, H11, H12, G9, G12	VSS	I	—	**Digital Ground**
L20	VSS	I	—	**Oscillator Ground, VSS(OSC)**
Y6	VAREF1	I	—	**Positive Analog Reference Voltage 1**
Y7	VAGND1	I	—	**Negative Analog Reference Voltage 1**
T1	VAREF2	I	—	**Positive Analog Reference Voltage 2**
T2	VAGND2	I	—	**Negative Analog Reference Voltage 2**
A1, Y1, U4	NC1	I	—	**Not connected. These pins are not connected on package level and will not be used for future extensions**
G8, H7	VDDSB (VDD)	I	—	**Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)**
T11	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
N19	VDD	I	—	**Digital Power Supply for Oscillator (1.25V), VDD(OSC)**
N20	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

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2.3 LQFP-176 Package Pinning of TC37xEXT

Note: In the following QFP package the VFLEX and VFLEX2 supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

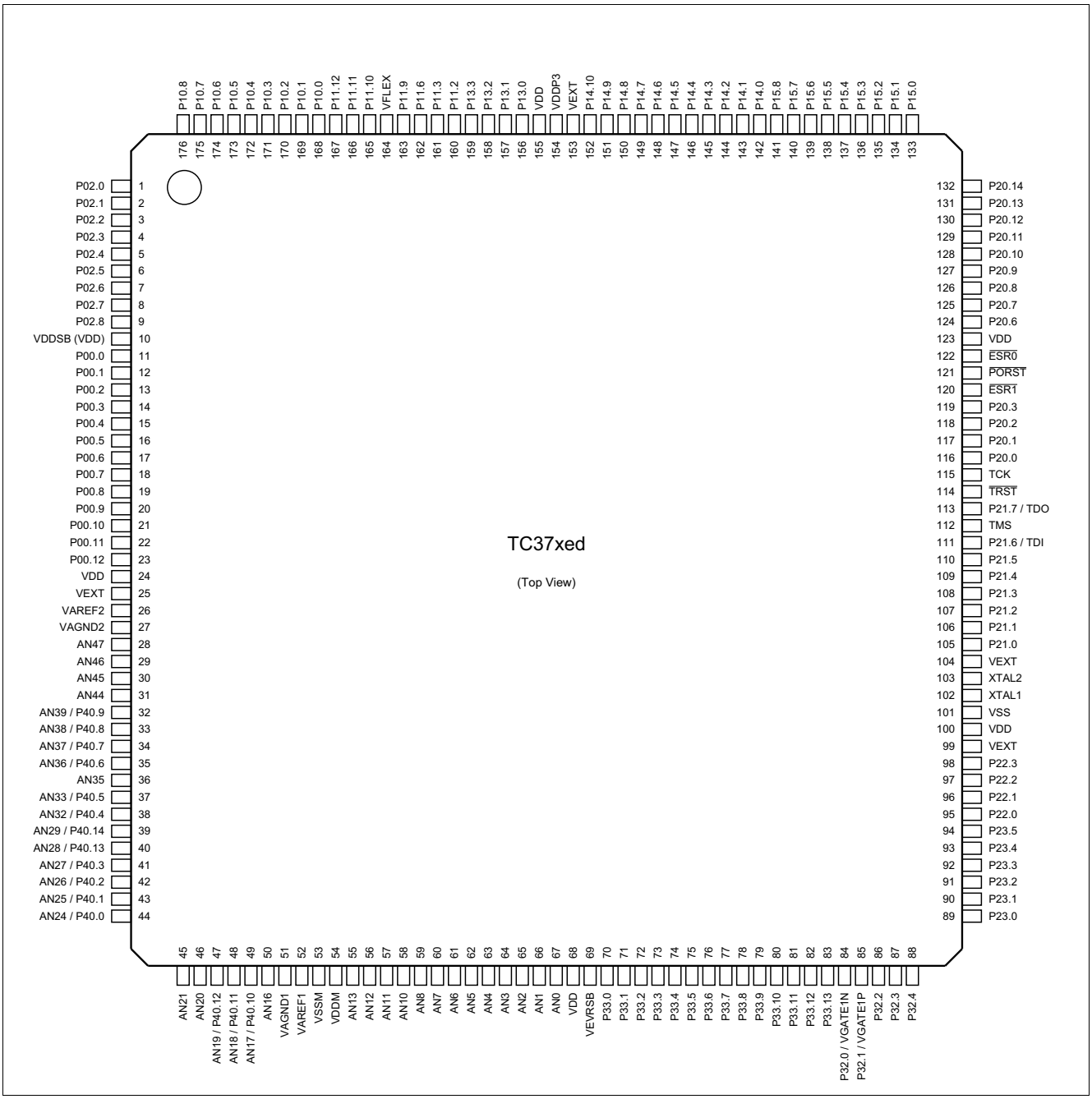


Figure 2-3 TC37xEXT package variant LQFP-176

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Table 2-39 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	CIF_D9			**sensor pixel data input**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CIF_D10			**sensor pixel data input**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	CIF_D11			**sensor pixel data input**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CIF_D12			**sensor pixel data input**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	CIF_D13			**sensor pixel data input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CIF_D14			**sensor pixel data input**
	CAN11_RXDB			**CAN receive input node 1**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
17	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	CIF_D15			**sensor pixel data input**
	ASCLIN5_ARXA			**Receive input**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	CIF_PCLK			**Sensor Pixel Clock input**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
19	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CIF_VSYNC			**vertical synchronization signal input**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CIF_HSYNC			**horizontal synchronization signal input**
	CCU60_T12HRC			**External timer start 12**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.10	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN1_11			**Mux input channel 1 of TIM module 4**
	GTM_TIM1_IN1_1			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_1			**Mux input channel 1 of TIM module 0**
	SENT_SENT9B			**Receive input channel 9**
	EDSADC_DSDIN1A			**Digital datastream input, channel 1**
	EVADC_G9CH2	AI		**Analog input channel 2, group 9**
	EDSADC_EDS4PB			**Positive analog input channel 4, pin B**
	P00.10	O0		**General-purpose output**
	GTM_TOUT19	O1		**GTM muxed output**
	ASCLIN4_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	SENT_SPC9	O6		**Transmit output**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
22	P00.11	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN2_11			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN2_1			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_1			**Mux input channel 2 of TIM module 0**
	CCU60_CTRAPA			**Trap input capture**
	EDSADC_DSCIN0A			**Modulator clock input, channel 0**
	CCU61_T12HRE			**External timer start 12**
	SENT_SENT10B			**Receive input channel 10**
	EVADC_G9CH1	AI		**Analog input channel 1, group 9**
	EVADC_FC3CH0			**Analog input FC channel 3**
	P00.11	O0		**General-purpose output**
	GTM_TOUT20	O1		**GTM muxed output**
	ASCLIN4_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-39 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
23	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

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Table 2-40 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D0			**sensor pixel data input**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D1			**sensor pixel data input**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	CIF_D2			**sensor pixel data input**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	CIF_D3			**sensor pixel data input**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	CIF_D4			**sensor pixel data input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	CIF_D5			**sensor pixel data input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	CIF_D6			**sensor pixel data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	CIF_D7			**sensor pixel data input**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-40 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CIF_D8			**sensor pixel data input**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-41 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
168	P10.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_12			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN4_2			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_2			**Mux input channel 4 of TIM module 0**
	GPT120_T6EUDB			**Count direction control input of core timer T6**
	ASCLIN11_ARXA			**Receive input**
	GETH_RXERC			**Receive Error MII**
	P10.0	O0		**General-purpose output**
	GTM_TOUT102	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	QSPI1_SLSO10	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
169	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-41 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
170	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-41 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
171	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
172	P10.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_3			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN6_2			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_2			**Mux input channel 6 of TIM module 0**
	QSPI1_MTSRC			**Slave SPI data input**
	CCU60_CCPOS0C			**Hall capture input 0**
	GPT120_T3INB			**Trigger/gate input of core timer T3**
	ASCLIN11_ARXB			**Receive input**
	P10.4	O0		**General-purpose output**
	GTM_TOUT106	O1		**GTM muxed output**
	IOM_MON2_11			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SLSO8	O3		**Master slave select output**
	QSPI1_MTSR	O4		**Master SPI data output**
	MSC0_EN0	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-41 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
173	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**
174	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

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Table 2-41 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
175	P10.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_3			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_3			**Mux input channel 0 of TIM module 0**
	GPT120_T3EUDB			**Count direction control input of core timer T3**
	ASCLIN2_ACTSA			**Clear to send input**
	QSPI3_MRSTB			**Master SPI data input**
	SCU_E_REQ0_2			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS1C			**Hall capture input 1**
	P10.7	O0		**General-purpose output**
	GTM_TOUT109	O1		**GTM muxed output**
	IOM_REF2_11			**Reference input 2**
	—	O2		**Reserved**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	—	O4		**Reserved**
	CAN20_TXD	O5		**CAN transmit output node 0**
	CAN12_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

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Table 2-41 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
176	P10.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_13			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN5_2			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_2			**Mux input channel 5 of TIM module 0**
	CAN12_RXDB			**CAN receive input node 2**
	GPT120_T4INB			**Trigger/gate input of timer T4**
	QSPI3_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ1_2			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CCU60_CCPOS2C			**Hall capture input 2**
	CAN20_RXDB			**CAN receive input node 0**
	P10.8	O0		**General-purpose output**
	GTM_TOUT110	O1		**GTM muxed output**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI3_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

Table 2-42 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
160	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-42 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
161	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
162	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-42 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
163	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-42 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
165	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-42 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
166	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
167	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-43 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
156	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**
157	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**

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Table 2-43 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
158	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**
159	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-44 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-44 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
143	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
144	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-44 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
145	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
146	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-44 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
147	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
148	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

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Table 2-44 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
149	P14.7	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN7_10			**Mux input channel 7 of TIM module 4**
	GTM_TIM1_IN0_5			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_5			**Mux input channel 0 of TIM module 0**
	ERAY0_RXDB0			**Receive Channel B0**
	CAN10_RXDB			**CAN receive input node 0**
	CAN13_RXDA			**CAN receive input node 3**
	ASCLIN9_ARXC			**Receive input**
	P14.7	O0		**General-purpose output**
	GTM_TOUT87	O1		**GTM muxed output**
	ASCLIN0_ARTS	O2		**Ready to send output**
	QSPI2_SLSO4	O3		**Master slave select output**
	ASCLIN9_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
150	P14.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_3			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_3			**Mux input channel 2 of TIM module 2**
	ERAY0_RXDA0			**Receive Channel A0**
	CAN02_RXDD			**CAN receive input node 2**
	ASCLIN1_ARXD			**Receive input**
	P14.8	O0		**General-purpose output**
	GTM_TOUT88	O1		**GTM muxed output**
	ASCLIN5_ASLSO	O2		**Slave select signal output**
	ASCLIN7_ASLSO	O3		**Slave select signal output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-44 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
151	P14.9	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_3			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_3			**Mux input channel 3 of TIM module 2**
	ASCLIN0_ACTSA			**Clear to send input**
	QSPI2_MRSTFN			**Master SPI data input (LVDS N line)**
	ASCLIN9_ARXD			**Receive input**
	P14.9	O0		**General-purpose output**
	GTM_TOUT89	O1		**GTM muxed output**
	CAN23_TXD	O2		**CAN transmit output node 3**
	MSC0_EN1	O3		**Chip Select**
	CAN10_TXD	O4		**CAN transmit output node 0**
	ERAY0_TXENB	O5		**Transmit Enable Channel B**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	—	O7		**Reserved**
152	P14.10	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_3			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_3			**Mux input channel 4 of TIM module 2**
	CAN23_RXDA			**CAN receive input node 3**
	QSPI2_MRSTFP			**Master SPI data input (LVDS P line)**
	P14.10	O0		**General-purpose output**
	GTM_TOUT90	O1		**GTM muxed output**
	—	O2		**Reserved**
	MSC0_EN0	O3		**Chip Select**
	ASCLIN1_ATX	O4		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	—	O7		**Reserved**

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Table 2-45 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	SDMMC0_DAT7_IN			**read data in**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
	SDMMC0_DAT7	O		**write data out**
134	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	SDMMC0_CLK	O7		**card clock**

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Table 2-45 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
136	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	SDMMC0_CMD_IN			**command in**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_CMD	O		**command out**

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Table 2-45 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-45 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
139	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-45 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
141	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-46 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
117	P20.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_11			**Mux input channel 4 of TIM module 4**
	GTM_TIM3_IN3_5			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_5			**Mux input channel 3 of TIM module 2**
	CBS_TGI1			**Trigger input**
	GTM_DTMA1_1			**CDTM1_DTM4**
	P20.1	O0		**General-purpose output**
	GTM_TOUT60	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO1	O		**Trigger output**

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Table 2-46 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**
119	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
124	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-46 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
125	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	SDMMC0_DAT0_IN			**read data in**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
	SDMMC0_DAT0	O		**write data out**
126	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	SDMMC0_DAT1_IN			**read data in**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
	SDMMC0_DAT1	O		**write data out**

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Table 2-46 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
127	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
128	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	SDMMC0_DAT2_IN			**read data in**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
	SDMMC0_DAT2	O		**write data out**

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Table 2-46 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
129	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	SDMMC0_DAT3_IN			**read data in**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
	SDMMC0_DAT3	O		**write data out**
130	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	SDMMC0_DAT4_IN			**read data in**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SDMMC0_DAT4	O		**write data out**

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Table 2-46 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	SDMMC0_DAT5_IN			**read data in**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SDMMC0_DAT5	O		**write data out**
132	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	SDMMC0_DAT6_IN			**read data in**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_DAT6	O		**write data out**

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Table 2-47 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P21.0	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN0_11			**Mux input channel 0 of TIM module 4**
	GTM_TIM3_IN4_6			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_6			**Mux input channel 4 of TIM module 2**
	QSPI4_MRSTDN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXC			**Receive input**
	P21.0	O0		**General-purpose output**
	GTM_TOUT51	O1		**GTM muxed output**
	ASCLIN11_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**
	HSM_HSM1	O		**Pin Output Value**
106	P21.1	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN1_13			**Mux input channel 1 of TIM module 4**
	GTM_TIM3_IN5_6			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_6			**Mux input channel 5 of TIM module 2**
	QSPI4_MRSTDP			**Master SPI data input (LVDS P line)**
	ASCLIN11_ARXD			**Receive input**
	GTM_DTMA4_1			**CDTM4_DTM4**
	P21.1	O0		**General-purpose output**
	GTM_TOUT52	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSM_HSM2	O		**Pin Output Value**

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Table 2-47 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**
108	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**

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Table 2-47 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**
110	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**

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Table 2-47 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**

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Table 2-47 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input** DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

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Table 2-48 Port 22 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P22.0	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	**General-purpose input**
	GTM_TIM1_IN1_7			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_7			**Mux input channel 1 of TIM module 0**
	QSPI4_MTSRB			**Slave SPI data input**
	ASCLIN6_ARXE			**Receive input**
	GETH1_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH1_RXDVB			**Receive Data Valid MII**
	GETH1_CRSA			**Carrier Sense MII**
	P22.0	O0		**General-purpose output**
	GTM_TOUT47	O1		**GTM muxed output**
	ASCLIN3_ATXN	O2		**Differential Transmit output (low active)**
	QSPI4_MTSR	O3		**Master SPI data output**
	QSPI4_SCLKN	O4		**Master SPI clock output (LVDS N line)**
	MSC1_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	ASCLIN6_ATX	O7		**Transmit output**
96	P22.1	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	**General-purpose input**
	GTM_TIM1_IN0_8			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_8			**Mux input channel 0 of TIM module 0**
	QSPI4_MRSTB			**Master SPI data input**
	ASCLIN7_ARXE			**Receive input**
	GETH1_RXERA			**Receive Error MII**
	P22.1	O0		**General-purpose output**
	GTM_TOUT48	O1		**GTM muxed output**
	ASCLIN3_ATXP	O2		**Differential Transmit output (high active)**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI4_SCLKP	O4		**Master SPI clock output (LVDS P line)**
	MSC1_FCLP	O5		**Shift-clock direct part of the differential signal**
	—	O6		**Reserved**
	ASCLIN7_ATX	O7		**Transmit output**

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Table 2-48 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
97	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	GETH1_COLA			**Collision MII**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
98	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-49 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
89	P23.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_4			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_4			**Mux input channel 5 of TIM module 0**
	CAN10_RXDC			**CAN receive input node 0**
	P23.0	O0		**General-purpose output**
	GTM_TOUT41	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
90	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**
91	P23.2	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN6_5			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_5			**Mux input channel 6 of TIM module 0**
	ASCLIN7_ARXC			**Receive input**
	P23.2	O0		**General-purpose output**
	GTM_TOUT43	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	CAN23_TXD	O4		**CAN transmit output node 3**
	CAN12_TXD	O5		**CAN transmit output node 2**
	GETH1_TXD3	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-49 Port 23 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
92	P23.3	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_4			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_4			**Mux input channel 7 of TIM module 0**
	MSC1_INJ0			**Injection signal from port**
	ASCLIN6_ARXA			**Receive input**
	CAN12_RXDC			**CAN receive input node 2**
	CAN23_RXDB			**CAN receive input node 3**
	P23.3	O0		**General-purpose output**
	GTM_TOUT44	O1		**GTM muxed output**
	ASCLIN7_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH1_TXD2	O6		**Transmit Data**
	—	O7		**Reserved**
93	P23.4	I	RFAST / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN7_5			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_5			**Mux input channel 7 of TIM module 0**
	P23.4	O0		**General-purpose output**
	GTM_TOUT45	O1		**GTM muxed output**
	ASCLIN6_ASLSO	O2		**Slave select signal output**
	QSPI4_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN0	O5		**Chip Select**
	GETH1_TXD1	O6		**Transmit Data**
	—	O7		**Reserved**

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Table 2-49 Port 23 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
94	P23.5	I	FAST / RGMII_Input / PU1 / VFLEX2 / ES	**General-purpose input**
	GTM_TIM1_IN2_7			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_7			**Mux input channel 2 of TIM module 0**
	GETH1_RXD3A			**Receive Data 3 MII and RGMII (RGMII can use RXD3A only)**
	P23.5	O0		**General-purpose output**
	GTM_TOUT46	O1		**GTM muxed output**
	ASCLIN6_ATX	O2		**Transmit output**
	QSPI4_SLSO4	O3		**Master slave select output**
	—	O4		**Reserved**
	MSC1_EN1	O5		**Chip Select**
	CAN22_TXD	O6		**CAN transmit output node 2**
	—	O7		**Reserved**

Table 2-50 Port 32 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-50 Port 32 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
85	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
86	P32.2	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_8			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_8			**Mux input channel 3 of TIM module 0**
	CAN03_RXDB			**CAN receive input node 3**
	ASCLIN3_ARXD			**Receive input**
	CAN21_RXDD			**CAN receive input node 1**
	P32.2	O0		**General-purpose output**
	GTM_TOUT38	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	PMS_DCDCSYNCO	O6		**DC-DC synchronization output**
	—	O7		**Reserved**

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Table 2-50 Port 32 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
87	P32.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_5			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_5			**Mux input channel 4 of TIM module 0**
	P32.3	O0		**General-purpose output**
	GTM_TOUT39	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	ASCLIN3_ASCLK	O4		**Shift clock output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
88	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

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Table 2-51 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P33.0	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_13			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN4_6			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_6			**Mux input channel 4 of TIM module 0**
	EDSADC_ITR0E			**Trigger/Gate input, channel 0**
	SENT_SENT13C			**Receive input channel 13**
	IOM_PIN_0			**GPIO pad input to FPC**
	GTM_DTMT1_2			**CDTM1_DTM0**
	EVADC_G10CH7	AI		**Analog input channel 7, group 10**
	P33.0	O0		**General-purpose output**
	GTM_TOUT22	O1		**GTM muxed output**
	IOM_MON0_0			**Monitor input 0**
	IOM_GTM_0			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	—	O7		**Reserved**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
71	P33.1	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_15			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN5_6			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_6			**Mux input channel 5 of TIM module 0**
	EDSADC_ITR1E			**Trigger/Gate input, channel 1**
	PSI5_RX0C			**RXD inputs (receive data) channel 0**
	EDSADC_DSCIN2B			**Modulator clock input, channel 2**
	SENT_SENT9C			**Receive input channel 9**
	ASCLIN8_ARXC			**Receive input**
	IOM_PIN_1			**GPIO pad input to FPC**
	EVADC_G10CH6	AI		**Analog input channel 6, group 10**
	P33.1	O0		**General-purpose output**
	GTM_TOUT23	O1		**GTM muxed output**
	IOM_MON0_1			**Monitor input 0**
	IOM_GTM_1			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	QSPI2_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P33.2	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN2_14			**Mux input channel 2 of TIM module 3**
	GTM_TIM1_IN6_6			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_6			**Mux input channel 6 of TIM module 0**
	EDSADC_ITR2E			**Trigger/Gate input, channel 2**
	SENT_SENT8C			**Receive input channel 8**
	EDSADC_DSDIN2B			**Digital datastream input, channel 2**
	IOM_PIN_2			**GPIO pad input to FPC**
	EVADC_G10CH5	AI		**Analog input channel 5, group 10**
	P33.2	O0		**General-purpose output**
	GTM_TOUT24	O1		**GTM muxed output**
	IOM_MON0_2			**Monitor input 0**
	IOM_GTM_2			**GTM-provided inputs to EXOR combiner**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	QSPI2_SLSO10	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P33.3	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN3_12			**Mux input channel 3 of TIM module 3**
	GTM_TIM1_IN7_6			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_6			**Mux input channel 7 of TIM module 0**
	PSI5_RX1C			**RXD inputs (receive data) channel 1**
	SENT_SENT7C			**Receive input channel 7**
	EDSADC_DSCIN1B			**Modulator clock input, channel 1**
	IOM_PIN_3			**GPIO pad input to FPC**
	EVADC_G10CH4	AI		**Analog input channel 4, group 10**
	P33.3	O0		**General-purpose output**
	GTM_TOUT25	O1		**GTM muxed output**
	IOM_MON0_3			**Monitor input 0**
	IOM_GTM_3			**GTM-provided inputs to EXOR combiner**
	ASCLIN5_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO2	O3		**Master slave select output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
79	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
80	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_14			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_9			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_9			**Mux input channel 0 of TIM module 0**
	QSPI4_SLSIA			**Slave select input**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	GTM_TOUT32	O1		**GTM muxed output**
	IOM_MON0_10			**Monitor input 0**
	QSPI1_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO0	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	PSI5S_CLK	O5		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**
81	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_8			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_8			**Mux input channel 2 of TIM module 0**
	QSPI4_SCLKA			**Slave SPI clock inputs**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	GTM_TOUT33	O1		**GTM muxed output**
	IOM_MON0_11			**Monitor input 0**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	QSPI4_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_CGPWMN	O6		**Negative carrier generator output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
82	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-51 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
83	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-52 Analog Inputs

Pin	Symbol	Ctrl.	Buffer Type	Function
67	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
66	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
65	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**

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Table 2-52 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
64	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
63	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
62	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**
61	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
60	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
59	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
58	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
57	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
56	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
55	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
50	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
49	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-52 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
48	AN18/P40.11	I	S / HighZ / VDDM	**Analog Input 18**
	SENT_SENT11A			**Receive input channel 11**
	EVADC_G11CH8			**Analog input channel 8, group 11**
	EVADC_G2CH2			**Analog input channel 2, group 2**
47	AN19/P40.12	I	S / HighZ / VDDM	**Analog Input 19**
	SENT_SENT12A			**Receive input channel 12**
	EVADC_G11CH9			**Analog input channel 9, group 11**
	EVADC_G2CH3			**Analog input channel 3, group 2**
46	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
45	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
44	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
43	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
42	AN26/P40.2	I	S / HighZ / VDDM	**Analog Input 26**
	SENT_SENT2A			**Receive input channel 2**
	EVADC_G3CH2			**Analog input channel 2, group 3**
	CCU60_CCPOS1D			**Hall capture input 1**
	EVADC_G11CH10			**Analog input channel 10, group 11**
41	AN27/P40.3	I	S / HighZ / VDDM	**Analog Input 27**
	SENT_SENT3A			**Receive input channel 3**
	EVADC_G3CH3			**Analog input channel 3, group 3**
	CCU60_CCPOS2B			**Hall capture input 2**
	EVADC_G11CH11			**Analog input channel 11, group 11**
40	AN28/P40.13	I	S / HighZ / VDDM	**Analog Input 28**
	SENT_SENT13A			**Receive input channel 13**
	EVADC_G3CH4			**Analog input channel 4, group 3**

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Table 2-52 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
39	AN29/P40.14	I	S / HighZ / VDDM	**Analog Input 29**
	SENT_SENT14A			**Receive input channel 14**
	EVADC_G3CH5			**Analog input channel 5, group 3**
38	AN32/P40.4	I	S / HighZ / VDDM	**Analog Input 32**
	SENT_SENT4A			**Receive input channel 4**
	EVADC_G8CH0			**Analog input channel 0, group 8**
	CCU60_CCPOS2D			**Hall capture input 2**
	EVADC_G11CH12			**Analog input channel 12, group 11**
37	AN33/P40.5	I	S / HighZ / VDDM	**Analog Input 33**
	SENT_SENT5A			**Receive input channel 5**
	EVADC_G8CH1			**Analog input channel 1, group 8**
	CCU61_CCPOS0D			**Hall capture input 0**
	EVADC_G11CH13			**Analog input channel 13, group 11**
36	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
35	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
34	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
33	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**
32	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**

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Table 2-52 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
31	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
30	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
29	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
28	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

5. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
6. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-53 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
84	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
85	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
102	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
103	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
112	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input** TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		**DAP: DAP1 Data I/O**
114	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input** TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
	DAPE0	I		**DAPE: DAPE0 Clock Input**

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Table 2-53 System I/O (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
115	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input** TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		**DAP: DAP0 Clock Input**
120	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
121	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
122	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

Table 2-54 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
164	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
54	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
154	VDDP3	I	—	**Flash Power Supply (3.3V)**
52	VAREF1	I	—	**Positive Analog Reference Voltage 1**
26	VAREF2	I	—	**Positive Analog Reference Voltage 2**
10	VDDSB (VDD)	I	—	**Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)**
69	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
155	VDD	I	—	**Digital Core Power Supply (1.25V)**
24	VDD	I	—	**Digital Core Power Supply (1.25V)**
68	VDD	I	—	**Digital Core Power Supply (1.25V)**

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Table 2-54 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
100	VDD	I	—	**Digital Core Power Supply (1.25V)**
123	VDD	I	—	**Digital Core Power Supply (1.25V)**
153	VEXT	I	—	**External Power Supply (5V / 3.3V)**
25	VEXT	I	—	**External Power Supply (5V / 3.3V)**
99	VEXT	I	—	**External Power Supply (5V / 3.3V)**
E-PAD	VSS	I	—	**Digital Ground (Exposed PAD), VSS**
53	VSSM	I	—	**Analog Ground for VDDM**
51	VAGND1	I	—	**Negative Analog Reference Voltage 1**
27	VAGND2	I	—	**Negative Analog Reference Voltage 2**
101	VSS	I	—	**Oscillator Ground, VSS(OSC)**
104	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

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2.4 LQFP-144 Package Pinning of TC37xEXT

Note: In the following QFP package the VFLEX and VFLEX2 supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

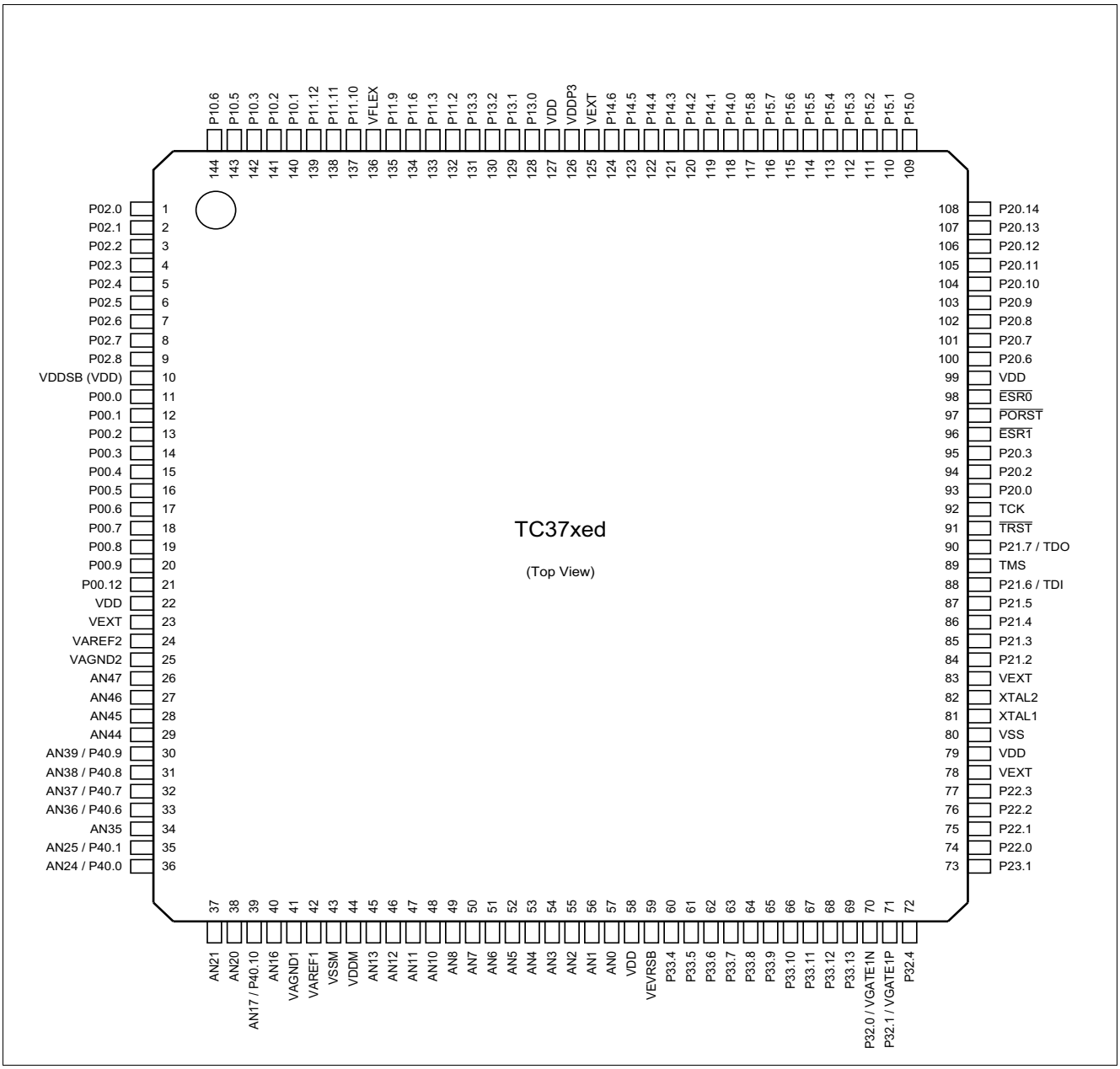


Figure 2-4 TC37xEXT package variant LQFP-144

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Table 2-55 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
11	P00.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_10			**Mux input channel 4 of TIM module 5**
	GTM_TIM3_IN0_1			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_1			**Mux input channel 0 of TIM module 2**
	CCU61_CTRAPA			**Trap input capture**
	CCU60_T12HRE			**External timer start 12**
	MSC0_INJ0			**Injection signal from port**
	CIF_D9			**sensor pixel data input**
	GETH_MDIOA			**MDIO Input**
	P00.0	O0		**General-purpose output**
	GTM_TOUT9	O1		**GTM muxed output**
	IOM_REF0_9			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN3_ATX	O3		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O4		**Reserved**
	CAN10_TXD	O5		**CAN transmit output node 0**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	GETH_MDIO	O		**MDIO Output**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_11			**Mux input channel 5 of TIM module 5**
	GTM_TIM3_IN1_1			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_1			**Mux input channel 1 of TIM module 2**
	CCU60_CC60INB			**T12 capture input 60**
	ASCLIN3_ARXE			**Receive input**
	EDSADC_DSCIN5A			**Modulator clock input, channel 5**
	CAN10_RXDA			**CAN receive input node 0**
	PSI5_RX0A			**RXD inputs (receive data) channel 0**
	CIF_D10			**sensor pixel data input**
	CCU61_CC60INA			**T12 capture input 60**
	SENT_SENT0B			**Receive input channel 0**
	EVADC_G9CH11	AI		**Analog input channel 11, group 9**
	EDSADC_EDS5NA			**Negative analog input channel 5, pin A**
	P00.1	O0		**General-purpose output**
	GTM_TOUT10	O1		**GTM muxed output**
	IOM_REF0_10			**Reference input 0**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	—	O3		**Reserved**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC0	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
13	P00.2	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN6_11			**Mux input channel 6 of TIM module 5**
	GTM_TIM3_IN1_2			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_2			**Mux input channel 1 of TIM module 2**
	EDSADC_DSDIN5A			**Digital datastream input, channel 5**
	SENT_SENT1B			**Receive input channel 1**
	CIF_D11			**sensor pixel data input**
	EVADC_G9CH10	AI		**Analog input channel 10, group 9**
	EDSADC_EDS5PA			**Positive analog input channel 5, pin A**
	P00.2	O0		**General-purpose output**
	GTM_TOUT11	O1		**GTM muxed output**
	IOM_REF0_11			**Reference input 0**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	CAN21_TXD	O3		**CAN transmit output node 1**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	QSPI3_SLSO4	O6		**Master slave select output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM5_IN7_10			**Mux input channel 7 of TIM module 5**
	GTM_TIM3_IN2_1			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_1			**Mux input channel 2 of TIM module 2**
	CCU60_CC61INB			**T12 capture input 61**
	EDSADC_DSCIN3A			**Modulator clock input, channel 3**
	EDSADC_ITR5F			**Trigger/Gate input, channel 5**
	PSI5_RX1A			**RXD inputs (receive data) channel 1**
	CAN03_RXDA			**CAN receive input node 3**
	CAN21_RXDA			**CAN receive input node 1**
	PSI5S_RXA			**RX data input**
	SENT_SENT2B			**Receive input channel 2**
	CIF_D12			**sensor pixel data input**
	CCU61_CC61INA			**T12 capture input 61**
	EVADC_G9CH9	AI		**Analog input channel 9, group 9**
	EDSADC_EDS5NB			**Negative analog input channel 5, pin B**
	P00.3	O0		**General-purpose output**
	GTM_TOUT12	O1		**GTM muxed output**
	IOM_REF0_12			**Reference input 0**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	—	O5		**Reserved**
	SENT_SPC2	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
15	P00.4	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN3_1			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_1			**Mux input channel 3 of TIM module 2**
	SCU_E_REQ2_2			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT3B			**Receive input channel 3**
	EDSADC_DSDIN3A			**Digital datastream input, channel 3**
	EDSADC_SGNA			**Carrier sign signal input**
	ASCLIN10_ARXA			**Receive input**
	CIF_D13			**sensor pixel data input**
	EVADC_G9CH8	AI		**Analog input channel 8, group 9**
	EDSADC_EDS5PB			**Positive analog input channel 5, pin B**
	P00.4	O0		**General-purpose output**
	GTM_TOUT13	O1		**GTM muxed output**
	IOM_REF0_13			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	CAN11_TXD	O3		**CAN transmit output node 1**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	—	O5		**Reserved**
	SENT_SPC3	O6		**Transmit output**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN4_1			**Mux input channel 4 of TIM module 3**
	GTM_TIM3_IN0_11			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN4_1			**Mux input channel 4 of TIM module 2**
	CCU60_CC62INB			**T12 capture input 62**
	EDSADC_DSCIN2A			**Modulator clock input, channel 2**
	CCU61_CC62INA			**T12 capture input 62**
	SENT_SENT4B			**Receive input channel 4**
	CIF_D14			**sensor pixel data input**
	CAN11_RXDB			**CAN receive input node 1**
	GTM_DTMT1_1			**CDTM1_DTM0**
	EVADC_G9CH7	AI		**Analog input channel 7, group 9**
	P00.5	O0		**General-purpose output**
	GTM_TOUT14	O1		**GTM muxed output**
	IOM_REF0_14			**Reference input 0**
	EDSADC_CGPWMN	O2		**Negative carrier generator output**
	QSPI3_SLSO3	O3		**Master slave select output**
	EDSADC_DSCOUT2	O4		**Modulator clock output**
	EVADC_FC0BFLOUT	O5		**Boundary flag output, FC channel 0**
	SENT_SPC4	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
17	P00.6	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN5_1			**Mux input channel 5 of TIM module 3**
	GTM_TIM3_IN1_14			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN5_1			**Mux input channel 5 of TIM module 2**
	EDSADC_ITR4F			**Trigger/Gate input, channel 4**
	EDSADC_DSDIN2A			**Digital datastream input, channel 2**
	SENT_SENT5B			**Receive input channel 5**
	CIF_D15			**sensor pixel data input**
	ASCLIN5_ARXA			**Receive input**
	EVADC_G9CH6	AI		**Analog input channel 6, group 9**
	P00.6	O0		**General-purpose output**
	GTM_TOUT15	O1		**GTM muxed output**
	IOM_REF0_15			**Reference input 0**
	EDSADC_CGPWMP	O2		**Positive carrier generator output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC5	O6		**Transmit output**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN6_1			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN2_11			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN6_1			**Mux input channel 6 of TIM module 2**
	CCU61_CC60INC			**T12 capture input 60**
	SENT_SENT6B			**Receive input channel 6**
	EDSADC_DSCIN4A			**Modulator clock input, channel 4**
	GPT120_T2INA			**Trigger/gate input of timer T2**
	CCU61_CCPOS0A			**Hall capture input 0**
	CCU60_T12HRB			**External timer start 12**
	CIF_PCLK			**Sensor Pixel Clock input**
	GTM_DTMT0_2			**CDTM0_DTM0**
	EVADC_G9CH5	AI		**Analog input channel 5, group 9**
	EDSADC_EDS4NA			**Negative analog input channel 4, pin A**
	P00.7	O0		**General-purpose output**
	GTM_TOUT16	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	EVADC_FC2BFLOUT	O3		**Boundary flag output, FC channel 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC6	O6		**Transmit output**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
19	P00.8	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM3_IN7_1			**Mux input channel 7 of TIM module 3**
	GTM_TIM3_IN3_11			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN7_1			**Mux input channel 7 of TIM module 2**
	CCU61_CC61INC			**T12 capture input 61**
	SENT_SENT7B			**Receive input channel 7**
	EDSADC_DSDIN4A			**Digital datastream input, channel 4**
	GPT120_T2EUDA			**Count direction control input of timer T2**
	CCU61_CCPOS1A			**Hall capture input 1**
	CIF_VSYNC			**vertical synchronization signal input**
	CCU60_T13HRB			**External timer start 13**
	ASCLIN10_ARXB			**Receive input**
	EVADC_G9CH4	AI		**Analog input channel 4, group 9**
	EDSADC_EDS4PA			**Positive analog input channel 4, pin A**
	P00.8	O0		**General-purpose output**
	GTM_TOUT17	O1		**GTM muxed output**
	QSPI3_SLSO6	O2		**Master slave select output**
	ASCLIN10_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	SENT_SPC7	O6		**Transmit output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN0_7			**Mux input channel 0 of TIM module 4**
	GTM_TIM1_IN0_1			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_1			**Mux input channel 0 of TIM module 0**
	CCU61_CC62INC			**T12 capture input 62**
	SENT_SENT8B			**Receive input channel 8**
	CCU61_CCPOS2A			**Hall capture input 2**
	EDSADC_DSCIN1A			**Modulator clock input, channel 1**
	EDSADC_ITR3F			**Trigger/Gate input, channel 3**
	GPT120_T4EUDA			**Count direction control input of timer T4**
	CCU60_T13HRC			**External timer start 13**
	CIF_HSYNC			**horizontal synchronization signal input**
	CCU60_T12HRC			**External timer start 12**
	EVADC_G9CH3	AI		**Analog input channel 3, group 9**
	EDSADC_EDS4NB			**Negative analog input channel 4, pin B**
	P00.9	O0		**General-purpose output**
	GTM_TOUT18	O1		**GTM muxed output**
	QSPI3_SLSO7	O2		**Master slave select output**
	ASCLIN3_ARTS	O3		**Ready to send output**
	EDSADC_DSCOUT1	O4		**Modulator clock output**
	ASCLIN4_ATX	O5		**Transmit output**
	SENT_SPC8	O6		**Transmit output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-55 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
21	P00.12	I	SLOW / PU1 / VEXT / ES1	**General-purpose input**
	GTM_TIM4_IN3_11			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN3_1			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_1			**Mux input channel 3 of TIM module 0**
	ASCLIN3_ACTSA			**Clear to send input**
	EDSADC_DSDIN0A			**Digital datastream input, channel 0**
	ASCLIN4_ARXA			**Receive input**
	SENT_SENT11B			**Receive input channel 11**
	EVADC_G9CH0	AI		**Analog input channel 0, group 9**
	EVADC_FC2CH0			**Analog input FC channel 2**
	P00.12	O0		**General-purpose output**
	GTM_TOUT21	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**

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Table 2-56 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_2			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_2			**Mux input channel 0 of TIM module 0**
	CCU61_CC60INB			**T12 capture input 60**
	ASCLIN2_ARXG			**Receive input**
	CCU60_CC60INA			**T12 capture input 60**
	SCU_E_REQ3_2			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D0			**sensor pixel data input**
	GTM_DTMA0_0			**CDTM0_DTM4**
	P02.0	O0		**General-purpose output**
	GTM_TOUT0	O1		**GTM muxed output**
	IOM_REF0_0			**Reference input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO1	O3		**Master slave select output**
	EDSADC_CGPWMN	O4		**Negative carrier generator output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	ERAY0_TXDA	O6		**Transmit Channel A**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_2			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_2			**Mux input channel 1 of TIM module 0**
	ERAY0_RXDA2			**Receive Channel A2**
	ASCLIN2_ARXB			**Receive input**
	CAN00_RXDA			**CAN receive input node 0**
	SCU_E_REQ2_1			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	CIF_D1			**sensor pixel data input**
	P02.1	O0		**General-purpose output**
	GTM_TOUT1	O1		**GTM muxed output**
	IOM_REF0_1			**Reference input 0**
	QSPI4_SLSO7	O2		**Master slave select output**
	QSPI3_SLSO2	O3		**Master slave select output**
	EDSADC_CGPWMP	O4		**Positive carrier generator output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
3	P02.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_2			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_2			**Mux input channel 2 of TIM module 0**
	CCU61_CC61INB			**T12 capture input 61**
	CCU60_CC61INA			**T12 capture input 61**
	CIF_D2			**sensor pixel data input**
	SENT_SENT14B			**Receive input channel 14**
	P02.2	O0		**General-purpose output**
	GTM_TOUT2	O1		**GTM muxed output**
	IOM_REF0_2			**Reference input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI3_SLSO3	O3		**Master slave select output**
	PSI5_TX0	O4		**TXD outputs (send data)**
	IOM_MON1_14			**Monitor input 1**
	IOM_REF1_14			**Reference input 1**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ERAY0_TXDB	O6		**Transmit Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
4	P02.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN3_2			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_2			**Mux input channel 3 of TIM module 0**
	EDSADC_DSCIN5B			**Modulator clock input, channel 5**
	ERAY0_RXDB2			**Receive Channel B2**
	CAN02_RXDB			**CAN receive input node 2**
	ASCLIN1_ARXG			**Receive input**
	MSC1_SDI1			**Upstream assynchronous input signal**
	PSI5_RX0B			**RXD inputs (receive data) channel 0**
	CIF_D3			**sensor pixel data input**
	SENT_SENT13B			**Receive input channel 13**
	P02.3	O0		**General-purpose output**
	GTM_TOUT3	O1		**GTM muxed output**
	IOM_REF0_3			**Reference input 0**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI3_SLSO4	O3		**Master slave select output**
	EDSADC_DSCOUT5	O4		**Modulator clock output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
5	P02.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN4_1			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_1			**Mux input channel 4 of TIM module 0**
	CCU61_CC62INB			**T12 capture input 62**
	EDSADC_DSDIN5B			**Digital datastream input, channel 5**
	QSPI3_SLSIA			**Slave select input**
	CCU60_CC62INA			**T12 capture input 62**
	I2C0_SDAA			**Serial Data Input 0**
	CAN11_RXDA			**CAN receive input node 1**
	CAN0_ECTT1			**External CAN time trigger input**
	CIF_D4			**sensor pixel data input**
	SENT_SENT12B			**Receive input channel 12**
	P02.4	O0		**General-purpose output**
	GTM_TOUT4	O1		**GTM muxed output**
	IOM_REF0_4			**Reference input 0**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_SLSO0	O3		**Master slave select output**
	PSI5S_CLK	O4		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	I2C0_SDA	O5		**Serial Data Output**
	ERAY0_TXENA	O6		**Transmit Enable Channel A**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
6	P02.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_1			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_1			**Mux input channel 5 of TIM module 0**
	EDSADC_DSCIN4B			**Modulator clock input, channel 4**
	I2C0_SCLA			**Serial Clock Input 0**
	PSI5_RX1B			**RXD inputs (receive data) channel 1**
	PSI5S_RXB			**RX data input**
	QSPI3_MRSTA			**Master SPI data input**
	SENT_SENT3C			**Receive input channel 3**
	CAN0_ECTT2			**External CAN time trigger input**
	CIF_D5			**sensor pixel data input**
	P02.5	O0		**General-purpose output**
	GTM_TOUT5	O1		**GTM muxed output**
	IOM_REF0_5			**Reference input 0**
	CAN11_TXD	O2		**CAN transmit output node 1**
	QSPI3_MRST	O3		**Slave SPI data output**
	IOM_MON2_3			**Monitor input 2**
	IOM_REF2_3			**Reference input 2**
	EDSADC_DSCOUT4	O4		**Modulator clock output**
	I2C0_SCL	O5		**Serial Clock Output**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_10			**Mux input channel 0 of TIM module 3**
	GTM_TIM1_IN6_1			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_1			**Mux input channel 6 of TIM module 0**
	CCU60_CC60INC			**T12 capture input 60**
	SENT_SENT2C			**Receive input channel 2**
	EDSADC_DSDIN4B			**Digital datastream input, channel 4**
	EDSADC_ITR5E			**Trigger/Gate input, channel 5**
	GPT120_T3INA			**Trigger/gate input of core timer T3**
	CCU60_CCPOS0A			**Hall capture input 0**
	CCU61_T12HRB			**External timer start 12**
	QSPI3_MTSRA			**Slave SPI data input**
	CIF_D6			**sensor pixel data input**
	P02.6	O0		**General-purpose output**
	GTM_TOUT6	O1		**GTM muxed output**
	IOM_REF0_6			**Reference input 0**
	PSI5S_TX	O2		**TX data output**
	QSPI3_MTSR	O3		**Master SPI data output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX00	O5		**Control of external analog multiplexer interface 0**
	—	O6		**Reserved**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_10			**Mux input channel 1 of TIM module 3**
	GTM_TIM1_IN7_1			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_1			**Mux input channel 7 of TIM module 0**
	CCU60_CC61INC			**T12 capture input 61**
	SENT_SENT1C			**Receive input channel 1**
	EDSADC_DSCIN3B			**Modulator clock input, channel 3**
	EDSADC_ITR4E			**Trigger/Gate input, channel 4**
	GPT120_T3EUDA			**Count direction control input of core timer T3**
	CCU60_CCPOS1A			**Hall capture input 1**
	CIF_D7			**sensor pixel data input**
	QSPI3_SCLKA			**Slave SPI clock inputs**
	CCU61_T13HRB			**External timer start 13**
	P02.7	O0		**General-purpose output**
	GTM_TOUT7	O1		**GTM muxed output**
	IOM_REF0_7			**Reference input 0**
	—	O2		**Reserved**
	QSPI3_SCLK	O3		**Master SPI clock output**
	EDSADC_DSCOUT3	O4		**Modulator clock output**
	EVADC_EMUX01	O5		**Control of external analog multiplexer interface 0**
	SENT_SPC1	O6		**Transmit output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**

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Table 2-56 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
9	P02.8	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_10			**Mux input channel 2 of TIM module 3**
	GTM_TIM3_IN0_2			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_2			**Mux input channel 0 of TIM module 2**
	CCU60_CC62INC			**T12 capture input 62**
	SENT_SENT0C			**Receive input channel 0**
	CCU60_CCPOS2A			**Hall capture input 2**
	EDSADC_DSDIN3B			**Digital datastream input, channel 3**
	EDSADC_ITR3E			**Trigger/Gate input, channel 3**
	GPT120_T4INA			**Trigger/gate input of timer T4**
	CCU61_T12HRC			**External timer start 12**
	CIF_D8			**sensor pixel data input**
	CCU61_T13HRC			**External timer start 13**
	GTM_DTMA0_1			**CDTM0_DTM4**
	P02.8	O0		**General-purpose output**
	GTM_TOUT8	O1		**GTM muxed output**
	IOM_REF0_8			**Reference input 0**
	QSPI3_SLSO5	O2		**Master slave select output**
	ASCLIN8_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	EVADC_EMUX02	O5		**Control of external analog multiplexer interface 0**
	GETH_MDC	O6		**MDIO clock**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-57 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P10.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN4_12			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN1_3			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_3			**Mux input channel 1 of TIM module 0**
	GPT120_T5EUDB			**Count direction control input of timer T5**
	QSPI1_MRSTA			**Master SPI data input**
	GTM_DTMT0_1			**CDTM0_DTM0**
	P10.1	O0		**General-purpose output**
	GTM_TOUT103	O1		**GTM muxed output**
	QSPI1_MTSR	O2		**Master SPI data output**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	MSC0_EN1	O4		**Chip Select**
	EVADC_FC1BFLOUT	O5		**Boundary flag output, FC channel 1**
	—	O6		**Reserved**
	—	O7		**Reserved**
141	P10.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_12			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN2_3			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_3			**Mux input channel 2 of TIM module 0**
	CAN02_RXDE			**CAN receive input node 2**
	MSC0_SDI1			**Upstream assynchronous input signal**
	QSPI1_SCLKA			**Slave SPI clock inputs**
	GPT120_T6INB			**Trigger/gate input of core timer T6**
	SCU_E_REQ2_0			**ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GTM_DTMT2_2			**CDTM2_DTM0**
	P10.2	O0		**General-purpose output**
	GTM_TOUT104	O1		**GTM muxed output**
	IOM_MON2_9			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_SCLK	O3		**Master SPI clock output**
	MSC0_EN0	O4		**Chip Select**
	EVADC_FC3BFLOUT	O5		**Boundary flag output, FC channel 3**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-57 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P10.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN6_10			**Mux input channel 6 of TIM module 4**
	GTM_TIM1_IN3_3			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_3			**Mux input channel 3 of TIM module 0**
	QSPI1_MTSRA			**Slave SPI data input**
	SCU_E_REQ3_0			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T5INB			**Trigger/gate input of timer T5**
	P10.3	O0		**General-purpose output**
	GTM_TOUT105	O1		**GTM muxed output**
	IOM_MON2_10			**Monitor input 2**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	MSC0_EN0	O4		**Chip Select**
	—	O5		**Reserved**
	CAN02_TXD	O6		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	—	O7		**Reserved**
143	P10.5	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN3_13			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN2_4			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_4			**Mux input channel 2 of TIM module 0**
	PMS_HWCFG4IN			**HWCFG4 pin input**
	CAN20_RXDA			**CAN receive input node 0**
	MSC0_INJ1			**Injection signal from port**
	P10.5	O0		**General-purpose output**
	GTM_TOUT107	O1		**GTM muxed output**
	IOM_REF2_9			**Reference input 2**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI3_SLSO8	O3		**Master slave select output**
	QSPI1_SLSO9	O4		**Master slave select output**
	GPT120_T6OUT	O5		**External output for overflow/underflow detection of core timer T6**
	ASCLIN2_ASLSO	O6		**Slave select signal output**
	—	O7		**Reserved**

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Table 2-57 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
144	P10.6	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN2_13			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN3_4			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_4			**Mux input channel 3 of TIM module 0**
	ASCLIN2_ARXD			**Receive input**
	QSPI3_MTSRB			**Slave SPI data input**
	PMS_HWCFG5IN			**HWCFG5 pin input**
	P10.6	O0		**General-purpose output**
	GTM_TOUT108	O1		**GTM muxed output**
	IOM_REF2_10			**Reference input 2**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI3_MTSR	O3		**Master SPI data output**
	GPT120_T3OUT	O4		**External output for overflow/underflow detection of core timer T3**
	CAN20_TXD	O5		**CAN transmit output node 0**
	QSPI1_MRST	O6		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	—	O7		**Reserved**

Table 2-58 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
132	P11.2	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN1_3			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_3			**Mux input channel 1 of TIM module 2**
	P11.2	O0		**General-purpose output**
	GTM_TOUT95	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO5	O3		**Master slave select output**
	QSPI1_SLSO5	O4		**Master slave select output**
	MSC0_EN1	O5		**Chip Select**
	GETH_TXD1	O6		**Transmit Data**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**

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Table 2-58 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P11.3	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN2_2			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_2			**Mux input channel 2 of TIM module 2**
	MSC0_SDI3			**Upstream assynchronous input signal**
	QSPI1_MRSTB			**Master SPI data input**
	P11.3	O0		**General-purpose output**
	GTM_TOUT96	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MRST	O3		**Slave SPI data output**
	IOM_MON2_1			**Monitor input 2**
	IOM_REF2_1			**Reference input 2**
	ERAY0_TXDA	O4		**Transmit Channel A**
	—	O5		**Reserved**
	GETH_TXD0	O6		**Transmit Data**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**
134	P11.6	I	RFAST / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN3_2			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_2			**Mux input channel 3 of TIM module 2**
	QSPI1_SCLKB			**Slave SPI clock inputs**
	P11.6	O0		**General-purpose output**
	GTM_TOUT97	O1		**GTM muxed output**
	ERAY0_TXENB	O2		**Transmit Enable Channel B**
	QSPI1_SCLK	O3		**Master SPI clock output**
	ERAY0_TXENA	O4		**Transmit Enable Channel A**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	GETH_TXEN	O6		**Transmit Enable MII and RMII**
	GETH_TCTL			**Transmit Control for RGMII**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-58 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P11.9	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN4_2			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_2			**Mux input channel 4 of TIM module 2**
	QSPI1_MTSRB			**Slave SPI data input**
	ERAY0_RXDA1			**Receive Channel A1**
	GETH_RXD1A			**Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)**
	P11.9	O0		**General-purpose output**
	GTM_TOUT98	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI1_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**

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Table 2-58 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
137	P11.10	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN5_2			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_2			**Mux input channel 5 of TIM module 2**
	GTM_TIM2_IN0_9			**Mux input channel 0 of TIM module 2**
	CAN03_RXDD			**CAN receive input node 3**
	ERAY0_RXDB1			**Receive Channel B1**
	ASCLIN1_ARXE			**Receive input**
	SCU_E_REQ6_3			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	MSC0_SDI0			**Upstream assynchronous input signal**
	GETH_RXD0A			**Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)**
	QSPI1_SLSIA			**Slave select input**
	P11.10	O0		**General-purpose output**
	GTM_TOUT99	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO3	O3		**Master slave select output**
	QSPI1_SLSO3	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-58 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P11.11	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN6_2			**Mux input channel 6 of TIM module 3**
	GTM_TIM3_IN0_14			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN6_2			**Mux input channel 6 of TIM module 2**
	GETH_CRSDVA			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH_RXDVA			**Receive Data Valid MII**
	GETH_CRSB			**Carrier Sense MII**
	GETH_RCTLA			**Receive Control for RGMII**
	P11.11	O0		**General-purpose output**
	GTM_TOUT100	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO4	O3		**Master slave select output**
	QSPI1_SLSO4	O4		**Master slave select output**
	MSC0_EN0	O5		**Chip Select**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
139	P11.12	I	FAST / RGMII_Input / PU1 / VFLEX / ES	**General-purpose input**
	GTM_TIM3_IN7_2			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_2			**Mux input channel 7 of TIM module 2**
	GETH_REFCLKA			**Reference Clock input for RMII (50 MHz)**
	GETH_TXCLKB			**Transmit Clock Input for MII**
	GETH_RXCLKA			**Receive Clock MII**
	P11.12	O0		**General-purpose output**
	GTM_TOUT101	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	GTM_CLK2	O3		**CGM generated clock**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-59 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
128	P13.0	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN5_3			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_3			**Mux input channel 5 of TIM module 2**
	ASCLIN10_ARXC			**Receive input**
	P13.0	O0		**General-purpose output**
	GTM_TOUT91	O1		**GTM muxed output**
	ASCLIN10_ATX	O2		**Transmit output**
	QSPI2_SCLKN	O3		**Master SPI clock output (LVDS N line)**
	MSC0_EN1	O4		**Chip Select**
	MSC0_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	CAN10_TXD	O7		**CAN transmit output node 0**
129	P13.1	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN6_3			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_3			**Mux input channel 6 of TIM module 2**
	I2C0_SCLB			**Serial Clock Input 1**
	CAN10_RXDD			**CAN receive input node 0**
	ASCLIN10_ARXD			**Receive input**
	P13.1	O0		**General-purpose output**
	GTM_TOUT92	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLKP	O3		**Master SPI clock output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_FCLP	O5		**Shift-clock direct part of the differential signal**
	I2C0_SCL	O6		**Serial Clock Output**
	—	O7		**Reserved**

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Table 2-59 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
130	P13.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN7_3			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_3			**Mux input channel 7 of TIM module 2**
	GPT120_CAPINA			**Trigger input to capture value of timer T5 into CAPREL register**
	I2C0_SDAB			**Serial Data Input 1**
	P13.2	O0		**General-purpose output**
	GTM_TOUT93	O1		**GTM muxed output**
	ASCLIN10_ASCLK	O2		**Shift clock output**
	QSPI2_MTSRN	O3		**Master SPI data output (LVDS N line)**
	MSC0_FCLP	O4		**Shift-clock direct part of the differential signal**
	MSC0_SON	O5		**Data output - inverted part of the differential signal**
	I2C0_SDA	O6		**Serial Data Output**
	—	O7		**Reserved**
131	P13.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM3_IN0_3			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_3			**Mux input channel 0 of TIM module 2**
	P13.3	O0		**General-purpose output**
	GTM_TOUT94	O1		**GTM muxed output**
	ASCLIN10_ASLSO	O2		**Slave select signal output**
	QSPI2_MTSRP	O3		**Master SPI data output (LVDS P line)**
	—	O4		**Reserved**
	MSC0_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-60 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P14.0	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN3_5			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_5			**Mux input channel 3 of TIM module 0**
	P14.0	O0		**General-purpose output**
	GTM_TOUT80	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	ERAY0_TXDA	O3		**Transmit Channel A**
	ERAY0_TXDB	O4		**Transmit Channel B**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	CCU60_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_5			**Monitor input 1**
	IOM_REF1_1			**Reference input 1**

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Table 2-60 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P14.1	I	FAST / PU1 / VEXT / ES2	**General-purpose input**
	GTM_TIM1_IN4_3			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_3			**Mux input channel 4 of TIM module 0**
	ERAY0_RXDA3			**Receive Channel A3**
	ASCLIN0_ARXA			**Receive input**
	ERAY0_RXDB3			**Receive Channel B3**
	CAN01_RXDB			**CAN receive input node 1**
	SCU_E_REQ3_1			**ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	PMS_PINAWKP			**PINA (P14.1) pin input**
	P14.1	O0		**General-purpose output**
	GTM_TOUT81	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
120	P14.2	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_3			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_3			**Mux input channel 5 of TIM module 0**
	PMS_HWCFG2IN			**HWCFG2 pin input**
	P14.2	O0		**General-purpose output**
	GTM_TOUT82	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO1	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN2_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**

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Table 2-60 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
121	P14.3	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_3			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_3			**Mux input channel 6 of TIM module 0**
	PMS_HWCFG3IN			**HWCFG3 pin input**
	ASCLIN2_ARXA			**Receive input**
	MSC0_SDI2			**Upstream assynchronous input signal**
	SCU_E_REQ1_0			**ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P14.3	O0		**General-purpose output**
	GTM_TOUT83	O1		**GTM muxed output**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI2_SLSO3	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	ASCLIN3_ASLSO	O5		**Slave select signal output**
	—	O6		**Reserved**
	—	O7		**Reserved**
122	P14.4	I	SLOW / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_2			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_2			**Mux input channel 7 of TIM module 0**
	PMS_HWCFG6IN			**HWCFG6 pin input**
	GTM_DTMT0_0			**CDTM0_DTM0**
	P14.4	O0		**General-purpose output**
	GTM_TOUT84	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	GETH_PPS	O6		**Pulse Per Second**
	—	O7		**Reserved**

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Table 2-60 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
123	P14.5	I	FAST / PU2 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN0_4			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_4			**Mux input channel 0 of TIM module 0**
	PMS_HWCFG1IN			**HWCFG1 pin input**
	GTM_DTMA2_0			**CDTM2_DTM4**
	P14.5	O0		**General-purpose output**
	GTM_TOUT85	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ERAY0_TXDB	O6		**Transmit Channel B**
	—	O7		**Reserved**
124	P14.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_4			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_4			**Mux input channel 1 of TIM module 0**
	P14.6	O0		**General-purpose output**
	GTM_TOUT86	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SLSO2	O3		**Master slave select output**
	CAN13_TXD	O4		**CAN transmit output node 3**
	—	O5		**Reserved**
	ERAY0_TXENB	O6		**Transmit Enable Channel B**
	—	O7		**Reserved**

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Table 2-61 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P15.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN3_4			**Mux input channel 3 of TIM module 3**
	GTM_TIM2_IN3_4			**Mux input channel 3 of TIM module 2**
	SDMMC0_DAT7_IN			**read data in**
	P15.0	O0		**General-purpose output**
	GTM_TOUT71	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO13	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN02_TXD	O5		**CAN transmit output node 2**
	IOM_MON2_7			**Monitor input 2**
	IOM_REF2_7			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
	SDMMC0_DAT7	O		**write data out**
110	P15.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN4_4			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_4			**Mux input channel 4 of TIM module 2**
	CAN02_RXDA			**CAN receive input node 2**
	ASCLIN1_ARXA			**Receive input**
	QSPI2_SLSIB			**Slave select input**
	SCU_E_REQ7_2			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.1	O0		**General-purpose output**
	GTM_TOUT72	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_SLSO5	O3		**Master slave select output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	SDMMC0_CLK	O7		**card clock**

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Table 2-61 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P15.2	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_4			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_4			**Mux input channel 5 of TIM module 2**
	QSPI2_SLSIA			**Slave select input**
	SENT_SENT10D			**Receive input channel 10**
	QSPI2_MRSTE			**Master SPI data input**
	P15.2	O0		**General-purpose output**
	GTM_TOUT73	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SLSO0	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ASCLK	O6		**Shift clock output**
	—	O7		**Reserved**
112	P15.3	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_4			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_4			**Mux input channel 6 of TIM module 2**
	CAN01_RXDA			**CAN receive input node 1**
	ASCLIN0_ARXB			**Receive input**
	QSPI2_SCLKA			**Slave SPI clock inputs**
	SDMMC0_CMD_IN			**command in**
	P15.3	O0		**General-purpose output**
	GTM_TOUT74	O1		**GTM muxed output**
	ASCLIN0_ATX	O2		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	MSC0_EN1	O5		**Chip Select**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_CMD	O		**command out**

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Table 2-61 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
113	P15.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_4			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_4			**Mux input channel 7 of TIM module 2**
	I2C0_SCLC			**Serial Clock Input 2**
	QSPI2_MRSTA			**Master SPI data input**
	SCU_E_REQ0_0			**ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT11D			**Receive input channel 11**
	P15.4	O0		**General-purpose output**
	GTM_TOUT75	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	I2C0_SCL	O6		**Serial Clock Output**
	CCU60_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_0			**Monitor input 1**
	IOM_REF1_4			**Reference input 1**

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Table 2-61 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
114	P15.5	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_4			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_4			**Mux input channel 0 of TIM module 2**
	ASCLIN1_ARXB			**Receive input**
	I2C0_SDAC			**Serial Data Input 2**
	QSPI2_MTSRA			**Slave SPI data input**
	SCU_E_REQ4_3			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.5	O0		**General-purpose output**
	GTM_TOUT76	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	MSC0_EN0	O5		**Chip Select**
	I2C0_SDA	O6		**Serial Data Output**
	CCU60_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_1			**Monitor input 1**
	IOM_REF1_5			**Reference input 1**
115	P15.6	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM2_IN2_14			**Mux input channel 2 of TIM module 2**
	GTM_TIM1_IN0_6			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_6			**Mux input channel 0 of TIM module 0**
	QSPI2_MTSRB			**Slave SPI data input**
	P15.6	O0		**General-purpose output**
	GTM_TOUT77	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	QSPI2_SCLK	O5		**Master SPI clock output**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_2			**Monitor input 1**
	IOM_REF1_6			**Reference input 1**

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Table 2-61 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
116	P15.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN1_5			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_5			**Mux input channel 1 of TIM module 0**
	ASCLIN3_ARXA			**Receive input**
	QSPI2_MRSTB			**Master SPI data input**
	P15.7	O0		**General-purpose output**
	GTM_TOUT78	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI2_MRST	O3		**Slave SPI data output**
	IOM_MON2_2			**Monitor input 2**
	IOM_REF2_2			**Reference input 2**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU60_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_3			**Monitor input 1**
	IOM_REF1_3			**Reference input 1**
117	P15.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN2_5			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_5			**Mux input channel 2 of TIM module 0**
	QSPI2_SCLKB			**Slave SPI clock inputs**
	SCU_E_REQ5_0			**ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P15.8	O0		**General-purpose output**
	GTM_TOUT79	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI2_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	ASCLIN3_ASCLK	O6		**Shift clock output**
	CCU60_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_4			**Monitor input 1**
	IOM_REF1_2			**Reference input 1**

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Table 2-62 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P20.0	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_7			**Mux input channel 6 of TIM module 1**
	GTM_TIM1_IN4_9			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN6_7			**Mux input channel 6 of TIM module 0**
	CAN03_RXDC			**CAN receive input node 3**
	CCU_PAD_SYSCLK			**Sysclk input**
	CAN21_RXDC			**CAN receive input node 1**
	CBS_TGI0			**Trigger input**
	SCU_E_REQ6_0			**ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	GPT120_T6EUDA			**Count direction control input of core timer T6**
	P20.0	O0		**General-purpose output**
	GTM_TOUT59	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	HSCT0_SYSCLK_OUT	O5		**sys clock output**
	—	O6		**Reserved**
	—	O7		**Reserved**
	CBS_TGO0	O		**Trigger output**
94	P20.2	I	S / PU / VEXT	**General-purpose input** This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			**Testmode Enable Input**

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Table 2-62 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P20.3	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM4_IN5_11			**Mux input channel 5 of TIM module 4**
	GTM_TIM3_IN4_5			**Mux input channel 4 of TIM module 3**
	GTM_TIM2_IN4_5			**Mux input channel 4 of TIM module 2**
	ASCLIN3_ARXC			**Receive input**
	GPT120_T6INA			**Trigger/gate input of core timer T6**
	P20.3	O0		**General-purpose output**
	GTM_TOUT61	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	QSPI0_SLSO9	O3		**Master slave select output**
	QSPI2_SLSO9	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	CAN21_TXD	O6		**CAN transmit output node 1**
	—	O7		**Reserved**
100	P20.6	I	SLOW / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_5			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_5			**Mux input channel 6 of TIM module 2**
	CAN12_RXDA			**CAN receive input node 2**
	ASCLIN9_ARXE			**Receive input**
	P20.6	O0		**General-purpose output**
	GTM_TOUT62	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI0_SLSO8	O3		**Master slave select output**
	QSPI2_SLSO8	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-62 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
101	P20.7	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_5			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_5			**Mux input channel 7 of TIM module 2**
	GTM_TIM1_IN5_8			**Mux input channel 5 of TIM module 1**
	CAN00_RXDB			**CAN receive input node 0**
	ASCLIN1_ACTSA			**Clear to send input**
	ASCLIN9_ARXF			**Receive input**
	SDMMC0_DAT0_IN			**read data in**
	P20.7	O0		**General-purpose output**
	GTM_TOUT63	O1		**GTM muxed output**
	ASCLIN9_ATX	O2		**Transmit output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	CAN12_TXD	O5		**CAN transmit output node 2**
	—	O6		**Reserved**
	CCU61_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_7			**Monitor input 1**
	IOM_REF1_7			**Reference input 1**
	SDMMC0_DAT0	O		**write data out**
102	P20.8	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN7_3			**Mux input channel 7 of TIM module 1**
	GTM_TIM0_IN7_3			**Mux input channel 7 of TIM module 0**
	SDMMC0_DAT1_IN			**read data in**
	P20.8	O0		**General-purpose output**
	GTM_TOUT64	O1		**GTM muxed output**
	ASCLIN1_ASLSO	O2		**Slave select signal output**
	QSPI0_SLSO0	O3		**Master slave select output**
	QSPI1_SLSO0	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**
	SDMMC0_DAT1	O		**write data out**

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Table 2-62 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
103	P20.9	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN5_5			**Mux input channel 5 of TIM module 3**
	GTM_TIM2_IN5_5			**Mux input channel 5 of TIM module 2**
	CAN03_RXDE			**CAN receive input node 3**
	ASCLIN1_ARXC			**Receive input**
	QSPI0_SLSIB			**Slave select input**
	SCU_E_REQ7_0			**ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	P20.9	O0		**General-purpose output**
	GTM_TOUT65	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SLSO1	O3		**Master slave select output**
	QSPI1_SLSO1	O4		**Master slave select output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**
104	P20.10	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN6_6			**Mux input channel 6 of TIM module 3**
	GTM_TIM2_IN6_6			**Mux input channel 6 of TIM module 2**
	SDMMC0_DAT2_IN			**read data in**
	P20.10	O0		**General-purpose output**
	GTM_TOUT66	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI0_SLSO6	O3		**Master slave select output**
	QSPI2_SLSO7	O4		**Master slave select output**
	CAN03_TXD	O5		**CAN transmit output node 3**
	IOM_MON2_8			**Monitor input 2**
	IOM_REF2_8			**Reference input 2**
	ASCLIN1_ASCLK	O6		**Shift clock output**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**
	SDMMC0_DAT2	O		**write data out**

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Table 2-62 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P20.11	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN7_6			**Mux input channel 7 of TIM module 3**
	GTM_TIM2_IN7_6			**Mux input channel 7 of TIM module 2**
	QSPI0_SCLKA			**Slave SPI clock inputs**
	SDMMC0_DAT3_IN			**read data in**
	P20.11	O0		**General-purpose output**
	GTM_TOUT67	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI0_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**
	SDMMC0_DAT3	O		**write data out**
106	P20.12	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN0_5			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_5			**Mux input channel 0 of TIM module 2**
	QSPI0_MRSTA			**Master SPI data input**
	SDMMC0_DAT4_IN			**read data in**
	IOM_PIN_13			**GPIO pad input to FPC**
	P20.12	O0		**General-purpose output**
	GTM_TOUT68	O1		**GTM muxed output**
	IOM_MON0_13			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MRST	O3		**Slave SPI data output**
	IOM_MON2_0			**Monitor input 2**
	IOM_REF2_0			**Reference input 2**
	QSPI0_MTSR	O4		**Master SPI data output**
	—	O5		**Reserved**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SDMMC0_DAT4	O		**write data out**

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Table 2-62 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P20.13	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN1_4			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_4			**Mux input channel 1 of TIM module 2**
	QSPI0_SLSIA			**Slave select input**
	SDMMC0_DAT5_IN			**read data in**
	IOM_PIN_14			**GPIO pad input to FPC**
	P20.13	O0		**General-purpose output**
	GTM_TOUT69	O1		**GTM muxed output**
	IOM_MON0_14			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_SLSO2	O3		**Master slave select output**
	QSPI1_SLSO2	O4		**Master slave select output**
	QSPI0_SCLK	O5		**Master SPI clock output**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SDMMC0_DAT5	O		**write data out**
108	P20.14	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM3_IN2_4			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_4			**Mux input channel 2 of TIM module 2**
	QSPI0_MTSRA			**Slave SPI data input**
	SDMMC0_DAT6_IN			**read data in**
	IOM_PIN_15			**GPIO pad input to FPC**
	DMU_FDEST			**Enter destructive debug mode**
	P20.14	O0		**General-purpose output**
	GTM_TOUT70	O1		**GTM muxed output**
	IOM_MON0_15			**Monitor input 0**
	—	O2		**Reserved**
	QSPI0_MTSR	O3		**Master SPI data output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	SDMMC0_DAT6	O		**write data out**

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Table 2-63 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
84	P21.2	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN4_11			**Mux input channel 4 of TIM module 5**
	GTM_TIM1_IN0_7			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_7			**Mux input channel 0 of TIM module 0**
	QSPI2_MRSTCN			**Master SPI data input (LVDS N line)**
	SCU_EMGSTOP_PORT_B			**Emergency stop Port Pin B input request**
	ASCLIN3_ARXGN			**Differential Receive input (low active)**
	HSCT0_RXDN			**Rx data**
	QSPI4_MRSTCN			**Master SPI data input (LVDS N line)**
	ASCLIN11_ARXE			**Receive input**
	GTM_DTMA1_0			**CDTM1_DTM4**
	P21.2	O0		**General-purpose output**
	GTM_TOUT53	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	GETH_MDC	O5		**MDIO clock**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-63 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
85	P21.3	I	LVDS_RX / FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM5_IN5_12			**Mux input channel 5 of TIM module 5**
	GTM_TIM1_IN1_6			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_6			**Mux input channel 1 of TIM module 0**
	QSPI2_MRSTCP			**Master SPI data input (LVDS P line)**
	ASCLIN3_ARXGP			**Differential Receive input (high active)**
	GETH_MDIOD			**MDIO Input**
	HSCT0_RXDP			**Rx data**
	QSPI4_MRSTCP			**Master SPI data input (LVDS P line)**
	P21.3	O0		**General-purpose output**
	GTM_TOUT54	O1		**GTM muxed output**
	ASCLIN11_ASCLK	O2		**Shift clock output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	GETH_MDIO	O		**MDIO Output**
86	P21.4	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN6_12			**Mux input channel 6 of TIM module 5**
	GTM_TIM1_IN2_6			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_6			**Mux input channel 2 of TIM module 0**
	P21.4	O0		**General-purpose output**
	GTM_TOUT55	O1		**GTM muxed output**
	ASCLIN11_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDN	O		**Tx data**

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Table 2-63 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
87	P21.5	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM5_IN7_11			**Mux input channel 7 of TIM module 5**
	GTM_TIM1_IN3_6			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_6			**Mux input channel 3 of TIM module 0**
	ASCLIN11_ARXF			**Receive input**
	P21.5	O0		**General-purpose output**
	GTM_TOUT56	O1		**GTM muxed output**
	ASCLIN3_ASCLK	O2		**Shift clock output**
	ASCLIN11_ATX	O3		**Transmit output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
	HSCT0_TXDP	O		**Tx data**
88	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	**General-purpose input** PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
	GTM_TIM4_IN2_12			**Mux input channel 2 of TIM module 4**
	GTM_TIM1_IN4_8			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_8			**Mux input channel 4 of TIM module 0**
	GPT120_T5EUDA			**Count direction control input of timer T5**
	ASCLIN3_ARXF			**Receive input**
	CBS_TGI2			**Trigger input**
	TDI			**JTAG Module Data Input**
	P21.6	O0		**General-purpose output**
	GTM_TOUT57	O1		**GTM muxed output**
	ASCLIN3_ASLSO	O2		**Slave select signal output**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T3OUT	O7		**External output for overflow/underflow detection of core timer T3**
	CBS_TGO2	O		**Trigger output**
	DAP3	I/O		**DAP: DAP3 Data I/O**
	DAPE1	I/O		**DAPE: DAPE1 Data I/O**

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Table 2-63 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
90	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	**General-purpose input** DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
	GTM_TIM4_IN3_12			**Mux input channel 3 of TIM module 4**
	GTM_TIM1_IN5_7			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_7			**Mux input channel 5 of TIM module 0**
	GPT120_T5INA			**Trigger/gate input of timer T5**
	CBS_TGI3			**Trigger input**
	GETH_RXERB			**Receive Error MII**
	P21.7	O0		**General-purpose output**
	GTM_TOUT58	O1		**GTM muxed output**
	ASCLIN3_ATX	O2		**Transmit output**
	IOM_MON2_15			**Monitor input 2**
	IOM_REF2_15			**Reference input 2**
	ASCLIN3_ASCLK	O3		**Shift clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	GPT120_T6OUT	O7		**External output for overflow/underflow detection of core timer T6**
	CBS_TGO3	O		**Trigger output**
	DAP2	I/O		**DAP: DAP2 Data I/O**
	DAPE2	I/O		**DAPE: DAPE2 Data I/O**
	TDO	O		**JTAG Module Data Output**

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Table 2-64 Port 22 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P22.0	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	**General-purpose input**
	GTM_TIM1_IN1_7			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_7			**Mux input channel 1 of TIM module 0**
	QSPI4_MTSRB			**Slave SPI data input**
	ASCLIN6_ARXE			**Receive input**
	GETH1_CRSDVB			**Carrier Sense / Data Valid combi-signal for RMII**
	GETH1_RXDVB			**Receive Data Valid MII**
	GETH1_CRSA			**Carrier Sense MII**
	P22.0	O0		**General-purpose output**
	GTM_TOUT47	O1		**GTM muxed output**
	ASCLIN3_ATXN	O2		**Differential Transmit output (low active)**
	QSPI4_MTSR	O3		**Master SPI data output**
	QSPI4_SCLKN	O4		**Master SPI clock output (LVDS N line)**
	MSC1_FCLN	O5		**Shift-clock inverted part of the differential signal**
	—	O6		**Reserved**
	ASCLIN6_ATX	O7		**Transmit output**
75	P22.1	I	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	**General-purpose input**
	GTM_TIM1_IN0_8			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_8			**Mux input channel 0 of TIM module 0**
	QSPI4_MRSTB			**Master SPI data input**
	ASCLIN7_ARXE			**Receive input**
	GETH1_RXERA			**Receive Error MII**
	P22.1	O0		**General-purpose output**
	GTM_TOUT48	O1		**GTM muxed output**
	ASCLIN3_ATXP	O2		**Differential Transmit output (high active)**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI4_SCLKP	O4		**Master SPI clock output (LVDS P line)**
	MSC1_FCLP	O5		**Shift-clock direct part of the differential signal**
	—	O6		**Reserved**
	ASCLIN7_ATX	O7		**Transmit output**

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Table 2-64 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P22.2	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN3_7			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_7			**Mux input channel 3 of TIM module 0**
	QSPI4_SLSIB			**Slave select input**
	GETH1_COLA			**Collision MII**
	P22.2	O0		**General-purpose output**
	GTM_TOUT49	O1		**GTM muxed output**
	ASCLIN5_ATX	O2		**Transmit output**
	QSPI4_SLSO3	O3		**Master slave select output**
	QSPI4_MTSRN	O4		**Master SPI data output (LVDS N line)**
	MSC1_SON	O5		**Data output - inverted part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**
77	P22.3	I	LVDS_TX / FAST / PU1 / VEXT / ES6	**General-purpose input**
	GTM_TIM1_IN4_4			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_4			**Mux input channel 4 of TIM module 0**
	QSPI4_SCLKB			**Slave SPI clock inputs**
	ASCLIN5_ARXC			**Receive input**
	P22.3	O0		**General-purpose output**
	GTM_TOUT50	O1		**GTM muxed output**
	—	O2		**Reserved**
	QSPI4_SCLK	O3		**Master SPI clock output**
	QSPI4_MTSRP	O4		**Master SPI data output (LVDS P line)**
	MSC1_SOP	O5		**Data output - direct part of the differential signal**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-65 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P23.1	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN6_4			**Mux input channel 6 of TIM module 1**
	GTM_TIM0_IN6_4			**Mux input channel 6 of TIM module 0**
	MSC1_SDI0			**Upstream assynchronous input signal**
	ASCLIN6_ARXF			**Receive input**
	P23.1	O0		**General-purpose output**
	GTM_TOUT42	O1		**GTM muxed output**
	ASCLIN1_ARTS	O2		**Ready to send output**
	QSPI4_SLSO6	O3		**Master slave select output**
	GTM_CLK0	O4		**CGM generated clock**
	CAN10_TXD	O5		**CAN transmit output node 0**
	CCU_EXTCLK0	O6		**External Clock 0**
	ASCLIN6_ASCLK	O7		**Shift clock output**

Table 2-66 Port 32 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
70	P32.0	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
	GTM_TIM3_IN2_5			**Mux input channel 2 of TIM module 3**
	GTM_TIM2_IN2_5			**Mux input channel 2 of TIM module 2**
	P32.0	O0		**General-purpose output**
	GTM_TOUT36	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**

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Table 2-66 Port 32 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
71	P32.1	I	SLOW / PU1 / VEXT / ES	**General-purpose input** P32.1 / External Pass Device gate control for EVRC
	GTM_TIM3_IN3_15			**Mux input channel 3 of TIM module 3**
	P32.1	O0		**General-purpose output**
	GTM_TOUT37	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	—	O4		**Reserved**
	—	O5		**Reserved**
	—	O6		**Reserved**
	—	O7		**Reserved**
72	P32.4	I	FAST / PU1 / VEXT / ES	**General-purpose input**
	GTM_TIM1_IN5_5			**Mux input channel 5 of TIM module 1**
	GTM_TIM0_IN5_5			**Mux input channel 5 of TIM module 0**
	ASCLIN1_ACTSB			**Clear to send input**
	MSC1_SDI2			**Upstream assynchronous input signal**
	P32.4	O0		**General-purpose output**
	GTM_TOUT40	O1		**GTM muxed output**
	—	O2		**Reserved**
	—	O3		**Reserved**
	GTM_CLK1	O4		**CGM generated clock**
	MSC1_EN0	O5		**Chip Select**
	CCU_EXTCLK1	O6		**External Clock 1**
	CCU60_COUT63	O7		**T13 PWM channel 63**
	IOM_MON1_6			**Monitor input 1**
	IOM_REF1_0			**Reference input 1**
	PMS_DCDCSYNCO	O		**DC-DC synchronization output**

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Table 2-67 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
60	P33.4	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_10			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_10			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_10			**Mux input channel 0 of TIM module 0**
	EDSADC_ITR0F			**Trigger/Gate input, channel 0**
	SENT_SENT6C			**Receive input channel 6**
	EDSADC_DSDIN1B			**Digital datastream input, channel 1**
	CCU61_CTRAPC			**Trap input capture**
	ASCLIN5_ARXB			**Receive input**
	IOM_PIN_4			**GPIO pad input to FPC**
	GTM_DTMT2_0			**CDTM2_DTM0**
	EVADC_G10CH3	AI		**Analog input channel 3, group 10**
	P33.4	O0		**General-purpose output**
	GTM_TOUT26	O1		**GTM muxed output**
	IOM_MON0_4			**Monitor input 0**
	IOM_GTM_4			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ARTS	O2		**Ready to send output**
	QSPI2_SLSO12	O3		**Master slave select output**
	PSI5_TX1	O4		**TXD outputs (send data)**
	IOM_MON1_15			**Monitor input 1**
	EVADC_EMUX12	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC0BFLOUT	O6		**Boundary flag output, FC channel 0**
	CAN13_TXD	O7		**CAN transmit output node 3**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P33.5	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN5_10			**Mux input channel 5 of TIM module 4**
	GTM_TIM1_IN1_8			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_8			**Mux input channel 1 of TIM module 0**
	EDSADC_DSCIN0B			**Modulator clock input, channel 0**
	EDSADC_ITR1F			**Trigger/Gate input, channel 1**
	GPT120_T4EUDB			**Count direction control input of timer T4**
	PSI5S_RXC			**RX data input**
	ASCLIN2_ACTSB			**Clear to send input**
	CCU61_CCPOS2C			**Hall capture input 2**
	SENT_SENT5C			**Receive input channel 5**
	CAN13_RXDB			**CAN receive input node 3**
	IOM_PIN_5			**GPIO pad input to FPC**
	EVADC_G10CH2	AI		**Analog input channel 2, group 10**
	P33.5	O0		**General-purpose output**
	GTM_TOUT27	O1		**GTM muxed output**
	IOM_MON0_5			**Monitor input 0**
	IOM_GTM_5			**GTM-provided inputs to EXOR combiner**
	QSPI0_SLSO7	O2		**Master slave select output**
	QSPI1_SLSO7	O3		**Master slave select output**
	EDSADC_DSCOUT0	O4		**Modulator clock output**
	EVADC_EMUX11	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC2BFLOUT	O6		**Boundary flag output, FC channel 2**
	ASCLIN5_ASLSO	O7		**Slave select signal output**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
62	P33.6	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_9			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_9			**Mux input channel 2 of TIM module 0**
	EDSADC_ITR2F			**Trigger/Gate input, channel 2**
	GPT120_T2EUDB			**Count direction control input of timer T2**
	SENT_SENT4C			**Receive input channel 4**
	CCU61_CCPOS1C			**Hall capture input 1**
	EDSADC_DSDIN0B			**Digital datastream input, channel 0**
	ASCLIN8_ARXD			**Receive input**
	IOM_PIN_6			**GPIO pad input to FPC**
	GTM_DTMT2_1			**CDTM2_DTM0**
	EVADC_G10CH1	AI		**Analog input channel 1, group 10**
	P33.6	O0		**General-purpose output**
	GTM_TOUT28	O1		**GTM muxed output**
	IOM_MON0_6			**Monitor input 0**
	IOM_GTM_6			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASLSO	O2		**Slave select signal output**
	QSPI2_SLSO11	O3		**Master slave select output**
	—	O4		**Reserved**
	EVADC_EMUX10	O5		**Control of external analog multiplexer interface 1**
	EVADC_FC1BFLOUT	O6		**Boundary flag output, FC channel 1**
	PSI5S_TX	O7		**TX data output**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P33.7	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN3_9			**Mux input channel 3 of TIM module 1**
	GTM_TIM0_IN3_9			**Mux input channel 3 of TIM module 0**
	CAN00_RXDE			**CAN receive input node 0**
	GPT120_T2INB			**Trigger/gate input of timer T2**
	CCU61_CCPOS0C			**Hall capture input 0**
	SCU_E_REQ4_0			**ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)**
	SENT_SENT14C			**Receive input channel 14**
	IOM_PIN_7			**GPIO pad input to FPC**
	EVADC_G10CH0	AI		**Analog input channel 0, group 10**
	P33.7	O0		**General-purpose output**
	GTM_TOUT29	O1		**GTM muxed output**
	IOM_MON0_7			**Monitor input 0**
	IOM_GTM_7			**GTM-provided inputs to EXOR combiner**
	ASCLIN2_ASCLK	O2		**Shift clock output**
	QSPI4_SLSO7	O3		**Master slave select output**
	ASCLIN8_ATX	O4		**Transmit output**
	—	O5		**Reserved**
	EVADC_FC3BFLOUT	O6		**Boundary flag output, FC channel 3**
	—	O7		**Reserved**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P33.8	I	FAST / HighZ / VEVRSB	**General-purpose input**
	GTM_TIM1_IN4_7			**Mux input channel 4 of TIM module 1**
	GTM_TIM0_IN4_7			**Mux input channel 4 of TIM module 0**
	ASCLIN2_ARXE			**Receive input**
	SCU_EMGSTOP_PORT_A			**Emergency stop Port Pin A input request**
	IOM_PIN_8			**GPIO pad input to FPC**
	P33.8	O0		**General-purpose output**
	GTM_TOUT30	O1		**GTM muxed output**
	IOM_MON0_8			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO2	O3		**Master slave select output**
	—	O4		**Reserved**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_COUT62	O7		**T12 PWM channel 62**
	IOM_MON1_13			**Monitor input 1**
	IOM_REF1_8			**Reference input 1**
	SMU_FSP0	O		**FSP[1..0] Output Signals - Generated by SMU_core**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P33.9	I	SLOW / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN1_9			**Mux input channel 1 of TIM module 1**
	GTM_TIM0_IN1_9			**Mux input channel 1 of TIM module 0**
	IOM_PIN_9			**GPIO pad input to FPC**
	P33.9	O0		**General-purpose output**
	GTM_TOUT31	O1		**GTM muxed output**
	IOM_MON0_9			**Monitor input 0**
	ASCLIN2_ATX	O2		**Transmit output**
	IOM_MON2_14			**Monitor input 2**
	IOM_REF2_14			**Reference input 2**
	QSPI4_SLSO1	O3		**Master slave select output**
	ASCLIN2_ASCLK	O4		**Shift clock output**
	CAN01_TXD	O5		**CAN transmit output node 1**
	IOM_MON2_6			**Monitor input 2**
	IOM_REF2_6			**Reference input 2**
	ASCLIN0_ATX	O6		**Transmit output**
	IOM_MON2_12			**Monitor input 2**
	IOM_REF2_12			**Reference input 2**
	CCU61_CC62	O7		**T12 PWM channel 62**
	IOM_MON1_10			**Monitor input 1**
	IOM_REF1_11			**Reference input 1**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P33.10	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM4_IN4_14			**Mux input channel 4 of TIM module 4**
	GTM_TIM1_IN0_9			**Mux input channel 0 of TIM module 1**
	GTM_TIM0_IN0_9			**Mux input channel 0 of TIM module 0**
	QSPI4_SLSIA			**Slave select input**
	CAN01_RXDD			**CAN receive input node 1**
	ASCLIN0_ARXD			**Receive input**
	IOM_PIN_10			**GPIO pad input to FPC**
	P33.10	O0		**General-purpose output**
	GTM_TOUT32	O1		**GTM muxed output**
	IOM_MON0_10			**Monitor input 0**
	QSPI1_SLSO6	O2		**Master slave select output**
	QSPI4_SLSO0	O3		**Master slave select output**
	ASCLIN1_ASLSO	O4		**Slave select signal output**
	PSI5S_CLK	O5		**PSI5S CLK is a clock that can be used on a pin to drive the external PHY.**
	—	O6		**Reserved**
	CCU61_COUT61	O7		**T12 PWM channel 61**
	IOM_MON1_12			**Monitor input 1**
	IOM_REF1_9			**Reference input 1**
	SMU_FSP1	O		**FSP[1..0] Output Signals - Generated by SMU_core**
67	P33.11	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM1_IN2_8			**Mux input channel 2 of TIM module 1**
	GTM_TIM0_IN2_8			**Mux input channel 2 of TIM module 0**
	QSPI4_SCLKA			**Slave SPI clock inputs**
	IOM_PIN_11			**GPIO pad input to FPC**
	P33.11	O0		**General-purpose output**
	GTM_TOUT33	O1		**GTM muxed output**
	IOM_MON0_11			**Monitor input 0**
	ASCLIN1_ASCLK	O2		**Shift clock output**
	QSPI4_SCLK	O3		**Master SPI clock output**
	—	O4		**Reserved**
	—	O5		**Reserved**
	EDSADC_CGPWMN	O6		**Negative carrier generator output**
	CCU61_CC61	O7		**T12 PWM channel 61**
	IOM_MON1_9			**Monitor input 1**
	IOM_REF1_12			**Reference input 1**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
68	P33.12	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN0_6			**Mux input channel 0 of TIM module 3**
	GTM_TIM2_IN0_6			**Mux input channel 0 of TIM module 2**
	QSPI4_MTSRA			**Slave SPI data input**
	CAN00_RXDD			**CAN receive input node 0**
	PMS_PINBWKP			**PINB (P33.12) pin input**
	IOM_PIN_12			**GPIO pad input to FPC**
	P33.12	O0		**General-purpose output**
	GTM_TOUT34	O1		**GTM muxed output**
	IOM_MON0_12			**Monitor input 0**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MTSR	O3		**Master SPI data output**
	ASCLIN1_ASCLK	O4		**Shift clock output**
	CAN22_TXD	O5		**CAN transmit output node 2**
	EDSADC_CGPWMP	O6		**Positive carrier generator output**
	CCU61_COUT60	O7		**T12 PWM channel 60**
	IOM_MON1_11			**Monitor input 1**
	IOM_REF1_10			**Reference input 1**

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Table 2-67 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
69	P33.13	I	FAST / PU1 / VEVRSB / ES5	**General-purpose input**
	GTM_TIM3_IN1_5			**Mux input channel 1 of TIM module 3**
	GTM_TIM2_IN1_5			**Mux input channel 1 of TIM module 2**
	ASCLIN1_ARXF			**Receive input**
	EDSADC_SGNB			**Carrier sign signal input**
	QSPI4_MRSTA			**Master SPI data input**
	MSC1_INJ1			**Injection signal from port**
	CAN22_RXDA			**CAN receive input node 2**
	P33.13	O0		**General-purpose output**
	GTM_TOUT35	O1		**GTM muxed output**
	ASCLIN1_ATX	O2		**Transmit output**
	IOM_MON2_13			**Monitor input 2**
	IOM_REF2_13			**Reference input 2**
	QSPI4_MRST	O3		**Slave SPI data output**
	IOM_MON2_4			**Monitor input 2**
	IOM_REF2_4			**Reference input 2**
	QSPI2_SLSO6	O4		**Master slave select output**
	CAN00_TXD	O5		**CAN transmit output node 0**
	IOM_MON2_5			**Monitor input 2**
	IOM_REF2_5			**Reference input 2**
	—	O6		**Reserved**
	CCU61_CC60	O7		**T12 PWM channel 60**
	IOM_MON1_8			**Monitor input 1**
	IOM_REF1_13			**Reference input 1**

Table 2-68 Analog Inputs

Pin	Symbol	Ctrl.	Buffer Type	Function
57	AN0	I	D / HighZ / VDDM	**Analog Input 0**
	EVADC_G0CH0			**Analog input channel 0, group 0**
	EDSADC_EDS3PA			**Positive analog input channel 3, pin A**
56	AN1	I	D / HighZ / VDDM	**Analog Input 1**
	EVADC_G0CH1			**Analog input channel 1, group 0**
	EDSADC_EDS3NA			**Negative analog input channel 3, pin A**
55	AN2	I	D / HighZ / VDDM	**Analog Input 2**
	EVADC_G0CH2			**Analog input channel 2, group 0**
	EDSADC_EDS0PA			**Positive analog input channel 0, pin A**

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Table 2-68 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
54	AN3	I	D / HighZ / VDDM	**Analog Input 3**
	EVADC_G0CH3			**Analog input channel 3, group 0**
	EDSADC_EDS0NA			**Negative analog input channel 0, pin A**
53	AN4	I	D / HighZ / VDDM	**Analog Input 4**
	EVADC_G11CH0			**Analog input channel 0, group 11**
	EVADC_G0CH4			**Analog input channel 4, group 0**
52	AN5	I	D / HighZ / VDDM	**Analog Input 5**
	EVADC_G11CH1			**Analog input channel 1, group 11**
	EVADC_G0CH5			**Analog input channel 5, group 0**
51	AN6	I	D / HighZ / VDDM	**Analog Input 6**
	EVADC_G11CH2			**Analog input channel 2, group 11**
	EVADC_G0CH6			**Analog input channel 6, group 0**
50	AN7	I	D / HighZ / VDDM	**Analog Input 7**
	EVADC_G11CH3			**Analog input channel 3, group 11**
	EVADC_G0CH7			**Analog input channel 7, group 0**
49	AN8	I	D / HighZ / VDDM	**Analog Input 8**
	EVADC_G11CH4			**Analog input channel 4, group 11**
	EVADC_G1CH0			**Analog input channel 0, group 1**
48	AN10	I	D / HighZ / VDDM	**Analog Input 10**
	EVADC_G11CH6			**Analog input channel 6, group 11**
	EVADC_G1CH2			**Analog input channel 2, group 1**
47	AN11	I	D / HighZ / VDDM	**Analog Input 11**
	EVADC_G11CH7			**Analog input channel 7, group 11**
	EVADC_G1CH3			**Analog input channel 3, group 1**
46	AN12	I	D / HighZ / VDDM	**Analog Input 12**
	EVADC_G1CH4			**Analog input channel 4, group 1**
	EDSADC_EDS0PB			**Positive analog input channel 0, pin B**
45	AN13	I	D / HighZ / VDDM	**Analog Input 13**
	EVADC_G1CH5			**Analog input channel 5, group 1**
	EDSADC_EDS0NB			**Negative analog input channel 0, pin B**
40	AN16	I	D / HighZ / VDDM	**Analog Input 16**
	EVADC_G2CH0			**Analog input channel 0, group 2**
	EVADC_FC0CH0			**Analog input FC channel 0**
39	AN17/P40.10	I	S / HighZ / VDDM	**Analog Input 17**
	SENT_SENT10A			**Receive input channel 10**
	EVADC_G2CH1			**Analog input channel 1, group 2**
	EVADC_FC1CH0			**Analog input FC channel 1**

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Table 2-68 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
38	AN20	I	D / HighZ / VDDM	**Analog Input 20**
	EVADC_G2CH4			**Analog input channel 4, group 2**
	EDSADC_EDS2PA			**Positive analog input channel 2, pin A**
37	AN21	I	D / HighZ / VDDM	**Analog Input 21**
	EVADC_G2CH5			**Analog input channel 5, group 2**
	EDSADC_EDS2NA			**Negative analog input channel 2, pin A**
36	AN24/P40.0	I	S / HighZ / VDDM	**Analog Input 24**
	SENT_SENT0A			**Receive input channel 0**
	EVADC_G3CH0			**Analog input channel 0, group 3**
	CCU60_CCPOS0D			**Hall capture input 0**
	EDSADC_EDS2PB			**Positive analog input channel 2, pin B**
35	AN25/P40.1	I	S / HighZ / VDDM	**Analog Input 25**
	SENT_SENT1A			**Receive input channel 1**
	EVADC_G3CH1			**Analog input channel 1, group 3**
	CCU60_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS2NB			**Negative analog input channel 2, pin B**
34	AN35	I	D / HighZ / VDDM	**Analog Input 35**
	EVADC_G8CH3			**Analog input channel 3, group 8**
	EVADC_G11CH15			**Analog input channel 15, group 11**
33	AN36/P40.6	I	S / HighZ / VDDM	**Analog Input 36**
	SENT_SENT6A			**Receive input channel 6**
	EVADC_G8CH4			**Analog input channel 4, group 8**
	CCU61_CCPOS1B			**Hall capture input 1**
	EDSADC_EDS1PA			**Positive analog input channel 1, pin A**
32	AN37/P40.7	I	S / HighZ / VDDM	**Analog Input 37**
	SENT_SENT7A			**Receive input channel 7**
	EVADC_G8CH5			**Analog input channel 5, group 8**
	CCU61_CCPOS1D			**Hall capture input 1**
	EDSADC_EDS1NA			**Negative analog input channel 1, pin A**
31	AN38/P40.8	I	S / HighZ / VDDM	**Analog Input 38**
	SENT_SENT8A			**Receive input channel 8**
	EVADC_G8CH6			**Analog input channel 6, group 8**
	CCU61_CCPOS2B			**Hall capture input 2**
	EDSADC_EDS1PB			**Positive analog input channel 1, pin B**

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Table 2-68 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
30	AN39/P40.9	I	S / HighZ / VDDM	**Analog Input 39**
	SENT_SENT9A			**Receive input channel 9**
	EVADC_G8CH7			**Analog input channel 7, group 8**
	CCU61_CCPOS2D			**Hall capture input 2**
	EDSADC_EDS1NB			**Negative analog input channel 1, pin B**
29	AN44	I	D / HighZ / VDDM	**Analog Input 44**
	EVADC_G8CH12			**Analog input channel 12, group 8**
	EDSADC_EDS1PC			**Positive analog input channel 1, pin C**
28	AN45	I	D / HighZ / VDDM	**Analog Input 45**
	EVADC_G8CH13			**Analog input channel 13, group 8**
	EDSADC_EDS1NC			**Negative analog input channel 1, pin C**
27	AN46	I	D / HighZ / VDDM	**Analog Input 46**
	EVADC_G8CH14			**Analog input channel 14, group 8**
	EDSADC_EDS1PD			**Positive analog input channel 1, pin D**
26	AN47	I	D / HighZ / VDDM	**Analog Input 47**
	EVADC_G8CH15			**Analog input channel 15, group 8**
	EDSADC_EDS1ND			**Negative analog input channel 1, pin D**

Note: Port Pins P32.0 and P32.1 are bidirectional pads and are having the following two functionalities implemented:

7. *In case the pins are used as standard GPIOs the functions defined in the pin configuration tables of P32.0 and P32.1 are available.*
8. *In case the pins are used as pre-drivers for external MOSFETs (internal DCDC usecase) P32.0 and P32.1 act as analog IOs named VGATE1N and VGATE1P.*

Table 2-69 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
70	VGATE1N	O	—	**DCDC N ch. MOSFET gate driver output** P32.0 / SMPS mode: analog output. External Pass Device gate control for EVRC
71	VGATE1P	O	—	**DCDC P ch. MOSFET gate driver output** P32.1 / External Pass Device gate control for EVRC
81	XTAL1	I	XTAL / VEXT	**XTAL pad1** XTAL1. Main Oscillator/PLL/Clock Generator Input.
82	XTAL2	O	XTAL / VEXT	**XTAL pad2** XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT

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Table 2-69 System I/O (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
89	TMS	I	FAST / PD2 / VEXT	**JTAG Module State Machine Control Input** TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.
	DAP1	I/O		**DAP: DAP1 Data I/O**
91	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	**JTAG Module Reset/Enable Input** TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
	DAPE0	I		**DAPE: DAPE0 Clock Input**
92	TCK	I	FAST / PD2 / VEXT	**JTAG Module Clock Input** TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
	DAP0	I		**DAP: DAP0 Clock Input**
96	$\overline{\text{ESR1}}$	I	FAST / PU1 / VEXT	**ESR1 Port Pin input - can be used to trigger a reset or an NMI** ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR1WKP	I		**ESR1 pin input**
97	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	**PORST pin** Power On Reset Input. Additional strong PD in case of power fail.
98	$\overline{\text{ESR0}}$	I	FAST / OD / VEXT	**ESR0 Port Pin input - can be used to trigger a reset or an NMI** ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
	PMS_ESR0WKP	I		**ESR0 pin input**

Table 2-70 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
136	VFLEX	I	—	**Digital Power Supply for Flex Port Pads (5V / 3.3V)**
44	VDDM	I	—	**ADC Analog Power Supply (5V / 3.3V)**
126	VDDP3	I	—	**Flash Power Supply (3.3V)**
42	VAREF1	I	—	**Positive Analog Reference Voltage 1**
24	VAREF2	I	—	**Positive Analog Reference Voltage 2**

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Table 2-70 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
10	VDDSB (VDD)	I	—	**Devices with integrated EMEM: EMEM SRAM Standby Power Supply, VDDSB (1.25V); Devices without integrated EMEM: VDD (1.25V)**
59	VEVRSB	I	—	**Standby Power Supply (5V / 3.3V) for the Standby SRAM**
125	VEXT	I	—	**External Power Supply (5V / 3.3V)**
23	VEXT	I	—	**External Power Supply (5V / 3.3V)**
78	VEXT	I	—	**External Power Supply (5V / 3.3V)**
127	VDD	I	—	**Digital Core Power Supply (1.25V)**
22	VDD	I	—	**Digital Core Power Supply (1.25V)**
58	VDD	I	—	**Digital Core Power Supply (1.25V)**
79	VDD	I	—	**Digital Core Power Supply (1.25V)**
99	VDD	I	—	**Digital Core Power Supply (1.25V)**
E-PAD	VSS	I	—	**Digital Ground (Exposed PAD), VSS**
43	VSSM	I	—	**Analog Ground for VDDM**
41	VAGND1	I	—	**Negative Analog Reference Voltage 1**
25	VAGND2	I	—	**Negative Analog Reference Voltage 2**
80	VSS	I	—	**Oscillator Ground, VSS(OSC)**
83	VEXT	I	—	**Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)**

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2.5 Sequence of Pads in Pad Frame

Table 2-71 Pad List

Number	Pad Name	Pad Type	X	Y	Comment
1	VEXT	Vx	255699	175644	Supply Voltage
2	VSS	Vx	356499	185148	Supply Voltage
3	VSS	Vx	457299	185148	Supply Voltage
4	VDD	Vx	507699	344106	Supply Voltage
5	P15.0	FAST / PU1 / VEXT / ES	558099	185148	General-purpose I/O
6	P15.1	FAST / PU1 / VEXT / ES	608499	344106	General-purpose I/O
7	P15.2	FAST / PU1 / VEXT / ES	658899	185148	General-purpose I/O
8	P15.3	FAST / PU1 / VEXT / ES	709299	344106	General-purpose I/O
9	P15.4	FAST / PU1 / VEXT / ES	756297	185148	General-purpose I/O
10	P15.5	FAST / PU1 / VEXT / ES	803295	344106	General-purpose I/O
11	P15.6	FAST / PU1 / VEXT / ES	850293	185148	General-purpose I/O
12	P15.7	FAST / PU1 / VEXT / ES	897291	344106	General-purpose I/O
13	P15.8	FAST / PU1 / VEXT / ES	944289	185148	General-purpose I/O
14	P14.0	FAST / PU1 / VEXT / ES2	991287	344106	General-purpose I/O
15	VDD	Vx	1076499	185148	Supply Voltage
16	P14.1	FAST / PU1 / VEXT / ES2	1161999	344106	General-purpose I/O
17	VSS	Vx	1238499	185148	Supply Voltage
18	P14.2	SLOW / PU2 / VEXT / ES	1319499	344106	General-purpose I/O
19	VSS	Vx	1366497	185148	Supply Voltage
20	P14.3	SLOW / PU2 / VEXT / ES	1413495	344106	General-purpose I/O
21	VEXT	Vx	1460493	175644	Supply Voltage
22	P14.4	SLOW / PU2 / VEXT / ES	1507491	344106	General-purpose I/O
23	P14.5	FAST / PU2 / VEXT / ES	1554489	185148	General-purpose I/O
24	P14.6	FAST / PU1 / VEXT / ES	1601487	344106	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
25	P14.7	SLOW / PU1 / VEXT / ES	1648485	185148	General-purpose I/O
26	P14.8	SLOW / PU1 / VEXT / ES	1695483	344106	General-purpose I/O
27	P14.9	LVDS_RX / FAST / PU1 / VEXT / ES	1770534	185148	General-purpose I/O
28	P14.10	LVDS_RX / FAST / PU1 / VEXT / ES	1864530	185148	General-purpose I/O
29	VDD	Vx	1939581	344106	Supply Voltage
30	VSS	Vx	1986579	185148	Supply Voltage
31	VEXT	Vx	2033577	344106	Supply Voltage
32	VEXT	Vx	2093499	185148	Supply Voltage
33	VEXT	Vx	2164599	344106	Supply Voltage
34	VDDP3	Vx	2346597	185148	Supply Voltage
35	VDDP3	Vx	2453499	344106	Supply Voltage
36	VDDP3	Vx	2543499	185148	Supply Voltage
37	VDD	Vx	2669499	344106	Supply Voltage
38	VDD	Vx	2768499	185148	Supply Voltage
39	VDD	Vx	2826477	344106	Supply Voltage
40	VSS	Vx	2873475	185148	Supply Voltage
41	P13.0	LVDS_TX / FAST / PU1 / VEXT / ES6	2984976	344106	General-purpose I/O
42	P13.1	LVDS_TX / FAST / PU1 / VEXT / ES6	3078972	344106	General-purpose I/O
43	VSS	Vx	3190473	185148	Supply Voltage
44	P13.2	LVDS_TX / FAST / PU1 / VEXT / ES6	3301974	344106	General-purpose I/O
45	P13.3	LVDS_TX / FAST / PU1 / VEXT / ES6	3395970	344106	General-purpose I/O
46	VDDP3	Vx	3507471	338112	Supply Voltage
47	VSS	Vx	3554469	185148	Supply Voltage
48	VDD	Vx	3645999	322614	Supply Voltage
49	VEXT	Vx	3692997	175644	Supply Voltage
50	P12.0	SLOW / PU1 / VFLEX / ES	3767211	322614	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
51	P12.1	SLOW / PU1 / VFLEX / ES	3814209	175644	General-purpose I/O
52	P11.0	RFAST / PU1 / VFLEX / ES	3918213	322614	General-purpose I/O
53	VFLEX	Vx	3965211	175644	Supply Voltage
54	P11.1	RFAST / PU1 / VFLEX / ES	4040415	338112	General-purpose I/O
55	VSS	Vx	4087413	185148	Supply Voltage
56	P11.2	RFAST / PU1 / VFLEX / ES	4162617	344106	General-purpose I/O
57	VDD	Vx	4209615	175644	Supply Voltage
58	P11.4	RFAST / PU1 / VFLEX / ES	4325319	322614	General-purpose I/O
59	VSS	Vx	4412817	185148	Supply Voltage
60	P11.3	RFAST / PU1 / VFLEX / ES	4488021	344106	General-purpose I/O
61	VFLEX	Vx	4535019	175644	Supply Voltage
62	P11.6	RFAST / PU1 / VFLEX / ES	4610223	344106	General-purpose I/O
63	VSS	Vx	4657221	185148	Supply Voltage
64	P11.5	SLOW / RGMII_Input / PU1 / VFLEX / ES	4704219	338112	General-purpose I/O
65	P11.7	SLOW / RGMII_Input / PU1 / VFLEX / ES	4756617	175644	General-purpose I/O
66	P11.9	FAST / RGMII_Input / PU1 / VFLEX / ES	4807215	344106	General-purpose I/O
67	VFLEX	Vx	4857813	185148	Supply Voltage
68	P11.8	SLOW / RGMII_Input / PU1 / VFLEX / ES	4904811	338112	General-purpose I/O
69	P11.10	FAST / RGMII_Input / PU1 / VFLEX / ES	4955409	185148	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
70	P11.11	FAST / RGMII_Input / PU1 / VFLEX / ES	5006007	344106	General-purpose I/O
71	VSS	Vx	5056605	185148	Supply Voltage
72	P11.12	FAST / RGMII_Input / PU1 / VFLEX / ES	5103603	344106	General-purpose I/O
73	VSS	Vx	5211999	185148	Supply Voltage
74	VDD	Vx	5312493	322614	Supply Voltage
75	P11.14	SLOW / PU1 / VFLEX / ES	5397291	175644	General-purpose I/O
76	P11.13	SLOW / PU1 / VFLEX / ES	5444289	322614	General-purpose I/O
77	P11.15	SLOW / PU1 / VFLEX / ES	5491287	175644	General-purpose I/O
78	P10.0	SLOW / PU1 / VEXT / ES	5565501	344106	General-purpose I/O
79	P10.1	FAST / PU1 / VEXT / ES	5612499	185148	General-purpose I/O
80	VDD	Vx	5702499	322614	Supply Voltage
81	VSS	Vx	5792499	185148	Supply Voltage
82	VDDSB (VDD)	Vx	5839497	338112	Supply Voltage
83	VDDSB (VDD)	Vx	5940999	338112	Supply Voltage
84	VSS	Vx	5987997	185148	Supply Voltage
85	P10.2	FAST / PU1 / VEXT / ES	6068601	344106	General-purpose I/O
86	P10.3	FAST / PU1 / VEXT / ES	6115599	185148	General-purpose I/O
87	P10.4	FAST / PU1 / VEXT / ES	6165999	344106	General-purpose I/O
88	P10.5	SLOW / PU2 / VEXT / ES	6216399	185148	General-purpose I/O
89	P10.6	SLOW / PU2 / VEXT / ES	6266799	344106	General-purpose I/O
90	P10.7	SLOW / PU1 / VEXT / ES	6317199	185148	General-purpose I/O
91	P10.8	SLOW / PU1 / VEXT / ES	6367599	344106	General-purpose I/O
92	VSS	Vx	6436899	185148	Supply Voltage
93	VEXT	Vx	6537699	175644	Supply Voltage

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
94	P02.0	FAST / PU1 / VEXT / ES	6611292	259700	General-purpose I/O
95	P02.1	SLOW / PU1 / VEXT / ES	6611292	360500	General-purpose I/O
96	P02.2	FAST / PU1 / VEXT / ES	6611292	461300	General-purpose I/O
97	P02.3	SLOW / PU1 / VEXT / ES	6611292	562100	General-purpose I/O
98	P02.4	FAST / PU1 / VEXT / ES	6611292	662900	General-purpose I/O
99	VSS	Vx	6611292	772898	Supply Voltage
100	VDDSB (VDD)	Vx	6452334	827896	Supply Voltage
101	VDDSB (VDD)	Vx	6452334	972500	Supply Voltage
102	VSS	Vx	6611292	1027498	Supply Voltage
103	P02.5	FAST / PU1 / VEXT / ES	6452334	1107500	General-purpose I/O
104	P02.6	FAST / PU1 / VEXT / ES	6611292	1170500	General-purpose I/O
105	P02.7	FAST / PU1 / VEXT / ES	6452334	1233500	General-purpose I/O
106	P02.8	SLOW / PU1 / VEXT / ES	6611292	1296500	General-purpose I/O
107	VDD	Vx	6458328	1377500	Supply Voltage
108	VDD	Vx	6620796	1467500	Supply Voltage
109	VSS	Vx	6611292	1602500	Supply Voltage
110	VSS	Vx	6611292	1746500	Supply Voltage
111	VDDSB (VDD)	Vx	6452334	1801498	Supply Voltage
112	VDDSB (VDD)	Vx	6452334	1962500	Supply Voltage
113	VSS	Vx	6611292	2017498	Supply Voltage
114	P02.9	SLOW / PU1 / VEXT / ES	6473826	2124500	General-purpose I/O
115	P02.10	SLOW / PU1 / VEXT / ES	6620796	2187500	General-purpose I/O
116	P02.11	SLOW / PU1 / VEXT / ES	6458328	2250500	General-purpose I/O
117	VEXT	Vx	6620796	2313500	Supply Voltage
118	P01.3	SLOW / PU1 / VEXT / ES	6458328	2376500	General-purpose I/O
119	VSS	Vx	6611292	2431498	Supply Voltage
120	VSS	Vx	6611292	2529500	Supply Voltage
121	VDDSB (VDD)	Vx	6458328	2584498	Supply Voltage

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
122	VDDSB (VDD)	Vx	6458328	2718500	Supply Voltage
123	VSS	Vx	6611292	2773498	Supply Voltage
124	VDD	Vx	6458328	2907500	Supply Voltage
125	VSS	Vx	6611292	2970500	Supply Voltage
126	VDD	Vx	6458328	3033500	Supply Voltage
127	VEXT	Vx	6620796	3096500	Supply Voltage
128	P01.4	SLOW / PU1 / VEXT / ES	6473826	3159500	General-purpose I/O
129	P01.5	SLOW / PU1 / VEXT / ES	6620796	3222500	General-purpose I/O
130	P01.6	FAST / PU1 / VEXT / ES	6473826	3285500	General-purpose I/O
131	P01.7	FAST / PU1 / VEXT / ES	6473826	3411500	General-purpose I/O
132	VSS	Vx	6611292	3537500	Supply Voltage
133	VSS	—	6611292	3672500	Supply Voltage
134	P00.0	FAST / PU1 / VEXT / ES	6452334	3807500	General-purpose I/O
135	VDD	Vx	6620796	3942500	Supply Voltage
136	VDD	—	6620796	4055000	Supply Voltage
137	P00.1	SLOW / PU1 / VEXT / ES	6611292	4209430	General-purpose I/O
138	P00.2	SLOW / PU1 / VEXT / ES1	6433794	4264430	General-purpose I/O
139	P00.3	SLOW / PU1 / VEXT / ES1	6611292	4319428	General-purpose I/O
140	P00.4	SLOW / PU1 / VEXT / ES1	6433794	4374428	General-purpose I/O
141	P00.5	SLOW / PU1 / VEXT / ES1	6611292	4429426	General-purpose I/O
142	P00.6	SLOW / PU1 / VEXT / ES1	6433794	4484426	General-purpose I/O
143	P00.7	SLOW / PU1 / VEXT / ES1	6611292	4539424	General-purpose I/O
144	P00.8	SLOW / PU1 / VEXT / ES1	6433794	4594424	General-purpose I/O
145	P00.9	SLOW / PU1 / VEXT / ES1	6611292	4649422	General-purpose I/O
146	P00.10	SLOW / PU1 / VEXT / ES1	6433794	4704422	General-purpose I/O
147	P00.11	SLOW / PU1 / VEXT / ES1	6611292	4759420	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
148	P00.12	SLOW / PU1 / VEXT / ES1	6433794	4814420	General-purpose I/O
149	VSS	Vx	6611292	4869418	Supply Voltage
150	VSS	Vx	6611292	4968518	Supply Voltage
151	VDD	Vx	6611292	5067616	Supply Voltage
152	VDD	Vx	6611292	5166716	Supply Voltage
153	VEXT	Vx	6611292	5265814	Supply Voltage
154	VAREF3	Vx	6611292	5404730	Supply Voltage
155	VAGND3	Vx	6611292	5503828	Supply Voltage
156	VAREF2	Vx	6433794	5558828	Supply Voltage
157	VAGND2	Vx	6611292	5613826	Supply Voltage
158	AN47	D / HighZ / VDDM	6611292	5712926	Analog Input 47
159	AN46	D / HighZ / VDDM	6433794	5767924	Analog Input 46
160	AN45	D / HighZ / VDDM	6611292	5822924	Analog Input 45
161	AN44	D / HighZ / VDDM	6433794	5877922	Analog Input 44
162	AN43	D / HighZ / VDDM	6611292	5932922	Analog Input 43
163	AN42	D / HighZ / VDDM	6433794	5987920	Analog Input 42
164	AN41	D / HighZ / VDDM	6611292	6042920	Analog Input 41
165	AN40	D / HighZ / VDDM	6433794	6097918	Analog Input 40
166	AN39/P40.9	S / HighZ / VDDM	6611292	6262916	Analog Input 39
167	AN38/P40.8	S / HighZ / VDDM	6433794	6317914	Analog Input 38
168	AN37/P40.7	S / HighZ / VDDM	6611292	6372914	Analog Input 37
169	AN36/P40.6	S / HighZ / VDDM	6433794	6427912	Analog Input 36
170	AN35	D / HighZ / VDDM	6611292	6482912	Analog Input 35
171	AN34	D / HighZ / VDDM	6433794	6537910	Analog Input 34
172	AN33/P40.5	S / HighZ / VDDM	6611292	6592910	Analog Input 33

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
173	AN32/P40.4	S / HighZ / VDDM	6433794	6647908	Analog Input 32
174	AN31	D / HighZ / VDDM	6611292	6702908	Analog Input 31
175	AN30	D / HighZ / VDDM	6433794	6757906	Analog Input 30
176	AN29/P40.14	S / HighZ / VDDM	6611292	6812906	Analog Input 29
177	AN28/P40.13	S / HighZ / VDDM	6433794	6867904	Analog Input 28
178	AN27/P40.3	S / HighZ / VDDM	6611292	6922904	Analog Input 27
179	AN26/P40.2	S / HighZ / VDDM	6433794	6977902	Analog Input 26
180	AN25/P40.1	S / HighZ / VDDM	6611292	7032902	Analog Input 25
181	AN24/P40.0	S / HighZ / VDDM	6611292	7156300	Analog Input 24
182	AN23	D / HighZ / VDDM	6526440	7241292	Analog Input 23
183	AN22	D / HighZ / VDDM	6403140	7241292	Analog Input 22
184	AN21	D / HighZ / VDDM	6348141	7063794	Analog Input 21
185	AN20	D / HighZ / VDDM	6293142	7241292	Analog Input 20
186	AN19/P40.12	S / HighZ / VDDM	6238143	7063794	Analog Input 19
187	AN18/P40.11	S / HighZ / VDDM	6183144	7241292	Analog Input 18
188	AN17/P40.10	S / HighZ / VDDM	6128145	7063794	Analog Input 17
189	AN16	D / HighZ / VDDM	6073146	7241292	Analog Input 16
190	AN15	D / HighZ / VDDM	6018147	7063794	Analog Input 15
191	VAGND1	Vx	5963148	7241292	Supply Voltage
192	VAREF1	Vx	5908149	7063794	Supply Voltage
193	VAGND0	Vx	5853150	7241292	Supply Voltage
194	VAREF0	Vx	5798151	7063794	Supply Voltage
195	VSSM	Vx	5743152	7241292	Supply Voltage
196	VDDM	Vx	5688153	7063794	Supply Voltage

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
197	VSSM	Vx	5633154	7241292	Supply Voltage
198	VDDM	Vx	5578155	7063794	Supply Voltage
199	VSSM	Vx	5523156	7241292	Supply Voltage
200	VDDM	Vx	5468157	7063794	Supply Voltage
201	AN14	D / HighZ / VDDM	5413158	7241292	Analog Input 14
202	AN13	D / HighZ / VDDM	5358159	7063794	Analog Input 13
203	AN12	D / HighZ / VDDM	5303160	7241292	Analog Input 12
204	AN11	D / HighZ / VDDM	5248161	7063794	Analog Input 11
205	AN10	D / HighZ / VDDM	5193162	7241292	Analog Input 10
206	AN9	D / HighZ / VDDM	5138163	7063794	Analog Input 9
207	AN8	D / HighZ / VDDM	5083164	7241292	Analog Input 8
208	AN7	D / HighZ / VDDM	5028165	7063794	Analog Input 7
209	AN6	D / HighZ / VDDM	4973166	7241292	Analog Input 6
210	AN5	D / HighZ / VDDM	4918167	7063794	Analog Input 5
211	AN4	D / HighZ / VDDM	4863168	7241292	Analog Input 4
212	AN3	D / HighZ / VDDM	4808169	7063794	Analog Input 3
213	AN2	D / HighZ / VDDM	4753170	7241292	Analog Input 2
214	AN1	D / HighZ / VDDM	4698171	7063794	Analog Input 1
215	AN0	D / HighZ / VDDM	4643172	7241292	Analog Input 0
216	VDD	Vx	4525070	7241292	Supply Voltage
217	VDD	Vx	4467501	7082334	Supply Voltage
218	VSS	Vx	4386501	7241292	Supply Voltage
219	AGBTCLKN (VSS)	AGBT_CLK / VEXT	4230531	7250841	Input PAD (negative pole) for the external 100 MHz differential clock. AGBT Input; (TC3xx devices without AGBT: VSS)

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
220	AGBTCLKP (VSS)	AGBT_CLK / VEXT	4149441	7250841	Input PAD (positive pole) for the external 100 MHz differential clock. AGBT Input; (TC3xx devices without AGBT: VSS)
221	VEXT	Vx	4068531	7241336	Supply Voltage
222	VSS	Vx	3979071	7241337	Supply Voltage
223	AGBTTXN (VSS)	AGBT_TX / VEXT	3879599	7250841	Off-chip driver output PAD of the 2.5Gbps transmitter, negative pole AGBT Output; (TC3xx devices without AGBT: VSS)
224	AGBTTXP (VSS)	AGBT_TX / VEXT	3798509	7250841	Off-chip driver output PAD of the 2.5Gbps transmitter, positive pole AGBT Output; (TC3xx devices without AGBT: VSS)
225	AGBTERR (VSS)	FAST / PD / VEXT	3608311	7250702	Input PAD for CRC error from FPGA. AGBT Input; (TC3xx devices without AGBT: VSS)
226	VSS	Vx	3464001	7241292	Supply Voltage
227	VDD	Vx	3417003	7082334	Supply Voltage
228	VDD	Vx	3295503	7241292	Supply Voltage
229	VEVRSB	Vx	3189501	7082334	Supply Voltage
230	VEVRSB	Vx	3125997	7241292	Supply Voltage
231	P33.0	SLOW / PU1 / VEVRSB / ES5	3078999	7082334	General-purpose I/O
232	VSS	Vx	3032001	7241292	Supply Voltage
233	VDD	Vx	2933001	7082334	Supply Voltage
234	VSS	Vx	2886003	7241292	Supply Voltage
235	P33.1	SLOW / PU1 / VEVRSB / ES5	2781495	7082334	General-purpose I/O
236	P33.2	SLOW / PU1 / VEVRSB / ES5	2734497	7241292	General-purpose I/O
237	P33.3	SLOW / PU1 / VEVRSB / ES5	2687499	7082334	General-purpose I/O
238	P34.1	SLOW / PU1 / VEVRSB / ES5	2640501	7250796	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
239	VDD	Vx	2541501	7082334	Supply Voltage
240	VSS	Vx	2494503	7241292	Supply Voltage
241	P33.4	SLOW / PU1 / VEVRSB / ES5	2380491	7082334	General-purpose I/O
242	P34.2	SLOW / PU1 / VEVRSB / ES	2333493	7250796	General-purpose I/O
243	P33.5	SLOW / PU1 / VEVRSB / ES5	2286495	7082334	General-purpose I/O
244	P34.3	SLOW / PU1 / VEVRSB / ES	2239497	7250796	General-purpose I/O
245	P33.6	SLOW / PU1 / VEVRSB / ES5	2192499	7082334	General-purpose I/O
246	P34.4	SLOW / PU1 / VEVRSB / ES	2145501	7250796	General-purpose I/O
247	VDD_1V2_FLCS	Vx	2098503	7082334	Supply Voltage
248	VSS	Vx	2051505	7241292	Supply Voltage
249	P34.5	FAST / PU1 / VEVRSB / ES	1947195	7250796	General-purpose I/O
250	P33.7	SLOW / PU1 / VEVRSB / ES5	1900197	7082334	General-purpose I/O
251	P33.8	FAST / HighZ / VEVRSB	1853199	7241292	General-purpose I/O
252	P33.9	SLOW / PU1 / VEVRSB / ES5	1806201	7082334	General-purpose I/O
253	VSS	Vx	1713501	7241292	Supply Voltage
254	VDD	Vx	1666503	7082334	Supply Voltage
255	VEVRSB	Vx	1578519	7250796	Supply Voltage
256	P33.10	FAST / PU1 / VEVRSB / ES5	1531521	7082334	General-purpose I/O
257	P33.14	FAST / PU1 / VEVRSB / ES5	1451907	7250796	General-purpose I/O
258	P33.11	FAST / PU1 / VEVRSB / ES5	1352907	7241292	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
259	P33.15	SLOW / PU1 / VEVRSB / ES5	1305909	7088328	General-purpose I/O
260	P33.12	FAST / PU1 / VEVRSB / ES5	1258911	7241292	General-purpose I/O
261	P33.13	FAST / PU1 / VEVRSB / ES5	1211913	7082334	General-purpose I/O
262	VSS	Vx	1164915	7241292	Supply Voltage
263	VDD	Vx	1038501	7082334	Supply Voltage
264	VSS	Vx	977301	7241292	Supply Voltage
265	VSS	Vx	876501	7241292	Supply Voltage
266	P32.0	SLOW / PU1 / VEXT / ES	771597	7241292	General-purpose I/O
267	VGATE1N	Vx	724599	7082334	DCDC N ch. MOSFET gate driver output
268	P32.1	SLOW / PU1 / VEXT / ES	677601	7241292	General-purpose I/O
269	VGATE1P	Vx	627201	7082334	DCDC P ch. MOSFET gate driver output
270	P32.2	SLOW / PU1 / VEXT / ES	576801	7241292	General-purpose I/O
271	P32.3	SLOW / PU1 / VEXT / ES	526401	7082334	General-purpose I/O
272	P32.4	FAST / PU1 / VEXT / ES	476001	7241292	General-purpose I/O
273	P32.5	SLOW / PU1 / VEXT / ES	425601	7088328	General-purpose I/O
274	P32.6	SLOW / PU1 / VEXT / ES	356301	7250796	General-purpose I/O
275	P32.7	SLOW / PU1 / VEXT / ES	255951	7250796	General-purpose I/O
276	VDD	Vx	175644	7169301	Supply Voltage
277	VSS	Vx	185148	7068501	Supply Voltage
278	VSS	Vx	185148	6967701	Supply Voltage
279	VEXT	Vx	185148	6866901	Supply Voltage
280	P23.0	SLOW / PU1 / VEXT / ES	344106	6766101	General-purpose I/O
281	P23.1	FAST / PU1 / VEXT / ES	185148	6719103	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
282	P23.2	RFAST / PU1 / VFLEX2 / ES	344106	6616683	General-purpose I/O
283	VFLEX	Vx	175644	6569685	Supply Voltage
284	P23.3	RFAST / PU1 / VFLEX2 / ES	344106	6494481	General-purpose I/O
285	VSS	Vx	185148	6447483	Supply Voltage
286	P23.4	RFAST / PU1 / VFLEX2 / ES	344106	6372279	General-purpose I/O
287	VDD	Vx	175644	6325281	Supply Voltage
288	P22.12	RFAST / PU1 / VFLEX2 / ES	322614	6209577	General-purpose I/O
289	VSS	Vx	185148	6122079	Supply Voltage
290	P22.10	RFAST / PU1 / VFLEX2 / ES	338112	6046875	General-purpose I/O
291	VFLEX	Vx	175644	5999877	Supply Voltage
292	P22.11	RFAST / PU1 / VFLEX2 / ES	338112	5924673	General-purpose I/O
293	VSS	Vx	185148	5877675	Supply Voltage
294	P22.7	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	338112	5830677	General-purpose I/O
295	P23.5	FAST / RGMII_Input / PU1 / VFLEX2 / ES	185148	5764059	General-purpose I/O
296	P23.7	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	338112	5713461	General-purpose I/O
297	VFLEX	Vx	185148	5662863	Supply Voltage
298	P23.6	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	338112	5615865	General-purpose I/O
299	P22.4	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	175644	5565267	General-purpose I/O
300	P22.6	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	338112	5514669	General-purpose I/O

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
301	VSS	Vx	185148	5464071	Supply Voltage
302	P22.5	SLOW / RGMII_Input / PU1 / VFLEX2 / ES	338112	5417073	General-purpose I/O
303	P22.8	SLOW / PU1 / VFLEX2 / ES	175644	5366475	General-purpose I/O
304	P22.9	SLOW / PU1 / VFLEX2 / ES	322614	5319477	General-purpose I/O
305	P22.0	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	185148	5207976	General-purpose I/O
306	P22.1	LVDS_TX / FAST / PU1 / VFLEX2 / ES6	185148	5113980	General-purpose I/O
307	VDDP_3V3_FLANA1	—	344106	4966263	Supply Voltage
308	VSS	Vx	185148	4919265	Supply Voltage
309	VDD	Vx	338112	4872267	Supply Voltage
310	P22.2	LVDS_TX / FAST / PU1 / VEXT / ES6	344106	4760766	General-purpose I/O
311	P22.3	LVDS_TX / FAST / PU1 / VEXT / ES6	344106	4666770	General-purpose I/O
312	VEXT	Vx	185148	4555269	Supply Voltage
313	VEXT	Vx	344106	4508271	Supply Voltage
314	VEXT	Vx	185148	4461273	Supply Voltage
315	RESERVED	Vx	185148	4364001	Must be bonded to VSS
316	VDD	Vx	344106	4317003	Supply Voltage
317	VSS	Vx	185148	4256001	Supply Voltage
318	VDD	Vx	344106	4184001	Supply Voltage
319	VDD	Vx	362646	4071951	Supply Voltage
320	VSS	—	185148	4022541	Supply Voltage
321	XTAL1	XTAL / VEXT	185148	3865392	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
322	XTAL2	XTAL / VEXT	185148	3766392	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
323	VSS	—	185148	3609243	Supply Voltage

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
324	VEXT	Vx	362646	3559833	Supply Voltage
325	VEXT	Vx	185148	3423501	Supply Voltage
326	VDD	Vx	185148	3261501	Supply Voltage
327	VSS	Vx	185148	3135501	Supply Voltage
328	P21.0	LVDS_RX / FAST / PU1 / VEXT / ES	344106	3044646	General-purpose I/O
329	P21.1	LVDS_RX / FAST / PU1 / VEXT / ES	344106	2950650	General-purpose I/O
330	VSS	Vx	185148	2875599	Supply Voltage
331	P21.2	LVDS_RX / FAST / PU1 / VEXT / ES	344106	2800548	General-purpose I/O
332	P21.3	LVDS_RX / FAST / PU1 / VEXT / ES	344106	2706552	General-purpose I/O
333	VSS	Vx	185148	2631501	Supply Voltage
334	VDD	Vx	185148	2519001	Supply Voltage
335	P21.4	LVDS_TX / FAST / PU1 / VEXT / ES6	344106	2363976	General-purpose I/O
336	P21.5	LVDS_TX / FAST / PU1 / VEXT / ES6	344106	2269980	General-purpose I/O
337	DAPE2	FAST / PD2 / VEXT	175644	2158479	DAPE: DAPE2 Data I/O DAPE: DAPE2 Data I/O (PD Devices: VSS)
338	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	344106	2111481	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ. DAPE: DAPE1 Data I/O.
339	DAPE1	FAST / PD2 / VEXT	175644	2064483	DAPE: DAPE1 Data I/O DAPE: DAPE1 Data I/O (PD Devices: VSS)
340	TMS	FAST / PD2 / VEXT	344106	2017485	JTAG Module State Machine Control Input TMS: JTAG Module State Machine Control Input. DAP: DAP1 Data I/O.

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
341	DAPE0	FAST / PD2 / VEXT	175644	1970487	DAPE: DAPE0 Clock Input DAPE: DAPE0 clock input (PD Devices: NC)
342	P21.7/TDO	FAST / PU2 / VEXT / ES4	344106	1923489	General-purpose I/O DAP: DAP2 Data I/O; DAPE: DAPE2 Data I/O.
343	VSS	Vx	185148	1876491	Supply Voltage
344	$\overline{\text{TRST}}$	FAST / PU2 / VEXT	344106	1829493	JTAG Module Reset/Enable Input TRST_N: JTAG Module Reset/Enable Input. DAPE: DAPE0 Clock Input
345	TCK	FAST / PD2 / VEXT	185148	1782495	JTAG Module Clock Input TCK: JTAG Module Clock Input. DAP: DAP0 Clock Input.
346	P20.0	FAST / PU1 / VEXT / ES	344106	1735497	General-purpose I/O
347	VEXT	Vx	185148	1688499	Supply Voltage
348	P20.1	SLOW / PU1 / VEXT / ES	344106	1641501	General-purpose I/O
349	VSS	Vx	185148	1542501	Supply Voltage
350	VDD	Vx	185148	1434501	Supply Voltage
351	P20.2	S / PU / VEXT	344106	1334493	General-purpose I/O This pin is latched at power on reset release to enter test mode.
352	P20.3	SLOW / PU1 / VEXT / ES	185148	1287495	General-purpose I/O
353	$\overline{\text{ESR1}}$	FAST / PU1 / VEXT	344106	1240497	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin

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Table 2-71 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
354	$\overline{\text{PORST}}$	PORST / PD / VEXT	185148	1193499	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
355	$\overline{\text{ESR0}}$	FAST / OD / VEXT	344106	1146501	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter ´Reset Control Unit´ and SCU_IOCR register description. PMS_EVRWUP: EVR Wakepup Pin
356	VSS	Vx	185148	1056501	Supply Voltage
357	VDD	Vx	344106	944001	Supply Voltage
358	VDD	Vx	185148	831501	Supply Voltage
359	P20.6	SLOW / PU1 / VEXT / ES	344106	725499	General-purpose I/O
360	P20.7	FAST / PU1 / VEXT / ES	185148	678501	General-purpose I/O
361	P20.8	FAST / PU1 / VEXT / ES	344106	628101	General-purpose I/O
362	P20.9	FAST / PU1 / VEXT / ES	185148	577701	General-purpose I/O
363	P20.10	FAST / PU1 / VEXT / ES	344106	527301	General-purpose I/O
364	P20.11	FAST / PU1 / VEXT / ES	185148	476901	General-purpose I/O
365	P20.12	FAST / PU1 / VEXT / ES	344106	426501	General-purpose I/O
366	P20.13	FAST / PU1 / VEXT / ES	185148	357201	General-purpose I/O
367	P20.14	FAST / PU1 / VEXT / ES	185148	256401	General-purpose I/O

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Whenever in table of section 3 ’Electrical Specification’ the term ‘neighbor pads’ is used, the detailed definition is provided by **Figure 2-71**. This statement is also valid for next/nearest neighbor pads.

In order to find out who is affecting operation on a target pad (interfering) a number of active close-neighbor pads (ACNP) has to be defined.

Finding close-neighbor pads.

The Pad Ring has four edges: bottom, left, top, right. Each edge is limited, i.e. it has two ends.

Each pad has two direct (first) neighbors unless it is located at the end of the edge. In that case it only has one neighbor. Similarly, each pad has two indirect (second) neighbors unless it or its first neighbor is located at the end of the edge. These first and second neighbors we will collectively call Close-Neighbor pads. Therefore each pad has 2 to 4 close-neighbor pads.

Finding close-neighbors can be done with the following sequence:

1.) Choose a target pad and lookup its “X” and “Y” coordinates in table **Figure 2-71**.

2.) Find first and second neighbors by calculating “X” and “Y” distance from the selected pad. **Figure 2-71** is sorted by “Y” coordinate, which might help locate the 4 close-neighbor candidates (if the pad is near the edge, it might end up with less than 4 close-neighbors).

Defining active pads:

Pad is active if it is currently in use and if it doesn’t have “Vxx” in the name.

Figuring out number of active close-neighbor pads follow next rules:

- If the first neighbor is active, then we count it and also check if second neighbor (on the same side of selected pad) is active.

- If the first neighbor is not active, then we do not check the second on the same side.

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2.6 Legend

The data in this chapter 2 for TE and TX match with the file TC37xed_IO_Spirit_v2.0.0.1.27.xml.

Column “Ctrl.”:

I = Input (for GPIO port lines with IOCR bit field Selection PCx = $0XXX_B$)

O = Output (for GPIO port lines the ´O´ represents in most cases the port HWOUT function)

O0 = Output with IOCR bit field selection PCx = $1X000_B$

O1 = Output with IOCR bit field selection PCx = $1X001_B$ (ALT1)

O2 = Output with IOCR bit field selection PCx = $1X010_B$ (ALT2)

O3 = Output with IOCR bit field selection PCx = $1X011_B$ (ALT3)

O4 = Output with IOCR bit field selection PCx = $1X100_B$ (ALT4)

O5 = Output with IOCR bit field selection PCx = $1X101_B$ (ALT5)

O6 = Output with IOCR bit field selection PCx = $1X110_B$ (ALT6)

O7 = Output with IOCR bit field selection PCx = $1X111_B$ (ALT7)

Column “Buffer Type”:

RFAST = Pad class RFAST (5V/3.3V)

FAST = Pad class FAST (5V/3.3V)

SLOW = Pad class SLOW (5V/3.3V)

LVDS_TX = Pad class LVDS Transmit

LVDS_RX = Pad class LVDS Receive

S = Pad class S (Analog Input overlayed with General Purpose Input)

D = Pad class D (Analog Input)

Porst = Porst input Pad

XTAL1 = XTAL1 input Pad

XTAL2 = XTAL2 input Pad

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)

PU1 = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PU2 = with pull-up device connected during startup and reset, HighZ in Standby mode

PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)

PD1 = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)[1)]

PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode

OD = open drain during reset ($\overline{\text{PORST}}$ = 0)

ES = Supports Emergency Stop

ES1 = ES. ES can be overruled by VADC, control via P00_PCSR

ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message

ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI

ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode

1) The default state of GPIOs (Px.y) during and after PORST active is controllled via HWCFG6 (P14.4). Pls. see also chapter PMS, HWCFG[6].

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ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR

ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event

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3 Electrical Specification

3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC37xEXT and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC37xEXT and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must be provided by the microcontroller system in which the TC37xEXT designed in.

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3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ T_J = 150°C
Voltage at V_{DD} power supply pins with respect to V_{SS} 1) 2)	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all analog and class S input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all other input pins with respect to V_{SS} 3)	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition 4) 5)	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. 4)	ΣI_{IN} SR	-100	-	100	mA	

1) Valid for cumulated for up to 2.8h and pulse forms followed a power supply switch on phase, where the rise and fall times are related to the system capacities and coils.

2) Due to EVRC output voltage oscillation during switch off phase V_{DD} can drop down to -0.72V. For V_{DD} an input level down to -0.72V during switch off phase will not cause any damage or reliability problem.

3) Voltages below V_{INmin} have no Impact to the device reliability as Long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.

4) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

5) The specified min. and max. values represent the current limits, which have to be maintained, in case of a short circuit condition on the output of any Fast, RFast, Slow and Class S pad, not being used during operation.
This covers also output currents due to switching in operation for C_L=200pF.

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3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined the allowed time includes both ‘Operation Lifetime hours’ and ‘Inactive Lifetime hours’. The number of hours in **Table 3-71** and **Table 3-72** are examples only and the applicable numbers are defined by the customer profiles accepted by Infineon.
- **Operating Conditions** are met for
  - pad supply levels
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Table 3-2 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 [1]	-	15 [1]	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	V_{SS} - 2	-	$V_{EXT/FLEX/FLEX2}$ + 2	V	limited to 60h over lifetime; Valid for non LVDS and analoge pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	I_{OUT} CC	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

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Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	K_{OVDN} CC	-	-	$3*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; -5mA < I_{IN} < 0mA
		-	-	$2*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads VGASTE1N and VGATE1P; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; -5mA < I_{IN} < 0mA
		-	-	0.8		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	0.5		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for digital inputs, positive	K_{OVDP} CC	-	-	$1.5*10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
		-	-	1		Overload injected on LVDS RX pad and affecting neighbor LVDS pads
		-	-	$5*10^{-3}$		Overload injected on LVDS TX pad and affecting neighbor LVDS pads
Overload coupling factor for analog inputs, negative [2)]	K_{OVAN} CC	-	-	$1*10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; -5mA < I_{IN} < 0mA
		-	-	$1*10^{-5}$		else; -5mA < I_{IN} < 0mA

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Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, positive [2]	K_{OVAP} CC	-	-	$2*10^{-4}$		Analoge inputs overlaid with slow pads or pull down diagnostics; 0mA < I_{IN} < 5mA
		-	-	$2*10^{-5}$		else; 0mA < I_{IN} < 5mA

1) Reduced VADC / DSADC result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.

2) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

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3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC37xEXT. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC37xEXT must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

Table 3-3 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	200	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
BBB frequency	f_{BBB} SR	-	-	150	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
I2C frequency	f_{I2C} SR	-	-	100	MHz	
Operating MSC Frequency	f_{MSC} SR	-	-	200	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
ADAS clock frequency	f_{ADAS} CC	200	-	300	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
GETH frequency	f_{GETH} CC	100	-	150	MHz	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package
		-40	-	170	°C	valid for all SAL products without package

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Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	V_{DD} SR	1.125 [1]	1.25	1.375 [2]	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 [3]	V	
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 [3]	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid; also vaild for V_{FLEX2}
		4.5	5.0	5.5 [3]	V	5V pad parameters are valid; also vaild for V_{FLEX2}
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 [4]	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	

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Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97 5)	-	5.5	V	
Voltage to ensure defined pad states	V_{DDPPA} CC	1.3 6)	-	-	V	
Digital supply voltage for Flex2 port	V_{FLEX2} SR	2.97	3.3	3.63	V	3.3V pad parameters are valid
		3.63	5	5.5	V	5V pad parameters are valid

1) For V_{DD} 1.08V ≤ V_{DD} < 1.125V operation is still possible but with relaxed parameters.
2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
4) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
5) V_{EVRSB} supply voltage can drop down upto 2.6V during Standby mode. It is required to have a capictor of 100nF on V_{EVRSB} supply pin.
6) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when VEXT has reached this level.

Limitation of Supply Voltage over Time

The maximum operation voltage for $V_{EXT/FLEX/DDM}$ supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-4 Example Voltage Profile

$V_{EXT/FLEX/DDM}$=	Duration [h]
5.4 V < $V_{EXT/FLEX/DDM}$ ≤ 5.5 V	≤ 5% of lifetime
5.15 V < $V_{EXT/FLEX/DDM}$ ≤ 5.4 V	≤ 15% of lifetime
4.85 V < $V_{EXT/FLEX/DDM}$ ≤ 5.15 V	≤ 60% of lifetime
4.6 V < $V_{EXT/FLEX/DDM}$ ≤ 4.85 V	≤ 15% of lifetime
4.5 V < $V_{EXT/FLEX/DDM}$ ≤ 4.6 V	≤ 5% of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-5 Example Voltage Profile

V_{DD}=	Duration [h]
1.325 V < V_{DD} ≤ 1.375 V	≤ 5% of lifetime
1.275 V < V_{DD} ≤ 1.325 V	≤ 15% of lifetime
1.225 V < V_{DD} ≤ 1.275 V	≤ 60% of lifetime

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Table 3-5 Example Voltage Profile

V_{DD}=	Duration [h]
1.175 V < V_{DD} ≤ 1.225 V	≤ 15% of lifetime
1.125 V < V_{DD} ≤ 1.175 V	≤ 5% of lifetime

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3.5 5 V / 3.3 V switchable Pads

Pad classes slow GPIO and fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

Table 3-6 $\overline{\text{PORST}}$ Pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{PORST}}$ pad Output current	I_{PORST} CC	13	-	-	mA	V_{EXT} = 2.97V; V_{PORST} = 0.9V
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	260	-	-	ns	without additional PORST Digtial Filter active (PORSTDF = 0).
Input hysteresis [1]	HYS CC	0.055 * V_{EXT}	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
Pull-down current [2]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; TTL (degraded, used for CIF)
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-450	-	450	nA	TJ≤150°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-500	-	500	nA	TJ≤150°C ;else
		-900	-	900	nA	TJ≤170°C ; (0.1 * V_{EXT}) < V_{IN} < (0.9 * V_{EXT})
		-950	-	950	nA	TJ≤170°C ; else
Input high voltage level	V_{IH} SR	1.4	-	-	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		2.0	-	-	V	TTL; V_{EXT} = 4.5V
Input low voltage level	V_{IL} SR	-	-	0.5	V	TTL (degraded, used for CIF); V_{EXT} = 2.97V
		-	-	0.8	V	TTL; V_{EXT} = 4.5V
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

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Table 3-7 Fast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time [1) 2)]	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/FLEX2/EVRSB}$ to 0.8 * $V_{EXT/FLEX/FLEX2/EVRSB}$
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3)]	HYS CC	0.09 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4)]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5)]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

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Table 3-7 Fast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	$0.7 * V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	$0.44 * V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB}$ = constant; AL

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Table 3-7 Fast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-8 Fast 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/FLEX2/EVRSB}$ to 0.8 * $V_{EXT/FLEX/FLEX2/EVRSB}$
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.055 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)

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Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 150°C$; $(0.1 * V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-6000	-	6000	nA	$T_J \leq 150°C$; LVDS_RX / Fast pad type ; else
		-3200	-	3200	nA	$T_J \leq 150°C$; LVDS_TX / Fast pad type ; else
		-1500	-	1500	nA	$T_J \leq 150°C$; else
		-2000	-	2000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/FLEX2/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2/EVRSB})$
		-4000	-	4000	nA	$T_J \leq 170°C$; $(0.1 * V_{EXT/FLEX/FLEX2}) < V_{IN} < (0.9 * V_{EXT/FLEX/FLEX2})$; LVDS_TX / Fast pad type
		-13500	-	13500	nA	$T_J \leq 170°C$; LVDS_RX / Fast pad type ; else
		-5100	-	5100	nA	$T_J \leq 170°C$; LVDS_TX / Fast pad type ; else
		-2500	-	2500	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available

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Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-9 Slow 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time 1) 2)	t_{RF} CC	4+0.55*C_L	4+0.75*C_L	12+1*C_L	ns	driver = medium edge = medium ; C_L≤200pF
		1.5+0.25* C_L	2.5+0.40* C_L	7+0.55*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis 3)	HYS CC	0.09 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

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Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH};AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|130|	µA	V_{IL}; AL or TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	T_J ≤ 150°C; (0.1 * $V_{EXT/FLEX/FLEX2/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/FLEX2/EVRSB}$)
		-400	-	400	nA	T_J ≤ 150°C; else
		-600	-	600	nA	T_J ≤ 170°C; (0.1 * $V_{EXT/FLEX/FLEX2/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/FLEX2/EVRSB}$)
		-750	-	750	nA	T_J ≤ 170°C; else
		-18000	-	18000	nA	P32.0 and P32.1;T_J≤150°C
		-38000	-	38000	nA	P32.0 and P32.1;T_J≤170°C
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

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2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-10 Slow 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
Rise / Fall time 1) 2)	t_{RF} CC	2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium edge = medium ; C_L≤200pF
		2+0.30*C_L	3.5+0.50* C_L	5+0.70*C_L	ns	driver = medium edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis 3)	HYS CC	0.055 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL

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Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
		|11|	-	-	µA	V_{IH}; TTL; exept VGATE1P; except VGATE1N and T_J > 150°C
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF); exept VGATE1P; except VGATE1N and T_J > 150°C
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-300	-	300	nA	T_J ≤ 150°C; (0.1 * $V_{EXT/FLEX/FLEX2/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/FLEX2/EVRSB}$)
		-400	-	400	nA	T_J ≤ 150°C; else
		-600	-	600	nA	T_J ≤ 170°C; (0.1 * $V_{EXT/FLEX/FLEX2/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/FLEX2/EVRSB}$)
		-750	-	750	nA	T_J ≤ 170°C; else
		-18000	-	18000	nA	P32.0 and P32.1;T_J≤150°C
		-38000	-	38000	nA	P32.0 and P32.1;T_J≤170°C
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/FLEX2/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/FLEX2/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low/high voltage level	V_{ILH} SR	1.0	-	1.9	V	RGMII; no hysteresis available
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/FLEX2/EVRSB}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-11 RFast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	3.2	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{FLEX/FLEX2}$ to 0.8 * $V_{FLEX/FLEX2}$
		4+0.55*C_L	4+0.75*C_L	12+1.0*C_L	ns	driver = medium; C_L≤200pF
		1.0+0.18* C_L	2.5+0.27* C_L	5.0+0.35* C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.5+0.08* C_L	0.5+0.11* C_L	1.0+0.17* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.5	-	0.5	ns	valid for all data rates excluding clock tolerance

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Table 3-11 RFast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [3]	HYS CC	0.09 * $V_{FLEX/FLEX2}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{FLEX/FLEX2}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [5]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{FLEX/FLEX2}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{FLEX/FLEX2}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{FLEX/FLEX2}$ = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

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3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-12 RFast 3.3V pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	8	20	30	Ohm	Driver = RGMII; $I_{OH/OL}$ = 8mA
		125	225	320	Ohm	medium driver; $I_{OH/OL}$ = 2mA
		31	55	80	Ohm	strong driver; $I_{OH/OL}$ = 8mA
Input Duty Cycle	f_D SR	47.5	50	52.5		
Rise / Fall time 1) 2)	t_{RF} CC	1.6	-	4.5	ns	C_L = 25pF; driver = strong sharp edge; from 0.2 * $V_{FLEX/FLEX2}$ to 0.8 * $V_{FLEX/FLEX2}$
		-	-	5	ns	C_L = 25pF; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		-	-	1	ns	Driver = RGMII; from 20%V to 80%V; C_L=15pF
		2+0.57*C_L	5.5+0.75* C_L	10+1.25* C_L	ns	driver = medium; C_L≤200pF
		1.5+0.18* C_L	1.5+0.28* C_L	8+0.4*C_L	ns	driver = strong edge = medium; C_L≤200pF
		0.75+0.08 *C_L	0.75+0.11 *C_L	2.5+0.21* C_L	ns	driver = strong edge = sharp ; C_L≤200pF
Asymmetry of sending	t_{TX_ASYM} CC	-0.4	-	0.4	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [3]	HYS CC	0.055 * $V_{FLEX/FLEX2}$	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{FLEX/FLEX2}$	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{FLEX/FLEX2}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [4]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}; AL and TTL and TTL (degraded, used for CIF)
Pull-down current [5]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1700	-	1700	nA	$T_J \leq 150°C$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-2100	-	2100	nA	$T_J \leq 150°C$; else
		-3000	-	3000	nA	$T_J \leq 170°C$; $(0.1 * V_{FLEX/FLEX2}) < V_{IN} < (0.9 * V_{FLEX/FLEX2})$
		-4000	-	4000	nA	$T_J \leq 170°C$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{FLEX/FLEX2}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-12 RFast 3.3V pad (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{FLEX/FLEX2}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{FLEX} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3.5	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
2) Rise / fall times are defined 10% - 90% of pad supply voltage.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-13 Class S 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis [1]	HYS CC	0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [2]	I_{PUH} CC	|30|	-	-	µA	V_{IH}; AL or TTL
		-	-	|130|	µA	V_{IL}; AL or TTL
Pull-down current [3]	I_{PDL} CC	-	-	|130|	µA	V_{IH}; AL or TTL
		|30|	-	-	µA	V_{IL}; AL
		|28|	-	-	µA	V_{IL}; TTL

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Table 3-13 Class S 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300	-	300	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-14 Class S 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	

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Table 3-14 Class S 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis [1]	*HYS* CC	0.055 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		0.065 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL (degraded used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current [2]	I_{PUH} CC	|17|	-	-	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		|11|	-	-	µA	V_{IH}; TTL
		-	-	|80|	µA	V_{IL}
Pull-down current [3]	I_{PDL} CC	-	-	|105|	µA	V_{IH}; AL and TTL (degraded, used for CIF)
		-	-	|115|	µA	V_{IH}; TTL
		|19|	-	-	µA	V_{IL}; AL and TTL
		|15|	-	-	µA	V_{IL}; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300	-	300	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600	-	600	nA	$T_J \leq 170°C$; PDD option available
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

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Table 3-14 Class S 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-15 Class D

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150°C$; else
		-300 [1]	-	300 [1]	nA	$T_J \leq 150°C$; PDD option available, or AltRef option available and EDSADC channel connected
		-300	-	300	nA	$T_J \leq 170°C$; else
		-600 [2]	-	600 [2]	nA	$T_J \leq 170°C$; PDD option available, or AltRef option available and EDSADC channel connected
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) For AN11 100 nA need to be added.
2) For AN11 200 nA need to be added.

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Table 3-16 ADC Reference Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} CC	-1	-	1	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-2	-	2	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; used for EVADC
		-3.5	-	3.5	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC
		-7	-	7	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; used for EVADC
		-2 [1]	-	2 [1]	µA	$T_J \leq 150°C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-4 [1]	-	4 [1]	µA	$T_J \leq 170°C$; $V_{AREF} < V_{DDM}$; for EDSADC
		-6 [1]	-	6 [1]	µA	$T_J \leq 150°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC
		-12 [1]	-	12 [1]	µA	$T_J \leq 170°C$; $V_{AREF} \leq V_{DDM}$+50mV; for EDSADC

1) Limit is valid for VAREF1 pin.

Table 3-17 Driver Mode Selection for Slow Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

Table 3-18 Driver Mode Selection for Fast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

Table 3-19 Driver Mode Selection for RFast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)

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Table 3-19 Driver Mode Selection for RFast Pads (cont'd)

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	RGMII function active

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3.6 High performance LVDS Pads

This LVDS pad type is used for the high speed chip to chip communication interface of the new TC37xEXT. It compose out of a LVDSH pad and a fast pad.

C_L = 2.5 pF for all LVDSH parameters.

Table 3-20 LVDS - IEEE standard LVDS general purpose link (GPL)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance	R_0 CC	40	-	140	Ohm	V_{cm} = 1.0 V and 1.4 V
Rise time (20% - 80%)	t_{rise20} CC	-	-	0.75 [1]	ns	Z_L = 100 Ohm ±20% @2pF external load
Fall time (20% - 80%)	t_{fall20} CC	-	-	0.75 [2]	ns	Z_L = 100 Ohm ±20% @2pF external load
Output differential voltage [3]	V_{OD} CC	240	-	330	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=00
		280	-	370	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=01
		320	-	410	mV	R_T = 100 Ohm ±1%; LPCRx.VDIFFADJ=10
		380	-	500	mV	RT = 100 Ohm ± 1%; LPCRx.VDIFFADJ=11; Multi slave operation
Output voltage high	V_{OH} CC	-	-	1475	mV	RT = 100 Ohm +/- 1% VDIFFADJ=00 and 01
		-	-	1500	mV	RT = 100 Ohm ± 1% VDIFFADJ=10 and 11
Output voltage low	V_{OL} CC	925	-	-	mV	RT = 100 Ohm ± 1% VDIFFADJ=00 and 01
		900	-	-	mV	RT = 100 Ohm +/- 1% VDIFFADJ=10 and 11
Output offset (Common mode) voltage	V_{OS} CC	1125	-	1275	mV	RT = 100 Ohm ± 1%
Input voltage range	V_I SR	0	-	1600	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±10%
		0	-	2400	mV	Driver ground potential difference < 925 mV; R_T = 100 Ohm ±20%
Input differential threshold	V_{idth} SR	-100	-	100	mV	Driver ground potential difference < 900 mV; VDIFFADJ=10 and 11
		-100	-	100	mV	Driver ground potential difference < 925 mV; VDIFFADJ=00 and 01

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Table 3-20 LVDS - IEEE standard LVDS general purpose link (GPL) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Receiver differential input impedance	R_{in} CC	80	-	120	Ohm	V_I ≤ 2400 mV
Output differential voltage Sleep Mode 4)	V_{ODSM} CC	-5	-	20	mV	RT = 100 Ohm ± 20%; LPCRx.VDIFFADJ=xx
Delta output impedance	$dR0$ SR	-	-	10	%	V_{cm} = 1.0 V and 1.4 V
Change in VOS between 0 and 1	$dVOS$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Change in Vod between 0 and 1	$dVod$ CC	-	-	25	mV	R_T = 100 Ohm ±1%
Pad set-up time	t_{SET_LVDS} CC	-	10	13	µs	
Duty cycle	t_{duty} CC	45	-	55	%	

1) t_{rise20} = 0.75ns + (C_L - 2)[pF]*20ps. C_L defines the external load.
2) t_{fall20} = 0.75ns + (C_L - 2)[pF]*20ps. C_L defines the external load.
3) Potential violations of the IEEE Std 1596.3 are intended for the new multislave support feature. To be compliant to IEEE Std 1596.3 LPCRx.VDIFFADJ has to be configured to 01.
4) Common Mode voltage of Tx is maintained.

Note: Driver ground potential difference is defined as driver-receiver potentital difference, that can result in a voltage shift when comparing driver output voltage level and receiver input voltage level of a transmitted signal.

*Note: R_T in table 'LVDS - IEEE standard LVDS general purpose Link (GPL)' is as termination resistor of the receiver according to figure 3-5 in IEEE Std 1596.3-1996 and is represent in **Figure 3-1** either by R_{in} or by R_T=100Ohm but not both. If R_T is mentioned in column Note / Test Condition always the internal resistor R_{in} in **Figure 3-1** is the selected one.*

default after start-up = CMOS function

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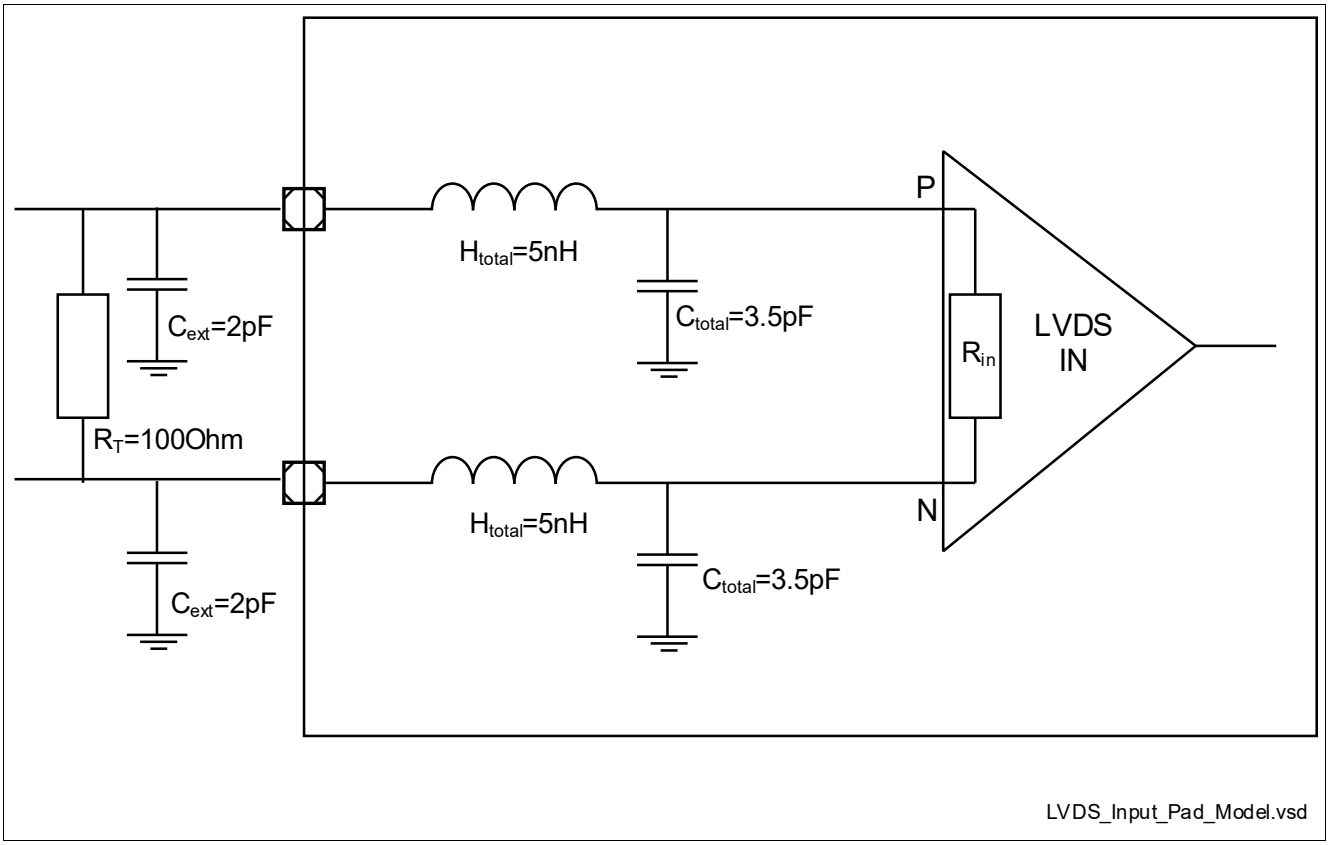


Figure 3-1 LVDS pad Input model

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3.7 VADC Parameters

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of (V_{AREF} - V_{AGND}) >= 4.5 V. If the reference voltage range is below 4.5 V by a factor of k (e.g. 3.3 V), the accuracy parameters increase by a factor of 1.1/k (e.g. 1.1 × 4.5 / 3.3 = 1.5).

Noise on the voltage supply influences the conversion. The accuracy parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Digital functions overlapping analog inputs influence accuracy.

The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and EN_{RMS} = 1.0 the additional peak-peak noise error is 8 LSB.

Fast compare operations are executed with 10-bit values.

The noise reduction feature improves the result by adding additional conversion steps. The conversion times, therefore, increase accordingly (4 × t_{ADCI} + 3 × t_{ADC} for each of 1, 3, or 7 steps).

Table 3-21 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	V_{DDK} CC	1.15	-	1.35	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	dV_{DDK} CC	-2	-	2	%	Based on device-specific value
Analog reference voltage [1]	V_{AREF} SR	4.5	5.0	V_{DDM} + 0.05	V	4.5 V ≤ V_{DDM} ≤ 5.5 V
		2.97	3.3	V_{DDM} + 0.05	V	2.97 V ≤ V_{DDM} < 4.5 V
Analog reference ground	V_{AGND} SR	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	V_{AIN} SR	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	f_{ADCI} SR	16	40	53.33	MHz	4.5 V ≤ V_{DDM} ≤ 5.5 V
		16	20	26.67	MHz	2.97 V ≤ V_{DDM} < 4.5 V
Total Unadjusted Error [2] [3]	TUE CC	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error [2]	EA_{INL} CC	-3	-	3	LSB	
DNL error [2][4]	EA_{DNL} CC	-1	-	3	LSB	
Gain Error [2]	EA_{GAIN} CC	-3.5	-	3.5	LSB	
Offset Error [2][3]	EA_{OFF} CC	-4	-	4	LSB	
RMS Noise [2][5] [6]	EN_{RMS} CC	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference input charge consumption per conversion (from V_{AREF}) [7) 8) 9)]	Q_{CONV} CC	-	-	20	pC	V_{AIN} = 0 V (worst case), precharging disabled
		-	-	10	pC	V_{AIN} = 0 V (worst case), precharging enabled, V_{DDM} - 5% < V_{AREF} < V_{DDM} + 50 mV
Switched capacitance of an analog input	C_{AINS} CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption [10)]	Q_{AINS} CC	-	-	3.5	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150°C
		-	-	3.8	pC	Primary groups and fast compare channels; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C
		-	-	4.4	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J ≤ 150 °C
		-	-	4.8	pC	Secondary groups; V_{AIN} = V_{AREF}; V_{DDM} = 5.0 V; input buffer enabled; T_J > 150°C

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	t_S SR	100	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		500	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer disabled
		700	-	-	ns	Secondary group, 4.5 V ≤ V_{DDM} ≤ 5.5 V; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
		1000	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer disabled
		1200	-	-	ns	Secondary group, 2.97 V ≤ V_{DDM} < 4.5 V; input buffer enabled
Sampling time for calibration	t_{SCAL} SR	50	-	-	ns	4.5 V ≤ V_{DDM} ≤ 5.5 V
		100	-	-	ns	2.97 V ≤ V_{DDM} < 4.5 V
Input buffer switch-on time	t_{BUF} CC	-	0.4	1	µs	
Wakeup time	t_{WU} CC	-	0.1	0.2	µs	Fast standby mode
		-	1.6	3	µs	Slow standby mode
Broken wire detection delay against V_{AREF}	t_{BWR} CC	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	t_{BWG} CC	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance [11]	R_{CSD} CC	45	-	75	kOhm	
Converter diagnostics voltage accuracy	dV_{CSD} CC	-10	-	10	%	Percentage refers to V_{DDM}

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Table 3-21 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	R_{MDU} CC	30	-	42	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, Automotive Levels
		56	-	78	kOhm	0 V ≤ V_{IN} ≤ 0.9* V_{DDM}, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	R_{MDD} CC	43	-	58	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, Automotive level
		18	-	25	kOhm	0.1*V_{DDM} ≤ V_{IN} ≤ V_{DDM}, TTL level
Resistance of the pull-down test device	R_{PDD} CC	-	-	0.3	kOhm	Measured at pad input voltage V_{IN} = V_{DDM} / 2.

1) These limits apply to the standard reference input as well as to the alternate reference input.
2) Parameter depends on reference voltage range and supply ripple, see introduction.
Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
Tests are done with postcalibration disabled, after completing the startup calibration.
3) Analog inputs mapped to pads of the type SLOW influence accuracy. The values for this parameter increase by 3 LSB_{12}.
4) Monotonic characteristic, no missing codes when calibrated.
5) Parameter EN_{RMS} refers to a 1 sigma distribution.
6) Analog inputs mapped to pads of the type SLOW the RMS noise (EN_{RMS}) can be up to 2 LSB_{12} (soft switching for DC/DC enabled).
7) For reduced reference voltages VAREF < 3.375V, the consumed charge QCONV is reduced by the factor of k2 = VAREF [V] / 3.375. For reduced reference voltages 4.5V < VAREF ≤ 3.375V, QCONV is not reduced.
8) Maximum charge increases by 15 pC when BWD (Broken Wire Detection) is active.
9) Fast compare channels only consume 1/3 of the charge for a primary/secondary group.
10) For analog inputs with overlaid digital GPIOs or with PDD function this value increases by 1 pC.
11) Use a sample time of at least 1.1 µs to enable proper settling of the test voltage.

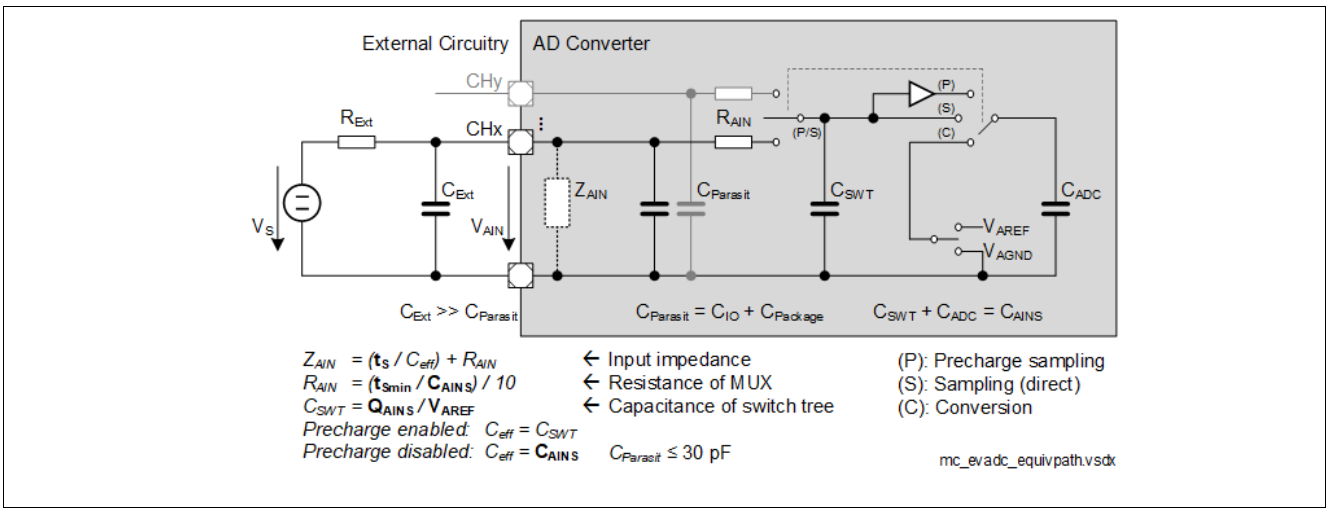


Figure 3-2 Equivalent Circuitry for Analog Inputs

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3.8 DSADC Parameters

The DSADC parameters are valid only for voltage range 4.5 V <= V_{DDM} <= 5.5 V.

These parameters describe the product properties and do not include external circuitry. The values are valid for junction temperatures T_J <= 150°C if not defined explicitly.

Calibration is specified for gain factors 1 and 2, calibrated values refer to these settings.

The signal-noise ratio (SNR) is specified for differential inputs. For single ended operation the resulting signal-noise ratio is reduced by 6 dB. For quasi-differential mode (i.e. using V_{CM}) its reduced by 3dB with gain=2 (6dB with gain=1).

Table 3-22 DSADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Common mode voltage bias resistance	R_{BIAS} CC	105	130	155	kOhm	On-chip variation ≤ ±2.5%.
Positive reference voltage	V_{AREF} SR	4.5	-	V_{DDM} + 0.05	V	
Reference ground voltage	V_{AGND} SR	V_{SSM}	-	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Reference load current	I_{REF} CC	-	10	12	µA	Per modulator
		-	-	14	µA	Per modulator, T_J>150°C
Common mode voltage accuracy [1]	dV_{CM} CC	-100	-	100	mV	Deviation from selected voltage
Analog input voltage range	V_{DSIN} SR	V_{SSM}	-	2 * V_{DDM}	V	Differential;V_{DSxP} - V_{DSxN}
		V_{SSM}	-	V_{DDM}	V	Single ended
Input current [2]	I_{RMS} CC	7	10	13	µA	Exact value (±1%) available in UCB; valid for gain = 1 and f_{MOD} = 26.7 MHz
On-chip modulator clock frequency	f_{MOD} SR	16	-	40	MHz	
Gain error [3] [4]	ED_{GAIN} CC	-0.2 [5]	±0.1[5]	0.2 [5]	%	T_J≤150°C; Target, calibrated, V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-	±0.25	-	%	T_J>150°C; V_{AREF} constant after calibration; f_{MOD} = 26.67 MHz
		-1	-	1	%	Calibrated once; f_{MOD} = 26.67 MHz
		-2.5	-	2.5	%	Uncalibrated; f_{MOD} = 26.67 MHz

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Table 3-22 DSADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DC offset error [3]	ED_{OFF} CC	-5 [5]	-	5 [5]	mV	Calibrated; f_{MOD} = 26.67 MHz
		-10	-	10	mV	Calibrated once; f_{MOD} = 26.67 MHz
		-30	-	30	mV	Uncalibrated; f_{MOD} = 26.67 MHz
Signal-Noise Ratio for differential input signals [2][6][7]	*SNR* CC	80	-	-	dB	T_J≤150°C; f_{PB} = 30 kHz; f_{MOD} = 26.67 MHz
		78	-	-	dB	T_J≤150°C; f_{PB} = 50 kHz; f_{MOD} = 26.67 MHz
		74	-	-	dB	T_J≤150°C; f_{PB} = 100 kHz; f_{MOD} = 26.67 MHz
Signal-Noise Ratio degradation	*DSNR* CC	-	-	3	dB	T_J>150°C; Resulting Signal-Noise Ratio value is SNR - DSNR
Spurious-free dynamic range [3]	*SFDR* CC	60	-	-	dB	f_{MOD} = 26.67 MHz
Output sampling rate	f_D CC	3.906	-	300	kHz	16 MHz / 4096, without integrator
Pass band	f_{PB} CC	1.302	-	100	kHz	Output data rate: f_D = f_{PB} * 3; without integrator
		1.302	-	10	kHz	Output data rate: f_D = f_{PB} * 6; without integrator
Pass band ripple	df_{PB} CC	-0.08	-	0.08	dB	FIR filters enabled
Stop band attenuation	*SBA* CC	40	-	-	dB	0.5 f_D ... 1.0 f_D
		45	-	-	dB	1.0 f_D ... 1.5 f_D
		50	-	-	dB	1.5 f_D ... 2.0 f_D
		55	-	-	dB	2.0 f_D ... 2.5 f_D
		60	-	-	dB	2.5 f_D ... OSR/2 f_D
DC compensation factor	*DCF* CC	-3	-	-	dB	10^{-5} f_D, offset compensation filter enabled (FCFGMx.OCEN = 001_B)
Modulator settling time	t_{MSET} CC	-	-	20	µs	After switching on, voltage regulator already running

1) On pins with overlaid GPIO function the max. limit increases by up to 25 mV due to leakage current for T_J > 150°C.
2) For detailed information, refer to the User Manual chapter.
3) This parameter is valid within the defined range of f_{MOD}.
4) Gain mismatch error between the different EDSADC channels is within ±0.5% if they have the same calibration strategy

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5) Recalibration needed in case of a temperature change >20ºC
6) These values are valid for an analog gain factor of 1. Subtract 3 dB for each higher gain factor.
7) For single ended input signals and gain1, the SNR is reduced by 6 dB.

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3.9 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 16 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

Table 3-23 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	µA	V_{IN}>0V ; V_{IN}<V_{EXT}
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 [1]	ms	20MHz ≤ f_{OSC} and 8pF load capacitance
Input voltage at XTAL1 [2]	V_{IX} SR	-0.7	-	V_{EXT} + 0.5	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	0.3*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} > 25MHz
		0.35*V_{EXT}	-	V_{EXT} + 1.0	V	If shaper is not bypassed; f_{OSC} ≤ 25MHz
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 [3]	DC_{X1} SR	35	-	65	%	V_{XTAL1} = 0.5*V_{PPX}
Absolute RMS jitter at XTAL1 [3]	J_{ABSX1} SR	-	-	28	ps	10 KHz to f_{OSC}/2
Slew rate at XTAL1 [3]	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) t_{OSCS} is defined from the moment when the Oscillator Mode is set to External Crystal Mode until the oscillations reach an amplitude at XTAL1 of 0.3 * VEXT.
This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

2) For Supply (V_{EXT} < 5.3V V_{IX}) min could be down to -0.9V. For XTAL1 an input level down to -0.9V will not cause a damage or a reliability problem operating with an external crystal.

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3) Square wave input signal for XTAL1.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

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3.10 Back-up Clock

The back-up clock provides an alternative clock source.

Table 3-24 Back-up Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	f_{BACKUT} CC	70	100	130	MHz	V_{EXT}≥2.97V
Back-up clock accuracy after trimming [1]	f_{BACKT} CC	98	100	102	MHz	V_{EXT}≥2.97V
Standby clock	f_{SB} CC	25	70	110	kHz	V_{EXT}≥2.97V

1) A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125 celcius

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3.11 Temperature Sensor

Table 3-25 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

Table 3-26 DTS Core

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion [1]	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ T_J=-40°C and T_J=127°C
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

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3.12 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The real (realistic) power pattern defines the following conditions:

- T_J = 150 °C
- f_{SRI} = f_{CPUx} = 300 MHz
- f_{GTM} = 200 MHz
- f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = $f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.275 V
- V_{DDP3} / FLEX = 3.366 V
- $V_{EXT / EVRSB}$ = V_{DDM} = 5.1 V
- all cores are active including two lockstep core (IPC=0.6)
- the following peripherals are inactive: HSM, HSCT, GETH, Ethernet, PSI5, I2C, FCE, CIF, and MTU

The max power pattern defines the following conditions:

- T_J = 150 °C
- f_{SRI} = f_{CPUx} = 300 MHz
- f_{GTM} = 200 MHz
- f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = $f_{ASCLINx}$ = 100 MHz
- V_{DD} = 1.375 V
- V_{DDP3} / FLEX = 3.63 V
- $V_{EXT / EVRSB}$ = V_{DDM} = 5.5 V
- all cores are active including three lockstep cores (IPC=1.2)
- the following modules are inactive: GETH, FCE, CIF, and MTU

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Table 3-27 Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST}$+ ∑ I_{DDCx0}+ ∑ I_{DDCxx}+ I_{DDGTM}+I_{DDSB})	I_{DDRAIL} CC	-	-	775	mA	max power pattern; valid for Feature Package T, and TP products
		-	-	960 [1]	mA	max power pattern; valid for Feature Package TE, and TX products
		-	-	630	mA	real power pattern; valid for Feature Package T, and TP products
		-	-	775	mA	real power pattern; valid for Feature Package TE, and TX products
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. [2]	$I_{DDPORST}$ CC	-	-	190	mA	V_{DD} = 1.275V; T_J=125°C; valid for Feature Package TE, and TX products
		-	-	132	mA	V_{DD} = 1.275V; T_J=125°C; valid for Feature Package T, and TP products
		-	-	220	mA	V_{DD} = 1.275V; T_J=150°C; valid for Feature Package T, and TP products
		-	-	315	mA	V_{DD} = 1.275V; T_J=165°C; valid for Feature Package T, and TP products
		-	-	315	mA	V_{DD} = 1.275V; T_J=150°C; valid for Feature Package TE, and TX products
		-	-	425	mA	V_{DD} = 1.275V; T_J=165°C; valid for Feature Package TE, and TX products

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Table 3-27 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	45 [2]	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	36 [3]	mA	real power pattern incl. Flash read current and Dflash programming current.
∑ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX}$+I_{EVRSB}+$I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	50	mA	max power pattern
		-	-	35 [4]	mA	real power pattern
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	11 [5] [6]	mA	real power pattern with port activity absent; PORST output inactive.
I_{EVRSB} supply current [2]	I_{EVRSB} CC	-	-	8.5	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	27	mA	real power pattern; sum of currents of EDSADC and EVADC modules
∑ Sum of all currents (incl. $I_{EXTRAIL}$+$I_{DDMRAIL}$+$I_{DDx3RAIL}$+I_{DD})	I_{DDTOT} CC	-	-	728	mA	real power pattern; T_J=150°C; valid for Feature Package T, and TP products
		-	-	873	mA	real power pattern; T_J=150°C; valid for Feature Package TE, and TX products
		-	-	796	mA	real power pattern; TJ=160°C; valid for Feature Package T, and TP products
		-	-	1015	mA	real power pattern; TJ=160°C; valid for Feature Package TE, and TX products
∑ Sum of all currents with DC-DC EVRC regulator active [7]	$I_{DDTOTDC3}$ CC	-	-	430	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 3.3V; T_J=150°C

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Table 3-27 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of all currents with DC-DC EVRC regulator active [7]	$I_{DDTOTDC5}$ CC	-	-	320	mA	real power pattern; EVRC reset settings with 72% efficiency; V_{EXT} = 5V; T_J=150°C
∑ Sum of all currents (SLEEP mode) [2]	I_{SLEEP} CC	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB}$ = 1 MHz via LPDIV divider; T_J = 25$°C$
∑ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin [8]	$I_{STANDBY}$ CC	-	-	130 [9]	µA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. T_J = 25$°C$; V_{EVRSB} = 5V
Maximum power dissipation [10]	PD SR	-	-	1600	mW	max power pattern; valid for Feature Package T, and TP products
		-	-	1855	mW	max power pattern; valid for Feature Package TE, and TX products
		-	-	1240	mW	real power pattern; valid for Feature Package T, and TP products
		-	-	1425	mW	real power pattern; valid for Feature Package TE, and TX products

1) In QFP package for TC37xED emulation device, the total (IDDED + IDD) current need to be limited to 700 mA. The maximum (IDDED + IDD) current for TC37xED is supported only in BGA packages.
2) Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.
3) Realistic Pflash read pattern with 50% Pflash bandwidth utlilization and a code mix of 50% 0s and 50% 1s. A common decoupling capacitor of atleast 100nF for (V_{DDP3}) is used. Continuous Dflash programming in burst mode with 3.3 V supply and realistic Pflash read access in parallel. Erase currents of the corresponding flash modules are less than the respective programming currents at V_{DDP3} pin. Programming and erasing flash may generate transient current spikes of up to 45 mA / 20 ns
which are handled by the decoupling and buffer capacitors. This parameter is relevant for external power supply dimensioning and not for thermal considerations.
4) Limits are defined for real power pattern. For ADAS power pattern limit sum up to 42mA.
5) The current consumption includes only minimal port activity.
6) Limits are defined for real power pattern. For ADAS power pattern limit has to be multiplied by the factor 0.7.
7) The total current drawn from external regulator is estimated with 72% EVRC SMPS regulator efficiency. IDDTOTDCx is calculated from IDDTOT using the scaled core current [(IDD x VDD)/(VinxEfficiency)] and constitutes all other rail currents and IDDM.

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8) The same current limits apply also for the other power pattern.

9) ∑ Sum of all currents during RUN mode at VEVRSB supply pin is less than (IEVRSB + 4 mA Standby RAM current + ISCRSB if SCR active). ∑ It is recommended to have atleast 100 nF decoupling capacitor at this pin. 32kB of Standby SRAM contributes less than 10uA to ISTANDBY current.

10) The values are only valid if all supplies are applied from external and do not contain the power losses of EVR33 and EVRC.

Table 3-28 Module Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank [1]	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 [2]	mA	Pflash 3.3V programming current adder when using external 5V supply.
I_{EXT} supply current added by LVDS pads in LVDS mode [1]	$I_{EXTLVDS}$ CC	-	-	16	mA	real power pattern; 4 pairs of LVDS pins active with transmit function
		-	-	9 [3]	mA	real power pattern; 6 pairs of LVDS pins active with receive function

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Table 3-28 Module Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
∑ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC}$+$I_{DDMEDSADC}$)	I_{DDM} CC	-	-	14	mA	real power pattern; current for EDSADC modules only and EVADC modules are inactive; 4 EDSADC channels active continuously.
		-	-	22 [4]	mA	max power pattern; current for EDSADC modules only and EVADC modules are inactive; all EDSADC channels active continuously.
		-	-	13 [5]	mA	real power pattern; current for EVADC modules only and EDSADC modules are inactive; 8 EVADC modules active.
		-	-	15 [6]	mA	max power pattern; current for EVADC modules only and EDSADC modules are inactive; all EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE}$ CC	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at V_{EVRSB} supply pin	I_{SCRSB} CC	-	-	7 [7]	mA	SCR power pattern incl. PMS current consumption with fback clock active; f_{SYS_SCR} = 20MHz; T_J=150°C
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; fSYS_SCR = 70kHz; T_J=25°C
SCR 8-bit Standby Controller CPU in IDLE mode [8]	$I_{SCRIDLE}$ CC	-	-	3.5	mA	real power pattern. CPU set into idle mode.

1) The same current limits apply also for the other power pattern.
2) During Pflash programming at 5V, additional 2 mA is drawn at VEXT supply rail.
3) A single LVDS pair with receive function is limited to 1.5mA ($t_{EXTLVDS}$).

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4) A single DS channel instance consumes 4 mA.
5) EVADC current is limited to 3mA in "ADAS power pattern with 2 EVADC" at (I_{DDM}).
6) A single VADC unit consumes 1.3 mA.
7) If SCR ADCOMP is activated, an additional 0.6 mA adder is to be considered.
8) Limits are defined for real power pattern (V_{DD}=1.275V). For max power pattern limit has to be multiplied by the factor 1.22.

Table 3-29 Module Core Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	I_{DDCx0} CC	-	-	72	mA	max power pattern; IPC=1.2
		-	-	48	mA	real power pattern; IPC=0.6
I_{DD} core current of CPUx main core with CPUx lockstep core active	I_{DDCxx} CC	-	-	I_{DDCx0} + 48	mA	max power pattern; IPC=1.2
		-	-	I_{DDCx0} + 37	mA	real power pattern; IPC=0.6
I_{DD} core current added by GTM	I_{DDGTM} CC	-	-	110	mA	max power pattern
		-	-	90	mA	real power pattern; TIMx, TOMx, ATOMx , MCSx active. 2 clusters at 200 MHz.
		-	-	50	mA	TIMx, TOMx active at 100MHz. ATOMx , MCSx, DPLL inactive. 2 clusters at 100 MHz.
I_{DD} core current added by HSM	I_{DDHSM} CC	-	-	20 [1)]	mA	max power pattern; HSM running at 100MHz.
I_{DD} core current added by CIF	I_{DDCIF} CC	-	-	48	mA	conditions t.b.d.
I_{DD} core dynamic current added by LBIST	$I_{DDLBIST}$ CC	-	-	200 [2)]	mA	LBIST Configuration A; 1.2V ≤ V_{DD}
I_{DD} core dynamic current added by MBIST	$I_{DDMBIST}$ CC	-	-	225	mA	fMBIST = 300MHz; tMBIST < 6ms. MTU Ganging procedure for SRAM test and initialization; VDD = 1.375V.

1) The current consumption includes basic HSM activity incl. AES module.
2) LBIST is executed either during start-up phase or can be triggered by application software. Secondary voltage monitors are inactive during the LBIST execution time (t_{LBIST}).
During the start-up phase externally supplied V_{DD} voltage has to be equal or greater than 1.2V (V_{DD} nominal - 4%) for static accuracy.
If V_{DD} is supplied internally by EVRC, EVRC takes care not to violate the V_{DD} 1.2V static under voltage limit.

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3.12.1 Calculating the 1.25 V Current Consumption

The current consumption of the 1.25 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(3.1)

$$I_0 = 6,5\left[\frac{mA}{C}\right] \times e^{0,02 \times T_J[C]}$$

(3.2)

$$I_0 = 15,6\left[\frac{mA}{C}\right] \times e^{0,02 \times T_J[C]}$$

Equation (3.1) defines the typical static current consumption and **Equation (3.2)** defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.275 V.

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3.13 Power Supply Infrastructure and Supply Start-up

3.13.1 Supply Ramp-up and Ramp-down Behavior

Start-up slew rates for supply rails shall comply to SR (see **Table 3-33** Supply Ramp).

3.13.1.1 Single Supply mode (a)

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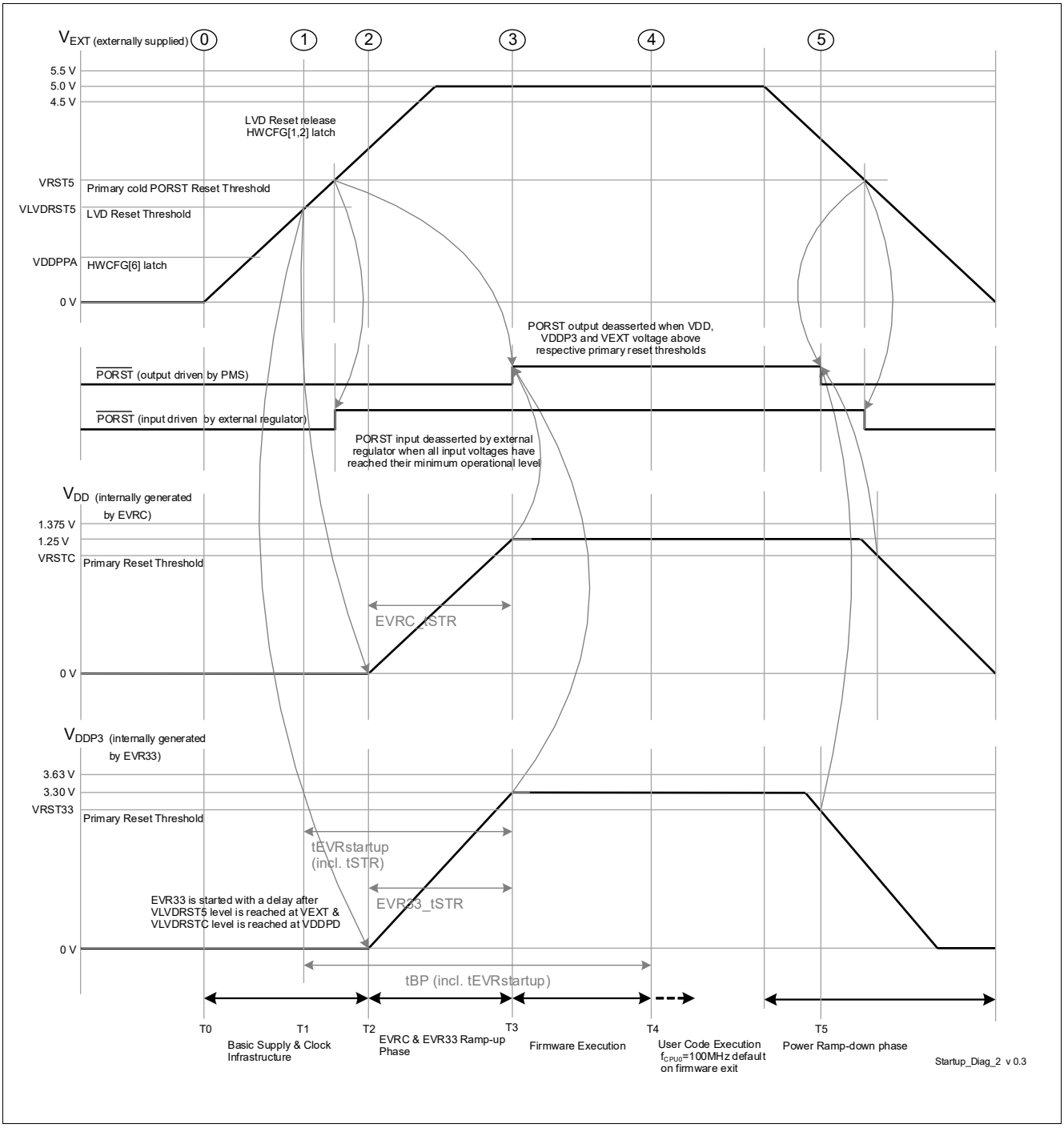


Figure 3-3 Single Supply mode (a) - VEXT (5 V) single supply

VEXT = 5 V single supply mode. VDD and VDDP3 are generated internally by the EVRC and EVR33 internal regulators.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited during the basic infrastructure and EVRx regulator start-up phase (T0 up to T2) to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

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- Furthermore it is also ensured that the current drawn from the regulator (dIDD/dt) is limited during the Firmware start-up phase (T3 up to T4) to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-3** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC and EVR33 regulators are initiated. PORST (input) does not have any affect on EVR33 or EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC and EVR33 regulators have ramped up.
    PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.2 Single Supply mode (e)

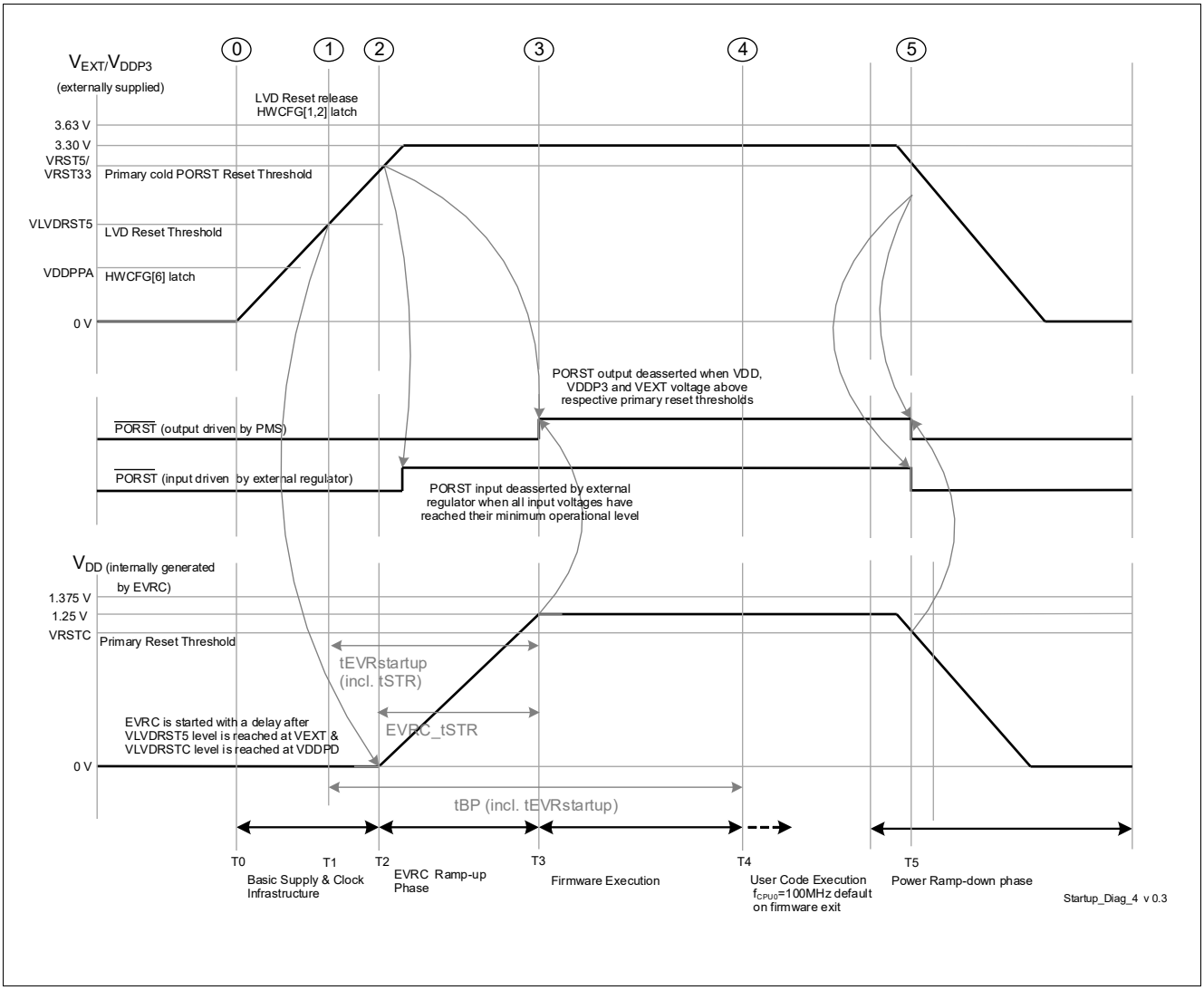


Figure 3-4 Single Supply mode (e) - (VEXT & VDDP3) 3.3 V single supply

VEXT = VDDP3 = 3.3 V single supply mode. VDD is generated internally by the EVRC regulator.

- The rate at which current is drawn from the external regulator (dIEXT /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time. Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the

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basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.

- The power sequence as shown in **Figure 3-4** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVRC regulator is initiated. PORST (input) does not have any affect on EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC regulator has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.3 External Supply mode (d)

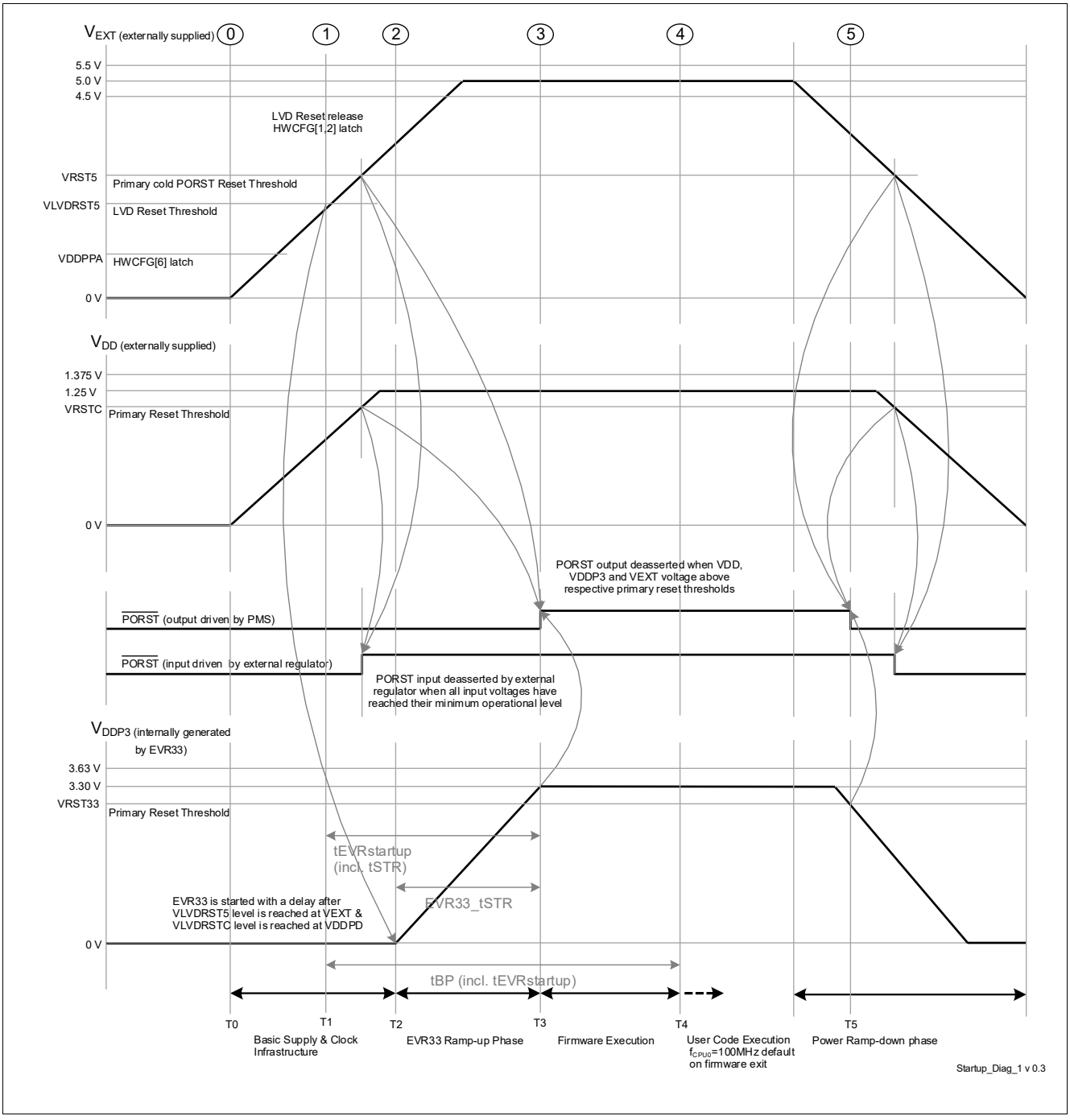


Figure 3-5 External Supply mode (d) - VEXT and VDD externally supplied

VEXT = 5 V and VDD supplies are externally supplied. 3.3V is generated internally by the EVR33 regulator.

- External supplies VEXT and VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, VEXT ramps up before VDD rail. If VDD voltage

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rail is ramped up before VEXT; VDD supply overshoots during start-up shall be limited within the operational voltage range.

- The rate at which current is drawn from the external regulator (dIEXT /dt or dIDD /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-5** is enumerated below
  - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T2 refers to the point in time where consequently a soft start of EVR33 regulator is initiated. PORST (input) does not have any affect on EVR33 output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR (datasheet parameter) time to avoid overshoots.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVR33 regulators has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup (datasheet parameter).
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.13.1.4 External Supply mode (h)

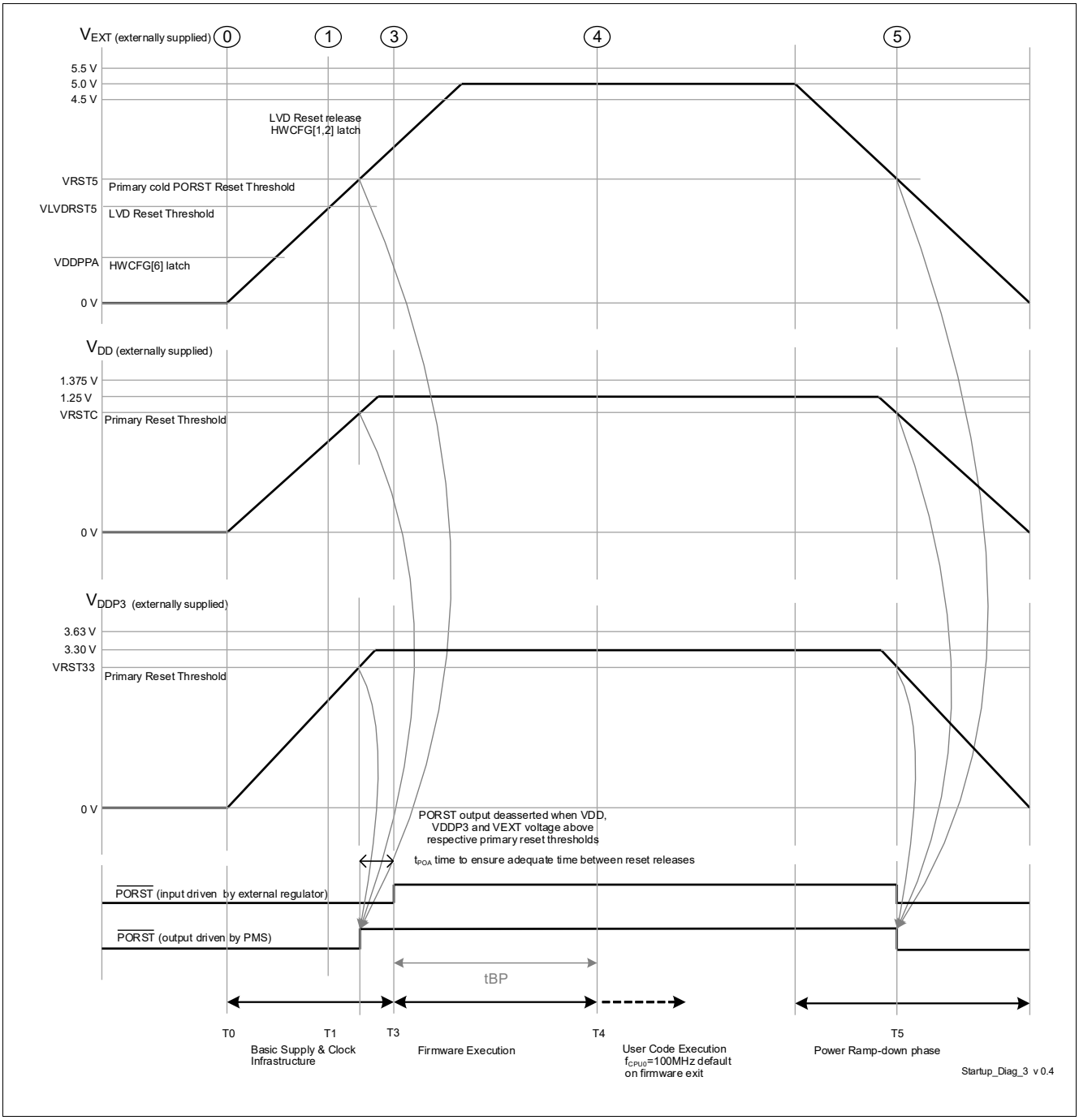


Figure 3-6 External Supply mode (h) - VEXT, VDDP3 & VDD externally supplied

All supplies, namely VEXT, VDDP3 & VDD are externally supplied.

- External supplies VEXT, VDDP3 & VDD may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to datasheet parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, VEXT ramps up before VDDP3 and VDD rails. If smaller voltage rails are ramped up before VEXT; VDD and VDDP3 supply overshoots during start-up shall be limited within the operational voltage ranges of the respective rails.

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- The rate at which current is drawn from the external regulator (dIEXT /dt, dIDD /dt or dIDDP3 /dt) is limited in the Start-up phase to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that µC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the µC when at least one among the three supply domains (VDD, VDDP3 or VEXT) violate their primary under-voltage reset thresholds.The PORST (output) is de-asserted by the µC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of upto 150 mA (dIDD) is expected.
- The power sequence as shown in **Figure 3-6** is enumerated below
  - T1 up to T3 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[2:1,4,5,6] and TESTMODE pins. T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started .The supply mode is evaluated based on the HWCFG[2:1,6] pins. These events are initiated after LVD reset release at T1. LVD reset is released the both input voltages VEXT and VEVRSB are above VLVDRST5 and VLVDRSTSB levels correspondingly. Internal pre-regulator VDDPD output voltage is above VLVDRSTC level.
  - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated.
  - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP (datasheet parameter).
  - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided supplies (VDD, VDDP3 or VEXT) drop below their respective primary under-voltage reset thresholds.

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3.14 Reset Timing

Table 3-30 Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_B CC	-	-	400	µs	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BS} CC	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time [1]	t_{BP} CC	-	-	3.1	ms	$dVEXT/dT$=1V/ms. $VEXT$>$VLVDRST5$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	t_{EVRPOR} CC	10 [2]	-	-	µs	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup}$ CC	-	-	1	ms	dV/dT=1V/ms. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} SR	1 [3]	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ CC	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ}$ CC	-	-	180	µs	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	16 / f_{SPB}	-	-	ns	

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Table 3-30 Reset (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	8000/f_{BACKT}	-	18000/f_{BACKT}	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	160	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.5	ms	without RAM initalization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; 1.2V ≤ V_{DD}
SCR reset boot time	t_{SCR} CC	-	-	5	µs	User Mode 0
		-	-	16	µs	User Mode 1
		-	13.3	-	µs	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	µs	external supplies are V_{EVRSB}, V_{EXT}, $V_{FLEX/FLEX2}$, V_{DDM}, V_{DDP3} and V_{DD}

1) RAM initialization add 500µs in addition.
2) Cold PORST reset is driven by uC and maintained in an extended voltage range between VDDPPA limit and absolute maximum rating voltage limits.
3) The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on VEXT, VDDP3 and VDD rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.

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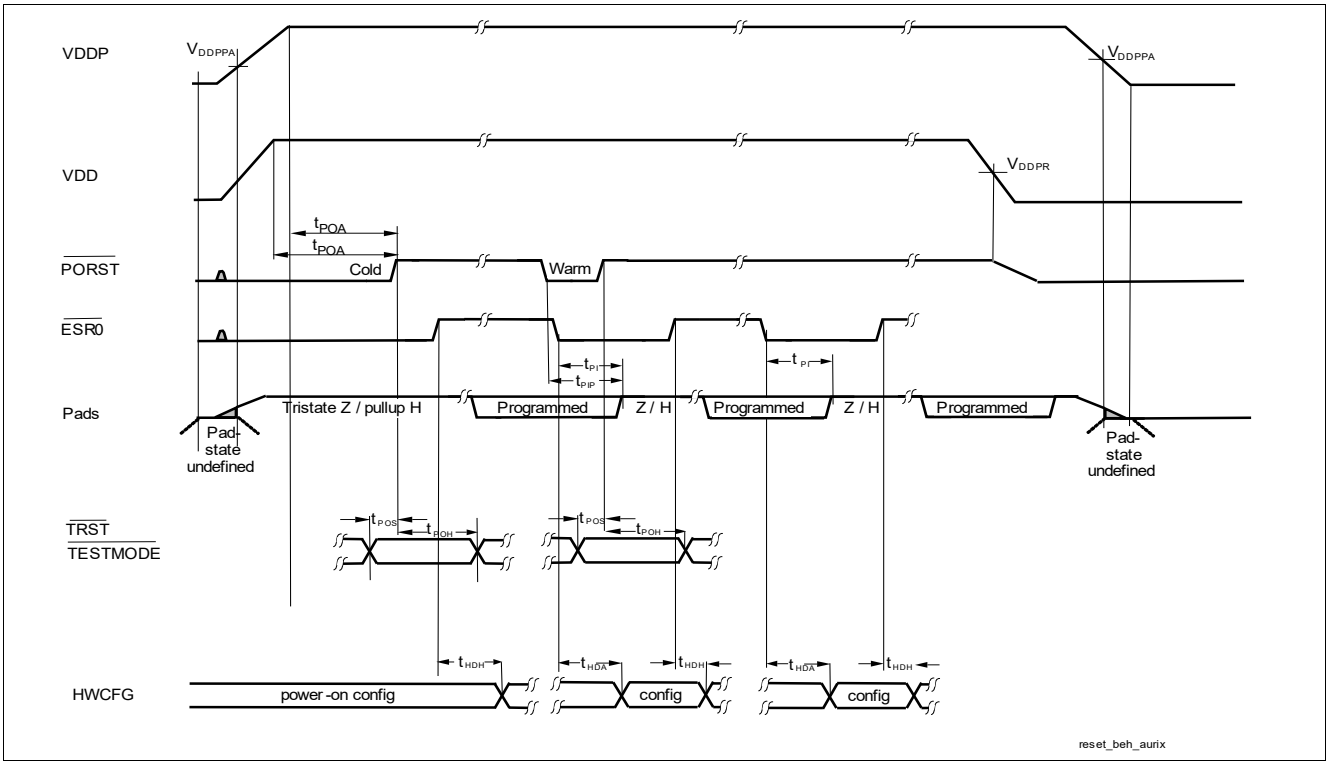


Figure 3-7 Power, Pad and Reset Timing

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3.15 PMS

Table 3-31 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_{IN} SR	3.60 [1]	-	5.50	V	Normal RUN mode
		2.97 [2]	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging [3]	V_{OUT} CC	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; I_{DDP3}=50mA
Output V_{DDx3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; I_{DDP3}=50mA
Output buffer capacitance on V_{OUT}	C_{OUT} SR	1.45	2.2	3	µF	
Output buffer capacitor ESR	C_{OUTESR} SR	-	-	100 [4]	mOhm	f > 0.5MHz; f < 10MHz
Maximum output current of the regulator	I_{MAX} CC	60 [5]	-	-	mA	Normal RUN mode
Startup time	t_{STR} CC	-	500	1000	µs	Normal RUN mode
External V_{IN} supply ramp [6]	$dVin/dt$ SR	-	1	-	V/ms	
Ripple on Output Voltage	ΔV_{OUTTC} CC	-	-	33	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{OUTTC} ≥ 10mA ; I_{OUTTC} ≤ 60mA; ΔV_{OUTTC} = (peak to peak ripple / 2)
Load step response [7]	$dVout/dIout$ CC	-165	-	-	mV	Normal RUN mode; dI=10 to 60mA; dt=20ns; $Tsettle$=20us
		-	-	165	mV	Normal RUN mode; dI=60 to 10mA; dt=20ns; $Tsettle$=20us
		-180	-	-	mV	Low voltage cranking mode; dI=10 to 50 mA; dt=20ns; $Tsettle$=20us
		-	-	180	mV	Low voltage cranking mode; dI=50 to 10mA; dt=20ns; $Tsettle$=20us

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Table 3-31 EVR33 LDO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	$dVout/dVin$ CC	-	-	40	mV	$dVin/dT$=1V/ms; dV= 3.6 to 5V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-40	-	-	mV	$dVin/dT$=1V/ms; dV= 5 to 3.6V; I_{MAX}=60mA; ΔV_{OUTTC} is included
		-	-	280	mV	$dVin/dT$=50V/ms; dV= 3.6 to 5V; I_{MAX}=60mA
		-165	-	-	mV	$dVin/dT$=50V/ms; dV= 5 to 3.6V; I_{MAX}=60mA

1) A maximum pass device dropout voltage of 300mV is included in the minimum input voltage to ensure optimal pass device performance during normal operation.
2) VEXT Input voltage drop up to 2.97V leading to VDDP3 output voltage drop upto 2.6V can be tolerated if Flash is switched before to low performance mode.
3) No external inductive load permissible if EVR33 is used.
4) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before Cout.
5) IMAX is limited to 40 mA incase of Low voltage mode (cranking case) with on chip pass devices. In case EVR33 is not used, Injection current into 3.3V VDDP3 supply rail with active sink on 5V VEXT rail should be limited to 500 mA if during power sequencing 3.3V is supplied before 5V by external regulator.
6) EVR is robust against residual voltage ramp-up starting between 0 - 2.97 V. A VEXT voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
7) Settling time is defined until output voltage is within +-1% of the mean(VOUTT) of the individual device.

Table 3-32 Supply Monitors

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming [1]	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming [2]	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming [2]	$V_{DDP3PRIUV}$ CC	2.86 [3]	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} primary undervoltage monitor accuracy after trimming [2]	$V_{DDPRIUV}$ CC	1.08 [3]	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT}, V_{DDP3} and V_{DD} rails.
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming [4] [5]	V_{EXTMON} CC	5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ECh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ECh(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For BGA packages: EVRMONFILT.SWDFI L=1.
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For BGA packages: EVR MONFILT.SWDFIL=1

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{EXT}, V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming (cont'd)	V_{EXTMON} CC	4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For QFP packages: EVRMONFILT.SWDFIL=2
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV)/DAh(OV). For BGA packages: EVRMONFILT.SWDFIL=1
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV)/DAh(OV). For QFP packages: EVRMONFILT.SWDFIL=2
V_{DDP3} secondary supply monitor accuracy after trimming [5)]	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh(UV)/CCh(OV). EVRMONFILT.EVR33FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh(OV,UV). EVRMONFILT.EVR33FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh(UV)/EFh(OV). EVRMONFILT.EVR33FIL = 3.

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Table 3-32 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming [5]	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h(UV)/C8h(OV). EVRMONFILT.EVRCFIL = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(OV,UV). EVRMONFILT.EVRCFIL = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh(UV)/EBh(OV). EVRMONFILT.EVRCFIL = 1.
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVRSB} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRSTSB}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVRSB} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5} CC	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON} CC	-	-	3.2	µs	HPOSC and SHPBG bandgap trimmed. Filter inactive.

1) The reset release on supply ramp-up is delayed by a time duration 20-40 us after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The reset limit of 2,97V at pin is for the case with 3.3V generated internally from EVR33. In case the 3.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 3.0V at the VDDP3 pin.

2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. The VxxPRIUV parameters are device individually tested in production with +-1% tolerance about the VxxPRIUV limits. All voltages are measured on pins.

3) VRSTxx parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as VxxPRIUV parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.

4) In case the application is using 3.3V single supply (Single Supply mode (e), i.e. VEXT and VDDP3 are shorted together), it is recommended to use secondary supply monitoring on channel VDDP3, because of the better accuracy of parameter VDDP3MON.

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5) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

Table 3-33 Supply Ramp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & V_{EVRSB} supply ramp-up and ramp-down slope 1) 2) 3)	*dVEXT/dt* SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope 1)3)	*dVDDP3/dt* SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope 1)3)	*dVDD/dt* SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope 1)3)	*dVDDM/dt* SR	8.3E-6	1	100	V/ms	

1) The device is robust against residual voltage ramp-up starting between 0 - 2.97 V for VEXT, VEVRSB, VDDP3 and VDDM and 0-1 V for VDD. A voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation.
2) Also valid in case EVR33 or EVRC is used. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
3) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

- Up to 1000000 power-cycles, matching the limits defined in the table 'Supply Ramp' are allowed for TC37x, without any restriction to reliability.

Table 3-34 EVRC SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} Voltage range	V_{IN} SR	2.97	-	5.5	V	Start-up VEXT voltage > 2.6 V
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 1mA ; I_{DDDC} ≤ 1.5A ; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	V_{DDDCT} CC	1.225	1.25	1.275	V	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 1mA ; I_{DDDC} ≤ 1.5A

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Table 3-34 EVRC SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Programmable switching frequency	f_{DCDC} SR	1.6	1.82	2.0	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation.
		-	0.8	-	MHz	Start-up frequency switches from 500 KHz in open loop operation to 1.82 MHz in closed loop Operation. 0.8 MHz to be set in SW.
Startup time	t_{STRDC} CC	-	-	900	µs	SMPS Start-up Mode. It is is defined beween $V_{EXTPRIUV}$ reset threshold till PORST release, on condition that all other PORST requirements were released before. I_{START} < 700mA.
Switching frequency modulation spread	Δf_{DCSPR} CC	-	1.8%	-	MHz	
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	16	mV	V_{EXT} ≥ 2.97V ; V_{EXT} ≤ 5.5V ; I_{DDDC} ≥ 300mA ; I_{DDDC} ≤ 1.5A ; ΔV_{DDDC} = (Peak to Peak ripple / 2)
No load current consumption of SMPS regulator	I_{DCNL} CC	-	15	19	mA	f_{DCDC}=1.82MHz; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C
		-	5	-	mA	LPM mode; I_{DDDC}=I_{SLEEP}; V_{EXT} > 2.97 V; T_J=25°C

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Table 3-34 EVRC SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SMPS regulator load transient response	dV_{DDDCT} / dI_{OUT} CC	-50	-	75	mV	dI < -250mA ; I_{DDDC}=280-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-50	-	87	mV	dI < -450mA ; I_{DDDC}=500-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-100	-	145	mV	dI < -700mA ; I_{DDDC}=750-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=100 us
		-26	-	26	mV	dI < 100mA ; I_{DDDC}=50-1500mA; t_r=0.1us; t_f=0.1us; V_{DDDC}=1.25V; T_{settle}=20us;
Maximum output current	I_{MAX} CC	100	-	-	mA	LPM mode. Typical current in LPM Mode = I_{SLEEP}
		1.5	-	-	A	limited by thermal constraints and component choice
SMPS regulator line transient response	dV_{DDDCT} / dV_{IN} CC	-75	-	75	mV	dV/dT=120V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
		-12.5	-	12.5	mV	dV/dT=1V/ms; dV < 2.97 - 5.5V ; I_{DDDC}=50-1500mA;
SMPS regulator efficiency	n_{DC} CC	-	80	-	%	V_{IN}=3.3V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
		-	75	-	%	V_{IN}=5V; I_{DDDC}=1500mA; f_{DCDC}=1.82MHz
Input Synchronisation frequency	$f_{DCDCSYNC}$ SR	1.6	1.82	2.0	MHz	

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Table 3-35 EVRC SMPS External components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value [1]	C_{OUT} SR	20.8	32	43.2	µF	I_{DDDC}=1.5A; f_{DDDC} = 0.8MHz
		15.4	22	29.7	µF	I_{DDDC}=1.5A; f_{DDDC} = 1.82MHz
External output capacitor ESR	C_{OUT_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=10Hz
External input capacitor value [1]	C_{IN} SR	6.5	10	13.5	µF	I_{DDDC}=1.5A
		4.42	6.8	9.18	µF	I_{DDDC}=500mA
External input capacitor ESR	C_{IN_ESR} SR	-	-	50	mOhm	f≥0.5MHz ; f≤10MHz
		-	-	100	Ohm	f=100Hz
External inductor value	L_{DC} SR	3.29	4.7	6.11		f_{DCDC}=0.8MHz
		2.31	3.3	4.29	µH	f_{DCDC}=1.82MHz
External inductor DCR	L_{DC_DCR} SR	-	-	0.2	Ohm	
P + N-channel MOSFET logic level	V_{LL} SR	-	-	2.5	V	
P + N-channel MOSFET drain source breakdown voltage	$\|V_{BR_DS}\|$ SR	+7	-	-	V	NMOS - V_{GS} = 0.
		-	-	-7	V	PMOS - V_{GS} = 0.
P + N-channel MOSFET drain source ON-state resistance	R_{ON} SR	-	150	-	mOhm	I_{DDDC}=1.5A; $\|V_{GS\|}$=2.5V ; T_A=25°C
		-	200	-	mOhm	I_{DDDC}=500mA; $\|V_{GS\|}$=2.5V ; T_A=25°C
P + N-channel MOSFET Gate Charge	Q_G SR	-	-	8	nC	I_{DDDC}=1.5A; NMOS- $\|V_{GS\|}$=5V; 1.5A pulsed drain current
		-8	-	-	nC	I_{DDDC}=1.5A; PMOS- $\|V_{GS\|}$=5V; 1.5A pulsed drain current
		-	-	4	nC	I_{DDDC}=500mA; NMOS- $\|V_{GS\|}$=5V; 0.5A pulsed drain current
		-4	-	-	nC	I_{DDDC}=500mA; PMOS- $\|V_{GS\|}$=5V; 0.5A pulsed drain current
External Inductor Saturation Current Margin	ΔI_{SAT} SR	400	-	-	mA	The saturation current of the coil must be larger than I_{DDDC} + ΔI_{SAT}

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Table 3-35 EVRC SMPS External components (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
P + N-channel MOSFET Gate threshold voltage	V_{GSTH} SR	-	1	-	V	NMOS
		-	-1	-	V	PMOS
N-channel MOSFET reverse diode forward voltage	V_{RDN} SR	-	0.8	-	V	

1) Capacitor min-max range represent typical +-35% tolerance including DC bias effect. The trace resistance from the capacitor to the supply or ground rail should be limited to 25 mOhm.

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3.16 System Phase Locked Loop (SYS_PLL)

Table 3-36 PLL System

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

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3.17 Peripheral Phase Locked Loop (PER_PLL)

Table 3-37 PLL Peripheral

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	D_{PP} CC	-1000	-	1000	ps	Peak only
Peak accumulated jitter	D_{PPI} CC	-700	-	700	ps	Peak only
RMS Accumulated jitter	D_{RMS} CC	-100	-	100	ps	measured over 1 µs; f_{REF} = 20 MHz and f_{DCO} = 640 MHz or f_{REF} = 25 MHz and f_{DCO} = 800 MHz
Peak Period jitter	DP CC	-200	-	200	ps	f_{DCO} = 640 MHz or f_{DCO} = 800 MHz
Absolute RMS jitter (PLL out)	J_{ABS10} CC	-125	-	125	ps	f_{REF} = 10 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS20} CC	-85	-	85	ps	f_{REF} = 20 MHz; f_{DCO} = 640 MHz
Absolute RMS jitter (PLL out)	J_{ABS25} CC	-85	-	85	ps	f_{REF} = 25 MHz; f_{DCO} = 800 MHz
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
DCO input frequency range	f_{REF} CC	10	-	40	MHz	
PLL lock-in time	t_L CC	4	-	100	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

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3.18 AC Specifications

All AC parameters are specified for the complete operating range defined in **Chapter 3.4** unless otherwise noted in column Note / Test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

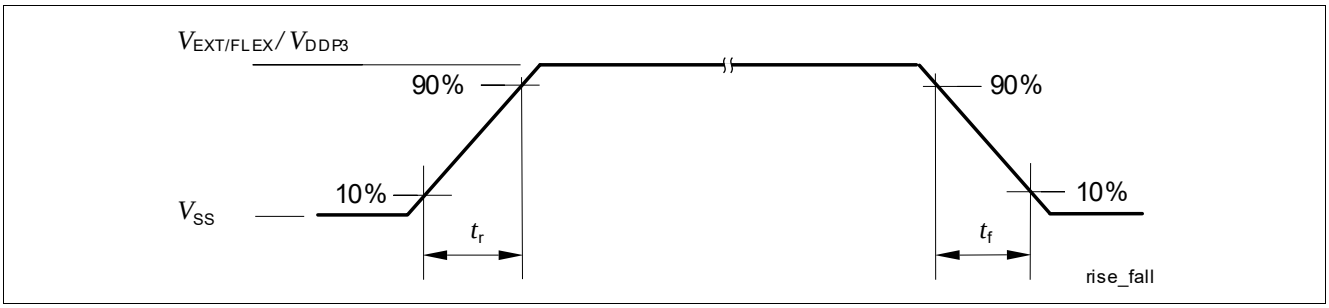


Figure 3-8 Definition of rise / fall times

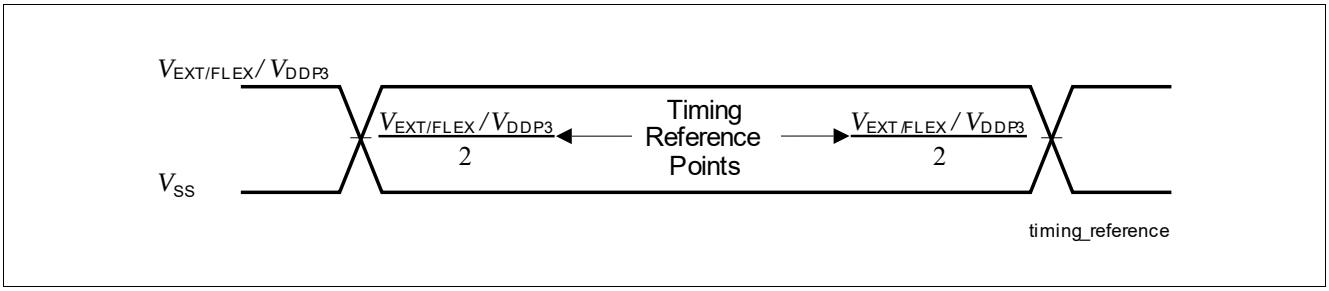


Figure 3-9 Time Reference Point Definition

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3.19 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Table 3-38 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	C_L≤20pF
		-	-	25	ns	C_L≤50pF
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	C_L≤50pF
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	C_L≤50pF

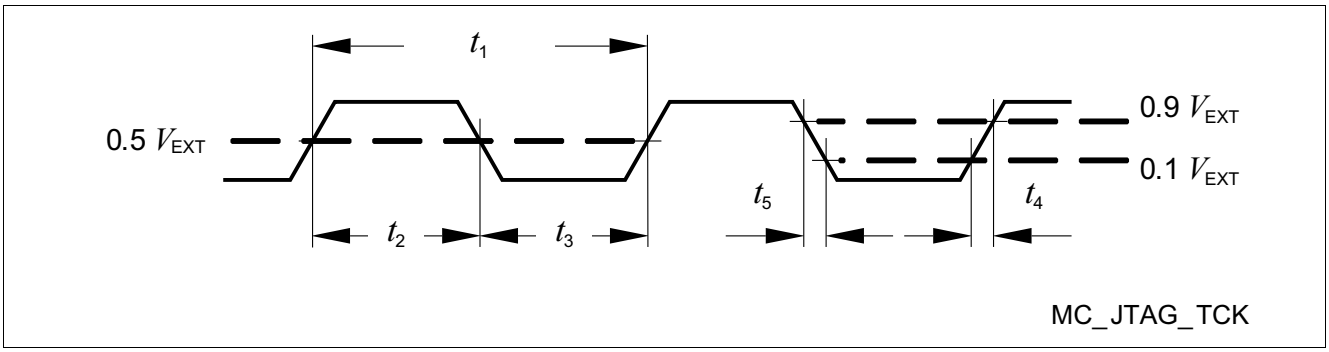


Figure 3-10 Test Clock Timing (TCK)

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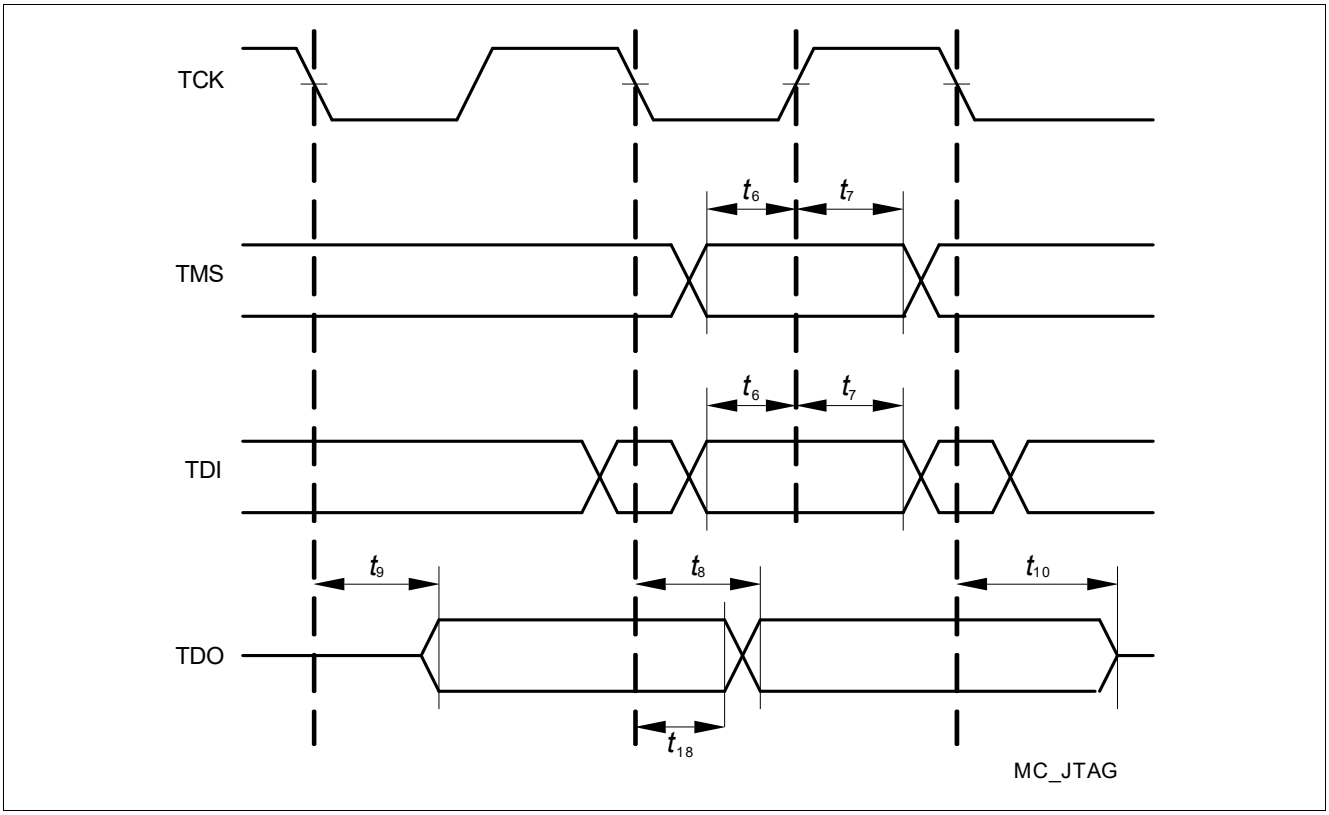


Figure 3-11 JTAG Timing

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3.20 DAP Parameters

The following parameters are applicable for communication through the DAP debug interface.

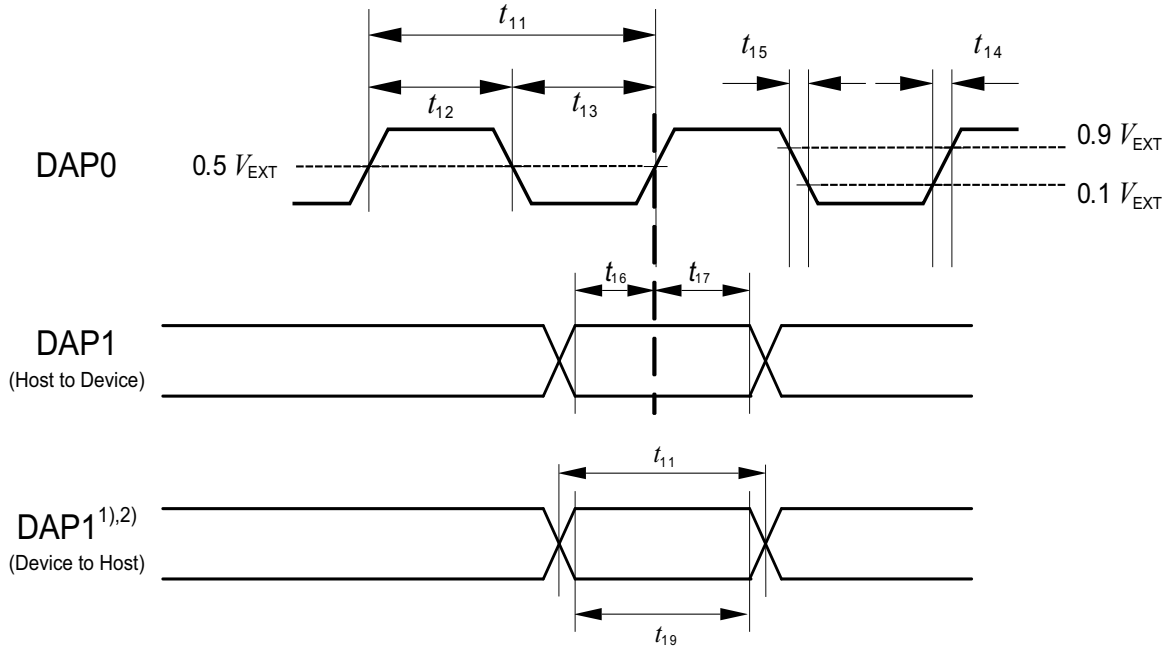
Table 3-39 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	C_L=20pF ; f=160MHz
		8	-	-	ns	C_L=20pF ; f=80MHz
		10	-	-	ns	C_L=50pF ; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

Table 3-40 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	C_L=20pF ; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	

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1) The DAP1 and DAP2 device to host timing is individual for both pins.
There is no guaranteed max. signal skew.

2) No explicite setup and hold times are given for DAP1 for the direction Device to Host.
Only t11 and t19 are guaranteed and the tool may set the sample point freely.

Figure 3-12 DAP Timing

Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

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3.21 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC37xEXT.

Note: Pad asymmetry is already included in the following timings.

Table 3-41 Master Mode strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	20	-	-	ns	C_L=25pF
Deviation from ideal duty cycle	t_{500} CC	-2	-	2	ns	C_L=25pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-3.5	-	3.5	ns	C_L=25pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-3	-	3.5	ns	C_L=25pF
MRST setup to ASCLKO latching edge	t_{52} SR	25	-	-	ns	C_L=25pF
MRST hold from ASCLKO latching edge	t_{53} SR	-2	-	-	ns	C_L=25pF

Table 3-42 Master Mode strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	50	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-5	-	5	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-7	-	7	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-7	-	7	ns	C_L=50pF
MRST setup to ASCLKO latching edge	t_{52} SR	35	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	C_L=50pF

Table 3-43 Master Mode medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	160	-	-	ns	C_L=50pF
Deviation from ideal duty cycle	t_{500} CC	-10	-	10	ns	C_L=50pF
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	C_L=50pF
ASLSOn delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	C_L=50pF

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Table 3-43 Master Mode medium (m) output pads (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	C_L=50pF
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	C_L=50pF

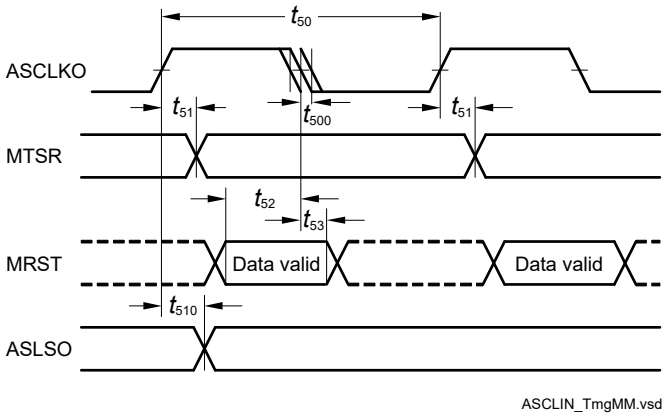


Figure 3-13 ASCLIN SPI Master Timing

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3.22 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC37xEXT.
It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

Note: Pad asymmetry is already included in the following timings.

Table 3-44 Master Mode Timing, LVDS output pads for data and clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	20 1)	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-1 1)	-	1 1)	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-3 1)	-	4 1)	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4 1)	-	5.5 1)	ns	C_L=25pF, driver strength ss
		-10 1)	-	10 1)	ns	C_L=25pF, driver strength sm
		-30 1)	-	30 1)	ns	C_L=25pF, driver strength m
MRST setup to SCLK latching edge	t_{52} SR	18 1)	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
		19.5 1)	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI4 only
MRST hold from SCLK latching edge	t_{53} SR	-1 1)	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) The load (C_L=25pF) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-45 Master Mode Strong Sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	t_{52} SR	25 1) 2)	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	t_{53} SR	-2 1)2)	-	-	ns	CL=25pF

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1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-46 Master Mode Strong Medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-7	-	7	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	35 [1) 2)]	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 [1)2)]	-	-	ns	CL=50pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-47 Master Mode Medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-20	-	20	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	80 [1) 2)]	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-15 [1)2)]	-	-	ns	CL=50pF
		-13 [1)2)]	-	-	ns	CL=50pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.
2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

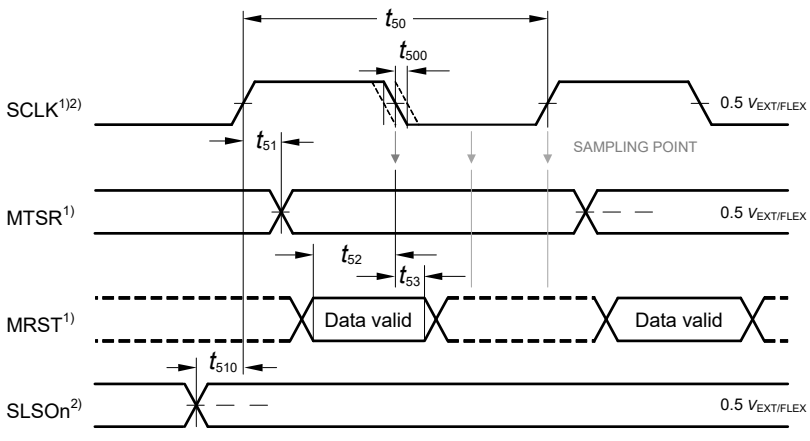
Table 3-48 Slave mode timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	4 x T_{MAX}	-	-	ns	
SCLK duty cycle	$t_{55/t54}$ SR	40	-	60	%	

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Table 3-48 Slave mode timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; C_L=50pF
		2	-	24	ns	driver = strong edge = sharp ; C_L=50pF
		15	-	80	ns	medium driver ; C_L=50pF
		14	-	-	ns	medium driver ; C_L=50pF; SCR SSC



1) This timing is based on the following setup: ECON.CPH = 1, ECON.CPOL = 0, ECON.B=0 (no sampling point delay).

2) t510 is the deviation from the ideal position configured with the leading delay, BACON.LPRE and BACON.LEAD > 0.

QSPI_TmgMM.vsd

Figure 3-14 Master Mode Timing

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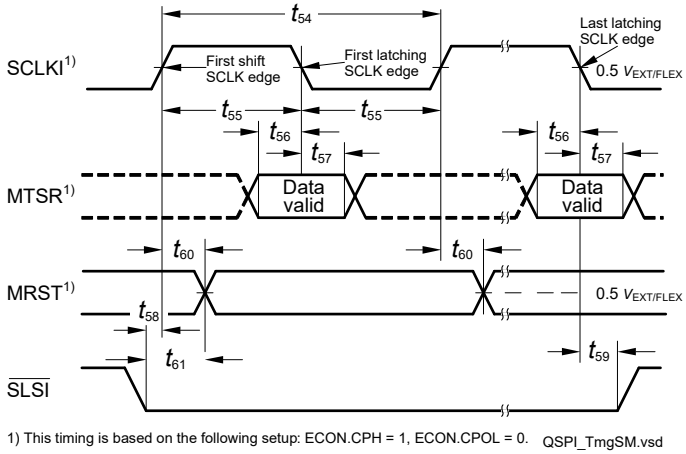


Figure 3-15 Slave Mode Timing

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3.23 MSC Timing 5 V Operation

The following section defines the timings.

Note: Pad asymmetry is already included in the following timings.

Note: Load for LVDS pads are defined as differential loads in the following timings.

Table 3-49 LVDS clock/data (LVDS pads in LVDS mode) valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A 1) 2) 3)	-	-	ns	LVDS; C_L=50pF
Deviation from ideal duty cycle	t_{400} CC	-1 3)	-	1 3)	ns	LVDS; 0 < C_L < 50pF
SOPx output delay	t_{44} CC	-3 3)	-	3 3)	ns	CL=50pF
ENx output delay	t_{45} CC	-4 3)	-	5 3)	ns	ss; C_L=50pF; ABRA block bypassed
		-4 3)	-	4 3)	ns	ss; C_L=50pF; ABRA block used
		-2 3)	-	10 3)	ns	sm; C_L=50pF
		-30 3)	-	30 3)	ns	m; C_L=50pF

1) T_A depends on the clock source selected for baud rate generation in the ABRA block of the MSC.
2) The capacitive load on the LVDS pins is differential, the capacitive load on the CMOS pins is single ended.
3) The load (C_L=50pF) defined in the condition list is a load definition for the single end signal EN and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-50 Strong sharp (ss) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-2	-	2	ns	CL=50pF
SOPx output delay	t_{44} CC	-4	-	3.5	ns	CL=50pF
ENx output delay	t_{45} CC	-4	-	3.5	ns	CL=50pF

Table 3-51 Strong medium (sm) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-5	-	5	ns	CL=50pF
SOPx output delay	t_{44} CC	-7	-	7	ns	CL=50pF
ENx output delay	t_{45} CC	-7	-	7	ns	CL=50pF

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Table 3-52 Medium (m) driver for clock/data valid for 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLPx clock period	t_{40} CC	2 * T_A	-	-	ns	CL=50pF
Deviation from ideal duty cycle	t_{400} CC	-10	-	10	ns	CL=50pF
SOPx output delay	t_{44} CC	-20	-	20	ns	CL=50pF
ENx output delay	t_{45} CC	-20	-	20	ns	CL=50pF

Table 3-53 Upstream Interface

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI bit time	t_{46} SR	8 * t_{MSC}	-	-	ns	
SDI rise time	t_{48} SR	-	-	200	ns	
SDI fall time	t_{49} SR	-	-	200	ns	

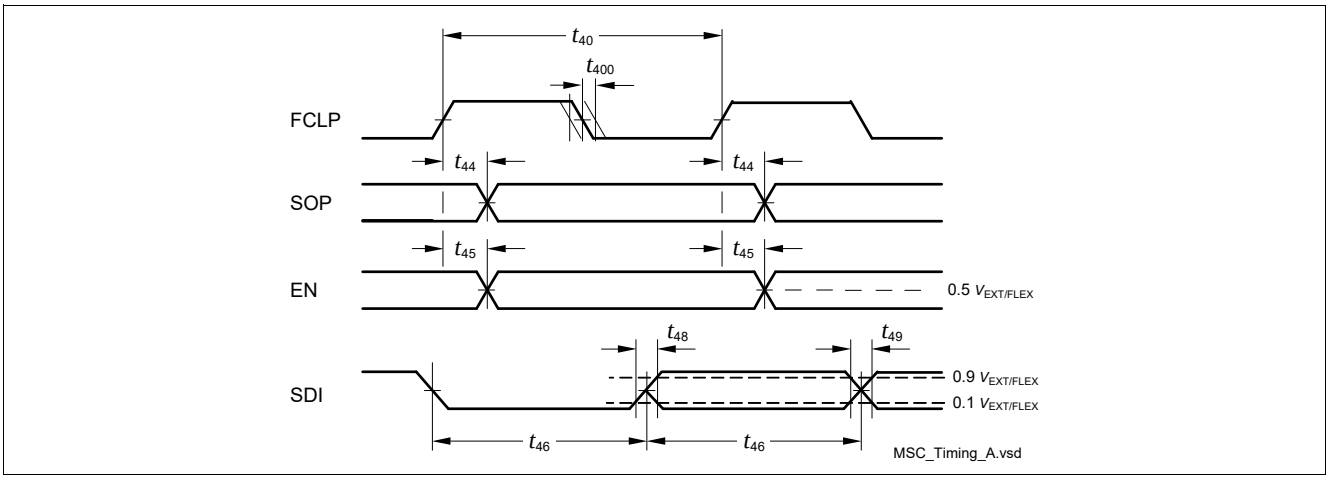


Figure 3-16 MSC Interface Timing

Note: The SOP data signal is sampled with the falling edge of FCLP in the target device.

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3.24 Ethernet Interface (ETH) Characteristics

3.24.1 ETH Measurement Reference Points

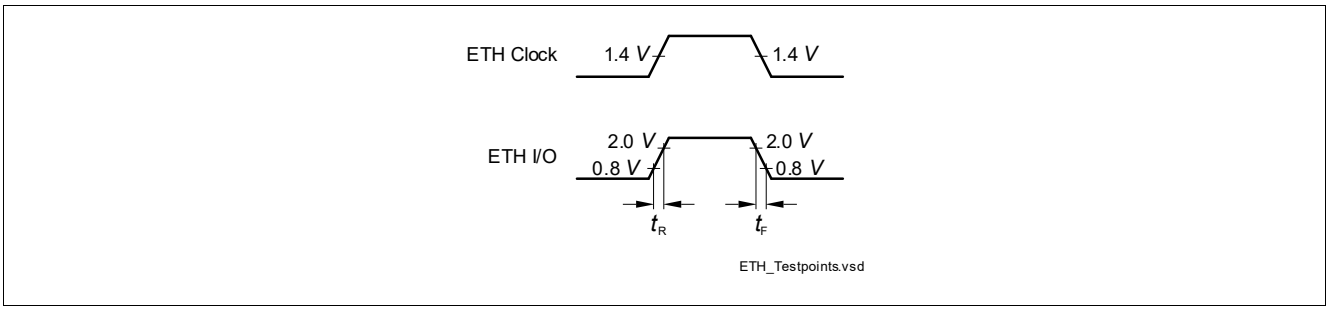


Figure 3-17 ETH Measurement Reference Points

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3.24.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 3-54 ETH Management Signal Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	-	-	ns	CL=25pF
ETH_MDC high time	t_2 CC	160	-	-	ns	CL=25pF
ETH_MDC low time	t_3 CC	160	-	-	ns	CL=25pF
ETH_MDIO setup time (output)	t_4 CC	10	-	-	ns	CL=25pF
ETH_MDIO hold time (output)	t_5 CC	10	-	-	ns	CL=25pF
ETH_MDIO data valid (input)	t_6 SR	0	-	300	ns	CL=25pF

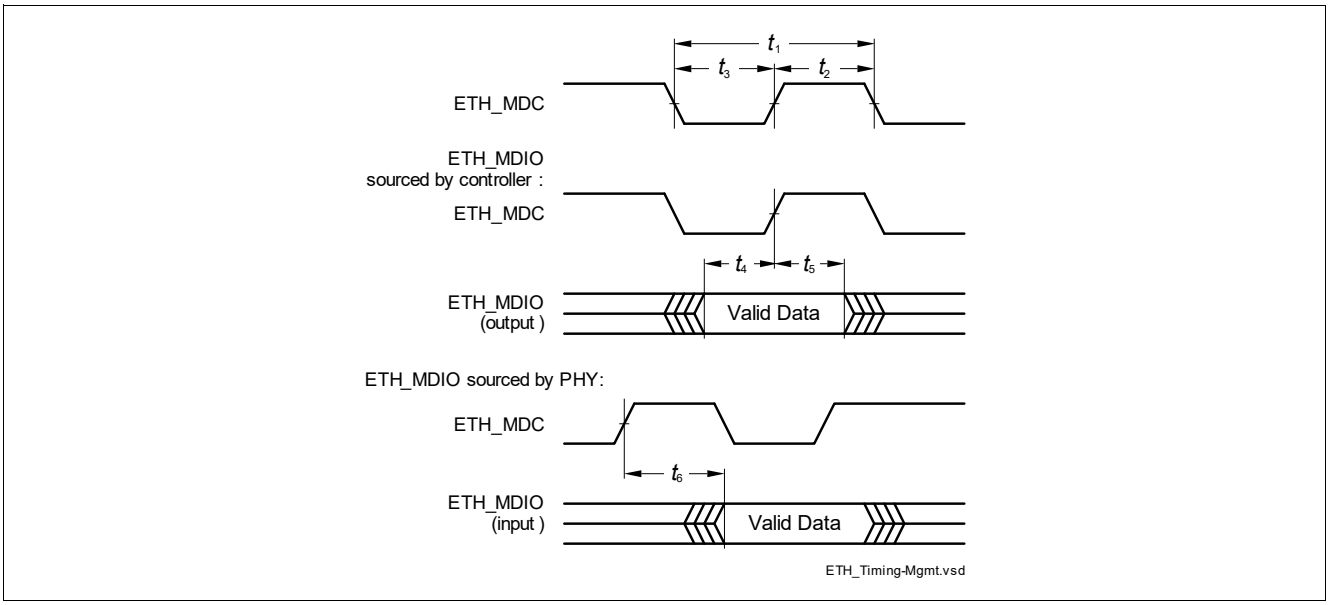


Figure 3-18 ETH Management Signal Timing

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3.24.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 3-55 ETH MII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_7 SR	-	40	-	ns	CL=25pF ; baudrate=100Mbps
		-	400	-	ns	CL=25pF ; baudrate=10Mbps
Clock high time	t_8 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Clock low time	t_9 SR	14	-	26	ns	CL=25pF ; baudrate=100Mbps
		140 1)	-	260 2)	ns	CL=25pF ; baudrate=10Mbps
Input setup time	t_{10} SR	10	-	-	ns	CL=25pF
Input hold time	t_{11} SR	10	-	-	ns	CL=25pF
Output valid time	t_{12} CC	0	-	25	ns	CL=25pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.

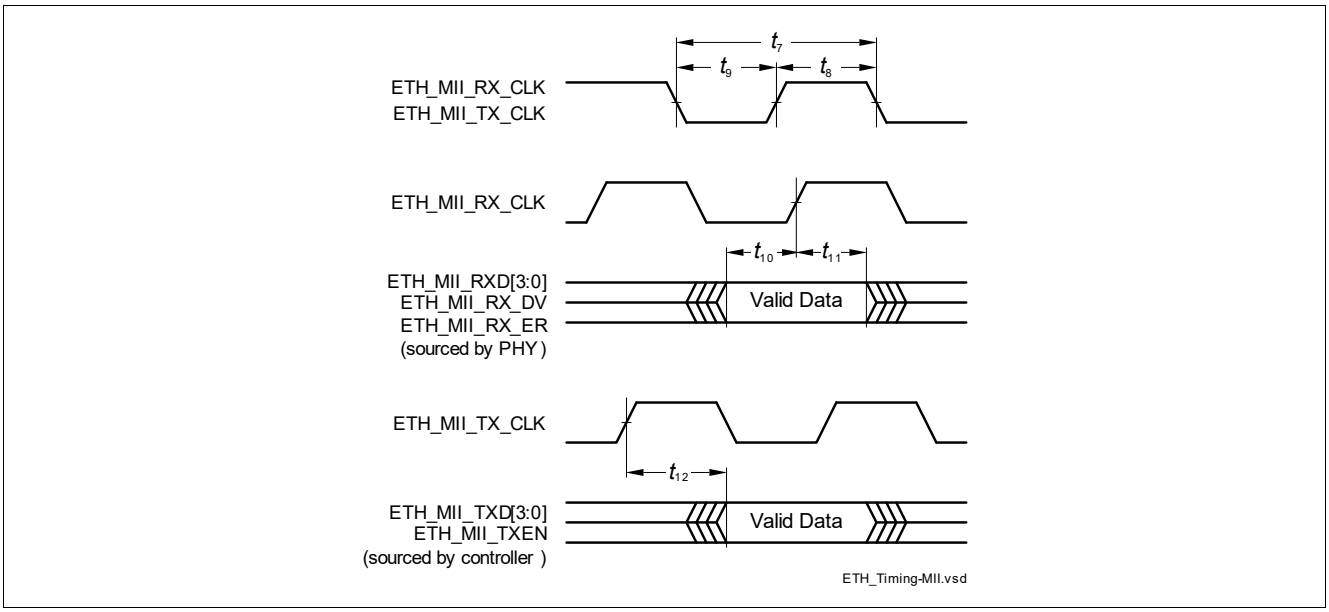


Figure 3-19 ETH MII Signal Timing

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3.24.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 3-56 ETH RMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	-	20	-	ns	50ppm ; CL=25pF
ETH_RMII_REF_CL clock high time	t_{14} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7 [1]	-	13 [2]	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; setup time [3]	t_{16} CC	4	-	-	ns	CL=25pF
ETHTXEN, ETHTXD[1:0], ETHRXD[1:0], ETHCRSDV; hold time [3]	t_{17} CC	2	-	-	ns	CL=25pF

1) Defined by 35% of clock period.
2) Defined by 65% of clock period.
3) For ETHRXD and ETHCRSDV signals this parameter is a SR.

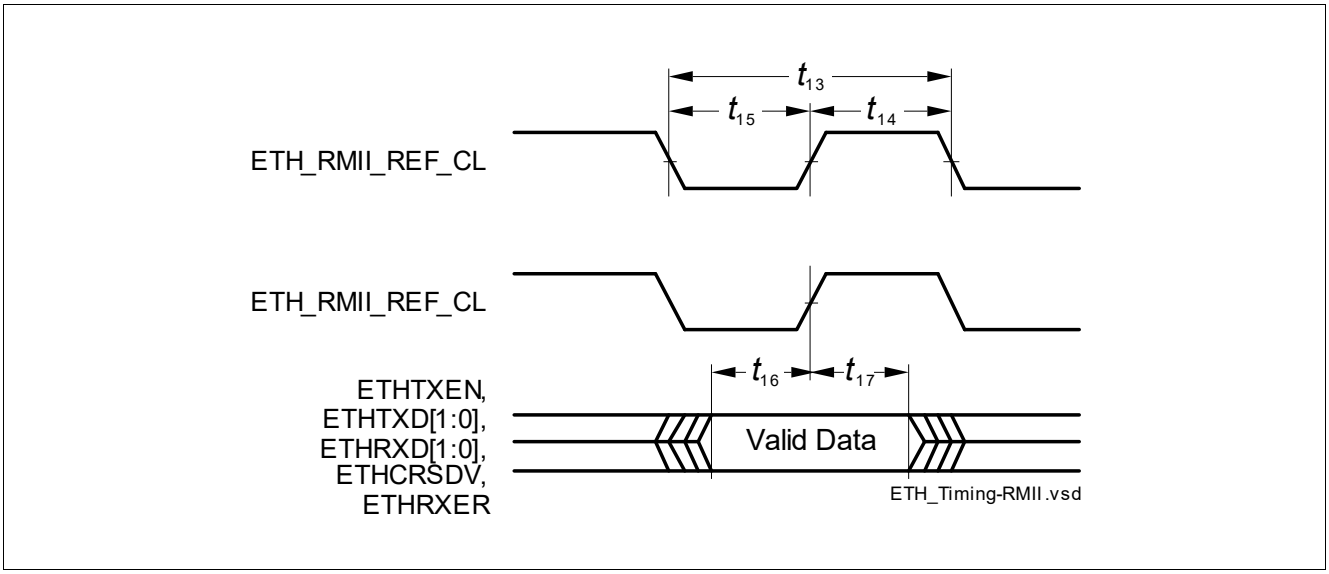


Figure 3-20 ETH RMII Signal Timing

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3.24.5 ETH RGMII Parameters

In the following, the parameters of the RGMII are described.

Table 3-57 ETH RGMII Signal Timing Parameters valid for 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TX Clock period	t_{19} CC	36	40	44	ns	100Mbps
		360	400	440	ns	10Mbps
		7.2	8	8.8	ns	Gigabit
Data to Clock Output skew	t_{20} CC	-500	0	500	ps	
Data to Clock input skew (at receiver)	t_{21} SR	1	1.8	2.6	ns	
Clock duty cycle	t_{duty} CC	40	50	60	%	10/100Mbps
		45	50	55	%	Gigabit
GREFCLK duty cycle	t_{duty_in} SR	45	-	55	%	
GREFCLK Input accuracy	ACC SR	-0.005	-	0.005	%	

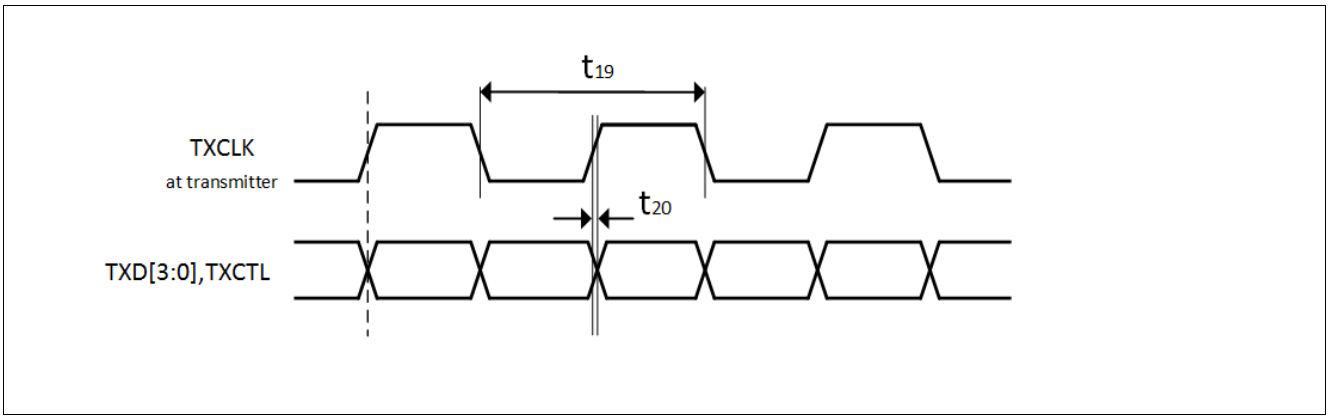


Figure 3-21 ETH RGMII TX Signal Timing (Delay on Destination (DoD))

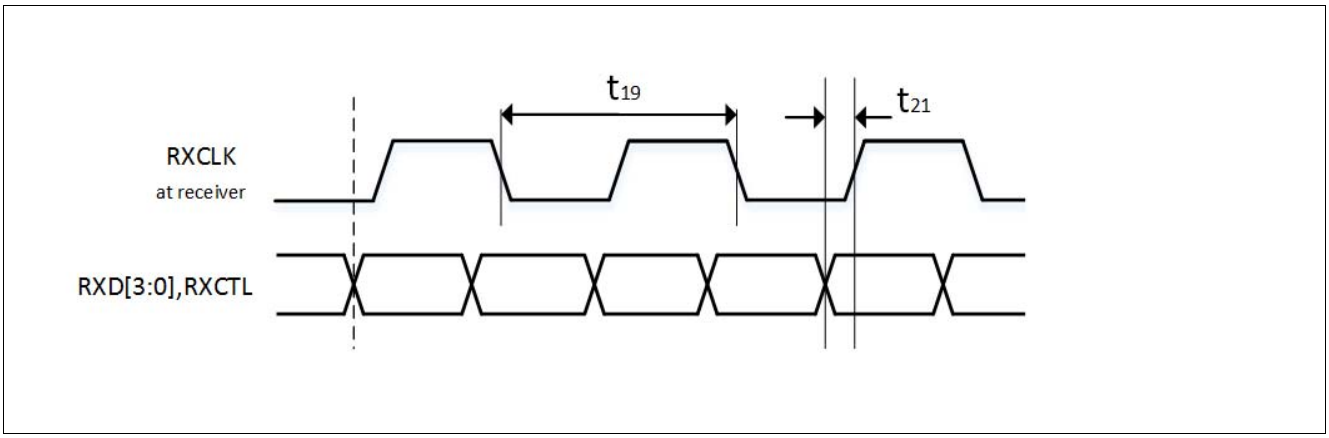


Figure 3-22 ETH RGMII RX Signal Timing (Delay on Source (DoS))

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3.25 E-Ray Parameters

The timings of this section are valid for the strong driver and sharp edge settings of the output drivers with C_L = 25 pF.

Table 3-58 Transmit Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25}$ CC	-	-	9	ns	C_L=25pF
Fall time of TxEN	$t_{dCCTxENFall25}$ CC	-	-	9	ns	C_L=25pF
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25}$ CC	-	-	9	ns	20% - 80% ; C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10}$ CC	-	-	25	ns	
Asymmetry of sending	t_{tx_asym} CC	-2.45	-	2.45	ns	C_L=25pF
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01}$ CC	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10}$ CC	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	t_{txd_sum} CC	-	-	9	ns	

Table 3-59 Receive Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25}$ SR	-30.5	-	43.0	ns	C_L=25pF
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15}$ SR	-31.5	-	44.0	ns	C_L=15pF
Threshold for detecting logical high	$T_{uCCLogic1}$ SR	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0}$ SR	30	-	65	%	

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Table 3-59 Receive Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

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3.26 HSCT Parameters

Table 3-60 HSCT - Rx parasitics and loads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitance total budget	C_{total} CC	-	3.5	5	pF	Total Budget for complete receiver including silicon, package, pins and bond wire
Parasitic inductance budget	*Htotal* CC	-	5	-	nH	

Table 3-61 HSCT - Rx/Tx setup timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX o/p duty cycle	*DCrx* CC	40	-	60	%	
Disable time of the LVDS pad	$t_{LVDSDIS}$ CC	-	-	20	ns	
Enable time of the LVDS pad	t_{LVDSEN} CC	-	-	400	ns	
Wakeup time from Sleep Mode	t_{SWU} CC	-	-	250	ns	
Maximum length of a wake-up glitch that does not wake-up the receiver	t_{WUP} CC	-	-	0.2	ns	
Bias startup time	t_{bias} CC	-	5	10	µs	Bias distributor waking up from power down and provide stable Bias.
RX startup time	t_{rxi} CC	-	-	600	ns	Wake-up RX from power down.
TX startup time	t_{tx} CC	-	-	280	ns	Wake-up TX from power down.

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3.27 Inter-IC (I2C) Interface Timing

This section defines the timings for I2C in the TC37xEXT.

All I2C timing parameter are SR for Master Mode and CC for Slave Mode.

Table 3-62 I2C Standard Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	-	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	-	-	1000	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	250	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Hold time for the (repeated) START condition	t_7	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

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Table 3-62 I2C Standard Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Set-up time for (repeated) START condition	t_8	4.7	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	4	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-63 I2C Fast Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Bus free time between a STOP and ATART condition	t_{10}	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Rise time of both SDA and SCL	t_2	20+0.1*C_b	-	300	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data hold time	t_3	0	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Data set-up time	t_4	100	-	-	ns	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Low period of SCL clock	t_5	1.3	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
High period of SCL clock	t_6	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

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Table 3-63 I2C Fast Mode Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Hold time for the (repeated) START condition	t_7	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for (repeated) START condition	t_8	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line
Set-up time for STOP condition	t_9	0.6	-	-	µs	Measured with a pull-up resistor of 4.7 kohms at each of the SCL and SDA line

Table 3-64 I2C High Speed Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Capacitive load for each bus line	C_b SR	-	-	400	pF	
Fall time of SCL	t_{11}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Fall time of SDA	t_{12}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Rise time of SCL	t_{13}	10 [1]	-	40 [1]	ns	bus line load of 100pF
Rise time of SDA	t_{14}	10 [1]	-	80 [1]	ns	bus line load of 100pF
Data hold time	t_3	0 [1]	-	70 [1]	ns	bus line load of 100pF
Data set-up time	t_4	10 [1]	-	-	ns	bus line load of 100pF
Low period of SCL clock	t_5	160 [1]	-	-	ns	bus line load of 100pF
High period of SCL clock	t_6	60 [1]	-	-	ns	bus line load of 100pF
Hold time for the (repeated) START condition	t_7	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for (repeated) START condition	t_8	160 [1]	-	-	ns	bus line load of 100pF
Set-up time for STOP condition	t_9	160 [1]	-	-	ns	bus line load of 100pF

1) Values are defined for C_b = 100pF, for the Timing of C_b = 400pF see the I2C Standard.

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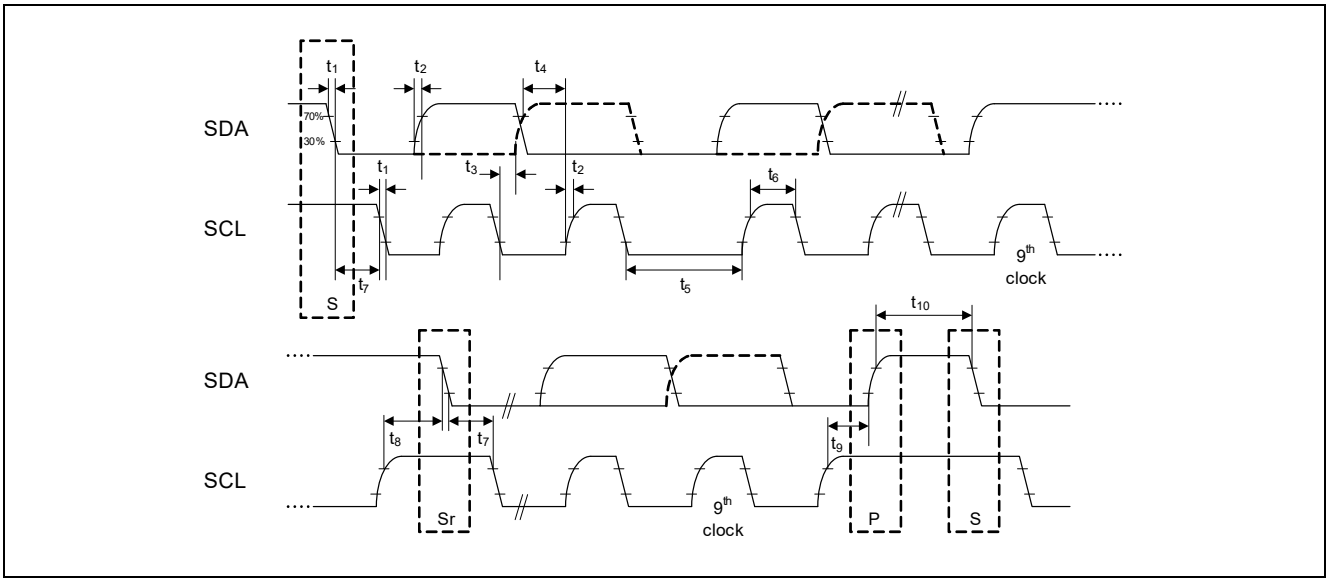


Figure 3-23 I2C Standard and Fast Mode Timing

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3.28 SDMMC Interface Timing

Table 3-65 SDMMC

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period Data Transfer Mode	t_1 CC	20	-	-	ns	push-pull, C_L ≤ 30pF, V_{EXT} = 3.3V
Clock period Indentification Mode	t_2 CC	-	-	2500	ns	open-drain, C_L ≤ 30pF, V_{EXT} = 3.3V
Clock low time	t_3 CC	6,5	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V
Clock high time	t_4 CC	6,5	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V
Data output valid time before rising clock edge	t_5 CC	3	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V
Data output valid time after rising clock edge	t_6 CC	3	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V
Data input hold time	t_7 SR	2,5	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V, TTL levels
Data Input delay time	t_8 SR	-	-	13,7	ns	C_L ≤ 30pF, V_{EXT} = 3.3V, TTL levels
Data Input setup time	t_9 SR	5,2	-	-	ns	C_L ≤ 30pF, V_{EXT} = 3.3V, TTL levels

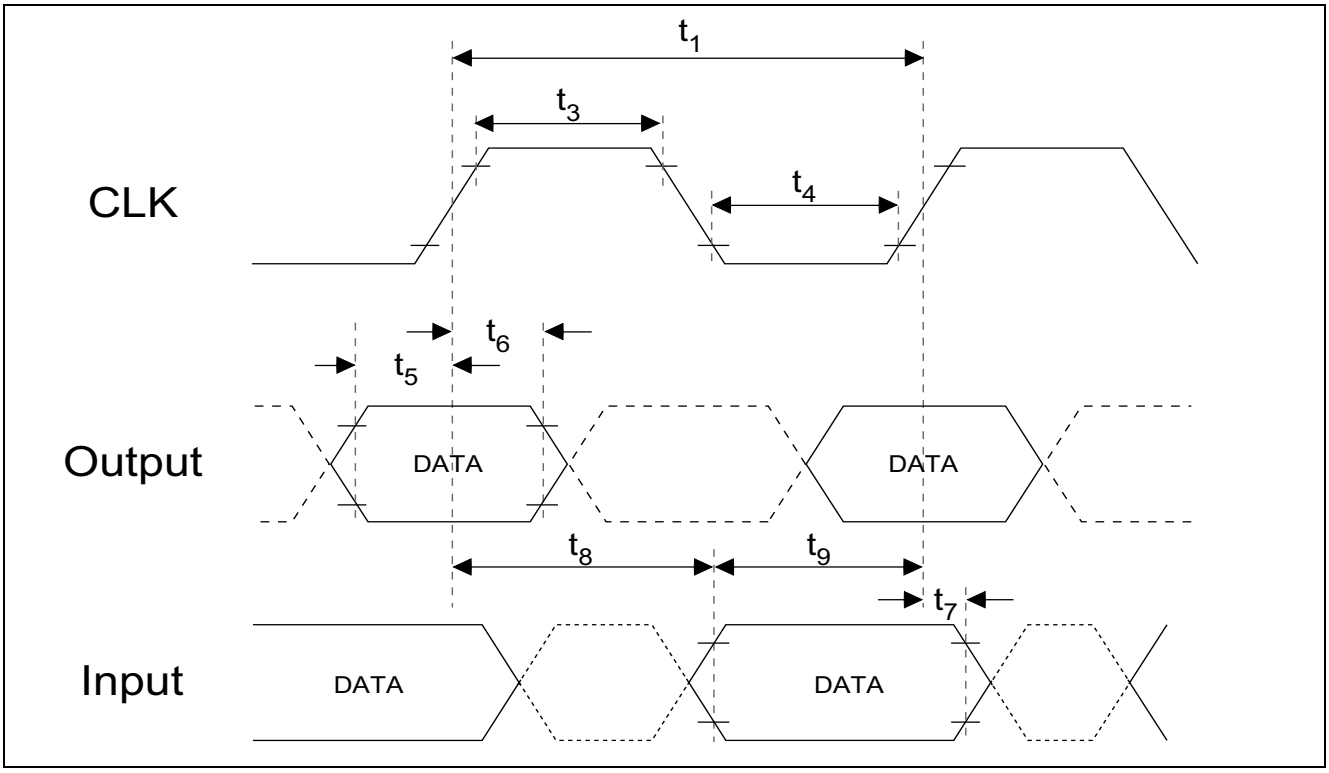


Figure 3-24 SDMMC Timing

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3.29 Camera Interface Timing (CIF)

Table 3-66 Timings for 3.3V+-10% pad power supply

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pixel clock period	t_{70} SR	10.42	-	-	ns	
HSYNC, VSYNC set up time	t_{71} SR	2.5	-	-	ns	CIF input level
		2.5	-	-	ns	AL input level
HSYNC, VSYNC hold time	t_{72} SR	2.5	-	-	ns	CIF input level
		2.5	-	-	ns	AL input level
Pixel data set up time	t_{73} SR	2.5	-	-	ns	AL input level
		2.5	-	-	ns	CIF input level
Pixel data hold time	t_{74} SR	2.5	-	-	ns	CIF input level
		2.5	-	-	ns	AL input level

Table 3-67 Timings for 0.4V to 2.4V input signals (2.8V imager)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pixel clock period	t_{70} SR	12.5	-	-	ns	
HSYNC, VSYNC set up time	t_{71} SR	3	-	-	ns	CIF Input Levels, 3.3V±10%
HSYNC, VSYNC hold time	t_{72} SR	3	-	-	ns	CIF Input Levels, 3.3V±10%
Pixel data set up time	t_{73} SR	3	-	-	ns	CIF Input Levels, 3.3V±10%
Pixel data hold time	t_{74} SR	3	-	-	ns	CIF Input Levels, 3.3V±10%

Table 3-68 Timings for 1.8V imager, CIF input level

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pixel clock period	t_{70} SR	10.42	-	-	ns	
HSYNC, VSYNC set up time	t_{71} SR	2	-	-	ns	Input signal 0.4V to 1.4V
HSYNC, VSYNC hold time	t_{72} SR	2	-	-	ns	Input signal 0.4V to 1.4V
Pixel data set up time	t_{73} SR	2	-	-	ns	Input signal 0.4V to 1.4V
Pixel data hold time	t_{74} SR	2	-	-	ns	Input signal 0.4V to 1.4V

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3.30 Flash Target Parameters

Table 3-69 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector [1]	t_{ERP} CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command [1]	t_{MERP} CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode [1]	t_{PRP5} CC	-	-	80	µs	32 Byte
Program Flash program time per page in 3.3 V mode [1]	t_{PRP3} CC	-	-	115	µs	32 Byte
Program Flash program time per burst in 5 V mode [1]	t_{PRPB5} CC	-	-	220	µs	256 Byte
Program Flash program time per burst in 3.3 V mode [1]	t_{PRPB3} CC	-	-	530	µs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication [1]	t_{PRPB3_1MB} CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_1MB} CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication [1]	t_{PRPB5_PF} CC	-	-	6	s	Derived value for documentation purpose
Write Page Once adder [1]	t_{ADD} CC	-	-	20	µs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency [1]	t_{SPNDP} CC	-	-	120	µs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD} CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC} CC	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD} CC	-	-	500	cycles	

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Table 3-69 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page [1)2)]	t_{PRD} CC	-	-	75	µs	8 Byte
Complete Device Flash Erase Time PFlash and DFlash [1)3) 4) 5)]	t_{ER_Dev} CC	-	4.3	7	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst [1)2)]	t_{PRDB} CC	-	-	140	µs	32 Byte
Data Flash suspend to read latency [1)]	t_{SPNDD} CC	-	-	120	µs	
Wait time after margin change	$t_{FL_MarginDel}$ CC	-	-	2	µs	
Program Flash Endurance per Logical Sector	N_{E_P} CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP} CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF} CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF} CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) [6)]	N_{ERD0C} CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) [7)]	N_{ERD0S} CC	-	-	750000	cycles	

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Table 3-69 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) [6]	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) [7]	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) [8]	N_{E_EEP10C} CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) [8]	N_{E_EEP10S} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) [8]	N_{E_HSMC} CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) [8]	N_{E_HSMS} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	
Data Flash Erase Time per Sector [1][3][5]	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector [1][3][5]	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode [1]	$t_{ER_ADDC32C}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

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Table 3-69 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command [1)3)5)]	t_{MERD1} CC	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors ≤ 256KBytes
Data Flash Erase Time per Multi-Sector Command [1)3)5)]	t_{MERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors ≤ 256 kByte
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF_low_VDDP3}$ CC	-	-	60	ns	see register DMU_HF_PWAIT.CFLASH
Data Flash Erase Verify time per page (Complement Sensing) [2)]	$t_{VER_PAGE_DC}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) [1)]	$t_{VER_PAGE_DS}$ CC	-	-	10	µs	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page [1)]	$t_{VER_PAGE_P}$ CC	-	-	10	µs	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) [1)]	$t_{VER_SEC_DC}$ CC	-	-	200	µs	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) [1)]	$t_{VER_SEC_DS}$ CC	-	-	360	µs	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector [1)]	$t_{VER_SEC_P}$ CC	-	-	360	µs	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) [1)]	$t_{VER_WL_DC}$ CC	-	-	30	µs	
Data Flash Erase Verify time per wordline (Single Ended Sensing) [1)]	$t_{VER_WL_DS}$ CC	-	-	50	µs	
Program Flash Erase Verify time per wordline [1)]	$t_{VER_WL_P}$ CC	-	-	30	µs	

1) Only vaild for f_{FSI} = 100MHz.

2) Time is not dependent on program mode (5V or 3.3V).

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3) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
4) Using 512 kByte / 256 kByte erase commands (PFlash / DFlash).
5) If the DataFlash is operated in Complement Sensing Mode the erase time is increased by erase_size / 32kByte x tER_ADDC32C
6) Allows segmentation of addressable memory into 8 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
7) Allows segmentation of addressable memory into 6 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD}.
8) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

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3.31 Quality Declarations

Table 3-70 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	*MSL* CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500 [1]	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000 [2]	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

1) Pads of the AGBT interface are limited to a maximum value of 250V.

2) Pads of the AGBT interface are limited to a maximum value of 1000V.

Example Temperature Profile

The following temperature profile is an example. Application specific temperature profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-71 Example Temperature Profile

T_J=	Duration [h]	Comment
≤ 170°C	≤ 30	
≤ 160°C	≤ 120	
≤ 150°C	≤ 220	
≤ 140°C	≤ 350	
≤ 130°C	≤ 780	
≤ 120°C	≤ 1600	
≤ 110°C	≤ 3000	
≤ 100°C	≤ 7000	
≤ 90°C	≤ 8000	
≤ 80°C	≤ 2400	
≤ 70°C	≤ 1000	
	≤ 24500	total time

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Table 3-72 Example Inactive Lifetime Temperature Profile

T_J=	Duration [h]	Comment
≤ 55°C	≤ 150700	

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3.32 Package Outline

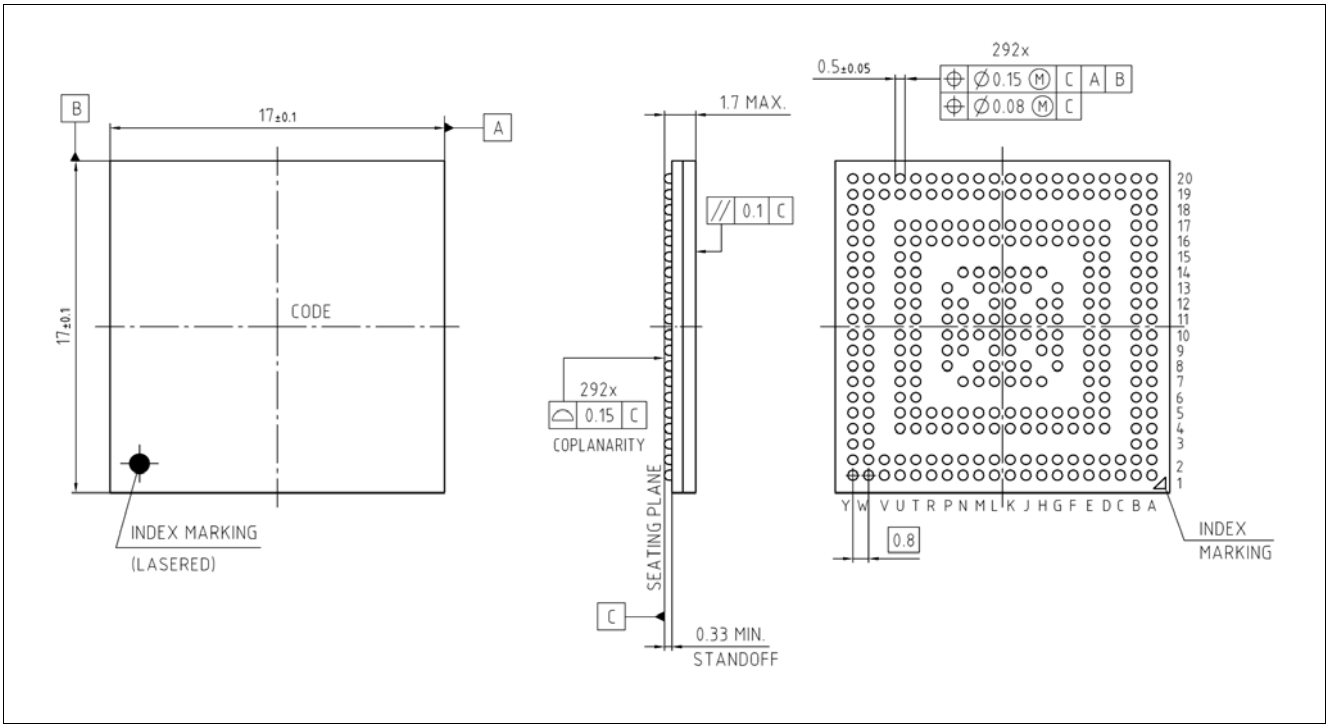


Figure 3-25 Package Outlines LFBGA-292

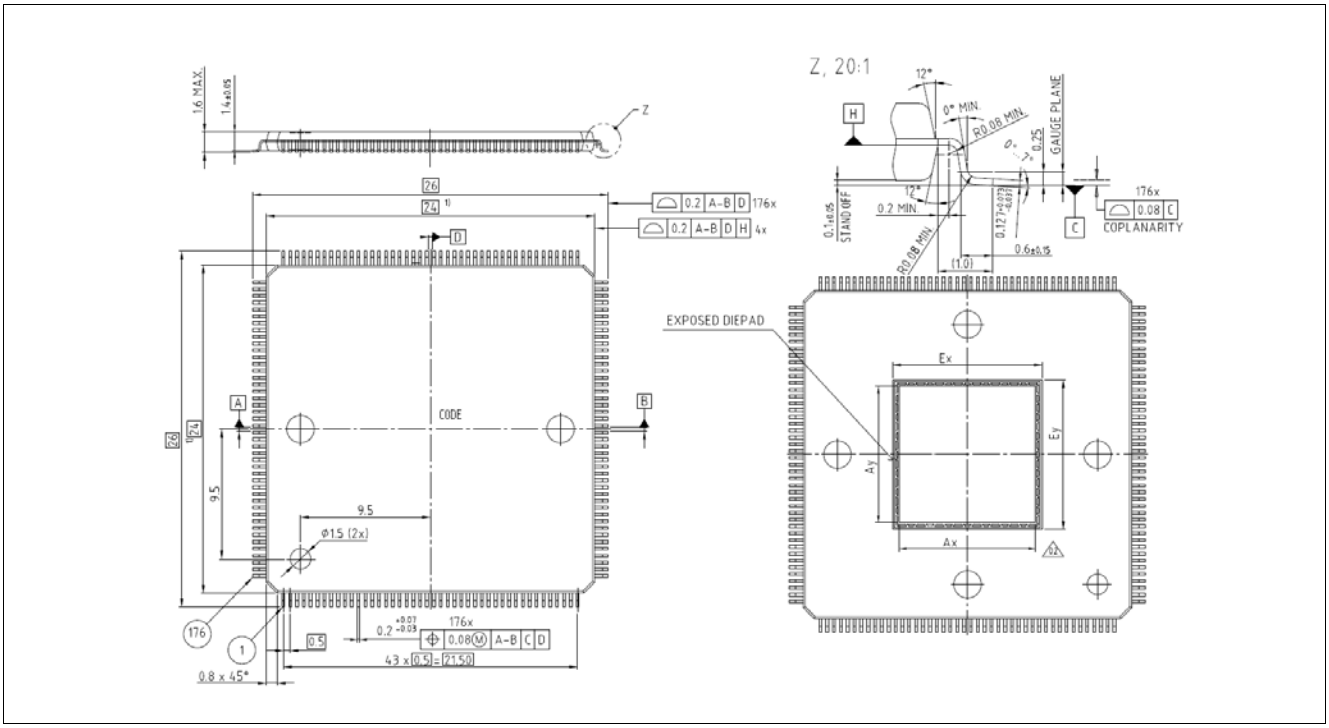


Figure 3-26 Package Outlines LQFP-176

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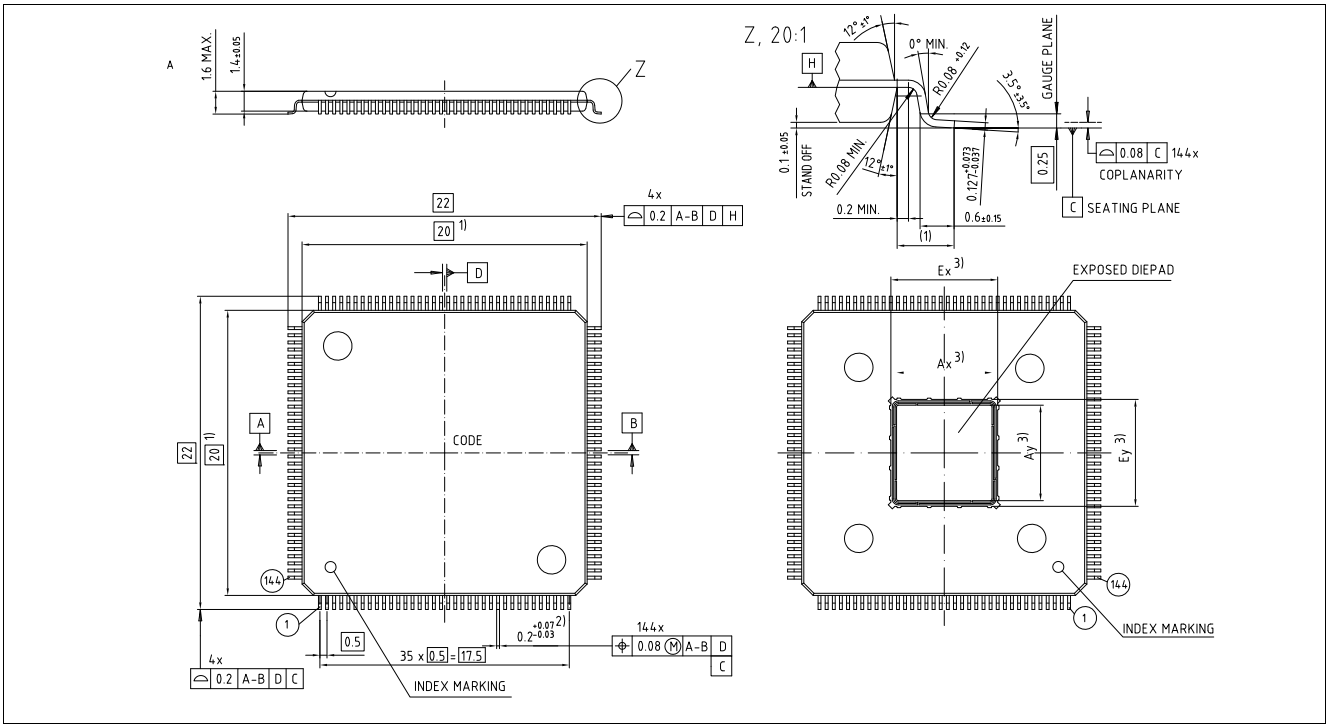


Figure 3-27 Package Outlines LQFP-144

Table 3-73 Exposed Pad Dimensions

Ex; nominal EPad size	8.7 mm ± 50 µm
Ey; nominal EPad size	8.7 mm ± 50 µm
Ax; solderable EPad size	7.9 mm ± 50 µm
Ay; solderable EPad size	7.9 mm ± 50 µm

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3.32.1 Package Parameters

Table 3-74 Package Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) [1]	RTH_JACC	-	-	22	K/W	LFBGA-292
		-	-	18	K/W	LQFP-144
		-	-	17	K/W	LQFP-176
Thermal resistance (junction to case bottom) [1]	RTH_JCBCC	-	-	4.5	K/W	LFBGA-292
		-	-	2	K/W	LQFP-144
		-	-	2	K/W	LQFP-176

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Table 3-74 Package Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to case top) [1]	RTH_JCTCC	-	-	5	K/W	LFBGA-292
		-	-	10	K/W	LQFP-144
		-	-	10	K/W	LQFP-176

1) The top and bottom thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) depend on the external system (PCB, case) characteristics and are under user responsibility. The junction temperature can be calculated using the following equation: TJ = TA + RTH_JA * PD, where the RTH_JA is the total thermal resistance between the junction and the ambient.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

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4 History

Version 0.4 is the first version of this document.

4.1 Changes from Version 0.4 to Version 0.6

Changes in chapter “Pin Definition and Functions”

- Changes in chapter TC37x T and TP - Pin Definition and Functions for package variant LFBGA-292
  - Changes in LFBGA-292 Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12
  - Changes in LFBGA-292 Package Variant 'Port 01 Functions' table; P01.5
  - Changes in LFBGA-292 Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.6, P02.7, P02.8,
  - Changes in LFBGA-292 Package Variant 'Port 10 Functions' table; P10.2, P10.5, P10.6, P10.7, P10.8
  - Changes in LFBGA-292 Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.2, P11.3, P11.4, P11.5, P11.6, P11.10, P11.12, P11.14
  - Changes in LFBGA-292 Package Variant 'Port 13 Functions' table; P13.1, P13.2
  - Changes in LFBGA-292 Package Variant 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5, P14.9, P14.10
  - Changes in LFBGA-292 Package Variant 'Port 15 Functions' table; P15.4, P15.5
  - Changes in LFBGA-292 Package Variant 'Port 20 Functions' table; P20.0, P20.3, P20.14
  - Changes in LFBGA-292 Package Variant 'Port 21 Functions' table; P21.0, P21.2, P21.3, P21.4, P21.5
  - Changes in LFBGA-292 Package Variant 'Port 22 Functions' table; P22.0, P22.1, P22.2, P22.4, P22.5, P22.6, P22.7, P22.8, P22.9, P22.10, P22.11
  - Changes in LFBGA-292 Package Variant 'Port 23 Functions' table; P23.1, P23.2, P23.3, P23.4, P23.5, P23.6, P23.7
  - Changes in LFBGA-292 Package Variant 'Port 32 Functions' table; P32.0, P32.1, P32.2, P32.3, P32.4, P32.6, P32.7
  - Changes in LFBGA-292 Package Variant 'Port 33 Functions' table; P33.0, P33.2, P33.5, P33.7, P33.10, P33.12, P33.13
  - Changes in LFBGA-292 Package Variant 'Port 34 Functions' table; P34.1, P34.2
  - Changes in LFBGA-292 Package Variant; Buffer Type changed for all Ports
  - Changes in LFBGA-292 Package Variant 'Analog Inputs' table; Buffer Type and Functions changed for all balls
  - Changes in LFBGA-292 Package Variant 'System I/O' table; Buffer Type changed for all balls
  - Changes in LFBGA-292 Package Variant 'System I/O' table; Symbol changed for balls Y17, W17
  - Changes in LFBGA-292 Package Variant 'System I/O' table; Function changed for balls Y17, W17,
  - Changes in LFBGA-292 Package Variant; 'Supply' table; Symbol and Function changed for balls L20, N19, N20
- Changes in chapter TC37x TE - Pin Definition and Functions for package variant LFBGA-292
  - Changes in LFBGA-292 Package Variant 'Port 00 Functions' table; P00.1, P00.2, P00.3, P00.4, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12
  - Changes in LFBGA-292 Package Variant 'Port 01 Functions' table; P01.5
  - Changes in LFBGA-292 Package Variant 'Port 02 Functions' table; P02.3, P02.4, P02.5

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  - Changes in LFBGA-292 Package Variant 'Port 10 Functions' table; P10.2, P10.5, P10.6
  - Changes in LFBGA-292 Package Variant 'Port 11 Functions' table; P11.0, P11.1, P11.2, P11.3, P11.4, P11.5, P11.10, P11.12
  - Changes in LFBGA-292 Package Variant 'Port 13 Functions' table; P13.1, P13.2
  - Changes in LFBGA-292 Package Variant 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5
  - Changes in LFBGA-292 Package Variant 'Port 15 Functions' table; P15.4, P15.5
  - Changes in LFBGA-292 Package Variant 'Port 20 Functions' table; P20.0, P20.6
  - Changes in LFBGA-292 Package Variant 'Port 21 Functions' table; P21.2, P21.3, P21.4, P21.5
  - Changes in LFBGA-292 Package Variant 'Port 23 Functions' table; P23.1
  - Changes in LFBGA-292 Package Variant 'Port 32 Functions' table; P32.1, P32.2, P32.4
  - Changes in LFBGA-292 Package Variant 'Port 33 Functions' table; P33.0, P33.2, P33.5, P33.7, P33.10
  - Changes in LFBGA-292 Package Variant; Buffer Type changed for all Ports
  - Changes in LFBGA-292 Package Variant 'Analog Inputs' table; Buffer Type and Functions changed for all balls
  - Changes in LFBGA-292 Package Variant 'System I/O' table; Buffer Type changed for all balls
  - Changes in LFBGA-292 Package Variant 'System I/O' table; Symbol changed for balls Y17, W17, M20, M19
  - Changes in LFBGA-292 Package Variant; 'Supply' table; Symbol and Function changed for balls L20, N19, N20
- Changes in chapter TC37x T and TP - Pin Definition and Functions for package variant LQFP-176
  - Changes in LQFP-176 Package Variant 'Port 00 Functions' table; P00.1, P00.2, P00.3, P00.4, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12
  - Changes in LQFP-176 Package Variant 'Port 02 Functions' table; P02.3, P02.4, P02.5
  - Changes in LQFP-176 Package Variant 'Port 10 Functions' table; P10.2, P10.5, P10.6
  - Changes in LQFP-176 Package Variant 'Port 11 Functions' table; P11.2, P11.3, P11.6, P11.10, P11.12
  - Changes in LQFP-176 Package Variant 'Port 13 Functions' table; P13.1, P13.2
  - Changes in LQFP-176 Package Variant 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5
  - Changes in LQFP-176 Package Variant 'Port 15 Functions' table; P15.4, P15.5
  - Changes in LQFP-176 Package Variant 'Port 20 Functions' table; P20.0
  - Changes in LQFP-176 Package Variant 'Port 21 Functions' table; P21.2, P21.3, P21.4, P21.5
  - Changes in LQFP-176 Package Variant 'Port 23 Functions' table; P23.1
  - Changes in LQFP-176 Package Variant 'Port 32 Functions' table; P32.0, P32.1, P32.2, P32.4
  - Changes in LQFP-176 Package Variant 'Port 33 Functions' table; P33.0, P33.2, P33.5, P33.7, P33.10
  - Changes in LQFP-176 Package Variant; Buffer Type changed for all Ports
  - Changes in LQFP-176 Package Variant 'Analog Inputs' table; Buffer Type and Functions changed for all pins
  - Changes in LQFP-176 Package Variant 'System I/O' table; Buffer Type changed for all pins
  - Changes in LQFP-176 Package Variant 'System I/O' table; Symbol and function changed for pins 84, 85
  - Changes in LQFP-176 Package Variant; 'Supply' table; Symbol and Function changed for pins e_pad, 101, 104
- Changes in chapter TC37x TE - Pin Definition and Functions for package variant LQFP-176
  - Changes in LQFP-176 Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12

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  - Changes in LQFP-176 Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.6, P02.7, P02.8
  - Changes in LQFP-176 Package Variant 'Port 10 Functions' table; P10.2, P10.5, P10.6, P10.7, P10.8
  - Changes in LQFP-176 Package Variant 'Port 11 Functions' table; P11.2, P11.3, P11.6, P11.10, P11.12
  - Changes in LQFP-176 Package Variant 'Port 13 Functions' table; P13.1, P13.2
  - Changes in LQFP-176 Package Variant 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5, P14.9, P14.10
  - Changes in LQFP-176 Package Variant 'Port 15 Functions' table; P15.4, P15.5
  - Changes in LQFP-176 Package Variant 'Port 20 Functions' table; P20.0, P20.3,
  - Changes in LQFP-176 Package Variant 'Port 21 Functions' table; P21.0, P21.2, P21.3, P21.4, P21.5
  - Changes in LQFP-176 Package Variant 'Port 22 Functions' table; P22.0, P22.1, P22.2
  - Changes in LQFP-176 Package Variant 'Port 23 Functions' table; P23.1, P23.2, P23.3, P23.4, P23.5
  - Changes in LQFP-176 Package Variant 'Port 32 Functions' table; P32.0, P32.1, P32.2, P32.3, P32.4
  - Changes in LQFP-176 Package Variant 'Port 33 Functions' table; P33.0, P33.2, P33.5, P33.7, P33.10, P33.12, P33.13
  - Changes in LQFP-176 Package Variant; Buffer Type changed for all Ports
  - Changes in LQFP-176 Package Variant 'Analog Inputs' table; Buffer Type and Functions changed for all pins
  - Changes in LQFP-176 Package Variant 'System I/O' table; Buffer Type changed for all pins
  - Changes in LQFP-176 Package Variant 'System I/O' table; Symbol and function changed for pins 84, 85
  - Changes in LQFP-176 Package Variant 'System I/O' table; function changed for pins 102, 103
  - Changes in LQFP-176 Package Variant; 'Supply' table; Symbols and Functions changed for pins 101, 104
  - Changes in LQFP-176 Package Variant; 'Supply' table; Symbol and Function added for pin 177
- Changes in chapter TC37x TE - Pin Definition and Functions for package variant LQFP-144
  - Changes in LQFP-144 Package Variant 'Port 00 Functions' table; P00.0, P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.7, P00.8, P00.9, P00.12
  - Changes in LQFP-144 Package Variant 'Port 02 Functions' table; P02.0, P02.1, P02.2, P02.3, P02.4, P02.5, P02.6, P02.7, P02.8
  - Changes in LQFP-144 Package Variant 'Port 10 Functions' table; P10.2, P10.5, P10.6
  - Changes in LQFP-144 Package Variant 'Port 11 Functions' table; P11.2, P11.3, P11.6, P11.10, P11.12
  - Changes in LQFP-144 Package Variant 'Port 13 Functions' table; P13.1, P13.2
  - Changes in LQFP-144 Package Variant 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5
  - Changes in LQFP-144 Package Variant 'Port 15 Functions' table; P15.4, P15.5
  - Changes in LQFP-144 Package Variant 'Port 20 Functions' table; P20.0, P20.3
  - Changes in LQFP-144 Package Variant 'Port 21 Functions' table; P21.2, P21.3, P21.4, P21.5
  - Changes in LQFP-144 Package Variant 'Port 22 Functions' table; P22.0, P22.1, P22.2
  - Changes in LQFP-144 Package Variant 'Port 23 Functions' table; P23.1
  - Changes in LQFP-144 Package Variant 'Port 32 Functions' table; P32.0, P32.1, P32.4
  - Changes in LQFP-144 Package Variant 'Port 33 Functions' table; P33.5, P33.7, P33.10, P33.12, P33.13
  - Changes in LQFP-144 Package Variant; Buffer Type changed for all Ports
  - Changes in LQFP-144 Package Variant 'Analog Inputs' table; Buffer Type and Functions changed for all pins
  - Changes in LQFP-144 Package Variant 'System I/O' table; Buffer Type changed for all pins

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  - Changes in LQFP-144 Package Variant 'System I/O' table; Symbol and function changed for pins 70, 71
  - Changes in LQFP-144 Package Variant 'System I/O' table; function changed for pins 81,82
  - Changes in LQFP-144 Package Variant; 'Supply' table; Symbols and Functions changed for pins 83, 80
  - Changes in LQFP-144 Package Variant; 'Supply' table; Symbol and Function added for pin 145
- Changes in chapter “Pad Position Configuration of TC37x”
  - Changes in table “Pad List” for all positions
- Changes in chapter 'Pad Position Definition'
  - Changed description in sub-chapter 'Legend' - Column “Buffer Type”: PU2

Changes in chapter “Electrical Specification”

- Changes in table 'Absolute Maximum Ratings'
  - Changed max value of V_{IN} from 7.0 V to 6.75 V
  - Changed description of V_{DDM} from 'Voltage at V_{DDM}, V_{EXT} and V_{FLEX} power supply pins with respect to V_{SS}' to 'Voltage at V_{DDM}, V_{EXT}, V_{FLEX} and V_{EVRSB} power supply pins with respect to V_{SS}'
  - Changed note of V_{DDM} from '7.0 V' to '6.75 V'
  - Added footnote 2) to V_{DD}
  - Changed order of footnotes
- Changes in table 'Overload Parameters'
  - Changed note of I_{INANA}
  - Removed parameters of I_{ID}
  - Changed note of K_{OVAN}
  - Changed parameter conditions of K_{OVAP}
  - Added footnote 2) to K_{OVAP} and K_{OVAN}
- Changes in 'Operating Conditions' table
  - Added footnote 1) to V_{DD}
  - Changed order of footnotes
- Changes in table '$\overline{\text{PORST}}$ Pad' of Standard Pads
  - Change value name of parameter *HYS*
  - Changed notes of parameter I_{OZ}
  - Added value of parameter V_{IH}
  - Added value of parameter V_{IL}
  - Add footnote 2) to I_{PDL}
- Changes in table 'Fast 5V GPIO' of Standard Pads
  - Changed values and conditions of parameter I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed conditions of parameter t_{RF}
  - Changed value names of parameter of V_{IH}
  - Changed value names of parameter *HYS*
  - Changed value names of parameter V_{IL}
  - Changed conditions of parameter V_{ILD}
  - Changed parameter t_{SET}
  - Added footnote 1) for t_{RF}
  - Changed footnote 2) for t_{RF}

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  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Fast 3.3V GPIO' of Standard Pads
  - Changed value names of parameter *HYS*
  - Changed condition of parameter t_{RF}
  - Changed value names of parameter V_{IH}
  - Changed value of parameter V_{IL}
  - Changed condition of parameter V_{ILD}
  - Changed values and conditions of parameter I_{OZ}
  - Combined equal values of I_{OZ} in single lines
  - Changed parameter t_{SET}
  - Added footnote 1) for t_{RF}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Slow 5V GPIO' of Standard Pads
  - Changed value names of parameter *HYS*
  - Changed conditions of parameter I_{PUH}
  - Changed values and conditions of parameter I_{OZ}
  - Combined equal values of I_{OZ} in single line
  - Changed value names of parameter V_{IL}
  - Changed value names of parameter V_{IH}
  - Changed conditions of parameter V_{ILD}
  - Changed parameter t_{SET}
  - Added footnote 1) for t_{RF}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Slow 3.3V GPIO' of Standard Pads
  - Changed value names of parameter *HYS*
  - Changed conditions of parameter I_{PUH}
  - Changed values and conditions of parameter I_{OZ}
  - Combined equal values of I_{OZ} in single line
  - Removed parameter of I_{OZ}
  - Changed value and name of parameter V_{IL}
  - Changed value names of parameter V_{IH}
  - Changed conditions of parameter V_{ILD}
  - Changed parameter of t_{SET}
  - Added footnote 1) for t_{RF}

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  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'RFast 5V GPIO' of Standard Pads
  - Changed condition of parameter t_{RF}
  - Changed value names of parameter *HYS*
  - Changed conditions of parameter I_{OZ}
  - Changed value names of parameter V_{IH}
  - Changed value names of parameter V_{IL}
  - Changed conditions of parameter V_{ILD}
  - Changed parameter of t_{SET}
  - Added footnote 1) for t_{RF}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'RFast 3.3V pad' of Standard Pads
  - Changed condition of parameter t_{RF}
  - Changed value names of parameter *HYS*
  - Changed conditions of parameter I_{OZ}
  - Changed value name of parameter V_{IH}
  - Changed value and name of parameter V_{IL}
  - Changed conditions of parameter V_{ILD}
  - Changed parameter t_{SET}
  - Added footnote 1) for t_{RF}
  - Changed footnote 2) for t_{RF}
  - Added footnote 4) for I_{PUH}
  - Added footnote 5) for I_{PDL}
  - Changed order of footnotes
- Changes in table 'Class S 5V' of Standard Pads
  - Changed value names of parameter *HYS*
  - Changed values of parameter I_{OZ}
  - Changed value name of parameter V_{IH}
  - Changed value name of parameter V_{IL}
  - Changed parameter of t_{SET}
  - Added footnote 2) for I_{PUH}
  - Added footnote 3) for I_{PDL}
- Changes in table 'Class D' of Standard Pads
  - Changed values of parameter I_{OZ}
- Changes in table 'ADC Reference Pads' of Standard Pads
  - Changed notes of parameter I_{OZ2}

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  - Added footnote 1) for I_{OZ2}
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)' of LVDS Pads
  - Changed condition of parameter R_{in}
  - Added parameter t_{SET_LVDS}
  - Added footnote 1) for t_{RISE20}
  - Added footnote 2) for t_{FALL20}
  - Changed order of footnotes
- Changes in table 'VADC 5V'
  - Added conditions of parameter V_{DDK}
  - Changed parameter naming of dV_{DDK}
  - Added conditions of parameter V_{AREF}
  - Changed values and conditions of V_{AREF}
  - Added note for parameter R_{PDD}
  - Added footnote 1) for V_{AREF}
  - Changed footnote 2) for TUE, EA_{INL}, EA_{DNL}, EA_{GAIN}, EA_{OFF}, EN_{RMS}
  - Added footnote 9) for Q_{CONV}
  - Changed order of footnotes
  - Changed figure 'Equivalent Circuitry for Analog Inputs'
- Changes in table 'DSADC 5V'
  - Added parameter for R_{BIAS}
  - Changed parameters of V_{AREF}
  - Changed parameters of I_{REF}
  - Added parameters of I_{REF}
  - Changed parameters of I_{RMS}
  - Changed parameters of ED_{GAIN}
  - Changed parameters of ED_{OFF}
  - Added footnote 2) for I_{RMS}, SNR
  - Added footnote 3) for $SFDR$, ED_{GAIN}, ED_{OFF},
  - Changed order of footnotes
- Changes in table 'OSC_XTAL'
  - Removed parameter for V_{IHBX}
  - Removed parameter for V_{ILBX}
  - Added parameter for DC_{X1}
  - Added parameter for J_{ABSX1}
  - Added parameter for SR_{XTAL1}
  - Added footnote 3) for DC_{X1}, J_{ABSX1}, SR_{XTAL1}
- Changes in table 'Back-up Clock'
  - Changed value of f_{SB}
  - Changed footnote 1) for f_{BACKT}
- Changes in table 'DTS PMS'
  - Added parameter conditions for T_{NL}
- Changes in table 'DTS Core'

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  - Added parameter ΔT
  - Added parameter conditions for T_{NL}
- Current Consumption
  - Added values and notes for I_{DDRAIL}
  - Changed values for I_{DDRAIL}
  - Added values and notes for $I_{DDPORST}$
  - Changed values and notes for $I_{DDPORST}$
  - Changed value and note for $I_{STANDBY}$
  - Changed value for I_{DDTOT}
  - Changed values for *PD*
  - Changed footnote 4) for $I_{EXTFLEX}$
  - Changed footnote 7) $I_{STANDBY}$
- Changes in table 'Module Current Consumption'
  - Changed value of parameters of $I_{DDP3PROG}$
  - Changed value of parameters of $I_{EXTLVDS}$
  - Changed value of $I_{DDP3ERASE}$
  - Changed value of parameter I_{SCRSB}
  - Changed value of parameter $I_{SCRIDLE}$
  - Added footnote 5) for I_{SCRSB}
  - Changed order of footnotes
- Changes in table 'Module Core Current Consumption'
  - Changed naming of I_{DDSPU1}
  - Changed condition of parameter $I_{DDLBIST}$
  - Changed value and condition of parameter $I_{DDLMBIST}$
  - Changed footnote 1) for I_{DDHSM}
  - Added footnote 2) for $I_{DDLBIST}$
- Changes in chapter “Single Supply mode”
  - Changed figure and description for 'Single Supply Mode (a)'
  - Changed figure and description for 'Single Supply Mode (e)'
  - Changed figure and description for 'Single Supply Mode (d)'
  - Changed figure and description for 'Single Supply Mode (h)'
- Changes in table 'Reset'
  - Changed value of parameter t_B
  - Changed value of parameter t_{BS}
  - Added parameter $t_{WARMRSTSEQ}$
  - Changed value of parameter t_{BWP}
  - Changed naming and condition of parameter t_{LBIST}
  - Added footnote 2) for t_{EVRPOR}
  - Changed order of footnotes
- Changes in table 'EVR33 LDO'
  - Changed condition of parameter t_{STR}
  - Added parameter for 'ΔV_{OUTTC}'

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  - Changed values and conditions of parameter dV_{OUT} / dV_{IN}
  - Added footnote 7) for dV_{OUT} / dI_{OUT}
- Changes in table 'Supply Monitors'
  - Changed value of V_{RSTC}
  - Changed values of parameter V_{EXTMON}
  - Changed condition of parameter t_{MON}
  - Changed footnote 2) for $V_{EXTPRIUV}$, $V_{DDP3PRIUV}$, $V_{DDPRIUV}$,
  - Changed footnote 3) for $V_{DDP3PRIUV}$, $V_{DDPRIUV}$,
  - Added footnote 4) for V_{EXTMON}
  - Added footnote 5) for V_{EXTMON}, $V_{DDP3MON}$, V_{DDMON}
- Changes in table 'EVRC SMPS'
  - Changed values and notes of parameter of 'f_{DCDC}'
  - Changed value of parameter of 'ΔV_{DDDC}'
  - Removed values and notes of parameter C_{OUT}
  - Added values of parameter 'L_{DC}'
  - Changed condition of parameter dV_{DDDCT} / dI_{OUT}
- Changed chapter naming from 'Phase Locked Loop (PLL)' to 'System Phase Locked Loop (SYS_PLL)'
- Changes in table 'PLL System'
  - Removed parameter values of 'f_{MV}'
- Changes in table 'PLL Peripheral'
  - Changed description and values of parameter D_{PP}
  - Added parameter D_{PPI}
  - Changed notes of parameter D_{RMS}
  - Changed notes of parameter DP
  - Added parameter J_{ABS25}
- Changes in table 'Master Mode Timing'
  - Added footnote 1) for all parameters
- Changes in table 'LVDS clock/data'
  - Added footnote 3) for all parameters
- Changes in table 'Receive Parameters' of ERAY
  - Changed description of $t_{dCCRxD10}$
- Changes in table 'Flash'
  - Changed description of parameter of N_{DFD}
  - Added parameter N_{DFDC}
  - Added parameter N_{UCBD}
  - Changed condition of parameter for N_{E_EEP10S}
  - Added values for parameter N_{E_EEP10S}
  - Changed condition of parameter for N_{E_HSMS}
  - Added values for parameter N_{E_HSMS}
  - Added parameter $t_{VER_PAGE_DC}$
  - Added parameter $t_{VER_PAGE_DS}$
  - Removed parameter $t_{VER_PAGE_D}$

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  - Changed order of footnotes
- Changes in table 'Quality Parameters'
  - Changed condition of parameter V_{HBM1}
  - Added footnote 1) for V_{CDM}
  - Added footnote 2) for V_{HBM}
- Changes in table 'Package Outline'
  - Added figures for Package Outline
  - Added tables 'Exposed Pad Dimensions'
- Changes in table 'Package Parameters'
  - Added table 'Package Parameters'
  - Added footnote 1) for all parameters

4.2 Changes from Version 0.6 to Version 0.61

Changes in chapter “Summary of Features”

- Changes in table “Platform Feature Overview” for Debug/AGBT and package variants

Changes in chapter “TC37x Pin Definition and Functions”

- Changes in overview list: spelling of LFBGA-292
- Changes in overview list for package types of LFBGA-292
- Pad Position Configuration for TP, TE and TX variants added
- Package variant LQFP-144 deleted
- Changes in chapter TC37x TP - Pin Definition and Functions for package variant LFBGA-292
  - Changes in 'Port 00 Functions' table; P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12
  - Changes in 'Port 01 Functions' table; P01.6
  - Changes in 'Port 02 Functions' table; P02.3, P02.4, P02.5, P02.6, P02.7, P02.8
  - Changes in 'Port 10 Functions' table; P10.3, P10.4, P10.5, P10.6
  - Changes in 'Port 11 Functions' table; P11.5, P11.7, P11.8, P11.9, P11.10, P11.11, P11.12, P11.15
  - Changes in 'Port 12 Functions' table; P12.0
  - Changes in 'Port 13 Functions' table; P13.1, P13.2
  - Changes in 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5
  - Changes in 'Port 15 Functions' table; P15.4, P15.5, P15.6
  - Changes in 'Port 20 Functions' table; P20.0, P20.8, P20.14
  - Changes in 'Port 21 Functions' table; P21.0, P21.2, P21.3, P21.4, P21.5, P21.6, P21.7
  - Changes in 'Port 22 Functions' table; P22.0, P22.1, P22.4, P22.5, P22.6, P22.7, P22.8, P22.9, P22.10, P22.11
  - Changes in 'Port 23 Functions' table; P23.1, P23.2, P23.3, P23.4, P23.5, P23.6, P23.7
  - Changes in 'Port 32 Functions' table; P32.2, P32.4
  - Changes in 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, p33.4, P33.5, P33.6, P33.10, P33.12
  - Changes in 'Port 34 Functions' table; P34.5
  - Changes in table “System I/O”
  - Changes in table “Supply”

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- Changes in chapter TC37x TE and TX - Pin Definition and Functions for package variant LFBGA-292
  - Changed order of Port Function tables
  - Changed spelling of LFBGA-292
  - Changes in 'Port 00 Functions' table; P00.8
  - Changes in 'Port 02 Functions' table; P02.4, P02.5
  - Changes in 'Port 11 Functions' table; P11.5, P11.12
  - Changes in 'Port 13 Functions' table; P13.1, P13.2
  - Changes in 'Port 20 Functions' table; P20.0
  - Changes in 'Port 23 Functions' table; P23.1
  - Changes in 'Port 32 Functions' table; P32.4
- Changes in chapter TC37x T and TP - Pin Definition and Functions for package variant LQFP-176
  - Changes in 'Port 00 Functions' table; P00.1, P00.2, P00.3, P00.4, P00.5, P00.6, P00.7, P00.8, P00.9, P00.10, P00.11, P00.12
  - Changes in 'Port 02 Functions' table; P02.3, P02.4, P02.5, P02.6, P02.7, P02.8
  - Changes in 'Port 10 Functions' table; P10.3, P10.4, P10.5, P10.6
  - Changes in 'Port 11 Functions' table; P11.9, P11.10, P11.11, P11.12
  - Changes in 'Port 13 Functions' table; P13.1, P13.2
  - Changes in 'Port 14 Functions' table; P14.2, P14.3, P14.4, P14.5
  - Changes in 'Port 15 Functions' table; P15.4, P15.5, P15.6
  - Changes in 'Port 20 Functions' table; P20.0, P20.8, P20.14
  - Changes in 'Port 21 Functions' table; P21.0, P21.2, P21.3, P21.4, P21.5, P21.6, P21.7
  - Changes in 'Port 22 Functions' table; P22.0, P22.1
  - Changes in 'Port 23 Functions' table; P23.1, P23.2, P23.3, P23.4, P23.5
  - Changes in 'Port 32 Functions' table; P32.2, P32.4
  - Changes in 'Port 33 Functions' table; P33.0, P33.1, P33.2, P33.3, P33.4, P33.5, P33.6, P33.10, P33.12
  - Changes in table “System I/O”
  - Changes in table “Supply”
- Changes in chapter TC37x TE - Pin Definition and Functions for package variant LQFP-176
  - Changes in 'Port 00 Functions' table; P00.8
  - Changes in 'Port 02 Functions' table; P02.4, P02.5
  - Changes in 'Port 11 Functions' table; P11.12
  - Changes in 'Port 13 Functions' table; P13.1, P13.2
  - Changes in 'Port 15 Functions' table; P15.4, P15.5
  - Changes in 'Port 20 Functions' table; P20.0
  - Changes in 'Port 23 Functions' table; P23.1
  - Changes in 'Port 32 Functions' table; P32.4
  - Changes in table “Supply”
- Deleted chapter TC37x TE - Pin Definition and Functions for package variant LQFP-144
- Changes in chapter “Pad Position Configuration of TC37x TP”
  - Changes in table “Pad List” for different positions
- Added chapter “Pad Position Configuration of TC37x TE and TX”
- Changes in chapter “Legend”

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  - Added description concerning pinning DB versions for packages

Changes in chapter “Electrical Specification”

- Changes in table 'RFast 3.3V pad'
  - Added parameter for f_{IND}
- Changes in table 'VADC 5V'
  - Added conditions for parameter V_{AIN}
- Changes in table 'DSADC 5V'
  - Added / changed values for parameter I_{RMS} and ED_{GAIN}
  - Added footnote 4)
  - Changed order of footnotes
- Changes in table “Current Consumption”
  - Added footnotes for $I_{EXTFLEX}$
  - Changed footnote for $I_{DDTOTDC3}$
  - Changed footnote for $I_{DDTOTDC5}$
  - Changed footnote for $I_{STANDBY}$
  - Changed footnote 2)
  - Added footnote 4) and 6)
  - Changed order of footnotes
- Changes in table 'Module Current Consumption'
  - Changed condition of $I_{EXTLVDS}$
  - Changed footnotes of I_{DDM}
  - Changed footnote of I_{SCRSB}
  - Changed footnote of $I_{SCRIDLE}$
  - Added footnote 3) and 5)
  - Changed order of footnotes
- Changes in table 'Module Core Current Consumption'
  - Changed / added values of parameter I_{DDGTM}
- Changes in table 'Reset'
  - Changed value of of parameter T_{BWP}
  - Changed values of of parameter T_{SCR}
- Changes in table 'Supply Monitors'
  - Changed condition of parameter V_{RST33}
  - Changed condition of parameter V_{RSTC}
- Changes in table 'Package Outline'
  - Changed spelling for figure from LF-BGA-292 to LFBGA-292
  - Deleted figure and table for QFP144
- Changes in table 'Package Parameters'
  - Deleted values and notes for QFP144
  - Changed value for RTH_JACC

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4.3 Changes from Version 0.61 to Version 0.7

Changes in chapter “Summary of Features”

- Changes in table “Platform Feature Overview”
  - added package LQFP-144
  - change package name from LFBGA-292-10 to LFBGA-292

Changes in chapter “TC37x Pin Definition and Functions”

- Changes in overview list - package variants of LFBGA-292
  - Split of package variant description for LFBGA-292 - TE and TX version
  - Added package variant LQFP-144
  - Changed package variant figure numbering
- Changes in chapter “LFBGA-292 Package Pinning of TC37x TE”
  - Changes in 'Port 00 Functions' table; P00.3, P00.4, P00.8, P00.9, P00.10
  - Changes in ‘Port 01 Functions’ table; P01.6
  - Changes in ‘Port 02 Functions’ table; P02.4, P02.5, P02.6, P02.7, P02.8, P02.11
  - Changes in ‘Port 10 Functions’ table; P10.3, P10.4, P10.6
  - Changes in ‘Port 11 Functions’ table; P11.9, P11.15
  - Changes in ‘Port 13 Functions’ table; P13.1, P13.2
  - Changes in ‘Port 14 Functions’ table; P14.4
  - Changes in ‘Port 15 Functions’ table; P15.4, P15.5, P15.6
  - Changes in ‘Port 20 Functions’ table; P20.0, P20.8, P20.14
  - Changes in ‘Port 21 Functions’ table; P21.2, P21.3, P21.4, P21.5
  - Changes in ‘Port 22 Functions’ table; P22.0, P22.5, P22.10
  - Changes in ‘Port 23 Functions’ table; P23.3, P23.4
  - Changes in ‘Port 32 Functions’ table; P32.2, P32.4
  - Changes in ‘Port 33 Functions’ table; P33.3, P33.10, P33.12
  - Changes in ‘Port 34 Functions’ table; P34.5
  - Changes in table “Analog Inputs”; ball U6, EDSADC; ball T6, EDSADC; ball W2, EDSADC; ball W1, EDSADC; ball M1, EDSADC; ball M2, EDSADC
  - Changes in table “System I/O”; ball L7, K7, P10, P11, L14, G11, K14

Added chapter “LFBGA-292 Package Pinning of TC37x TX”

- **Changes in chapter “LQFP-176 Package Pinning of TC37x TE”**
  - Changes in 'Port 00 Functions' table; P00.3, P00.4, P00.8, P00.9, P00.10
  - Changes in ‘Port 02 Functions’ table; P02.4, P02.5, P02.6, P02.7, P02.8
  - Changes in ‘Port 10 Functions’ table; P10.3, P10.4, P10.6
  - Changes in ‘Port 11 Functions’ table; P11.9
  - Changes in ‘Port 13 Functions’ table; P13.1, P13.2
  - Changes in ‘Port 14 Functions’ table; P14.4
  - Changes in ‘Port 15 Functions’ table; P15.4, P15.5, P15.6
  - Changes in ‘Port 20 Functions’ table; P20.0, P20.8, P20.14
  - Changes in ‘Port 21 Functions’ table; P21.2, P21.3, P21.4, P21.5
  - Changes in ‘Port 22 Functions’ table; P22.0

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  - Changes in ‘Port 23 Functions’ table; P23.3, P23.4
  - Changes in ‘Port 32 Functions’ table; P32.2, P32.4
  - Changes in ‘Port 33 Functions’ table; P33.3, P33.10, P33.12
  - Changes in table “Analog Inputs”; pin 44, EDSADC; pin 43, EDSADC; pin 29, EDSADC; pin 28, EDSADC;

Added chapter “LQFP-144 Package Pinning of TC37x TE”

Changes in chapter “Pad Position Configuration of TC37x TE/TX”

  - Changes in table “Pad List”, number 34, 35, 219, 220, 223, 224, 225, 307,
  - Added comment concerning “neighbor pads”

Changes in chapter “Legend”

  - Changed refering IO_Spirit_file version

Changes in chapter “Electrical Specification”

- Changes in table 'Operating Conditions'
  - Deleted parameter for f_{EBU}
- Changes in table 'LVDS - IEEE standard LVDS general purpose link (GPL)'
  - Changed value for parameter V_I
  - Changed test condition for parameter V_{idth}
  - Added values for parameter V_{idth}
  - Changed test condition for parameter R_{in}
  - Added notes to LVDS table
- Changes in table 'Current Consumption'
  - Deleted values for parameter I_{DDRAIL}
  - Deleted value for parameter $I_{DDPORST}$
  - Changed value of parameter $I_{EXTRAIL}$
  - Changed test condition for parameter I_{DDTOT}
  - Added values and test condition for parameter I_{DDTOT}
  - Added value for parameter $I_{DDTOTDC3}$
  - Changed test parameter for $I_{DDTOTDC3}$
  - Added value for parameter $I_{DDTOTDC5}$
  - Changed test conditions for $I_{DDTOTDC5}$
  - Changed test conditions for parameter *PD*
  - Added values for parameter *PD*
  - Modified footnote 9) for parameter *PD*
- Changes in table 'Module Core Current Consumption'
  - Changed values for parameter I_{DDCx0}
  - Changed values for parameter I_{DDCxx}
  - Deleted parameter for I_{DDSPU1}
  - Added value for parameter I_{DDCIF}
- Added sub-chapter 'Calculating the 1.25 V Current Consumption'
- Changes in table 'Reset'
  - Changed value for parameter t_{PIP}
- Changes in table 'PLL System'
  - Changed value for parameter f_{REF}

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- Changes in sub-chapter 'ETH RGMII Parameters'
  - Added figures for ETH RGMII TXand RX signals
- Added sub-chapter 'SDMMC Interface Timing'
- Changes in table 'Flash'
  - Changed value for parameter t_{PRPB5_PF}
  - Changed values for parameter t_{ER_Dev}
- Added figure for Package Outlines LQFP-144
- Changes in table 'Package Parameters'
  - Added value for parameter RTH_JA - QFP144
  - Added value for parameter RTH_JCB - QFP144

Added value for parameter RTH_JCT - QFP144

4.4 Changes from Version 0.7 to Version 1.0

- General changes in Data Sheet TC37x: Data Sheet splitted and renamed to TC37xEXT for feature package TE/TX and TC37x for feature package T/TP
- Changed Data Sheet version 0.7 to 1.0 and from AA-Step to AB-Step
- Changes in table “Platform Feature Overview”
  - Changed GTM features
  - ASIL Level deleted
  - Debug features deleted
  - Changed packages name spelling
- Changes in chapter “TC37x Pin Definition and Functions”
  - Deleted Package Pinning for LFBGA-292-10, TC37x TP
  - Deleted Package Pinning for LQFP-176, TC37x T and TP
  - Deleted Pad Position Configuration of TC37x TP
  - Changed package name spelling (LFBGA-292)
  - Updated "CIF.*" symbol and functional description for all packages
  - Updated EDSADC functional description for all packages
  - Deleted PMS symbol in package LFBGA-292, Port 02, Ball F1
  - Deleted PMS symbol in package LQFP-176, Port 02, Pin 9
  - Deleted PMS symbol in package LQFP-144, Port 02, Pin 9
  - LFBGA-292 (feature package TE): Changes in table “Analog Inputs”; functional descriptions of ball U6, T6, W2, W1, M1, M2
  - LFBGA-292 (feature package TE): Changes in table “System I/O”; functional descriptions of ball G10, G11, K14
  - LFBGA-292 (feature package TX): Changes in table “Analog Inputs”; functional descriptions of ball U6, T6, W2, W1, M1, M2
  - LFBGA-292 (feature package TX): Changes in table “System I/O”; functional descriptions of ball G10, G11, K14
  - LFBGA-176: Changes in table “Analog Inputs”; functional descriptions of pin 44, 43, 29, 28
  - LFBGA-144: Changes in table “Analog Inputs”; changed pin naming of pin E-PAD/145
  - LFBGA-144: Changes in table “Supply”; functional description of pin 36, 35, 27, 26

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  - Added description regarding “neighbor pads” in chapter “Electrical Specification”
- Changes in table "Legend"
  - Spirit version for feature package TC37x TP has been deleted
- Changes in chapter "Electrical Specification"
  - Changed description in table “Absolute Maximum Ratings” for parameter ΣI_{IN}
  - Added footnote to table “Absolute Maximum Ratings”
  - Added footnote in table “Absolute Maximum Ratings” for parameter I_{IN}
  - Changed value in table “Overload Parameters” for parameter V_{OUS}
  - Changed conditions in table “Operating Conditions” for parameter V_{FLEX}
  - Added parameter in table “Operating Conditions” for V_{FLEX2}
  - Changed conditions in table “Fast 5V GPIO” for parameter t_{RF}
  - Changed values in table “Fast 5V GPIO” for parameter *HYS*
  - Changed conditions in table “Fast 5V GPIO” for parameter I_{OZ}
  - Changed value in table “Fast 5V GPIO” for parameter V_{IH}
  - Changed value in table “Fast 5V GPIO” for parameter V_{IL}
  - Changed condition in table “Fast 5V GPIO” for parameter V_{ILD}
  - Changed conditions in table “Fast 3.3V GPIO” for parameter t_{RF}
  - Changed values in table “Fast 3.3V GPIO” for parameter *HYS*
  - Changed conditions in table “Fast 3.3V GPIO” for parameter I_{OZ}
  - Changed value in table “Fast 3.3V GPIO” for parameter V_{IH}
  - Changed value in table “Fast 3.3V GPIO” for parameter V_{IL}
  - Changed condition in table “Fast 5V GPIO” for parameter V_{ILD}
  - Changed values in table “Slow 5V GPIO” for parameter *HYS*
  - Changed conditions in table “Slow 5V GPIO” for parameter I_{OZ}
  - Changed value in table “Slow 5V GPIO” for parameter V_{IH}
  - Changed value in table “Slow 5V GPIO” for parameter V_{IL}
  - Changed condition in table “Slow 5V GPIO” for parameter V_{ILD}
  - Changed values in table “Slow 3.3V GPIO” for parameter *HYS*
  - Changed conditions in table “Slow 3.3V GPIO” for parameter I_{OZ}
  - Changed value in table “Slow 3.3V GPIO” for parameter V_{IH}
  - Changed value in table “Slow 3.3V GPIO” for parameter V_{IL}
  - Changed condition in table “Slow 3.3V GPIO” for parameter V_{ILD}
  - Changed conditions in table “RFast 5V GPIO” for parameter t_{RF}
  - Changed values in table “RFast 5V GPIO” for parameter *HYS*
  - Changed conditions in table “RFast 5V GPIO” for parameter I_{OZ}
  - Changed value in table “RFast 5V GPIO” for parameter V_{IH}
  - Changed value in table “RFast 5V GPIO” for parameter V_{IL}
  - Changed condition in table “RFast 5V GPIO” for parameter V_{ILD}
  - Changed conditions in table “RFast 3.3V pad” for parameter t_{RF}
  - Changed values in table “RFast 3.3V pad” for parameter *HYS*
  - Changed conditions in table “RFast 3.3V pad” for parameter I_{OZ}
  - Changed value in table “RFast 3.3V pad” for parameter V_{IH}

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  - Changed value in table “RFast 3.3V pad” for parameter V_{IL}
  - Added table for “Class S 3.3V” parameters to sub-chapter “5V/ 3.3V switchable Pads”
  - Changed footnote 1) at table “OSC_XTAL”
  - Added power pattern information to sub-chapter “Power Supply Current”
  - Deleted values in table “Current Consumption” for parameter $I_{DDPORST}$
  - Changed value in table “Current Consumption” for parameter $I_{EXTRAIL}$
  - Changed value in table “Current Consumption” for parameter I_{EVRSB}
  - Changed condition in table “Reset” for parameter $t_{SUPHOLD}$
  - Added values and conditions in table “Supply Monitors” for parameter V_{EXTMON}
  - Changed conditions in table “Supply Monitors” for parameter $V_{DDP3MON}$
  - Changed conditions in table “Supply Monitors” for parameter V_{DDMON}
  - Added note regarding power-cycles to table "Supply Ramp"
  - Changed symbol in table “EVRC SMPS” for parameter Δf_{DCSPR}
  - Changed symbol in table “EVRC SMPS” for parameter n_{DC}
  - Added sub-chapter “Camera Interface Timing (CIF)”
  - Changed value in table “Quality Parameters” for parameter V_{HBM1}
- Changes in “Package Outline”
  - Changed package name spelling for figure titles
  - Changed packages name spelling in table “Package Parameter”

4.5 Changes from Version 1.0 to Version 1.1

- Changes in chapter “Revision History”
  - Changed GTM features
  - Chronology completed
  -
- Changes in chapter “Summary of Features”
  - Changed wording for “DFLASH”
  - Added description for “AEC-Q100”
  - Added description for “ISO 26262 Safety Element”
  - Added description for Data Flash in table “Platform Feature Overview”
  - Changed numbering of GTM Clusters in table “Platform Feature Overview”
  - Added footnote 2) to parameter Debug/ AGBT in table “Platform Feature Overview”
  - Added footnote 2) for AGBT feature in table “Platform Feature Overview”
  -
- Changes in chapter “TC37xEXT Pin Definition and Functions”
  - Added note to chapter “LFBGA-292 Package Pinning of TC37xEXT TE”
  - Added notes to table “System I/O” for “LFBGA-292 Package Pinning of TC37xEXT TE”
  - Added notes to table “System I/O” for “LFBGA-292 Package Pinning of TC37xEXT TX”
  - Added note to chapter “LQFP-176 Package Pinning of TC37xEXT”
  - Added notes to table “System I/O” for “LQFP-176 Package Pinning of TC37xEXT”
  - Changed pin assignment for VSS in table “Supply” for “LQFP-176 Package Pinning of TC37xEXT”

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  - Added note to chapter “LQFP-144 Package Pinning of TC37xEXT”
  - Added notes to table “System I/O” for “LQFP-144 Package Pinning of TC37xEXT”
  - Changed sub-chapter title from “Pad Position Configuration of TC37xEXT” to “Sequence of Pads in Pad Frame”
  - Deleted sentence in sub-text for sub-chapter “Sequence of Pads in Pad Frame”
  -
- Changes in chapter “Legend”
  - Changed version number of “TC37xed_IO_Spirit” file
  -
- Changes in chapter “Electrical Specification”
  - Typos corrected in footnotes for sub-chapter “Absolute Maximum Ratings”
  - Changed entry text for sub-chapter “Pin Reliability in Overload”
  - Typo corrected for parameter I_{INSA} in table “Overload Parameters” of sub-chapter “Pin Reliability in Overload”
  - Changed values for parameter GETH frequency in table “Operating Conditions”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
  - Changed note for parameter t_{TX_ASYM} in table “RFast 3.3V pad” of sub-chapter “5V/3.3V switchable Pads”
  - Typos corrected in footnotes for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Extended sub-note for table “LVDS – IEEE standard LVDS general purpose link (GPL)” in sub-chapter “High performance LVDS Pads”
  - Typo corrected for parameter dV_{CSD} in table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed footnotes 3) and 6) for table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed footnote 7) of table “VADC 5V” in sub-chapter “VADC Parameters”
  - Changed figure “Equivalent Circuitry for Analog Inputs” in sub-chapter “VADC Parameters”
  - Changed value of parameter I_{RMS} in table “DSADC 5V” in sub-chapter “DSADC Parameters”
  - Changed footnote 4) in sub-chapter “DSADC Parameters”
  - Changed spelling in footnote 2) in sub-chapter “MHz Oscillator”
  - Added values and notes for parameter I_{DDRAIL} in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added values and notes for parameter $I_{DDPORST}$ in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added values and notes for parameter I_{DDTOT} in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added values and notes for parameter *PD* in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added footnote 10) to parameter *PD* in table “Current Consumption” in sub-chapter “Power Supply Current”
  - Changed footnote 3) for table “Current Consumption” in sub-chapter “Power Supply Current”
  - Added footnote 10) for table “Current Consumption” in sub-chapter “Power Supply Current”

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- Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
- Typo corrected for parameter t_{EVRPOR} in table “Reset” for sub-chapter “Reset Timing”
- Changed/added value for parameter t_{PI} in table “Reset” for sub-chapter “Reset Timing”
- Changed value order and notes for parameter V_{EXTMON} in table “Supply Monitors” for sub-chapter “PMS”
- Typos corrected for footnote 2) and additional note for table “Supply Ramp” for sub-chapter “PMS”
- Changed values (from Min. to Typ.) for parameter t_7 in table “ETH MII Signal Timing Parameters” for sub-chapter “ETH MII Parameters”
- Changed symbols for parameters t_{13}, t_{14}, t_{15} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Changed value (from Min. to Typ.) for parameter t_{13} in table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Added footnote 3) for table “ETH RMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RMII Parameters”
- Deleted note for parameter t_{21} in table “ETH RGMII Signal Timing Parameters valid for 3.3V” in sub-chapter “ETH RGMII Parameters”
- Added table “Example Inactive Lifetime Temperature Profile” to sub-chapter “Quality Declarations”

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