NCP571, NCV571

Voltage Regulator - CMOS, Low Iq, Low Output

150 mA

The NCP571 series of fixed output low dropout linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent current. The NCP571 series features an ultra−low quiescent current of 4.0 μA. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

The NCP571 has been designed to be used with low cost ceramic capacitors and requires a minimum output capacitor of 0.1 μF. The device is housed in the TSOP−5 or DFN6 surface mount package. Standard voltage versions are 0.8 V, 0.9 V, 1.0 V and 1.2 V.

Features

- Low Quiescent Current of 4.0 μA Typical
- Maximum Operating Voltage of 12 V
- Low Output Voltage Option down to 0.8 V
- High Accuracy Output Voltage of 3.0%
- Industrial Temperature Range of −40°C to +85°C (NCV571, T_A = −40°C to +125°C)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Typical Applications

- Battery Powered Instruments
- Hand−Held Instruments
- Camcorders and Cameras

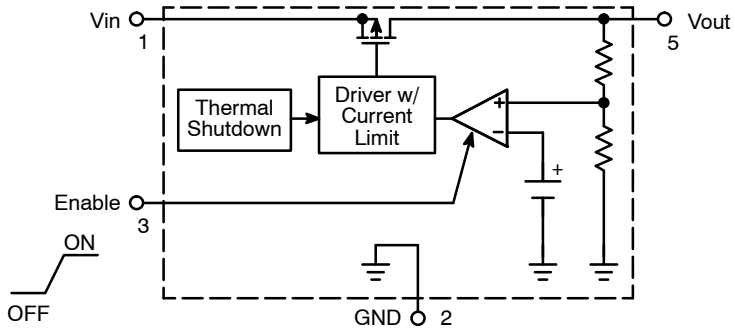
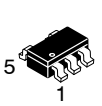


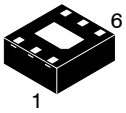
Figure 1. Representative Block Diagram

ON Semiconductor®

http://onsemi.com

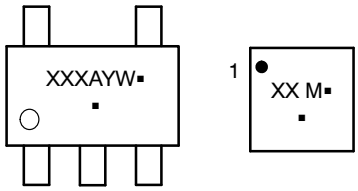


TSOP−5
SN SUFFIX
CASE 483



DFN6
MN SUFFIX
CASE 506BA

MARKING DIAGRAMS



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

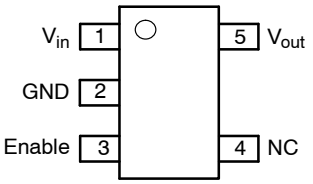
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

© Semiconductor Components Industries, LLC, 2014

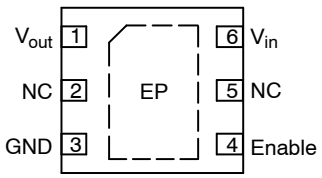
PIN CONNECTIONS

TSOP−5 package



(Top View)

DFN6 package



(Top View)

PIN FUNCTION DESCRIPTION

DFN6	TSOP−5	Pin Name	Description
1	5	V_{out}	Regulated output voltage.
2	4	NC	No Internal Connection. It is recommended to connect this pin to GND potential.
3	2	GND	Power supply ground.
4	3	Enable	This input is used to place the device into low−power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable pin should be connected to V_{in}.
5	−	NC	No Internal Connection. It is recommended to connect this pin to GND potential.
6	1	V_{in}	Positive power supply input voltage.
EP	−	EP	No Internal Connection. It is recommended to connect this pin to GND potential.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{in}	0 to 12	V
Enable Voltage		V_{EN}	−0.3 to V_{in} + 0.3	V
Output Voltage		V_{out}	−0.3 to V_{in} + 0.3	V
Power Dissipation		P_D	Internally Limited	W
Operating Junction Temperature		T_J	+150	°C
Operating Ambient Temperature	NCP571 NCV571	T_A	−40 to +85 −40 to +125	°C
Storage Temperature		T_{stg}	−55 to +150	°C
ESD Capability, Human Body Model (Note 1)		ESD_{HBM}	2000	V
ESD Capability, Machine Mode (Note 1)		ESD_{MM}	200	V
ESD Capability, Charged Device Model (Note 1)		ESD_{CDM}	1000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD Charged Device Model tested per EIA/JES D22/C101, Field Induced Charge Model (Jedec Standard)
2. Latchup capability (85°C) ±100 mA DC with trigger voltage.

THERMAL CHARACTERISTICS

Rating		Symbol	Test Conditions	Typical Value	Unit
Junction−to−Ambient	TSOP−5	$R_{\theta JA}$	1 oz Copper Thickness, 100 mm^2	250	°C/W
PSIJ−Lead 2	TSOP−5	Ψ_{J-L2}	1 oz Copper Thickness, 100 mm^2	68	°C/W
Junction−to−Ambient	DFN6	$R_{\theta JA}$	1 oz Copper Thickness, 100 mm^2	190	°C/W
PSIJ−Lead 2	DFN6	Ψ_{J-L2}	1 oz Copper Thickness, 100 mm^2	84	°C/W

NOTE: Single component mounted on an 80 x 80 x 1.5 mm FR4 PCB with stated copper head spreading area. Using the following boundary conditions as stated in EIA/JESD 51−1, 2, 3, 7, 12.

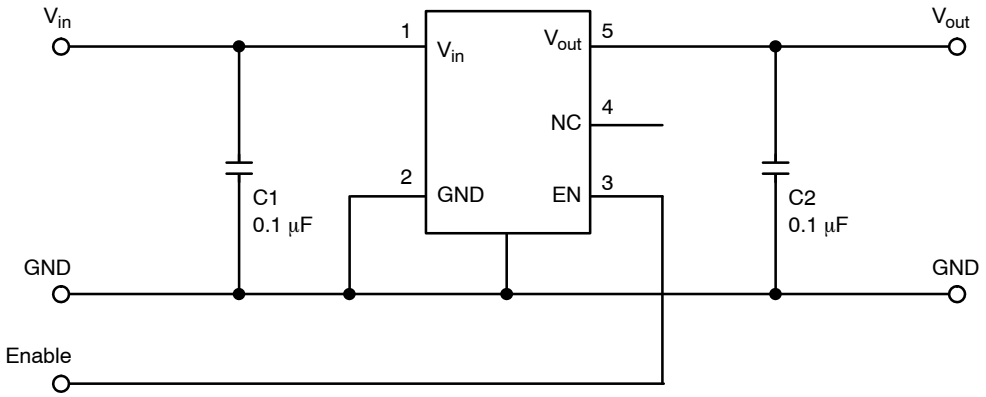


Figure 2. Typical Application Schematic for TSOP−5 Package

ELECTRICAL CHARACTERISTICS

(V_{in} = $V_{out(nom)}$ + 1.0 V, V_{EN} = V_{in}, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 10 mA) 0.8 V 0.9 V 1.0 V 1.2 V	V_{out}	− 3% 0.776 0.873 0.970 1.164	 0.8 0.9 1.0 1.2	+ 3% 0.824 0.927 1.030 1.236	V
Output Voltage (T_A = −40°C to +85°C for NCP571 or T_A = −40°C to +125°C for NCV571, I_{out} = 10 mA) (Note 5) 0.8 V 0.9 V 1.0 V 1.2 V	V_{out}	− 4% 0.768 0.864 0.960 1.152	 0.8 0.9 1.0 1.2	+ 4% 0.832 0.936 1.040 1.248	V
Line Regulation (V_{in} = V_{out} + 1.0 V to 12 V, I_{out} = 10 mA)	Reg_{line}	−	10	30	mV
Load Regulation (I_{out} = 10 mA to 150 mA, V_{in} = V_{out} + 2.0 V)	Reg_{load}	−	40	65	mV
Output Current (V_{out} = (V_{out} at I_{out} = 100 mA) − 3%) 0.8 V (V_{in} = 3.0 V) 0.9 V (V_{in} = 3.0 V) 1.0 V (V_{in} = 3.0 V) 1.2 V (V_{in} = 3.0 V)	$I_{o(nom)}$	 150 150 150 150	 − − − −	 − − − −	mA
Dropout Voltage (I_{out} = 10 mA, Measured at V_{out} − 3.0%) 0.8 V 0.9 V 1.0 V 1.2 V	V_{in}−V_{out}	 − − − −	 730 650 550 350	 850 750 650 450	mV
Quiescent Current (Enable Input = 0 V) (Enable Input = V_{in} = 3 V, I_{out} = 1.0 mA to 150 mA and V_{in} = Enable Input = 3 V, I_{out} = 150 mA)	I_Q	 − −	 0.1 4.0	 1.0 8.0	uA
Output Voltage Temperature Coefficient	T_c	−	100	−	ppm/°C
Enable Input Threshold Voltage (Voltage Increasing, Output Turns On, Logic High) (Voltage Decreasing, Output Turns Off, Logic Low)	$V_{th(en)}$	 1.3 −	 − −	 − 0.3	V
Output Short Circuit Current (V_{out} = 0 V) (Note 4) 0.8 V (V_{in} = 3.0 V) 0.9 V (V_{in} = 3.0 V) 1.0 V (V_{in} = 3.0 V) 1.2 V (V_{in} = 3.0 V)	$I_{out(max)}$	 160 160 160 160	 260 260 260 260	 600 600 600 600	mA

3. Maximum package power dissipation limits must be observed.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

5. NCP571 T_{low} = −40°C T_{high} = +85°C
   NCV571 T_{low} = −40°C T_{high} = +125°C.

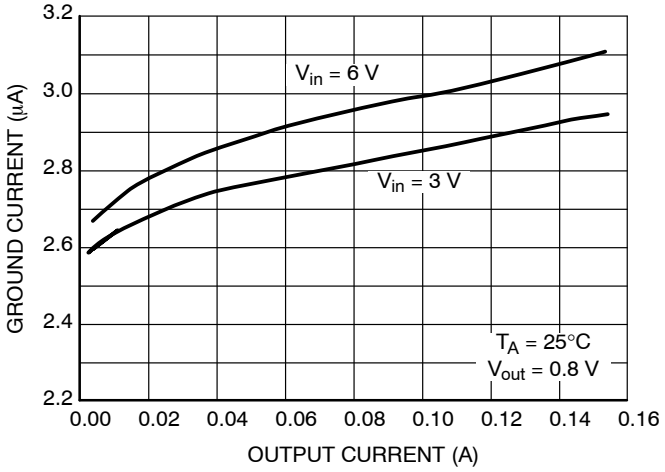


Figure 3. Ground Pin Current vs. Output Current

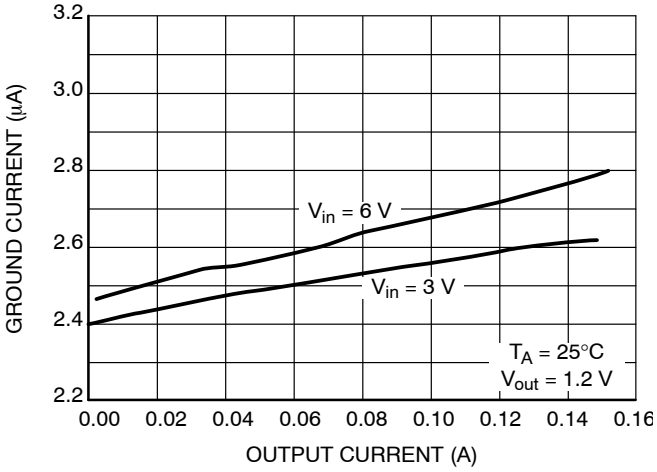


Figure 4. Ground Pin Current vs. Output Current

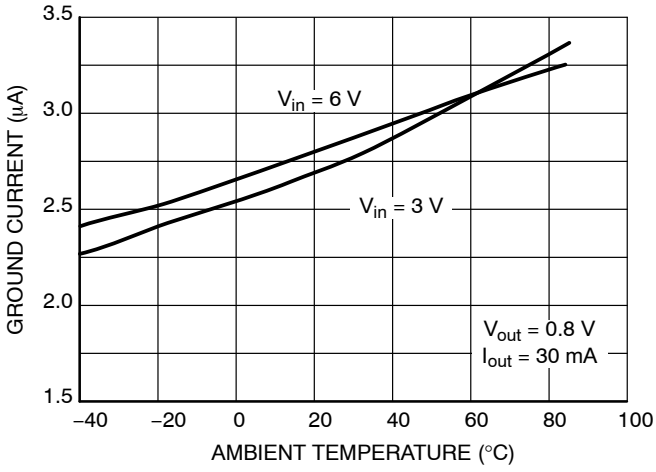


Figure 5. Ground Pin Current vs. Temperature

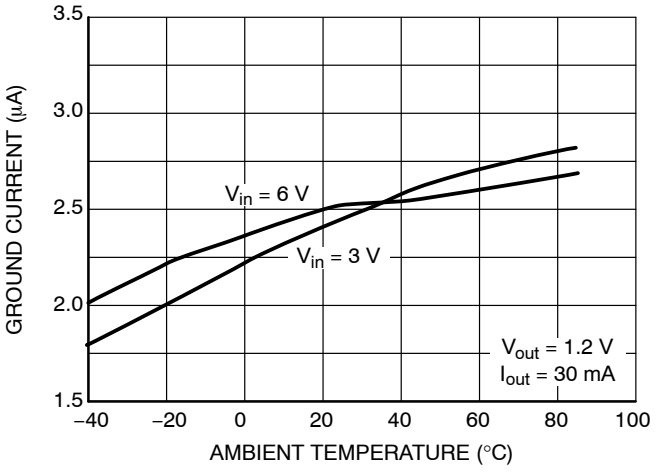


Figure 6. Ground Pin Current vs. Temperature

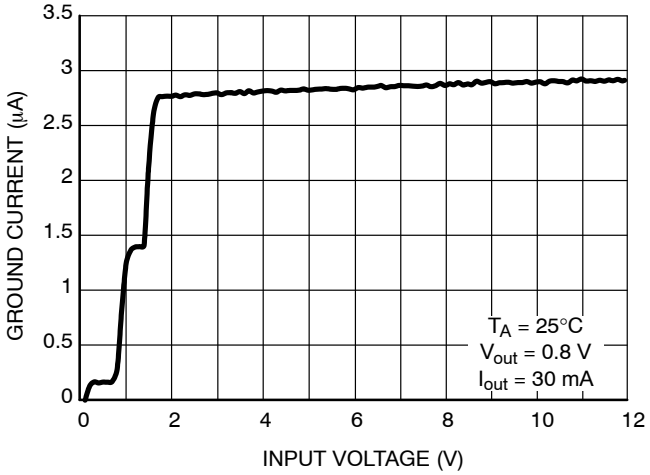


Figure 7. Ground Pin Current vs. Input Voltage

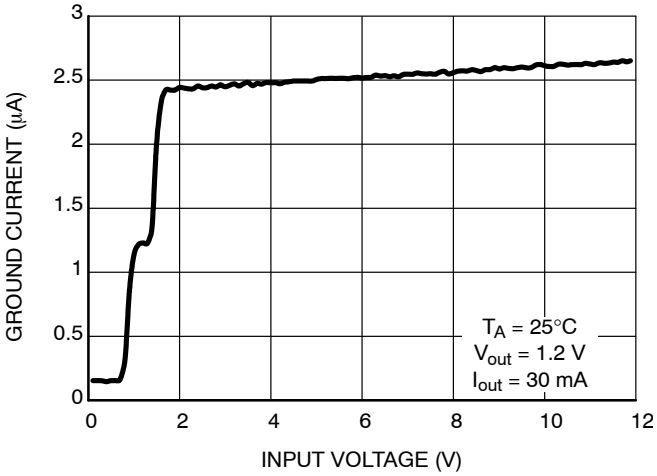


Figure 8. Ground Pin Current vs. Input Voltage

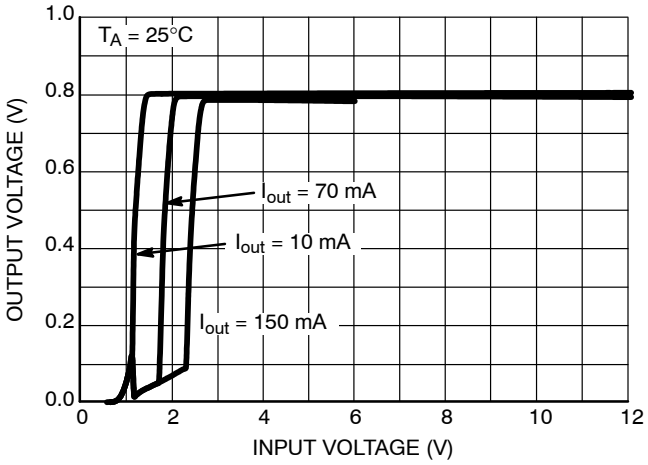


Figure 9. Output Voltage vs. Input Voltage

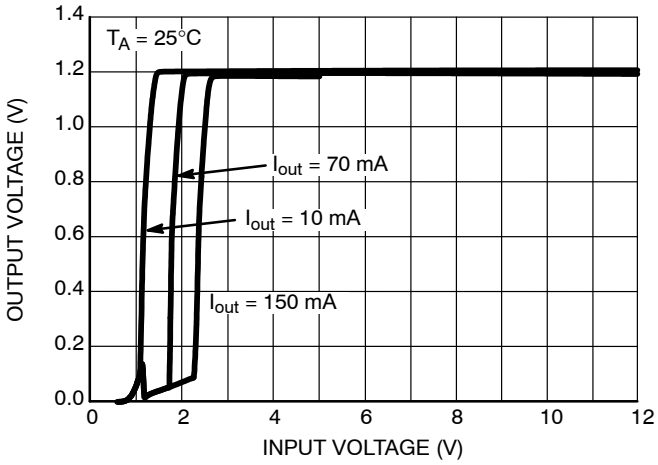


Figure 10. Output Voltage vs. Input Voltage

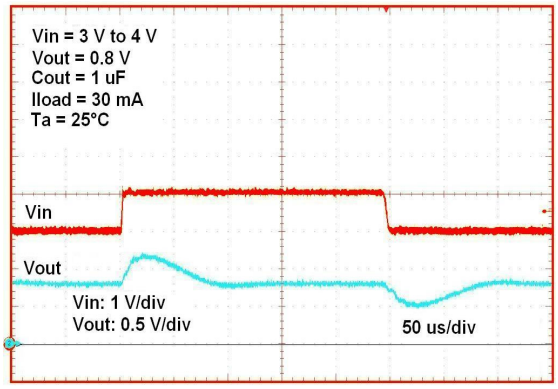


Figure 11. Line Transient Response

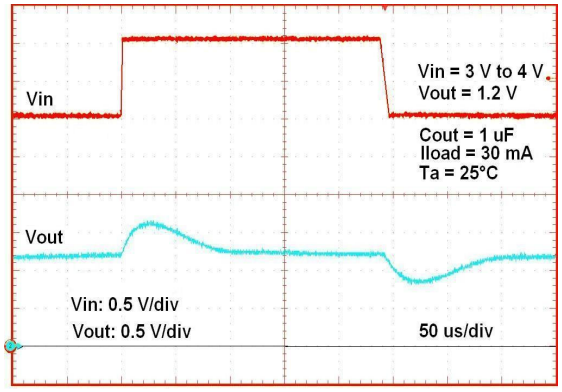


Figure 12. Line Transient Response

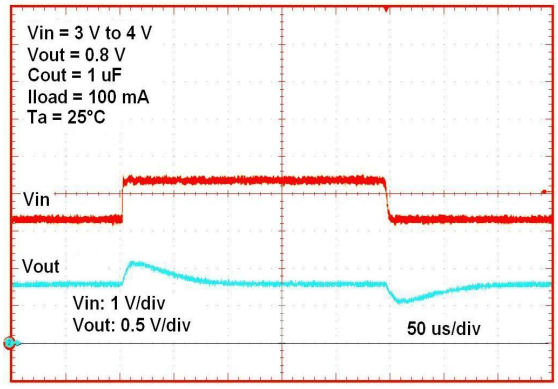


Figure 13. Line Transient Response

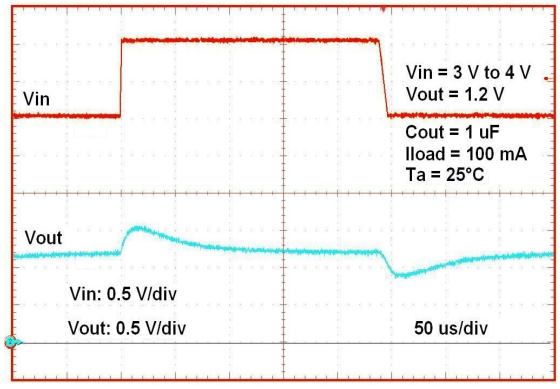


Figure 14. Line Transient Response

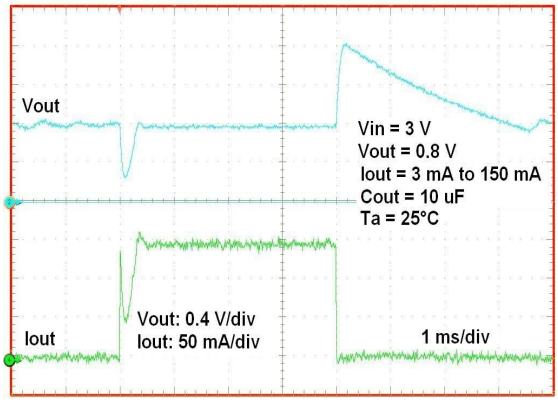


Figure 15. Load Transient Response

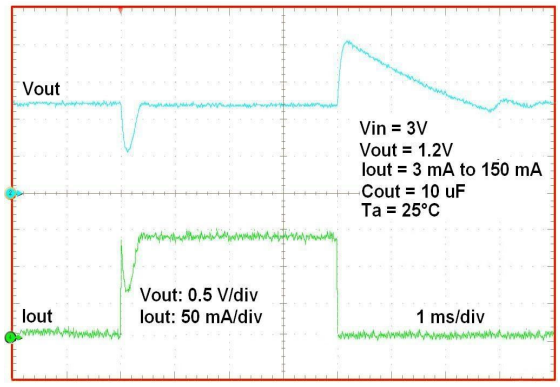


Figure 16. Load Transient Response

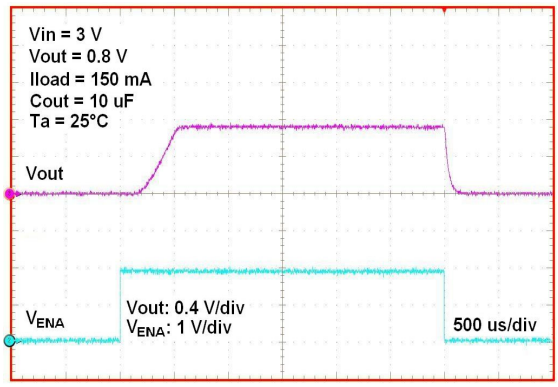


Figure 17. Enable Operation

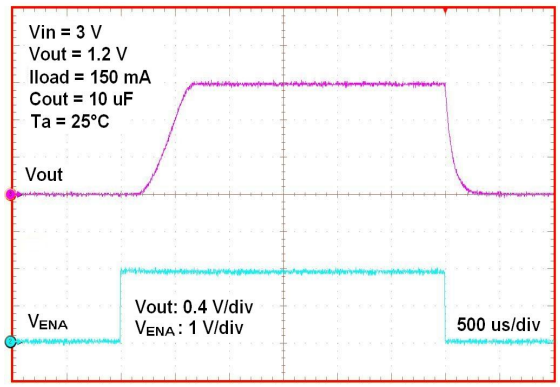


Figure 18. Enable Operation

APPLICATIONS INFORMATION

A typical application circuit for the NCP571 series is shown in Figure 2.

Input Decoupling (C1)

A 0.1 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP571 package. Higher values and lower ESR will improve the overall line transient response.

Output Decoupling (C2)

The NCP571 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger output capacitors can be used without fear of instabilities. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}. It is not recommended to leave this pin on air. In case the voltage of Enable signal is higher then Input voltage of NCP571 device it is necessary add an resistor divider in order to keep voltage at Enable pin bellow Input voltage. A single gate device of VHC family could be used for this logic level translation. The NL17SZ06 device could be chosen for non inverting open−drain buffer as shown in Figure 19. Other possibility is using NL17SZ16 device as shown in Figure 20. More information is mentioned in Application Note AND8101/D.

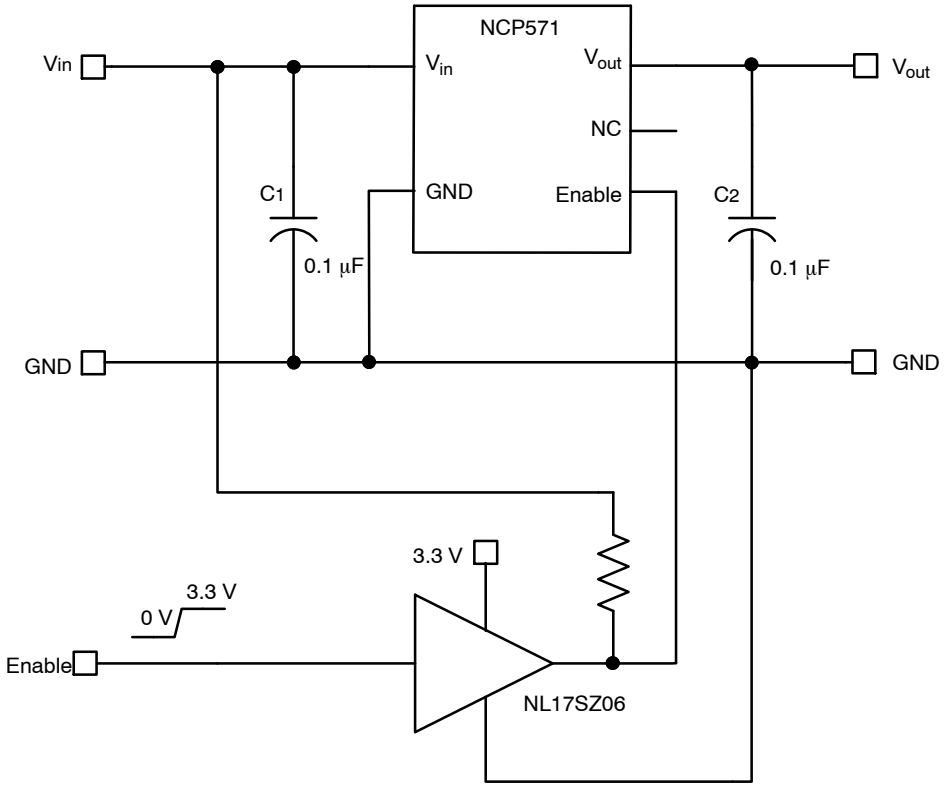


Figure 19.

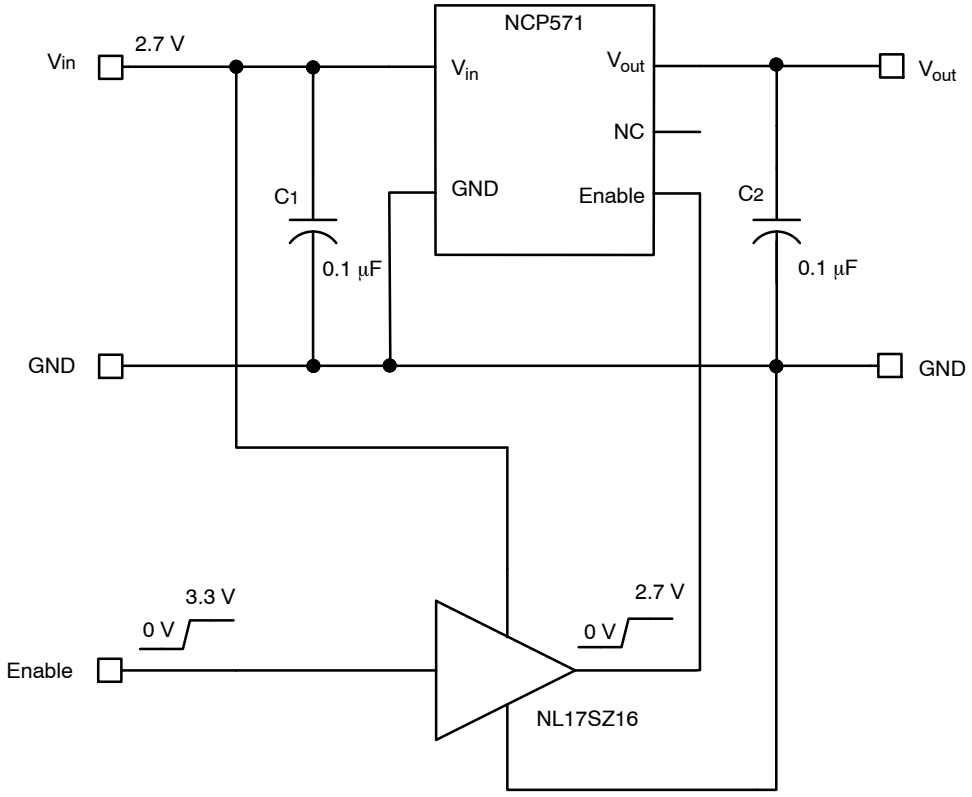


Figure 20.

Hints

Please be sure the V_{in} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP571 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP571 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the NCP571 can dissipate up to 400 mW @ 25°C.

The power dissipated by the NCP571 can be calculated from the following equation:

$$P_{tot} = V_{in(max)}\left(I_{GND} + I_{out}\right) - V_{out} * I_{out}$$

If a 150 mA output current is needed then the ground current from the data sheet is 4.0 μA.

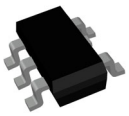
ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP571SN08T1G	0.8	N6A	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP571SN09T1G	0.9	N6E	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP571SN10T1G	1.0	N6C	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP571SN12T1G	1.2	N6D	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV571SN08T1G*	0.8	N6F	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV571SN09T1G*	0.9	N6G	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV571SN10T1G*	1.0	N6H	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV571SN12T1G*	1.2	N6J	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP571MN08TBG	0.8	AC	DFN6 (Pb−Free)	3000 / Tape & Reel
NCP571MN09TBG	0.9	AD	DFN6 (Pb−Free)	3000 / Tape & Reel
NCP571MN10TBG	1.0	AE	DFN6 (Pb−Free)	3000 / Tape & Reel
NCP571MN12TBG	1.2	AA	DFN6 (Pb−Free)	3000 / Tape & Reel
NCV571MN08TBG*	0.8	AF	DFN6 (Pb−Free)	3000 / Tape & Reel
NCV571MN09TBG*	0.9	AG	DFN6 (Pb−Free)	3000 / Tape & Reel
NCV571MN10TBG*	1.0	AH	DFN6 (Pb−Free)	3000 / Tape & Reel
NCV571MN12TBG*	1.2	AJ	DFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

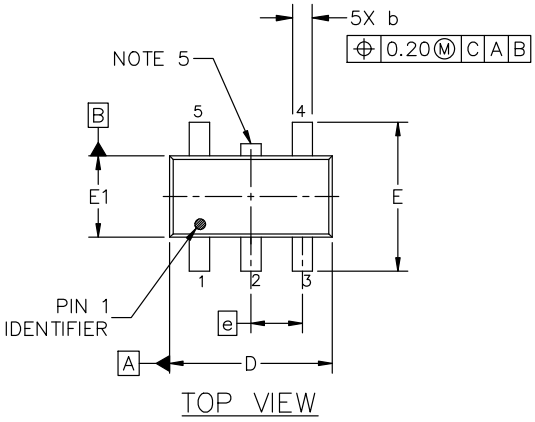
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

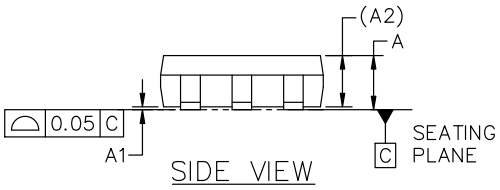


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

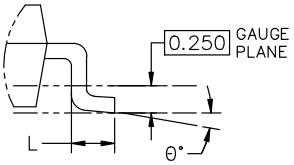
DATE 01 APR 2024



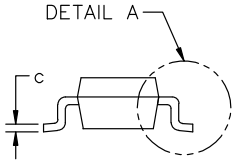
TOP VIEW



SIDE VIEW



DETAIL "A"
SCALE 2:1

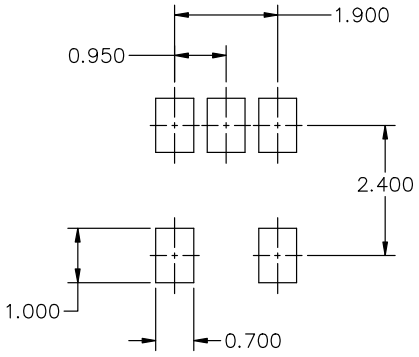


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

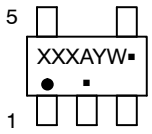
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

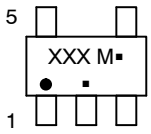
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

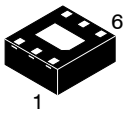
DOCUMENT NUMBER:	**98ARB18753C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TSOP−5 3.00x1.50x0.95, 0.95P**	**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

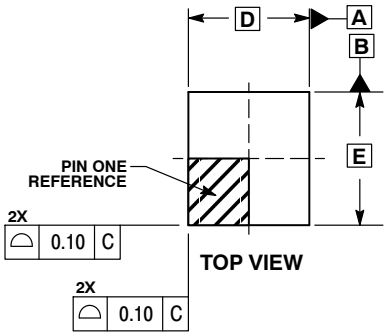
ON Semiconductor®

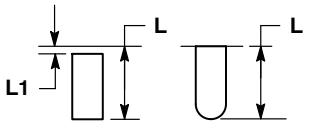


SCALE 4:1

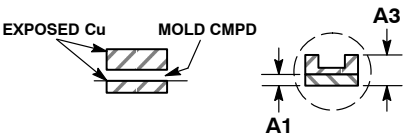
DFN6, 2x2.2, 0.65P
CASE 506BA−01
ISSUE A

DATE 07 JUL 2008

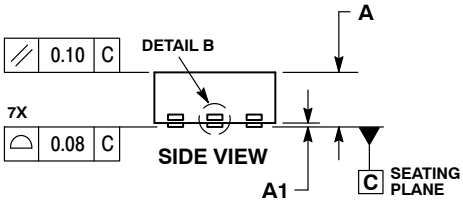


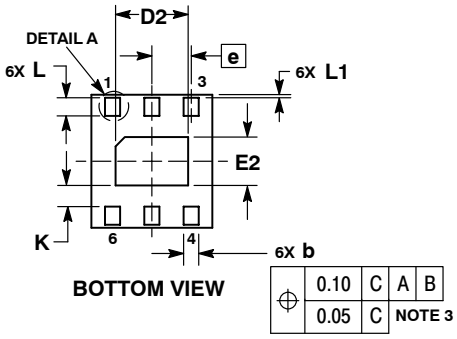


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

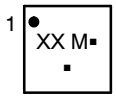




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.20 BSC	
E2	0.70	0.90
e	0.65 BSC	
K	0.20	−−−
L	0.25	0.35
L1	0.00	0.10

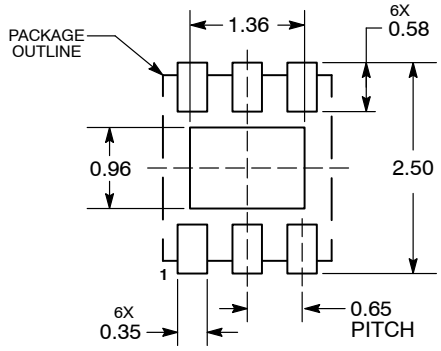
GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON23023D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**6 PIN DFN, 2.0X2.2, 0.65P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales