ESD Protection Diode Array, 5-Line

SMS05C, SMS12C, SMS15C, SMS24C

This 5−line surge protection array is designed for application requiring transient voltage protection capability. It is intended for use in over−transient voltage and ESD sensitive equipment such as computers, printers, automotive electronics, networking communication and other applications. This device features a monolithic common anode design which protects five independent lines in a single TSOP−6 package.

Features

- Protects up to 5 Lines in a Single TSOP−6 Package
- Peak Power Dissipation − 350 W (8 × 20 μs Waveform)
- ESD Rating of Class 3B (Exceeding 8.0 kV) per Human Body Model and Class C (Exceeding 400 V) per Machine Model
- Compliance with IEC 61000−4−2 (ESD) 15 kV (Air), 8.0 kV (Contact)
- Flammability Rating of UL 94 V−0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices

Applications

- Hand−Held Portable Applications
- Networking and Telecom
- Automotive Electronics
- Serial and Parallel Ports
- Notebooks, Desktops, Servers

MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Rating	Value	Unit
P_{PK} 1	Peak Power Dissipation 8 × 20 μs Double Exponential Waveform (Note 2)	350	W
T_J	Operating Junction Temperature Range	−40 to 150	°C
T_{STG}	Storage Temperature Range	−55 to 150	°C
T_L	Lead Solder Temperature (10 s)	260	°C
ESD	Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Air (ESD) IEC 61000−4−2 Contact (ESD)	>8000 >400 >15000 >8000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

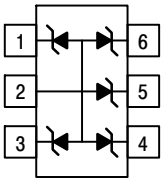
2. Non−repetitive current pulse per Figure 3.

TSOP−6 FIVE SURGE PROTECTION 350 W PEAK POWER

PIN ASSIGNMENT

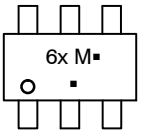


TSOP−6
CASE 318G
SCALE 2:1



PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

MARKING DIAGRAM



x = SMS05C:J
= SMS12C:K
= SMS15C:L
= SMS24C:M
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
SMS05CT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel
SMS15CT1G		
SMS24CT1G		
SZSMS24CT1G		

DISCONTINUED (Note 1)

SMS12CT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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SMS05C ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)			5.0	V
V_{BR}	Breakdown Voltage	I_T = 1.0 mA (Note 3)	6.2		7.2	V
I_R	Reverse Leakage Current	V_{RWM} = 5.0 V			5.0	μA
V_C	Clamping Voltage	I_{PP} = 5.0 A (8 × 20 μs Waveform)			9.8	V
V_C	Clamping Voltage	I_{PP} = 24 A (8 × 20 μs Waveform)			14.5	V
I_{PP}	Maximum Peak Pulse Current	8 × 20 μs Waveform			24	A
C_J	Capacitance	V_R = 0 V, f = 1.0 MHz (Line to GND)		260	400	pF

SMS12C ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)			12	V
V_{BR}	Breakdown Voltage	I_T = 1.0 mA (Note 3)	13.3		15	V
I_R	Reverse Leakage Current	V_{RWM} = 12 V		0.001	1.0	μA
V_C	Clamping Voltage	I_{PP} = 5.0 A (8 × 20 μs Waveform)			19	V
V_C	Clamping Voltage	I_{PP} = 15 A (8 × 20 μs Waveform)			23	V
I_{PP}	Maximum Peak Pulse Current	8 × 20 μs Waveform			15	A
C_J	Capacitance	V_R = 0 V, f = 1.0 MHz (Line to GND)		120	150	pF

SMS15C ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified) (See Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)			15	V
V_{BR}	Breakdown Voltage	I_T = 1.0 mA (Note 3)	17		19	V
I_R	Reverse Leakage Current	V_{RWM} = 15 V		0.05	1.0	μA
V_C	Clamping Voltage	I_{PP} = 5.0 A (8 × 20 μs Waveform)			24	V
V_C	Clamping Voltage	I_{PP} = 12 A (8 × 20 μs Waveform)			29	V
I_{PP}	Maximum Peak Pulse Current	8 × 20 μs Waveform			12	A
C_J	Capacitance	V_R = 0 V, f = 1.0 MHz (Line to GND)		95	125	pF

SZ/SMS24C ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	Reverse Working Voltage	(Note 2)			24	V
V_{BR}	Breakdown Voltage	I_T = 1.0 mA (Note 3)	26.7		32	V
I_R	Reverse Leakage Current	V_{RWM} = 24 V		0.001	1.0	μA
V_C	Clamping Voltage	I_{PP} = 5.0 A (8 × 20 μs Waveform)			40	V
V_C	Clamping Voltage	I_{PP} = 8 A (8 × 20 μs Waveform)			44	V
I_{PP}	Maximum Peak Pulse Current	8 × 20 μs Waveform			8.0	A
C_J	Capacitance	V_R = 0 V, f = 1.0 MHz (Line to GND)		60	75	pF

3. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at pulse test current I_T.
5. Parametrics are the same for the Pb−Free packages, which are suffixed with a “G”.

TYPICAL PERFORMANCE CURVES (T_J = 25°C UNLESS OTHERWISE SPECIFIED)

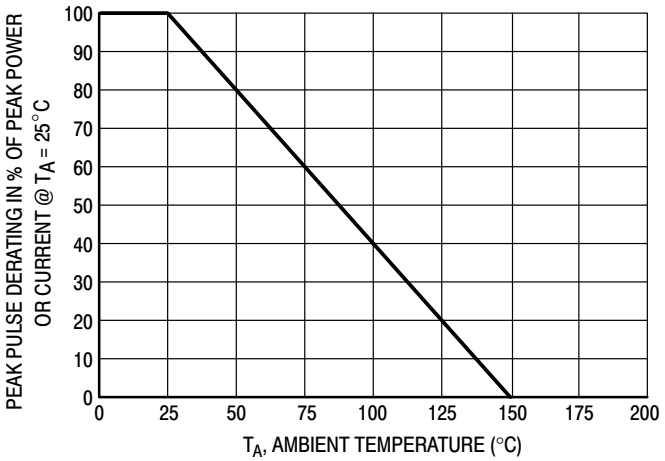


Figure 1. Pulse Derating Curve

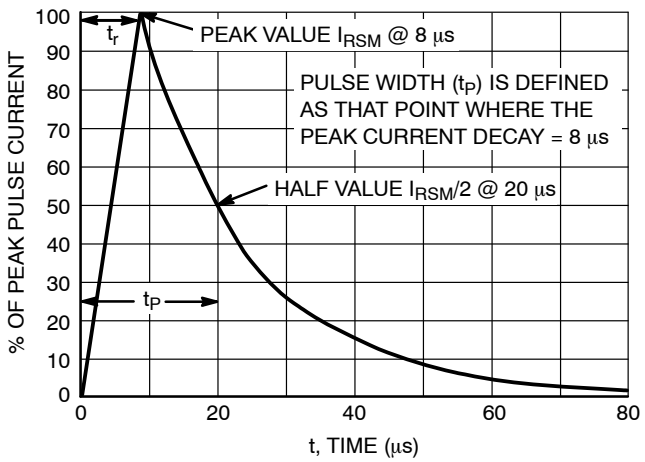


Figure 2. 8 × 20 μs Pulse Waveform

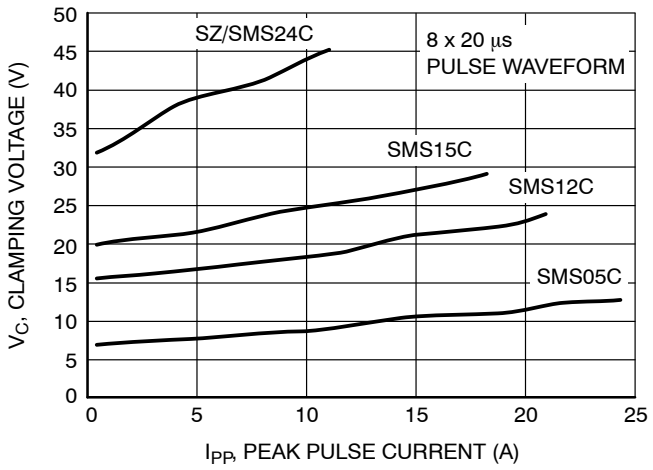


Figure 3. Clamping Voltage vs. Peak Pulse Current

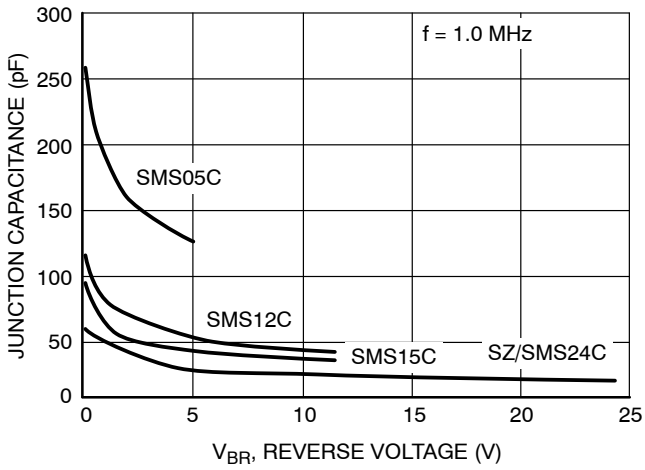


Figure 4. Junction Capacitance vs. Reverse Voltage

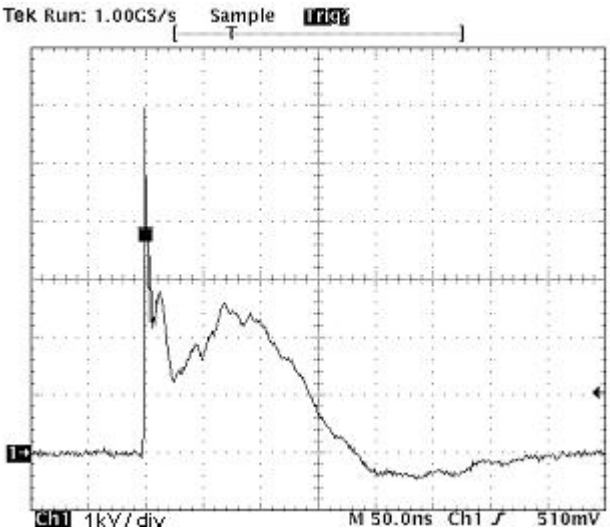


Figure 5. ESD Pulse IEC 61000−4−2 (8.0 kV Contact)

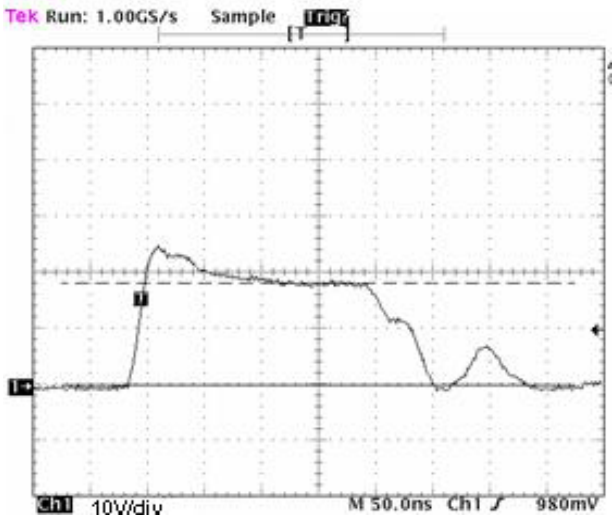


Figure 6. SMS15CT1 ESD Response for IEC 61000−4−2 (+8.0 kV Contact)

TYPICAL COMMON ANODE APPLICATIONS

A 5 surge protection junction common anode design in a TSOP−6 package protects four separate lines using only one package. This adds flexibility and creativity to PCB design especially when board space is at a premium. A simplified example of SMS05C Series Device applications is illustrated below.

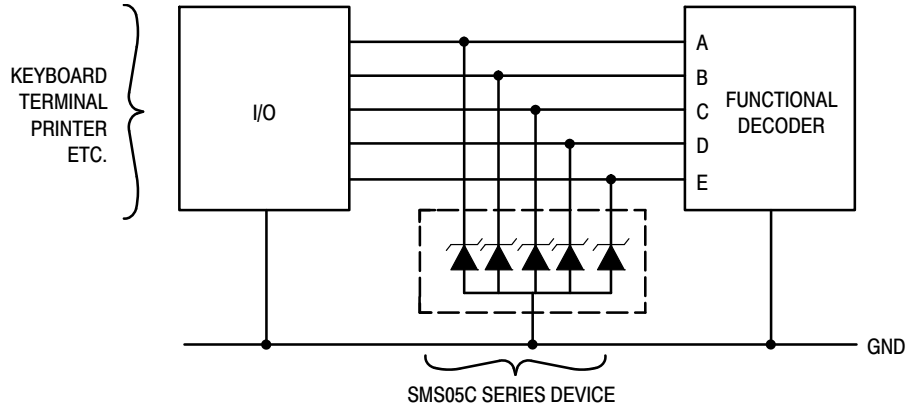


Figure 7. Computer Interface Protection

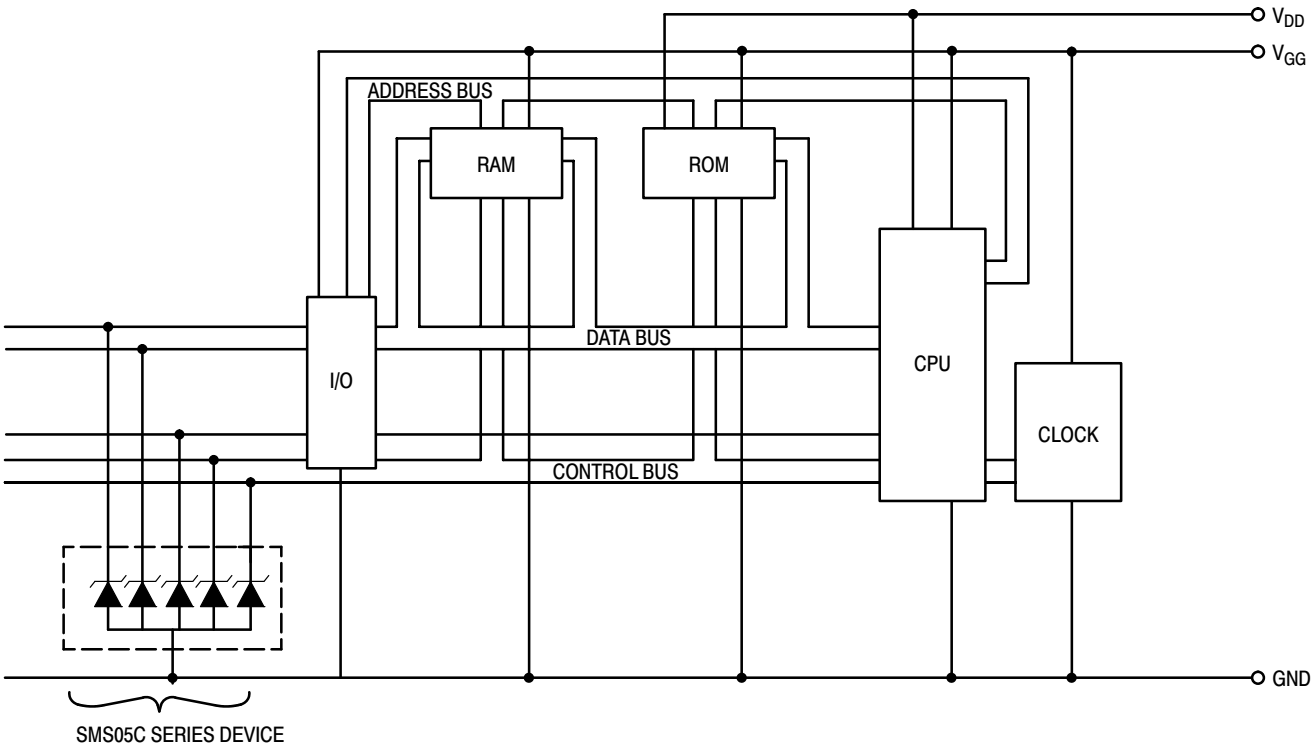
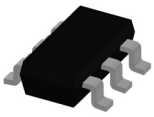
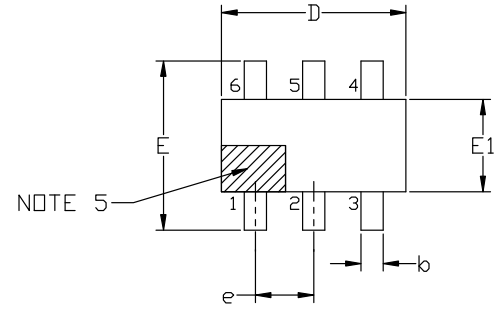


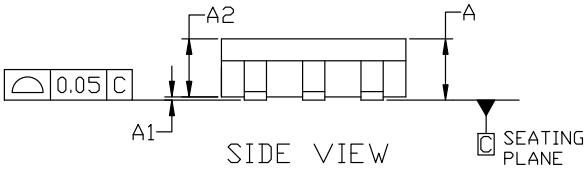
Figure 8. Microprocessor Protection

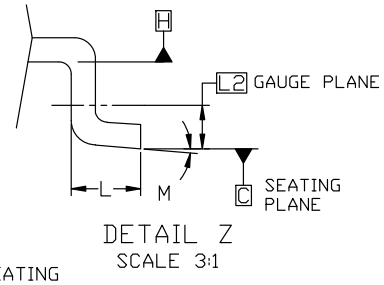


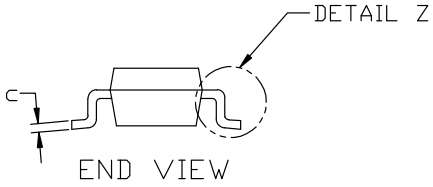
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024



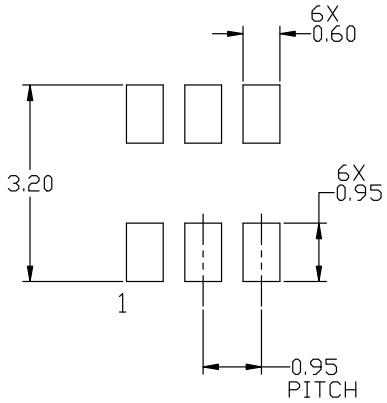






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

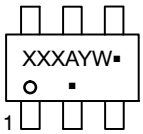
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CASE 318G
ISSUE W

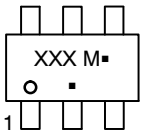
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

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