MPM3824C

2.75V to 6V, 2A, Ultra-Small Power Module with Ultra-Low Noise

DESCRIPTION

The MPM3824C is synchronous, step-down power module with an integrated inductor. The MPM3824C achieves 2A of continuous output current (I_{OUT}) from a 2.75V to 6V input voltage (V_{IN}) range with excellent load and line regulation. The MPM3824C works in forced continuous conduction mode (FCCM) and has a small output voltage (V_{OUT}) ripple with one output capacitor, making it well-suited for optical modules, FPGA, ASIC, and other applications requiring low ripple noise as well as a small PCB area.

V_{OUT} can be regulated to be as low as 0.6V. Only FB resistors, input capacitors, and output capacitors are required to complete the design. Constant-on-time (COT) control provides fast transient response, high efficiency, and easy loop stabilization.

Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPM3824C requires a minimal number of readily available, standard external components. It is available in an ultra-small ECLGA-14 (2.5mmx2.5mmx1.2mm) package.

FEATURES

- Wide 2.75V to 6V Operating Input Voltage (V_{IN}) Range
- Adjustable Output Voltage (V_{OUT}) from 0.6V
- Up to 2A Continuous Output Current (I_{OUT})
- 100% Duty Cycle in Dropout
- Forced Continuous Conduction Mode (FCCM)
- Enable (EN) and Power Good (PG) for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Only Four External Components Required
- Available in an ECLGA-14 (2.5mmx2.5mmx1.2mm) Package

APPLICATIONS

- FPGA, ASIC, DSP Power
- Optical Modules
- LDO Replacements
- Power for Portable Products
- Storage (Solid-State Drives and Hard-Disk Drives)
- Space-Constrained Applications

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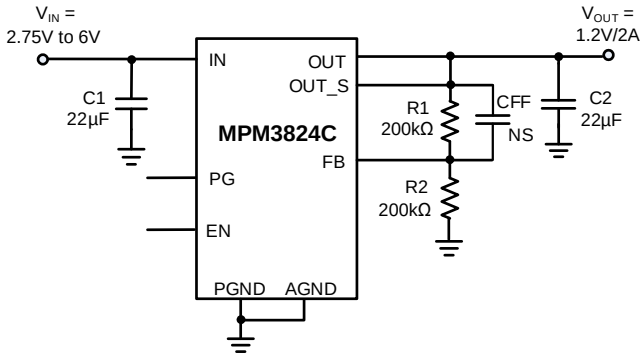
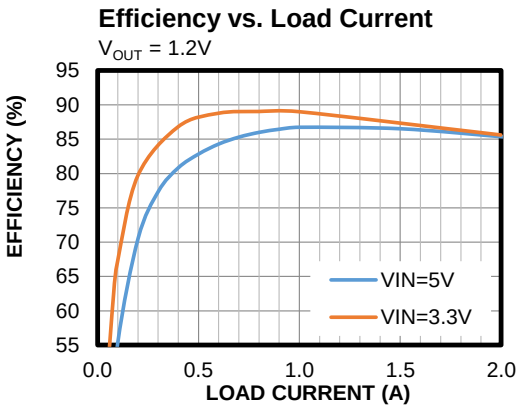
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3824CGPA	ECLGA-14 (2.5mmx2.5mm)	*See Below*	3

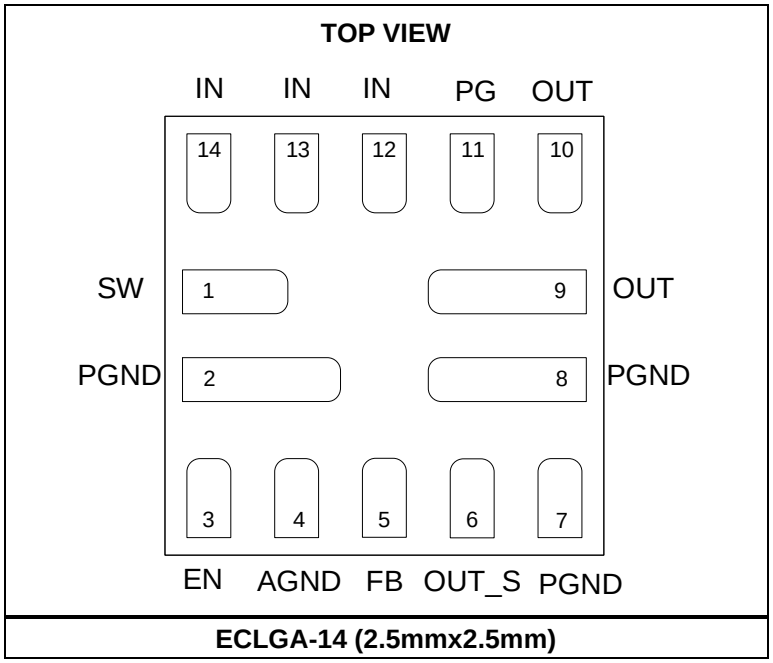
* For Tape & Reel, add suffix -Z (e.g. MPM3824CGPA-Z).

TOP MARKING

$\overline{\text{BTJ}}$
YWW
LLL

BTJ: Product code of MPM3824CGPA
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



ECLGA-14 (2.5mmx2.5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SW	**SW test pin.** Float the SW pin.
2, 7, 8	PGND	**Power ground.**
3	EN	**On/off control.**
4	AGND	**Analog ground for the internal control circuit.** The AGND pin is not connected to PGND internally. Connect AGND to the PGND on the PCB layout.
5	FB	**Feedback**. Use an external resistor divider from the output to AGND, tapped to the FB pin, to set the output voltage (V_{OUT}).
6	OUT_S	**Output voltage sense.**
9, 10	OUT	**Power output.**
11	PG	**Power good indicator.** The output of the PG pin is an open drain with an internal pull-up resistor connected to the IN pin. PG is pulled up to IN when the FB voltage is within 10% of the regulation level; otherwise, PG is low.
12, 13, 14	IN	**Power input.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{SW} .....
-0.3V (-5V for <10ns) to +6.5V (+10V for <10ns)
All other pins..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C)(5)
ECLGA-14 (2.5mmx2.5mm).....2.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....2000V

Recommended Operating Conditions (2)

Operation input voltage range..... 2.75V to 6V
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (3) (4) (5) (6) (7)

ECLGA-14 (2.5mmx2.5mm)
θ_{JA}.....56.7°C/W
θ_{JC_TOP}.....6.85°C/W
θ_{JB}.....25.5°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is the junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
4) The thermal parameter is based on a test on the MPS evaluation board (T-EVM3824C-PA-00A) under no airflow cooling condition in a standard enclosure. The board size is 5.1cmx5.1cm and 2 layers, of which top and bottom layer Cu thickness is 2oz.
5) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
6) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on equation $T_I = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$. Where P_{LOSS} is the entire loss of the module in real applications, and T_{CASE_TOP} is case top temperature
7) The junction-to-board thermal characterization parameter, θ_{JB}, estimation the junction temperature in the real system, based on equation $T_I = \theta_{JB} \times P_{LOSS} + T_{BOARD}$. Where P_{LOSS} is the entire power loss of the module in real applications, and T_{BOARD} is the board temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback (FB) voltage	V_{FB}	2.75V ≤ V_{IN} ≤ 6V	591	600	609	mV
FB current	I_{FB}	V_{FB} = 0.6V		10		nA
Inductor value	L	Inductance at 1MHz		0.47		µH
Dropout resistance	R_{DR}	100% on duty		75		mΩ
Switch leakage		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C		0	2	µA
P-channel MOSFET peak current limit		T_J = 25°C	4	5.2		A
N-channel MOSFET valley current limit [9]				2.5		A
On time	t_{ON}	V_{IN} = 5V, V_{OUT} = 1.2V		185		ns
		V_{IN} = 3.6V, V_{OUT} = 1.2V		250		
Switching frequency	f_{SW}	V_{OUT} = 1.2V, I_{LOAD} = 1A		1250		kHz
Minimum off time [9]	$t_{MIN-OFF}$			100		ns
Minimum on time [9]	t_{MIN-ON}			80		ns
Soft-start (SS) time [9]	t_{SS-ON}			1.7		ms
Soft shutdown time	t_{SS-OFF}			2		ms
Power good (PG) upper trip threshold	PG_OV	FB voltage in respect to the regulation		7		%
PG lower trip threshold	PG_UV			-12		%
PG delay				100		µs
PG sink current capability	V_{PG_LO}	Sink 1mA			0.4	V
PG logic high voltage	V_{PG_HI}	V_{IN} = 5V, V_{FB} = 0.6V	4			V
PG internal pull-up resistor	R_{PG}			440		kΩ
Under-voltage lockout (UVLO) rising threshold			2.3	2.5	2.75	V
UVLO threshold hysteresis				400		mV
EN input logic low voltage					0.3	V
EN input logic high voltage			1.2			V
EN input current		V_{EN} = 2V		2		µA
		V_{EN} = 0V		0		µA
Supply current (shutdown)		V_{EN} = 0V, T_J = 25°C		0	1	µA
Supply current (quiescent)		V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V		500		µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +125°C [8], typical value is tested at T_J = 25°C. The over-temperature limit is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Converter System [9]						
Output voltage range [9]			0.6		6	V
Recommended input capacitance [9]	C_{IN1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	4.7	22		µF
Output capacitance [9]	C_{OUT1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A	10	22		µF
Output voltage ripple [9]		V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 2A		8		mV
Efficiency [9]		V_{IN} = 3.6V, V_{OUT} = 1.2V, I_{OUT} = 2A		85		%
Load transient response peak-to-peak voltage [9]	V_{P2P1}	V_{IN} = 3.6V, V_{OUT} = 1.2V, C_{OUT} = 22µF, I_{OUT} = 0A to 2A at 1A/µs			140	mV
Thermal shutdown [9]				150		°C
Thermal hysteresis [9]				30		°C

Notes:

8) Not tested in production. Guaranteed by over-temperature correlation.
9) Guaranteed by engineering sample characterization.

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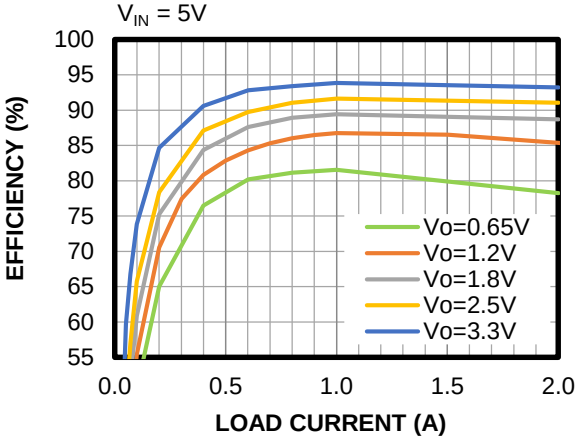
TYPICAL CHARACTERISTICS

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

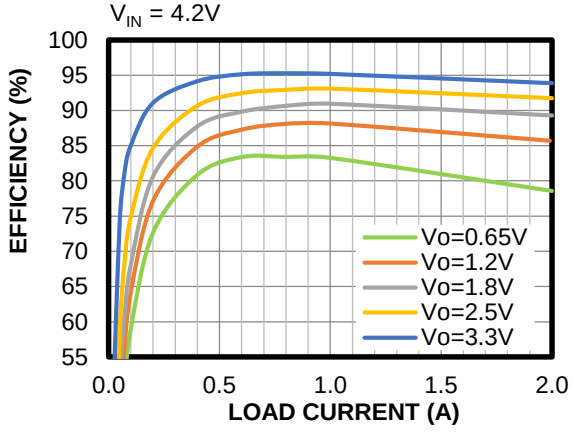
Efficiency vs. Load Current

V_{IN} = 5V



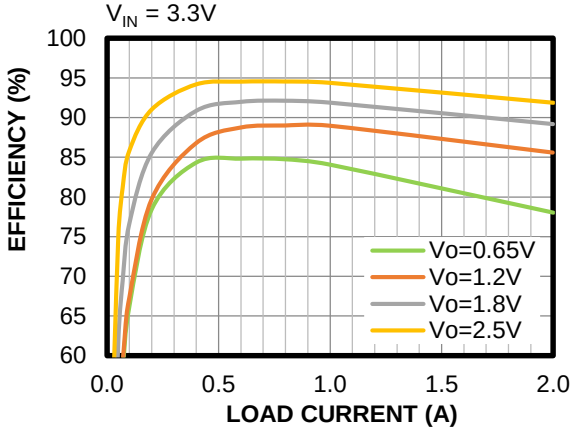
Efficiency vs. Load Current

V_{IN} = 4.2V



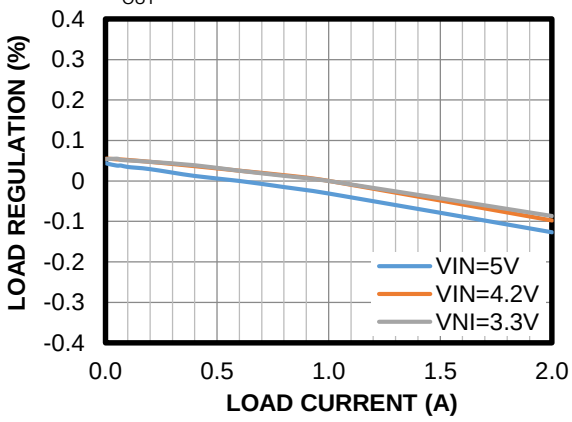
Efficiency vs. Load Current

V_{IN} = 3.3V



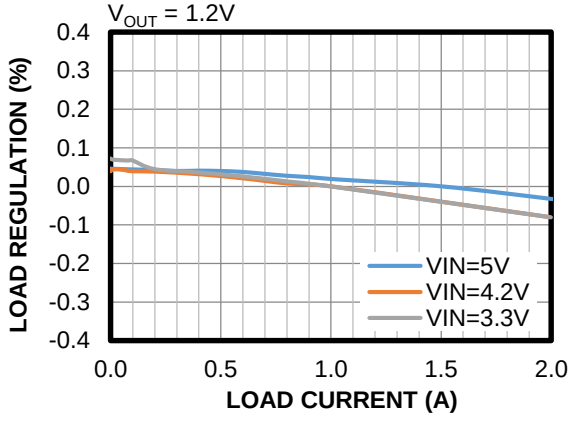
Load Regulation

V_{OUT} = 0.65V



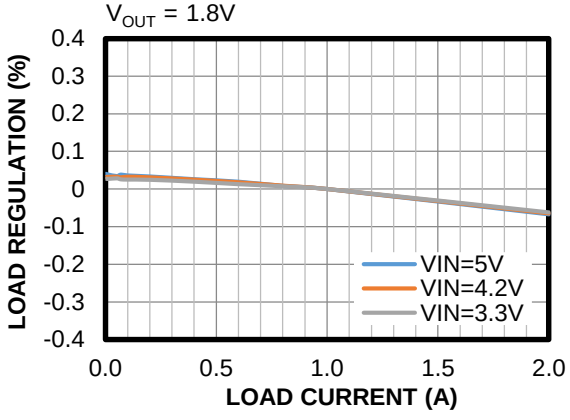
Load Regulation

V_{OUT} = 1.2V



Load Regulation

V_{OUT} = 1.8V



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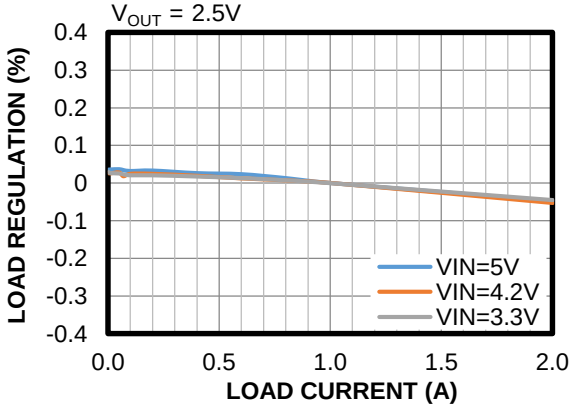
TYPICAL CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

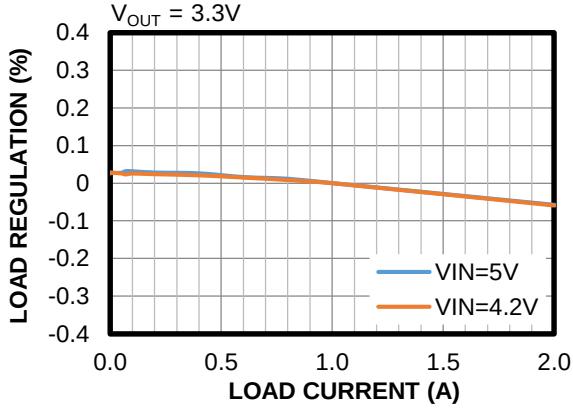
Load Regulation

V_{OUT} = 2.5V



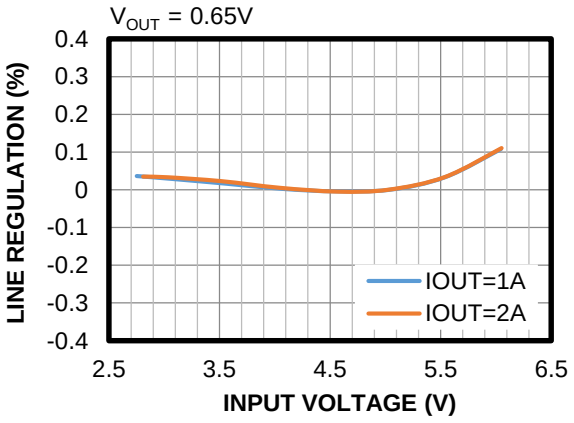
Load Regulation

V_{OUT} = 3.3V



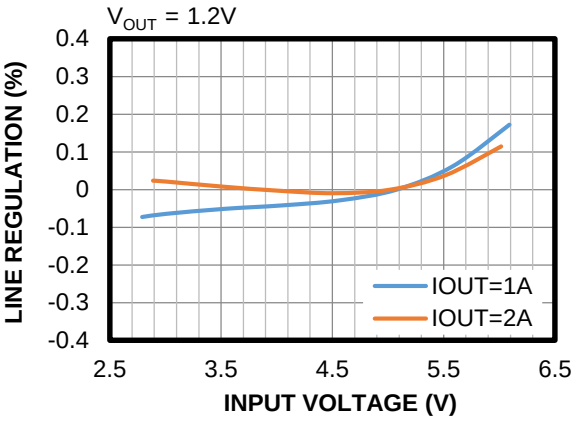
Line Regulation

V_{OUT} = 0.65V



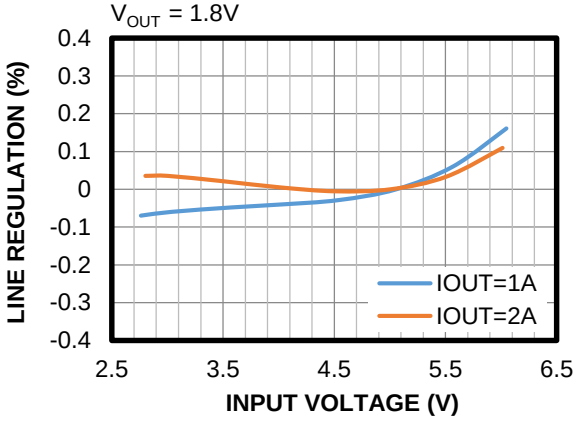
Line Regulation

V_{OUT} = 1.2V



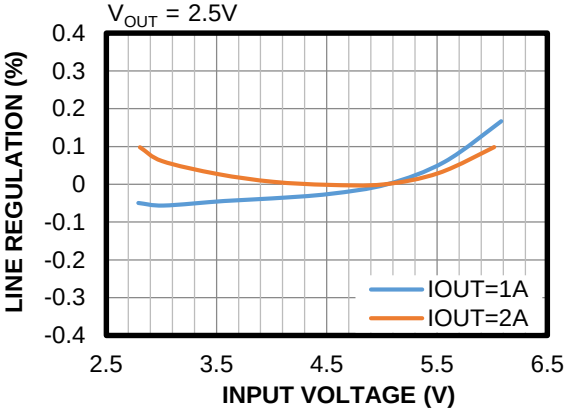
Line Regulation

V_{OUT} = 1.8V



Line Regulation

V_{OUT} = 2.5V



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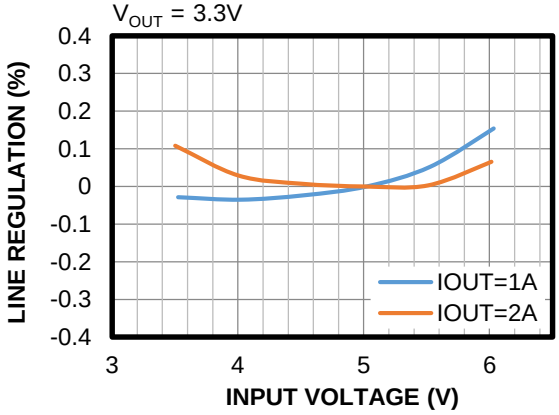
TYPICAL CHARACTERISTICS *(continued)*

Performance curves are tested on the evaluation board. V_{IN} = 5V, V_{OUT} = 1.2V, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

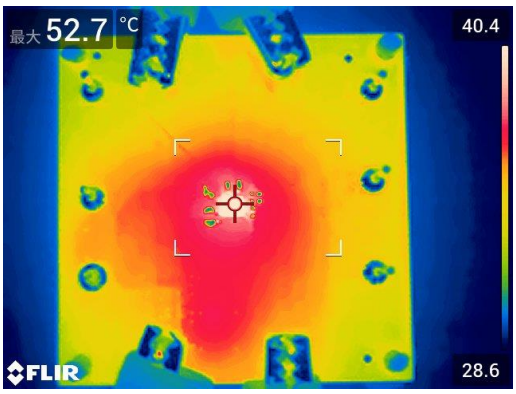
Line Regulation

V_{OUT} = 3.3V



Thermal Results

I_{OUT} = 2A, 4-layer PCB



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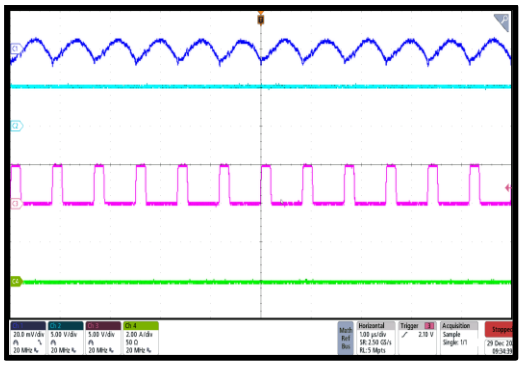
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. C_{IN} = 22µF, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

Steady State

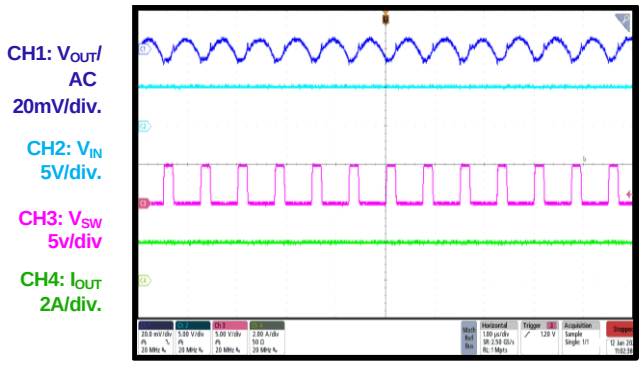
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



1µs/div.

Steady State

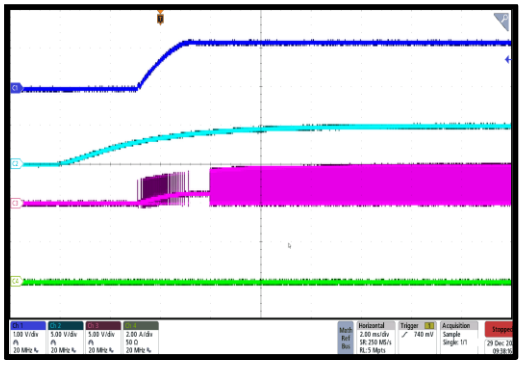
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



1µs/div.

Start-Up through VIN

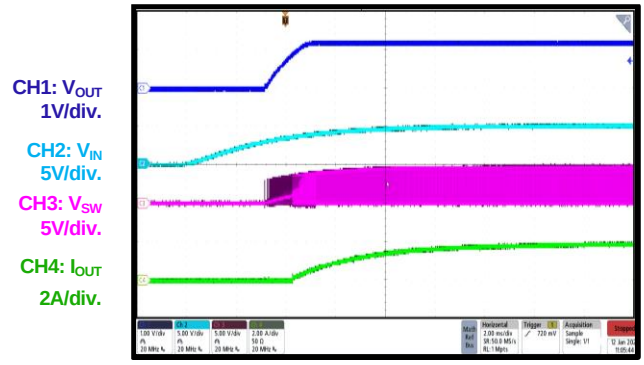
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



2ms/div.

Start-Up through VIN

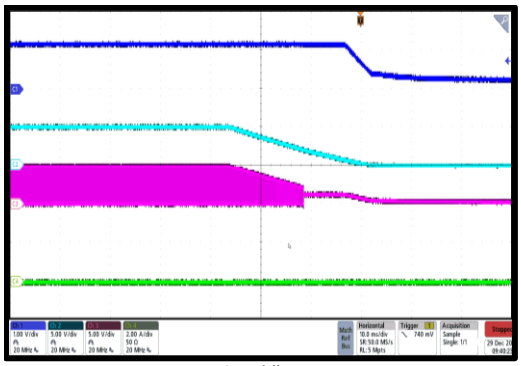
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



2ms/div.

Shutdown through VIN

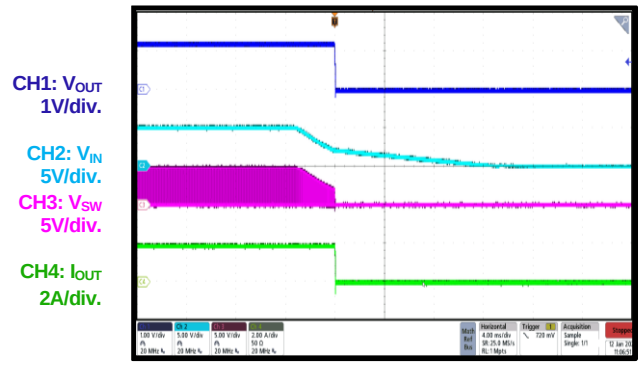
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



10ms/div.

Shutdown through VIN

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



4ms/div.

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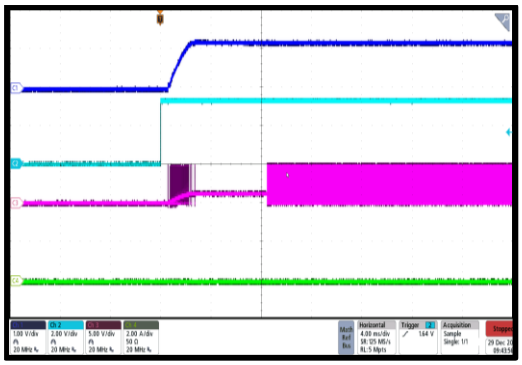
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. C_{IN} = 22µF, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

Start-Up through EN

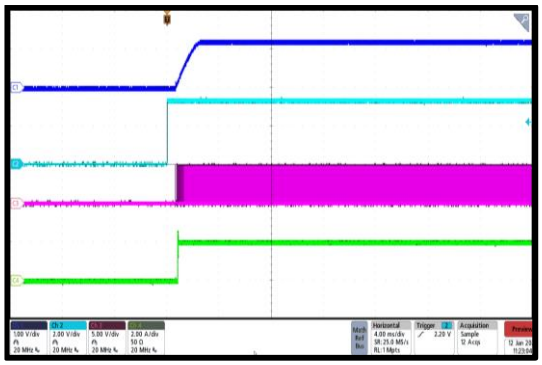
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



4ms/div.

Start-Up through EN

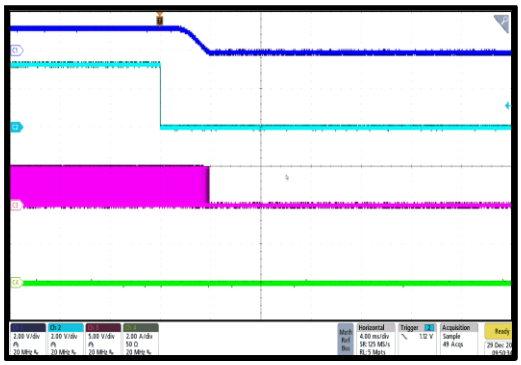
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



4ms/div.

Shutdown through EN

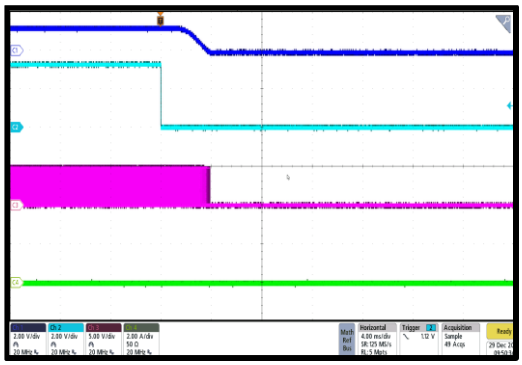
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



4ms/div.

Shutdown through EN

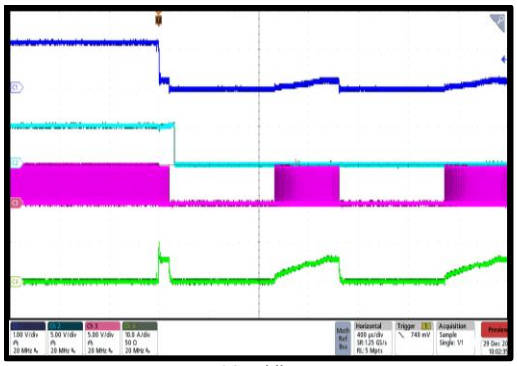
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



4ms/div.

SCP Entry

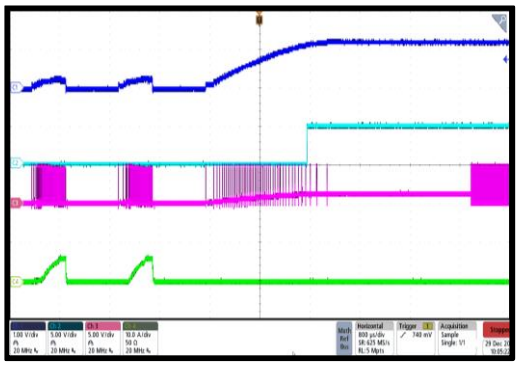
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



400µs/div.

SCP Recovery

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A



800µs/div.

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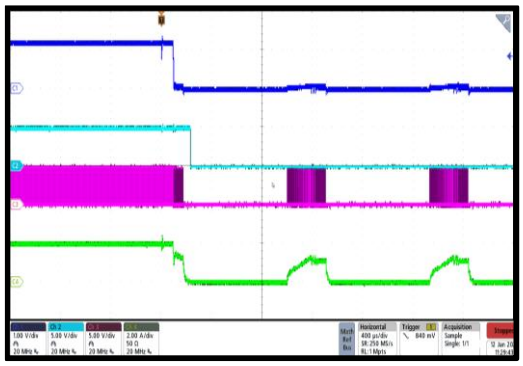
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. C_{IN} = 22µF, C_{OUT} = 22µF, V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

SCP Entry

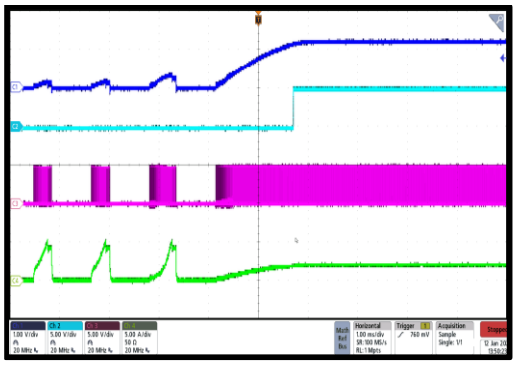
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



400µs/div.

SCP Recovery

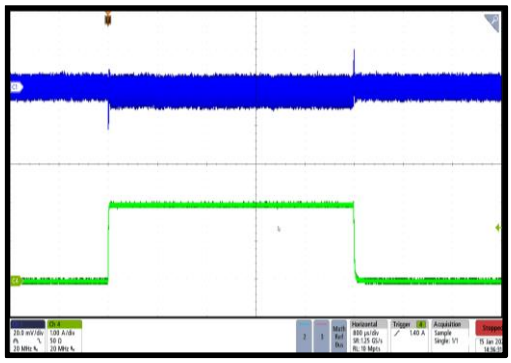
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 2A



1ms/div.

Load Transient Response

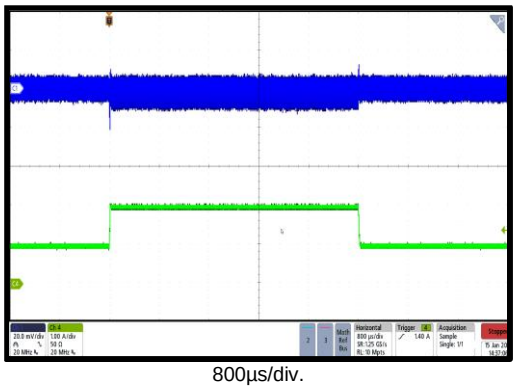
V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 0A to 2A, 2.5A/µs e-load



800µs/div.

Load Transient Response

V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 1A to 2A, 2.5A/µs e-load



800µs/div.

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FUNCTIONAL BLOCK DIAGRAM

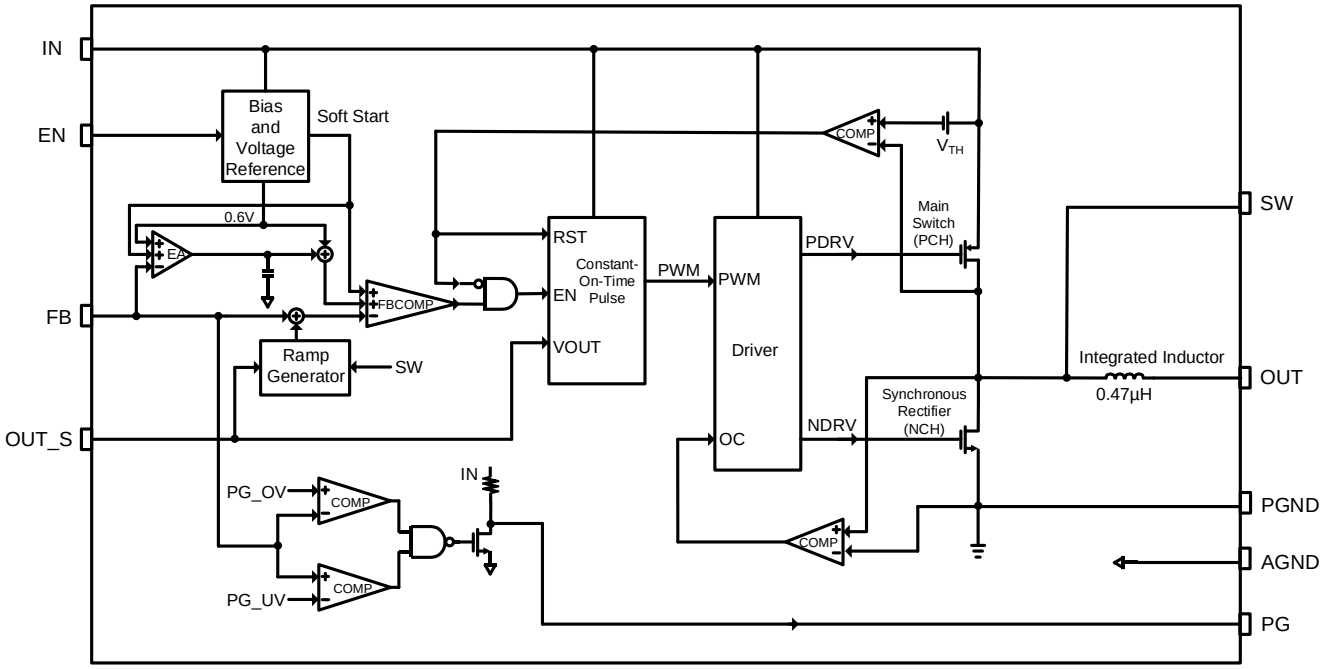

Figure 1: Functional Block Diagram

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OPERATION

The MPM3824C comes in a small surface-mounted ECLGA-14 (2.5mmx2.5mmx1.2mm) package. The MPM3824C's integrated inductor simplifies the schematic and layout design. Only FB resistors, input capacitors, and output capacitors are required to complete the design. The MPM3824C uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency across the full input range.

Constant-On-Time Control (COT)

Compared to fixed-frequency pulse-width modulation (PWM) control, COT control offers the advantage of a simpler control loop and faster transient response. By using input voltage feed-forward, the MPM3824C maintains a nearly constant switching frequency across the input and output voltage ranges. The on time of the switching pulse can be estimated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} x0.833\mu s \quad (1)$$

To prevent inductor current runaway during the load transition, the MPM3824C fixes the minimum off time to 230ns. This minimum off-time limit does not affect operation during steady state.

Forced PWM Operation

The MPM3824C works in continuous conduction mode (CCM) to achieve a smaller output voltage ripple, load regulation, and load transient response across the full load range.

Enable (EN)

If the input voltage (V_{IN}) exceeds the under-voltage lockout (UVLO) threshold (typically 2.5V), the MPM3824C can be enabled by pulling EN above the EN input logic high voltage (see the Electrical Characteristics section on page 5). Leave EN floating or pull EN down to ground to disable the MPM3824C. There is an internal 1MΩ resistor connected from the EN pin to ground.

Soft Start and Soft Shutdown

The MPM3824C has a built-in soft start that ramps up V_{OUT} at a controlled slew rate to prevent overshoots during start-up. The soft-start time is t_{SS-ON}.

When disabled, the MPM3824C ramps down the internal reference, so the load can discharge the output linearly. The soft-shutdown time is t_{SS-OFF}.

Power Good (PG) Indicator

The MPM3824C has an open drain power good (PG) pin with a 440kΩ pull-up resistor for power good indication. When FB is within PG_OV and PG_UV, PG is pulled up to IN by the internal resistor. If the FB voltage is out of the threshold window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum $R_{DS(ON)}$.

Current Limit

The MPM3824C high-side MOSFET (HS-FET) has a typical peak current limit, and the low-side MOSFET (LS-FET) has a valley current limit. When the HS-FET reaches its current limit, the HS-FET turns off, and the LS-FET turns on. When the current drops to the valley current-limit threshold, the MPM3824C turns on the HS-FET again.

The HS-FET turns off as soon as it reaches the peak current limit and the LS-FET turns off after it reaches the valley current limit. If the peak current or valley current are triggered for 64 cycles, the MPM3824C disables the regulator. This prevents the inductor current from continuously rising and damaging components.

Short-Circuit Protection (SCP) and Recovery

If the output is shorted to GND, the current limit is triggered. If the current limit lasts for about 64 cycles, the MPM3824C enters hiccup mode and disables the output power stage. The MPM3824C discharges the soft-start capacitor, then automatically attempts to soft start again. If the short-circuit condition remains after soft start ends, the MPM3824C repeats this operation until the short circuit is removed and the output rises back to the regulation level.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). Consider the tradeoff between stability and dynamics to choose a feedback resistor (R1) that is not too large or too small. There is no strict requirement for the feedback resistor. R2 can be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (2)$$

Figure 2 shows the feedback circuit.

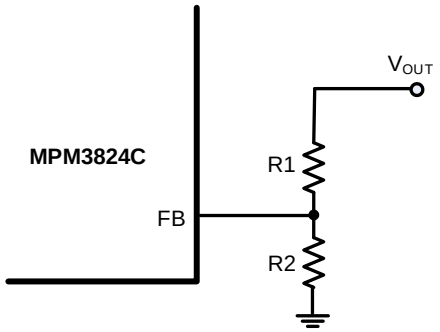

Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current while maintaining the DC input voltage. For optimal performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (i.e. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be calculated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage.

Low-ESR ceramic capacitors can be used to keep the output voltage ripple low. Generally, a 22µF output ceramic capacitor is sufficient for most applications. If V_{OUT} is higher, a 47µF capacitor may be required to stabilize the system.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

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When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output voltage ripple can be calculated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} x L_1} x \left(1 - \frac{V_{OUT}}{V_{IN}}\right) x R_{ESR} \quad (7)$$

Where L1 is the 0.47μH integrated inductor.

The output capacitor's characteristics affect the stability of the regulation system.

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PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation, especially for the high switching frequency converter. A poorly optimized layout can result in poor line or load regulation or stability issues. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place a 0805-sized ceramic input capacitor as close to the IC pins as possible.
2. Place a 0402-sized capacitor place at the bottom of the IC (optional).
3. Connect the two ends of the ceramic capacitor directly to IN and PGND.
4. Place the external feedback resistor next to FB.
5. Connect AGND and PGND at a single point.

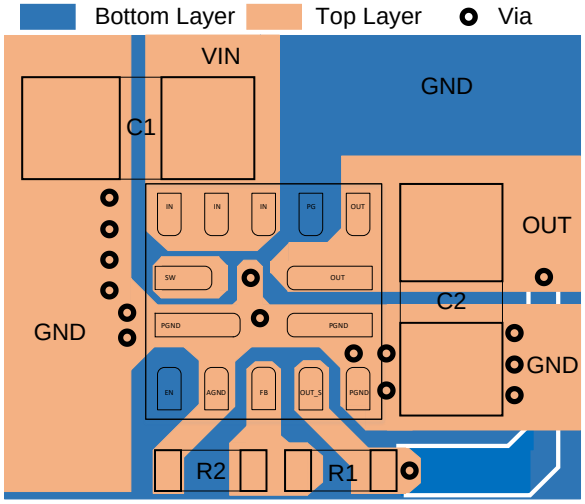

Figure 3: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

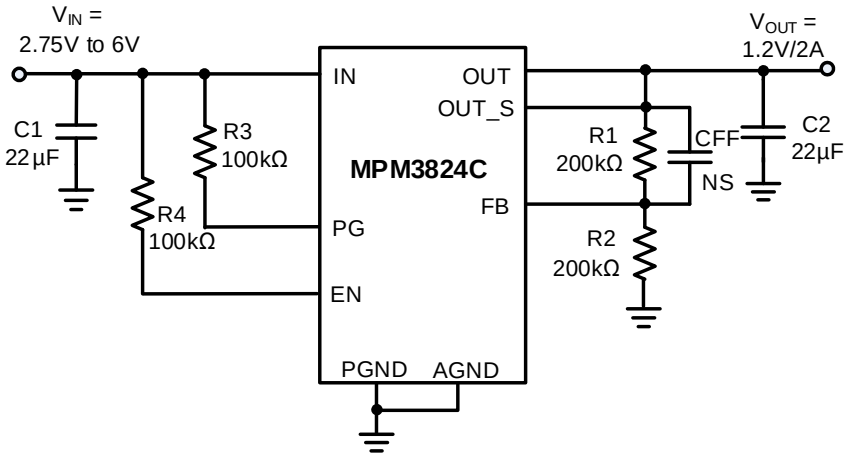

Figure 4: Typical Application Circuit (10)

Note:

10) Additional input capacitors may be required for applications where V_{IN} < 3.3V.

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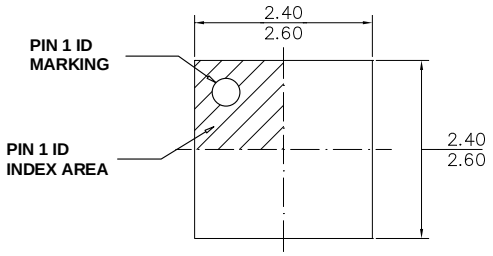
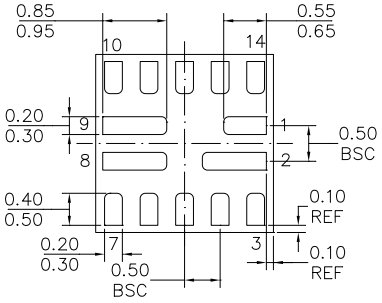
PACKAGE INFORMATION

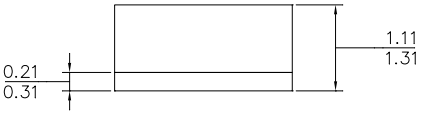
ECLGA-14 (2.5mmx2.5mm)



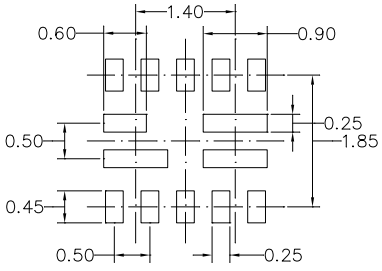
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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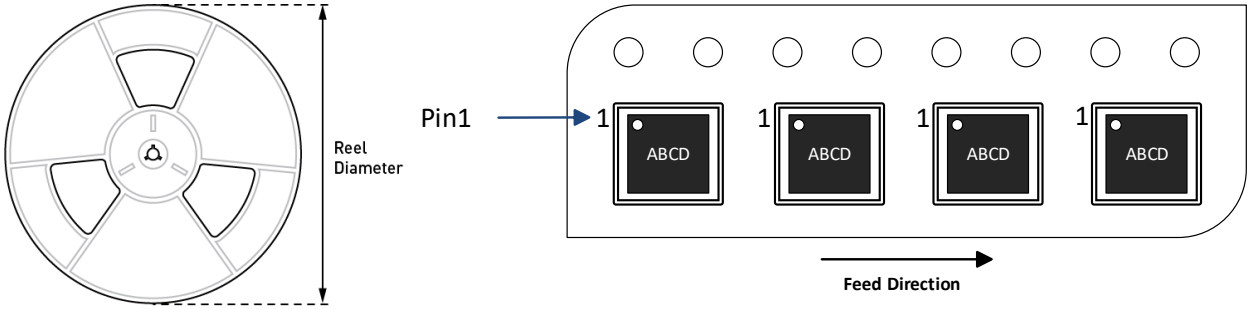
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3824CGPA-Z	ECLGA-14 (2.5mmx2.5mm)	2500	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/11/2022	Initial Release	-

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