

MOSFET – P-Channel, POWERTRENCH®

-30 V, -18 A, 20 mΩ

FDMS4435BZ

General Description

This P-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- Max $r_{DS(on)}$ = 20 mΩ at $V_{GS} = -10$ V, $I_D = -9.0$ A
- Max $r_{DS(on)}$ = 37 mΩ at $V_{GS} = -4.5$ V, $I_D = -6.5$ A
- Extended VGSS range (-25 V) for battery applications
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- HBM ESD Protection Level >7 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- High Side in DC-DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

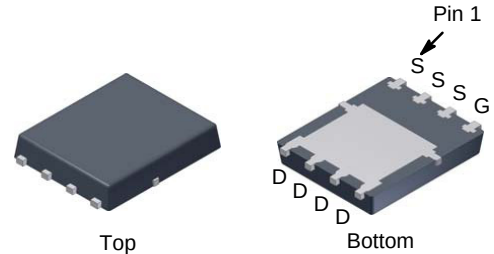
Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current - Continuous (Package Limited) $T_C = 25^\circ\text{C}$ - Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$ - Continuous $T_A = 25^\circ\text{C}$ (Note 1a) - Pulsed	-18 -35 -9.0 -50	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	18	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	39 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

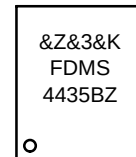
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
-30 V	20 mΩ @ -10 V	-18 A
	37 mΩ @ -4.5 V	



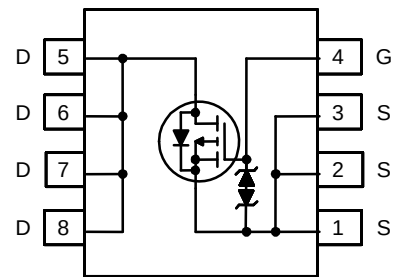
PQFN8 5X6, 1.27P
(Power 56)
CASE 483AE

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digits Lot Run Code
FDMS4435BZ = Specific Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	-30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C	-	-23	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	-1.0	-1.9	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C	-	6	-	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}$, $I_D = -9.0\ \text{A}$	-	15	20	m Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -6.5\ \text{A}$	-	22	37	
		$V_{GS} = -10\ \text{V}$, $I_D = -9.0\ \text{A}$ $T_J = 125^\circ\text{C}$	-	21	28	
g_{FS}	Forward Transconductance	$V_{DS} = -5\ \text{V}$, $I_D = -9.0\ \text{A}$	-	25	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	-	1540	2050	pF
C_{oss}	Output Capacitance		-	290	390	pF
C_{rss}	Reverse Transfer Capacitance		-	260	385	pF
R_g	Gate Resistance		-	5	-	Ω

SWITCHING CHARACTERISTICS

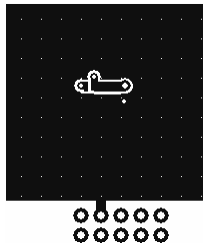
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\ \text{V}$, $I_D = -9.0\ \text{A}$, $V_{GS} = -10\ \text{V}$, $R_{GEN} = 6\ \Omega$	-	9	17	ns
t_r	Rise Time		-	10	18	ns
$t_{d(off)}$	Turn-Off Delay Time		-	35	56	ns
t_f	Fall Time		-	19	33	ns
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-10\ \text{V}$, $V_{DD} = -15\ \text{V}$, $I_D = -9.0\ \text{A}$	-	34	47	nC
Q_g	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-4.5\ \text{V}$, $V_{DD} = -15\ \text{V}$, $I_D = -9.0\ \text{A}$	-	18	25	nC
Q_{gs}	Gate to Source Charge	$V_{GS} = 10\ \text{V}$, $V_{DD} = -15\ \text{V}$, $I_D = -9.0\ \text{A}$	-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	9	-	nC

DRAIN-SOURCE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = -1.9\ \text{A}$ (Note 2)	-	0.75	1.2	V
		$V_{GS} = 0\ \text{V}$, $I_S = -9.0\ \text{A}$ (Note 2)	-	0.86	1.5	
t_{rr}	Reverse Recovery Time	$I_F = -9.0\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	-	25	39	ns
Q_{rr}	Reverse Recovery Charge		-	12	21	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
 3. E_{AS} of 18 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 1\ \text{mH}$, $I_{AS} = -6\ \text{A}$, $V_{DD} = -27\ \text{V}$, $V_{GS} = -10\ \text{V}$. 100% tested at $L = 0.3\ \text{mH}$, $I_{AS} = -8\ \text{A}$.
 4. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

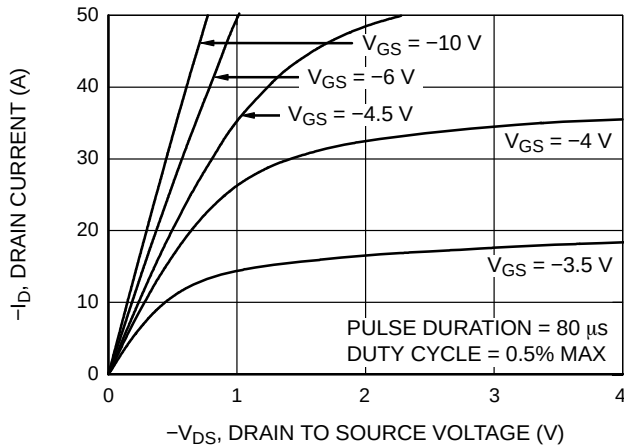


Figure 1. On-Region Characteristics

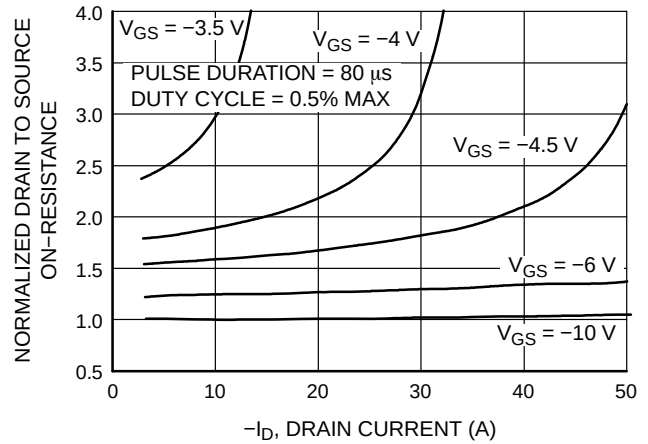


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

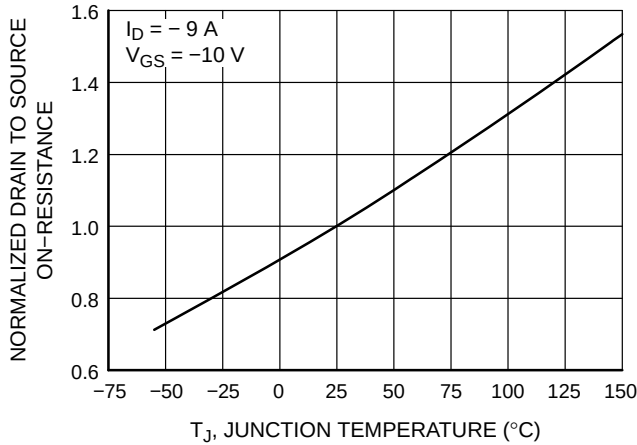


Figure 3. Normalized On-Resistance vs. Junction Temperature

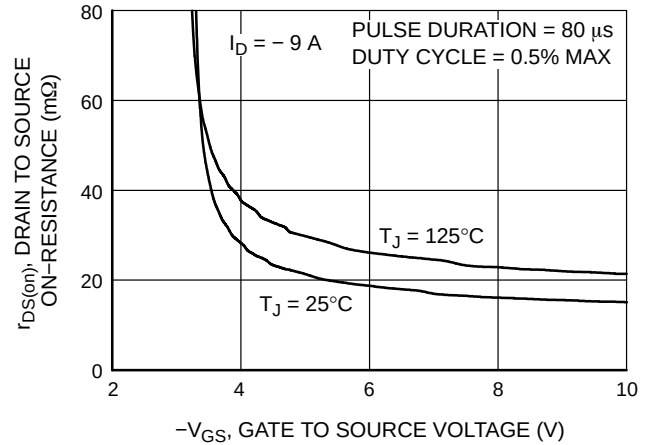


Figure 4. On-Resistance vs. Gate to Source Voltage

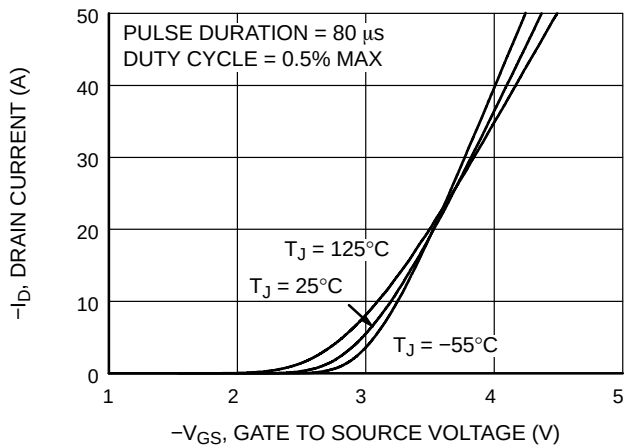


Figure 5. Transfer Characteristics

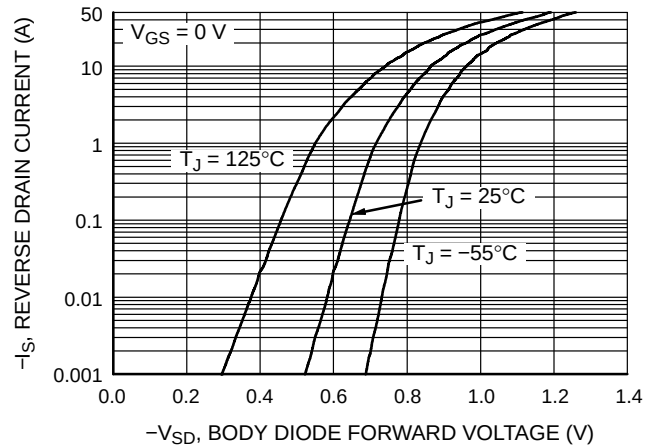


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

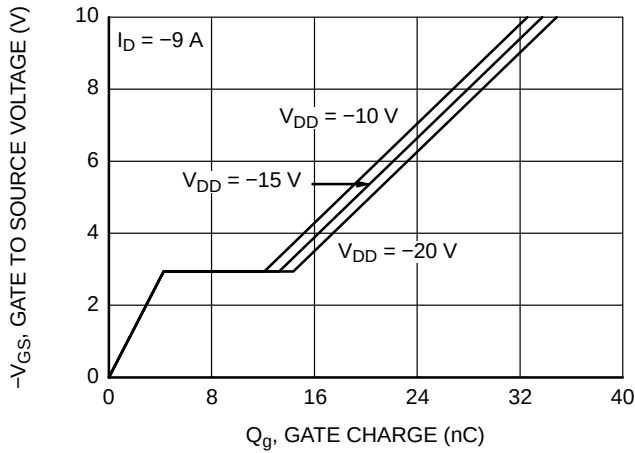


Figure 7. Gate Charge Characteristics

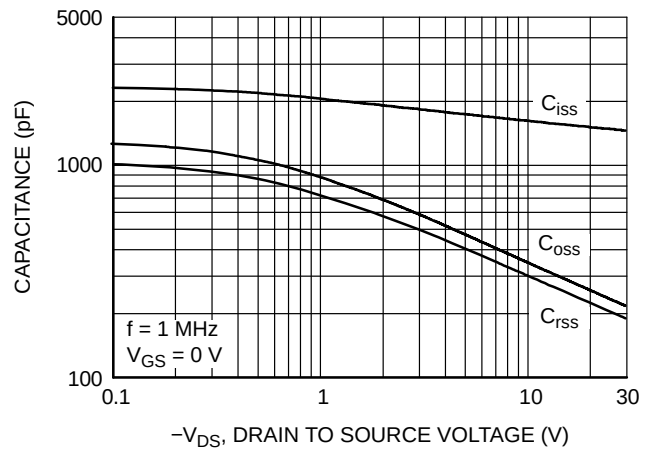


Figure 8. Capacitance vs. Drain to Source Voltage

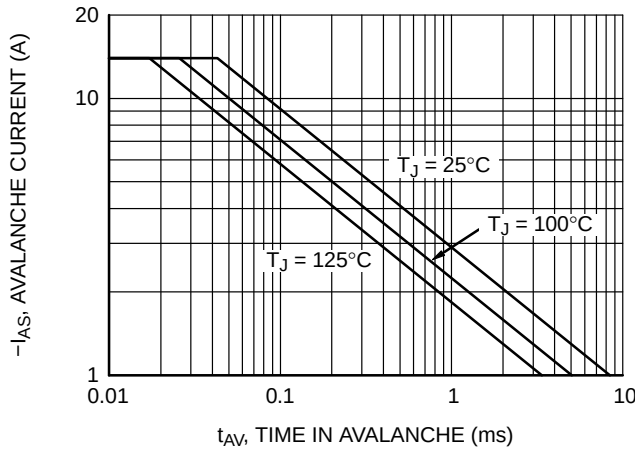


Figure 9. Unclamped Inductive Switching Capability

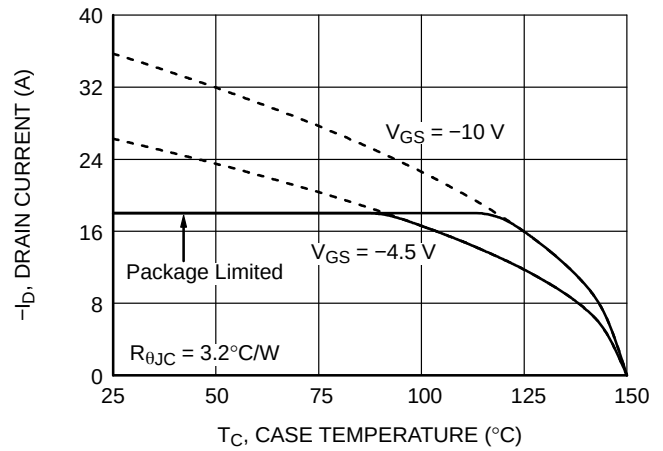


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

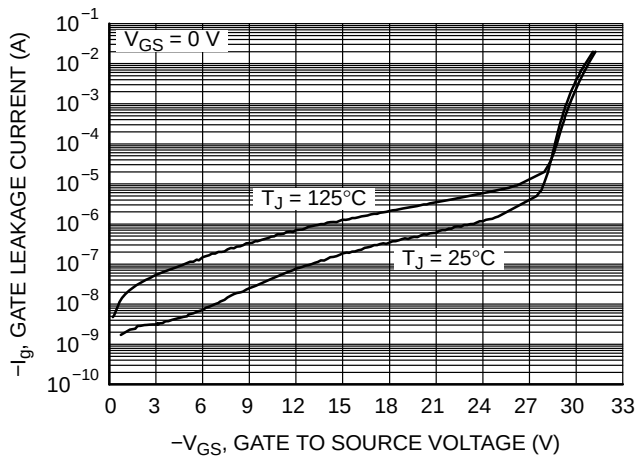


Figure 11. Gate Leakage Current vs. Gate to Source Voltage

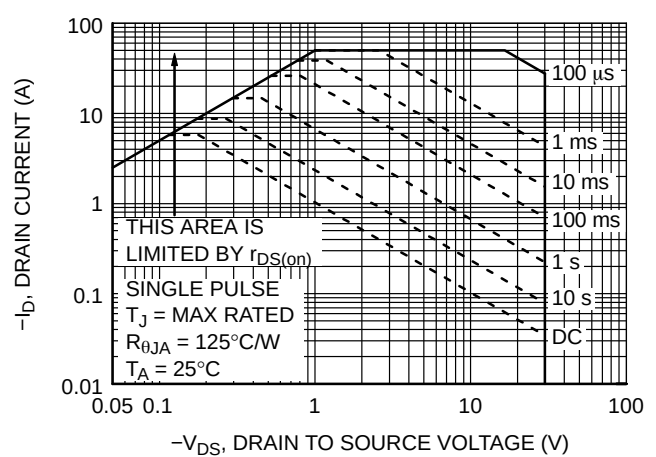


Figure 12. Forward Bias Safe Operating Area

FDMS4435BZ

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

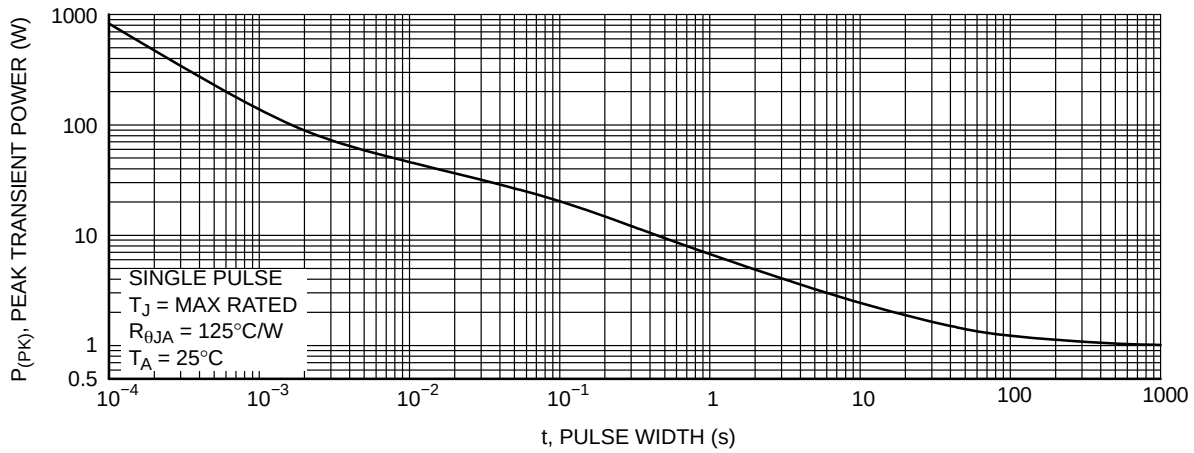


Figure 13. Single Pulse Maximum Power Dissipation

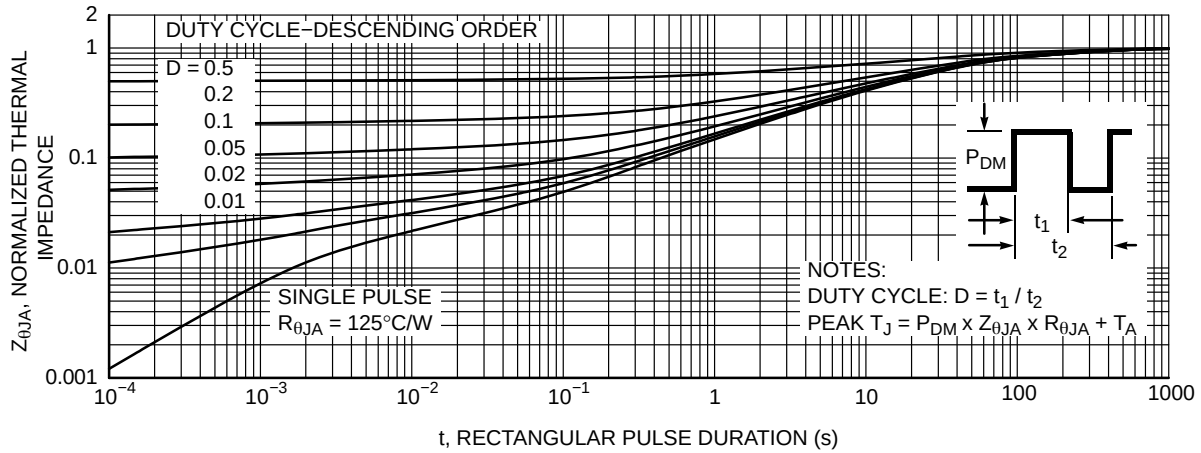
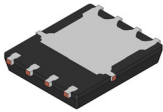


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

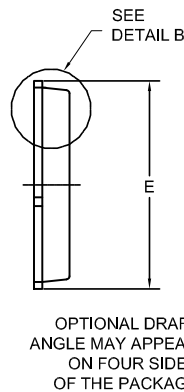
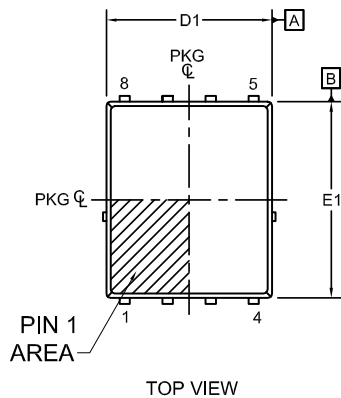
Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDMS4435BZ	FDMS4435BZ	PQFN8 5X6, 1.27P (Power 56) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



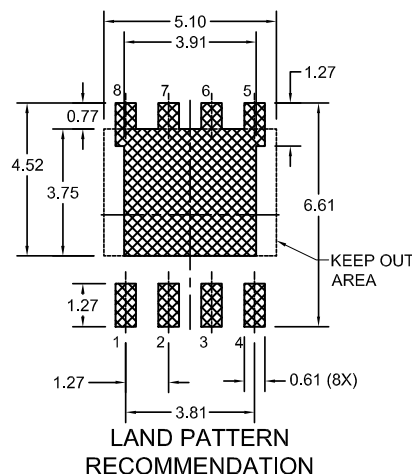
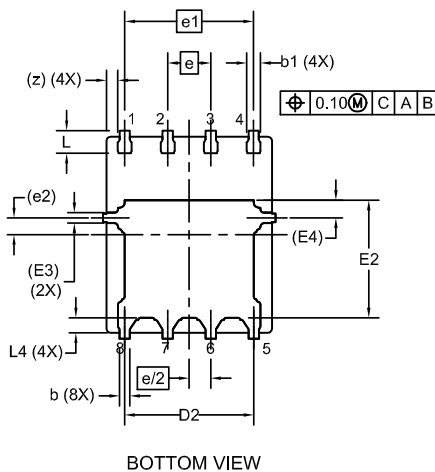
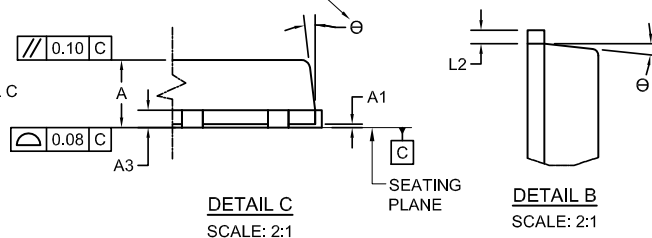
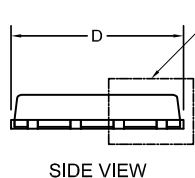
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

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