MDC97476/7/8

1 MSPS, 72dB SNR, 12-/10-/8-Bit ADCs in 6-Lead TSOT-23

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MDC97476/7/8 are 12-bit, 10-bit, and 8-bit, respectively, high speed, low power, successive approximation analog-to-digital converters (ADCs). The parts operate from a single 3 V to 3.6 V power supply with a conversion rate up to 1 MSPS.

The MDC97476/7/8 use a three–wire SPI compatible serial digital interface for chip control and data output. The sampling rate is determined by the serial clock, and the conversion process and data acquisition are controlled by a chip select pin.

The MDC97476/7/8 use the power supply as their reference, and power consumption is as low as 4.9mW at 1 MSPS conversion rate with a 3.3 V power supply. The parts are available in a 6-pin TSOT-23 package, with an operating temperature range of –40°C to +85°C.

FEATURES

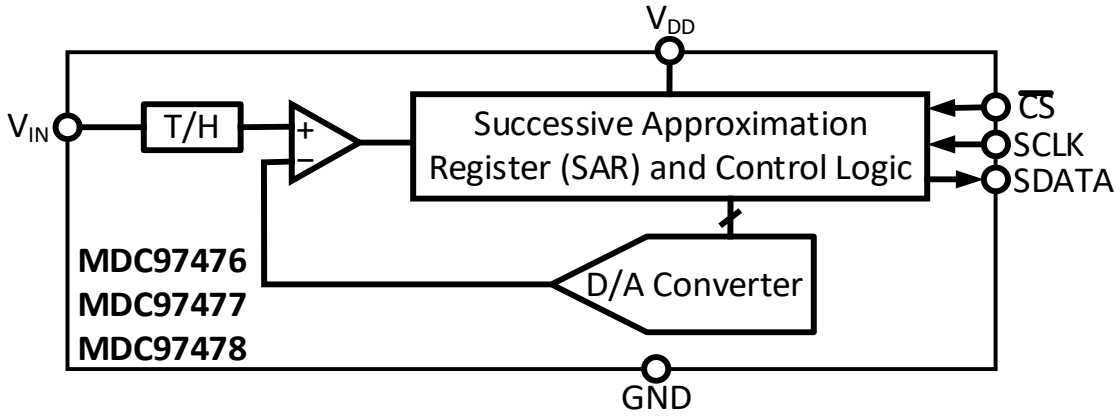
- 12-/10-/8-Bit SAR analog-to-digital converter
- Conversion rate up to 1 MSPS
- Single 3.0 V to 3.6 V Power Supply
- Low power: 4.9 mW at 1 MSPS with 3.3 V supplies
- 72 dB SNR at 120 kHz input frequency (MDC97476)
- Reference derived from power supply
- SPI-compatible serial interface
- 6-pin TSOT-23 package

APPLICATIONS

- Battery-powered systems
- Medical instruments
- Instrumentation and control systems
- Portable Systems
- Data acquisition systems
- Mobile Communications

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

BLOCK DIAGRAM



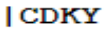
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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MDC97476GJ	TSOT-23-6	CDKY	1
MDC97477GJ		CDLY	
MDC97478GJ		CDMY	

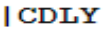
* For Tape & Reel, add suffix -Z (e.g. MDC97476GJ-Z);

TOP MARKING



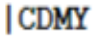
CDK: Product code of MDC97476
Y: Year code

TOP MARKING



CDL: Product code of MDC97477
Y: Year code

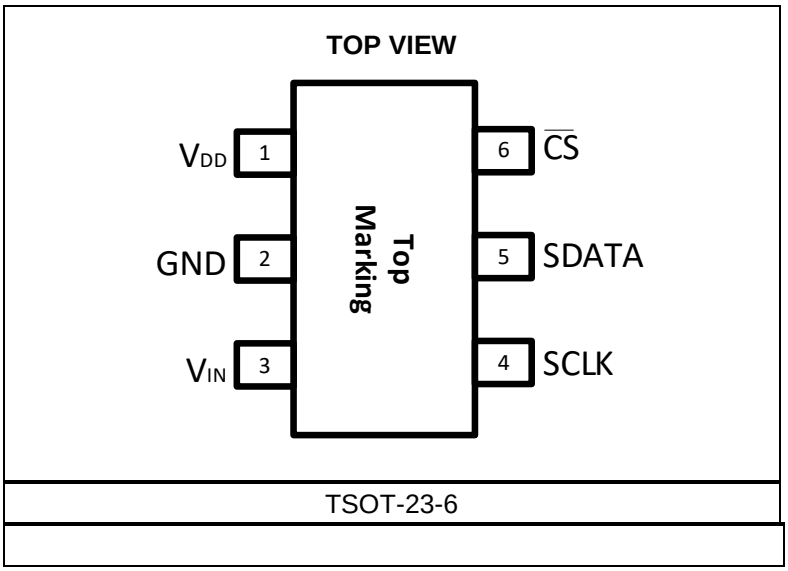
TOP MARKING



CDM: Product code of MDC97478
Y: Year code

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PACKAGE REFERENCE



TSOT-23-6

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	V_{DD}	Power	Positive power supply pin. Voltage range 3 V to 3.6 V
2	GND	Ground	Ground pin
3	V_{IN}	Input	Analog input pin, range is from 0 V to V_{DD}
4	SCLK	Input	Digital clock input
5	SDATA	Output	Digital data output, clocked out at falling edge of SCLK
6	$\overline{CS}$	Input	Chip Select, falling edge of $\overline{CS}$ starts the conversion

ABSOLUTE MAXIMUM RATINGS (1)

V_{DD} to GND .....-0.3 V to +4 V
V_{IN} to GND.....-0.3 V to V_{DD}+0.3 V
SCLK to GND .....-0.3 V to V_{DD}+0.3 V
$\overline{CS}$ to GND .....-0.3 V to V_{DD}+0.3 V
SDATA to GND .....-0.3 V to V_{DD}+0.3 V
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....3.5k V
Charged device model (CDM) .....250 V

Recommended Operating Conditions (2)

V_{DD} .....+3 V to +3.6 V
Digital input pins ..... 0V to 5 V
Operating Temp. (T_A).....-40°C to +85°C

Thermal Resistance (3) θ_{JA} θ_{JC}

TSOT-23-6 ..... 143 ..... 76 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS - MDC97476

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dynamic Characteristics						
Signal to Noise Ratio	SNR	f_{IN} = 120 kHz	71	72.2		dBFS
Signal to (Noise & Distortion) Ratio	SINAD	f_{IN} = 120 kHz	68	71.9		dBFS
Total Harmonic Distortion	THD	f_{IN} = 120 kHz		-84	-78	dB
Spurious Free Dynamic Range	SFDR	f_{IN} = 120 kHz	81	87		dB
Static Characteristics						
Integral Nonlinearity	INL		-1.2	±0.5	1.2	LSB
Differential Nonlinearity	DNL		-1	±0.4	1	LSB
Gain Error (4)	GE			±0.7		LSB
Offset Error (4)	V_{OFF}			±3.2		LSB
Analog Input						
Input voltage range	V_{IN}			0 to V_{DD}		V
DC leakage current	I_L				1	µA
Input capacitance (5)	C_{IN_A}			14		pF
Digital Input						
Input high voltage	V_{INH}			1.9		V
Input Low Voltage	V_{INL}			1.3		V
Input current	I_{IN}				1	µA
Input capacitance (5)	C_{IN_D}			2		pF
Digital Output						
Output high voltage	V_{OH}	I_{LOAD} = 1mA		3.2		V
Output Low Voltage	V_{OL}	I_{LOAD} = 1mA		0.1		V
Floating output capacitance (5)	C_{OUT}			2		pF
Floating output current (5)	I_{OL}				10	µA
POWER SUPPLY CHARACTERISTICS						
Power supply voltage	V_{DD}		3	3.3	3.6	V
Static normal mode current	I_{DDS}			0.9		mA
Operation normal mode current	I_{DDOP}			1.5		mA
Sleep mode current	I_{SD}	SCLK off		25		µA
	I_{SD}	SCLK on		200		µA
Operational normal mode power consumption	P_{OP}			4.9		mW
Sleep power consumption	P_{SD}	SCLK off		83		µW
		SCLK on		660		µW
AC ELECTRICAL CHARACTERISTICS						
Clock frequency	f_{SCLK}				20	MHz

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ELECTRICAL CHARACTERISTICS - MDC97476 *(continued)*

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK duty cycle				50%		
Throughput rate	f_{SAMPLE}				1	MHz

Notes:

4) The Offset Error/Gain Error are based on the relationship of the ADC output code and ADC input voltage (Vin). Please refer to “ADC CONVERSION RESULT” on page 17.

5) Values confirmed by engineering characterization

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ELECTRICAL CHARACTERISTICS - MDC97477

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dynamic Characteristics						
Signal to Noise Ratio	SNR	f_{IN} = 120 kHz		61.76		dBFS
Signal to (Noise & Distortion) Ratio	SINAD	f_{IN} = 120 kHz		61.71		dBFS
Total Harmonic Distortion	THD	f_{IN} = 120 kHz		-80		dB
Spurious Free Dynamic Range	SFDR	f_{IN} = 120 kHz		82.5		dB
Static Characteristics						
Integral Nonlinearity	INL			±0.15		LSB
Differential Nonlinearity	DNL			±0.14		LSB
Gain Error[4]	GE			±0.03		LSB
Offset Error[4]	V_{OFF}			±0.76		LSB
Analog Input						
Input voltage range	V_{IN}			0 to V_{DD}		V
DC leakage current	I_L				1	µA
Input capacitance[5]	C_{IN_A}			14		pF
Digital Input						
Input high voltage	V_{INH}			1.9		V
Input Low Voltage	V_{INL}			1.3		V
Input current	I_{IN}				1	µA
Input capacitance[5]	C_{IN_D}			2		pF
Digital Output						
Output high voltage	V_{OH}	I_{LOAD} = 1mA		3.2		V
Output Low Voltage	V_{OL}	I_{LOAD} = 1mA		0.1		V
Floating output capacitance[5]	C_{OUT}			2		pF
Floating output current[5]	I_{OL}				10	µA
POWER SUPPLY CHARACTERISTICS						
Power supply voltage	V_{DD}			3.3		V
Static normal mode current	I_{DDS}			0.9		mA
Operation normal mode current	I_{DDOP}			1.5		mA
Sleep mode current	I_{SD}	SCLK off		25		µA
	I_{SD}	SCLK on		200		µA
Operational normal mode power consumption	P_{OP}			4.9		mW
Sleep power consumption	P_{SD}	SCLK off		83		µW
		SCLK on		660		µW
AC ELECTRICAL CHARACTERISTICS						
Clock frequency	f_{SCLK}				20	MHz

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ELECTRICAL CHARACTERISTICS - MDC97477 *(continued)*

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK duty cycle				50%		
Throughput rate	f_{SAMPLE}				1	MHz

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ELECTRICAL CHARACTERISTICS - MDC97478

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dynamic Characteristics						
Signal to Noise Ratio	SNR	f_{IN} = 120 kHz		49.97		dBFS
Signal to (Noise & Distortion) Ratio	SINAD	f_{IN} = 120 kHz		49.95		dBFS
Total Harmonic Distortion	THD	f_{IN} = 120 kHz		-71		dB
Spurious Free Dynamic Range	SFDR	f_{IN} = 120 kHz		67		dB
Static Characteristics						
Integral Nonlinearity	INL			±0.04		LSB
Differential Nonlinearity	DNL			±0.03		LSB
Gain Error[4]	GE			±0.01		LSB
Offset Error[4]	V_{OFF}			±0.14		LSB
Analog Input						
Input voltage range	V_{IN}			0 to V_{DD}		V
DC leakage current	I_L				1	µA
Input capacitance[5]	C_{IN_A}			14		pF
Digital Input						
Input high voltage	V_{INH}			1.9		V
Input Low Voltage	V_{INL}			1.3		V
Input current	I_{IN}				1	µA
Input capacitance[5]	C_{IN_D}			2		pF
Digital Output						
Output high voltage	V_{OH}	I_{LOAD} = 1mA		3.2		V
Output Low Voltage	V_{OL}	I_{LOAD} = 1mA		0.1		V
Floating output capacitance[5]	C_{OUT}			2		pF
Floating output current[5]	I_{OL}				10	µA
POWER SUPPLY CHARACTERISTICS						
Power supply voltage	V_{DD}			3.3		V
Static normal mode current	I_{DDS}			0.9		mA
Operation normal mode current	I_{DDOP}			1.5		mA
Sleep mode current	I_{SD}	SCLK off		25		µA
	I_{SD}	SCLK on		200		µA
Operational normal mode power consumption	P_{OP}			4.9		mW
Sleep power consumption	P_{SD}	SCLK off		83		µW
		SCLK on		660		µW
AC ELECTRICAL CHARACTERISTICS						
Clock frequency	f_{SCLK}				20	MHz
SCLK duty cycle				50%		

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ELECTRICAL CHARACTERISTICS - MDC97478 *(continued)*

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Throughput rate	f_{SAMPLE}				1	MHz

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TIMING CHARACTERISTICS[6, 7, 8]

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCLK Period	t_{SCLK}		50			ns
Conversion time	t_{on}			16 × t_{SCLK}		ns
Quiet time	t_{quiet}		50			ns
Minimum $\overline{CS}$ pulse width	t_1		10			ns
$\overline{CS}$ to SCLK setup time	t_2		10			ns
Delay from $\overline{CS}$ until SDATA TRI-STATE disabled	t_3				20	ns
Data access time after SCLK falling edge	t_4				40	ns
SCLK low pulse width	t_5		0.4 × t_{SCLK}			ns
SCLK high pulse width	t_6		0.4 × t_{SCLK}			ns
SCLK to data valid hold time	t_7		5			ns
SCLK falling edge to SDATA high impedance	t_8		5			ns
Wake-up time from sleep mode	t_{wakeup}			50		µs
Power up wait time	t_{puwait}		200			µs
Wait time before normal operation after power up	$t_{clkwait}$			200 × t_{SCLK}		ns

[6]For t_{SCLK}, t_{on}, t_{quiet}, and t_1-t_8, refer to figure 2.

[7]For t_{puwait} and $t_{clkwait}$, refer to figure 12.

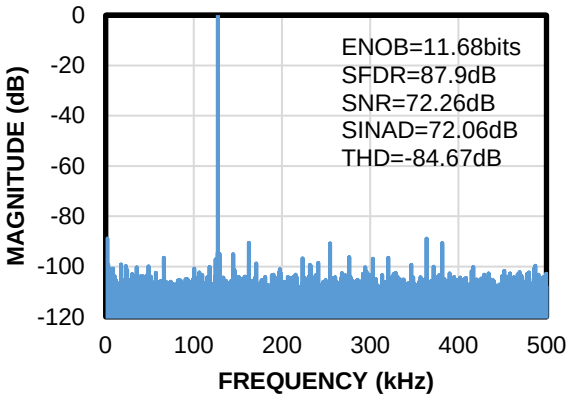
[8]Timing characteristics guaranteed by engineering characterization

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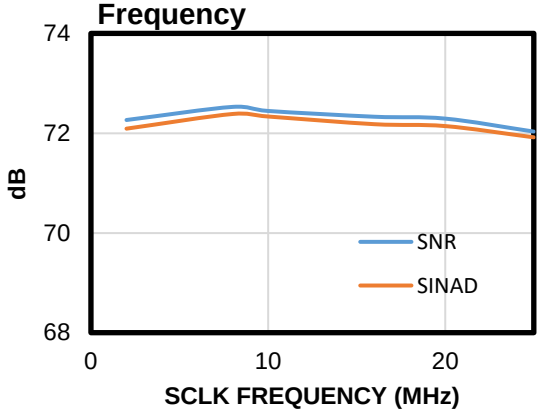
TYPICAL CHARACTERISTICS – MDC97476/7/8

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, f_{IN} = 120kHz, T_A = 25°C, unless otherwise noted.

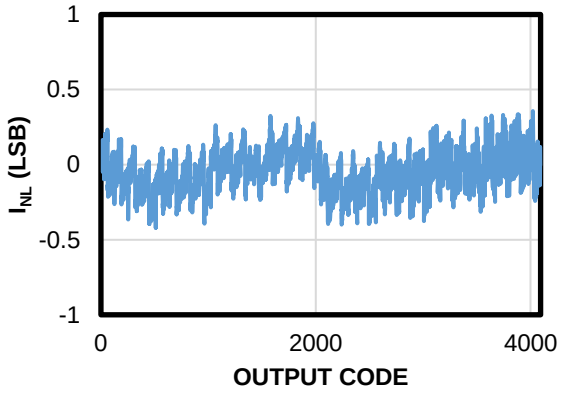
MDC97476 Dynamic Performance at 1Msps



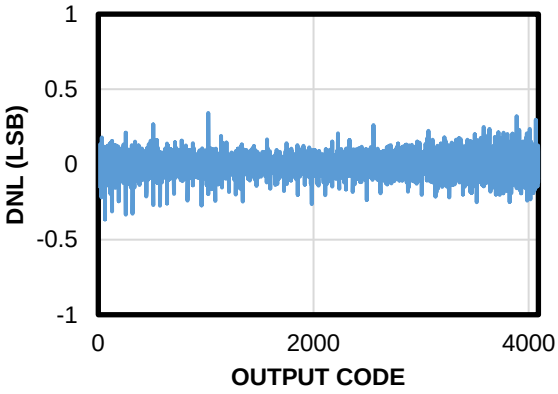
MDC97476 Dynamic Performance vs. SCLK Frequency



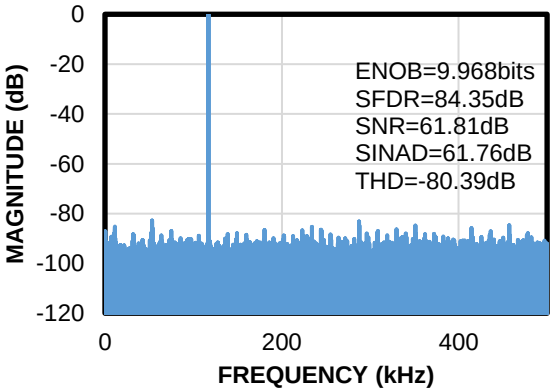
MDC97476 INL



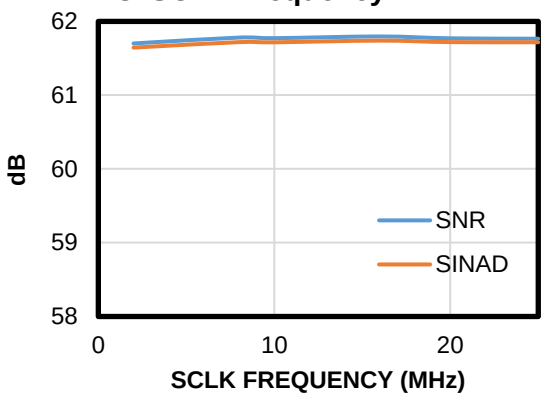
MDC97476 DNL



MDC97477 Dynamic Performance at 1Msps



MDC97477 Dynamic Performance vs. SCLK Frequency

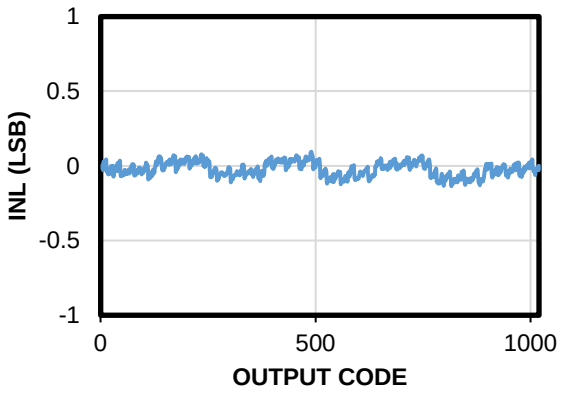


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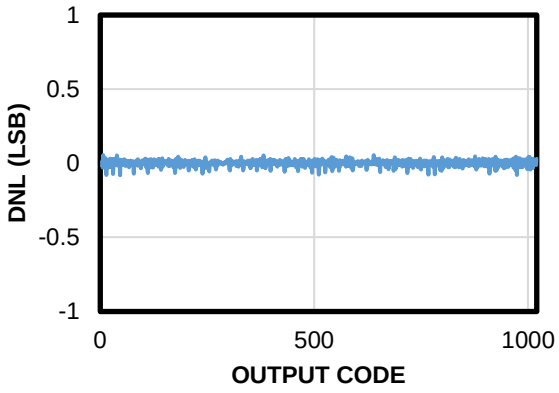
TYPICAL CHARACTERISTICS – MDC97476/7/8

V_{DD} = 3.3 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, f_{IN} = 120khz, T_A = 25°C, unless otherwise noted.

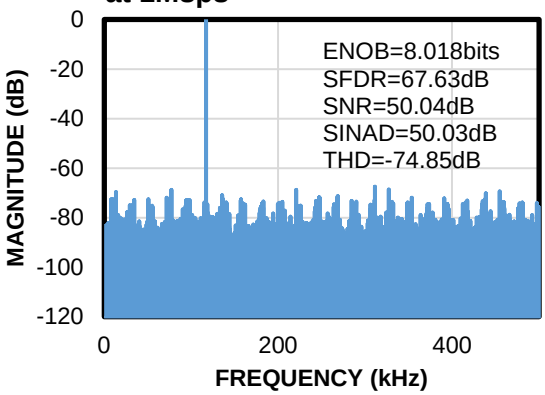
MDC97477 INL



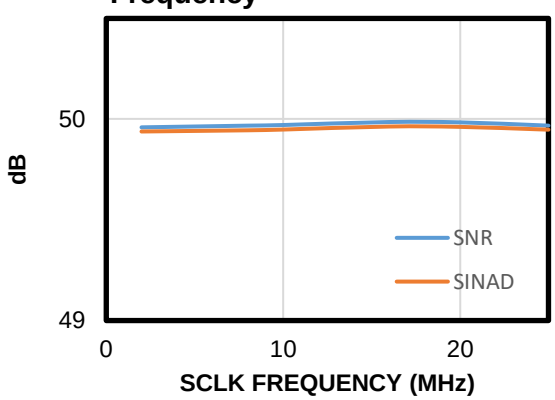
MDC97477 DNL



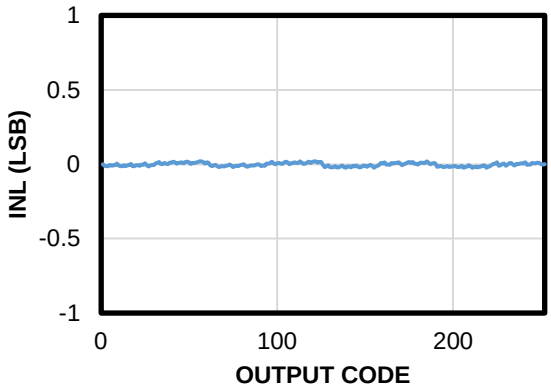
MDC97478 Dynamic Performance at 1Msps



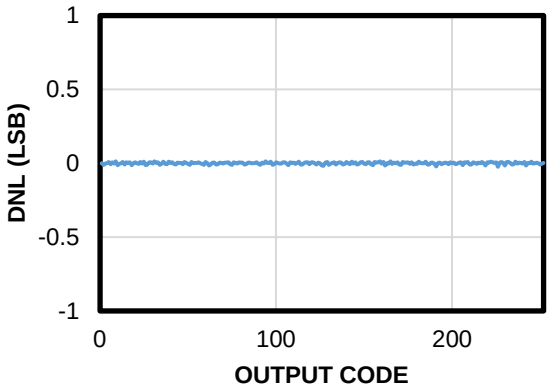
MDC97478 Dynamic Performance vs. SCLK Frequency



MDC97478 INL



MDC97478 DNL



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FUNCTIONAL BLOCK DIAGRAM

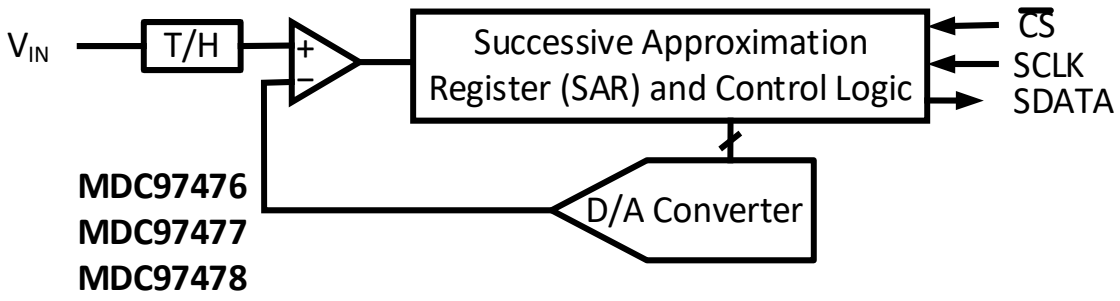


Figure 1: Functional Block Diagram

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OPERATION

The MDC97476/7/8 are, respectively, 12-bit, 10-bit, and 8-bit, fast, micropower, single-supply, successive-approximation analog-to-digital converters (ADCs). Operating from a single 3.3V supply, the MDC97476/7/8 are capable of throughput rates of 1 MSPS with a 20 MHz input clock.

Each MDC97476/7/8 provides an on-chip, track-and-hold ADC and a serial interface in a tiny 6-lead TSOT-23 package. The serial clock input accesses data from the part and provides the clock source for the SAR. The analog input range is 0 V to V_{DD}. There is no on-chip reference, and no external reference is required for the ADC. The reference for the MDC97476/7/8 is derived from the power supply and thus provides the widest dynamic input range.

As shown in Figure 1, there are 4 I/O pins. V_{IN} is the analog input signal pin. $\overline{CS}$ is chip select, which is used to start the conversion process. SCLK is the input clock, which controls the timing of serial data interface. SDATA is the serial data output pin, which outputs the conversion result.

The falling edge of $\overline{CS}$ initiates the end of the signal tracking phase and the start of the conversion process. Meanwhile, SDATA will transition from tri-state to logic low.

At the 13th rising edge of SCLK after $\overline{CS}$ goes low, the ADC transitions from hold phase to track phase. The SDATA pin goes into tri-state mode either at the 16th falling edge of SCLK after $\overline{CS}$ goes low, or at the rising edge of $\overline{CS}$. After SDATA outputs all data and goes back to tri-state, the ADC must wait at least the quiet time t_{QUIET} before starting a new conversion, i.e., the next falling edge of $\overline{CS}$ must be later than quiet time t_{QUIET} (see Figure 2).

To read a complete sample from the MDC97476/7/8, $\overline{CS}$ must remain low for at least 16 SCLK cycles. SDATA is clocked out on the falling edges of SCLK. SDATA outputs 4 leading zeroes first, followed by 12 (MDC97476), 10 (MDC97477), or 8 (MDC97478) data bits (order: MSB first). After the data bits, MDC97476 SDATA goes into tri-state mode; MDC97477 SDATA clocks out 2 trailing zeros and then goes into tri-state mode; MDC97478 SDATA clocks out 4 trailing zeros and then goes into tri-state mode. Please note that the $\overline{CS}$ falling edge should only occur when SCLK is high. The detailed timing diagrams are shown in Figures 2, 3, and 4.

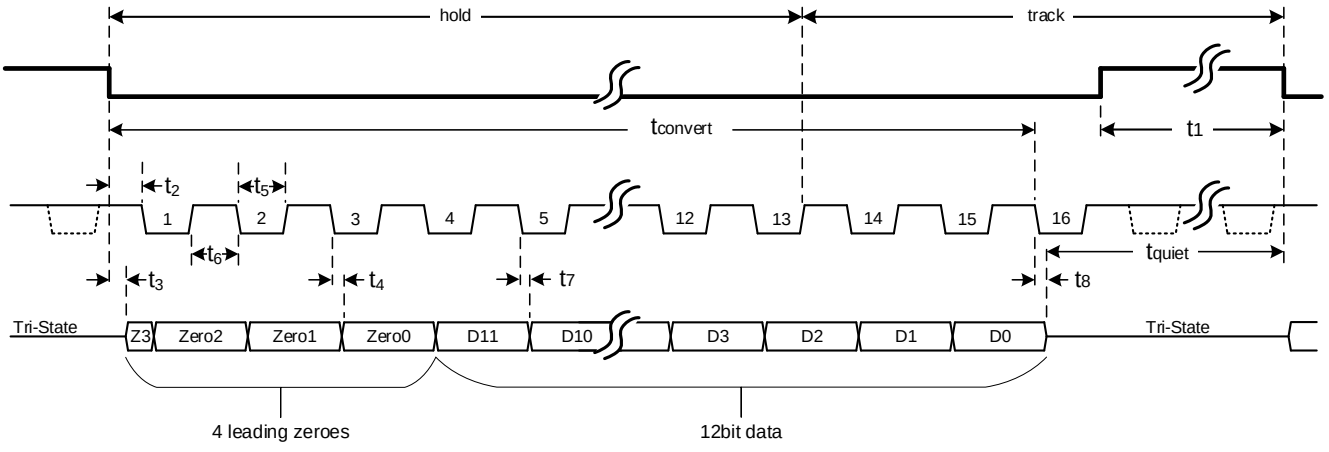


Figure 2: MDC97476 Serial Interface Timing Diagram

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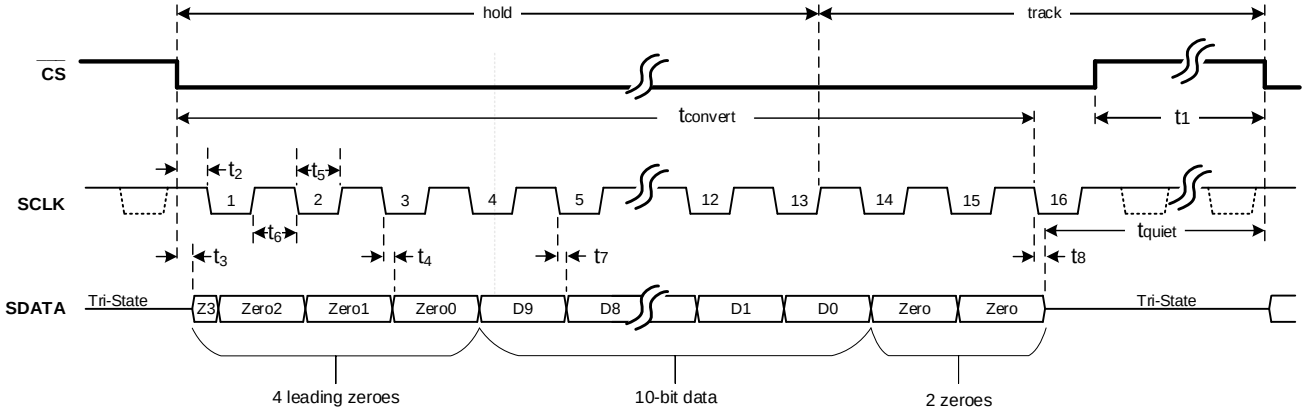


Figure 3: MDC97477 Serial Interface Timing Diagram

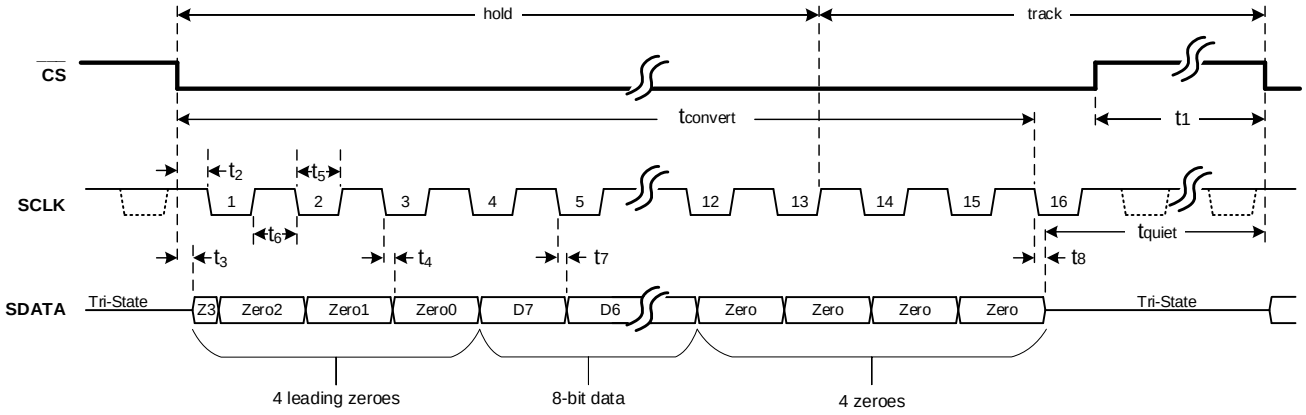


Figure 4: MDC97478 Serial Interface Timing Diagram

Device Functional Stages

The MDC97476/7/8 are fast, micropower, single-supply, successive-approximation ADCs with charge redistribution DACs. Figures 5 and 6 are simplified schematics of the ADC in track and hold phases.

Figure 5 shows the device in hold phase: SW2 is open, and the sampling capacitor is connected to ground via SW1, maintaining the sampled voltage at the comparator input. The control logic then controls the capacitive DAC to add or subtract charge from the sampling capacitor until the comparator is balanced.

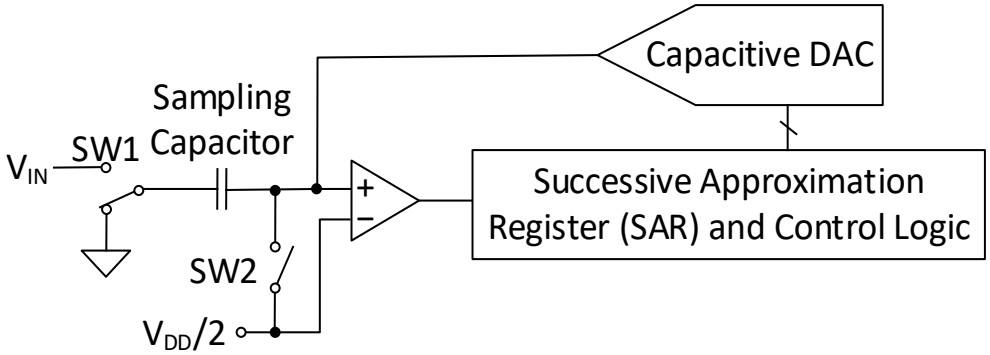


Figure 5: Hold Phase

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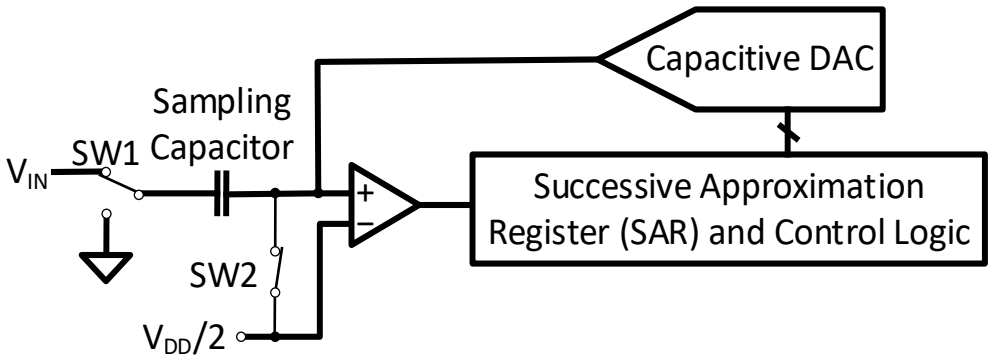


Figure 6: Track Phase

After the comparator is balanced, the control code applied to the DAC is the digital value of the analog input voltage. The device can then move into track phase as shown in Figure 6. In track phase, SW2 is closed, the comparator is balanced, and SW1 connects the sampling capacitor to V_{IN} thus storing the input voltage on the sampling capacitor.

ADC Transfer Function

The output coding of the MDC97476/7/8 is straight binary. Code transitions occur at integer LSB values, such as 1 LSB, 2 LSB, and so on. The LSB size for the MDC97476 is $V_{DD}/4096$; The LSB size for the MDC97477 is $V_{DD}/1024$; The LSB size for the MDC97478 is $V_{DD}/256$. Figure 7 shows an ideal transfer characteristic.

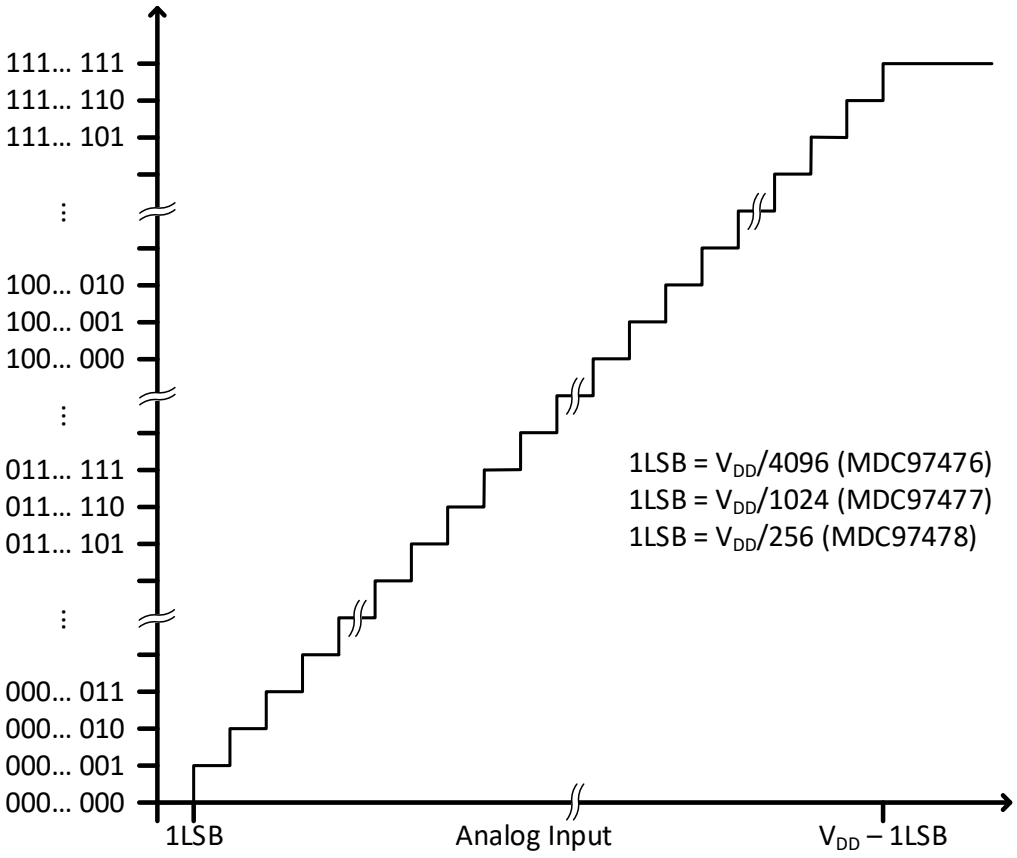


Figure 7: Ideal Transfer Curve

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ADC Conversion Result

The MDC97476/7/8 transfer function slightly varies from the ideal in a predictable fashion. After the conversion completes, the conversion result is sent out as adc_code. The relation between adc_code and ADC input (V_{IN}) is:

$$V_{IN} = \frac{V_{DD}}{4096} * (adc_code + 34 - 89 * \frac{adc_code - 1}{4094})$$

for the MDC97476,

$$V_{IN} = \frac{V_{DD}}{1024} * (adc_code + 9 - 22 * \frac{adc_code - 1}{1022})$$

for the MDC97477, and

$$V_{IN} = \frac{V_{DD}}{256} * (adc_code + 2.2 - 5.5 * \frac{adc_code - 1}{254})$$

for the MDC97478,

Analog input

Figure 8 shows an equivalent circuit for the MDC97476/7/8 input pin (V_{IN}). The analog input voltage must always be kept between GND – 300 mV and V_{DD} + 300 mV. Two diodes, D_{ESD1} and D_{ESD2}, provide ESD protection for the analog input. The capacitor C_{PIN} in Figure 8 represents the input pin capacitance, with a typical value of 2 pF. The resistor R_{ON} represents the lumped ON resistance of the track and hold switch, and has a typical value of 125Ω. The capacitor $C_{SAMPLING}$ represents the ADC sampling capacitor, and has a typical value of 14 pF.

In applications where harmonic distortion and signal-to-noise ratio are critical, MDC97476/7/8 should be driven by a low-impedance source. A band-pass or low-pass filter is helpful to reduce harmonics and noise, improving THD and SNR performance.

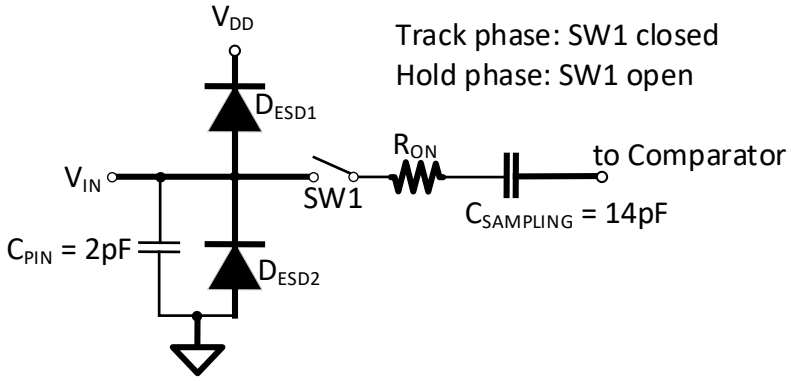


Figure 8: Equivalent Analog Input Circuit.

Digital inputs

ESD protection circuits are also used for the digital inputs and output, so the digital inputs and output share the same voltage limitations as the analog input.

MODES OF OPERATION

By controlling $\overline{CS}$ during conversion, MDC97476/7/8 can go into two possible modes: normal mode and sleep mode. The device enters normal mode when the $\overline{CS}$ signal goes low, and enters sleep mode when $\overline{CS}$ pulled high before the 10th falling edge of SCLK after $\overline{CS}$ is pulled low. Choosing different modes can help to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

The MDC97476/7/8 can obtain the highest throughput performance by staying in normal mode, as there is no wake-up delay.

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If $\overline{CS}$ is brought high after the 10th falling edge and before the 16th falling edge, the device stays in normal mode, but the current conversion is aborted, and SDATA goes into tri-state.

If $\overline{CS}$ remains low for more than 16 SCLK clock cycles, SDATA returns to tri-state at the 16th SCLK falling edge as shown in Figure 9. A new conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

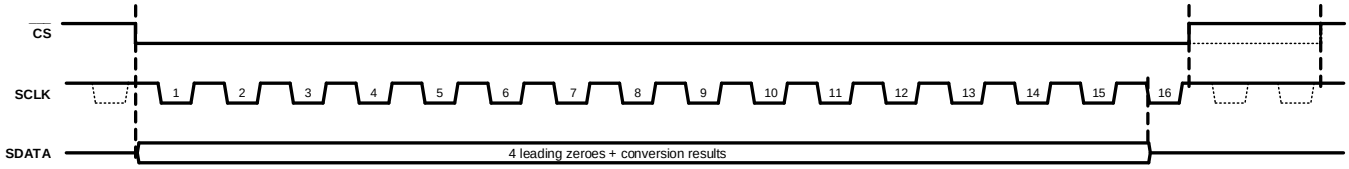


Figure 9: Normal Mode Operation

Sleep Mode

Sleep Mode is intended for saving power consumption in applications that either sample discontinuously, or with a slow throughput rate. When the MDC97476/7/8 is in sleep mode, most of the analog circuitry is turned off.

Figure 10 shows how the device enter sleep mode. When $\overline{CS}$ is brought high after the 2nd falling edge and before the 10th falling edge, the conversion is interrupted, and device enters sleep mode. The current conversion is aborted and SDATA enters tri-state. If $\overline{CS}$ is brought high before the 2nd falling edge of SCLK, the device stays in normal mode; this prevents noise on the $\overline{CS}$ line accidentally changing the mode.

To exit sleep mode, bring $\overline{CS}$ back low. At the falling edge of $\overline{CS}$, the MDC97476/7/8 begins waking up. Wake up typically takes 50 µs. This wake-up delay results in the first 50 conversion results being unusable. The valid result starts from the 51st conversion performed after wake-up begins, as shown in Figure 11.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to sleep mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit sleep mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK.

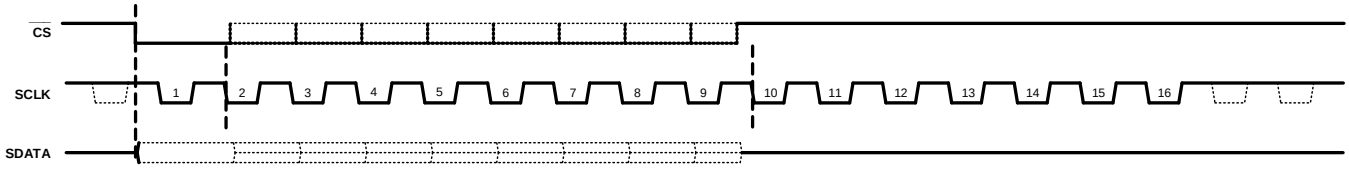


Figure 10: Entering Sleep Mode

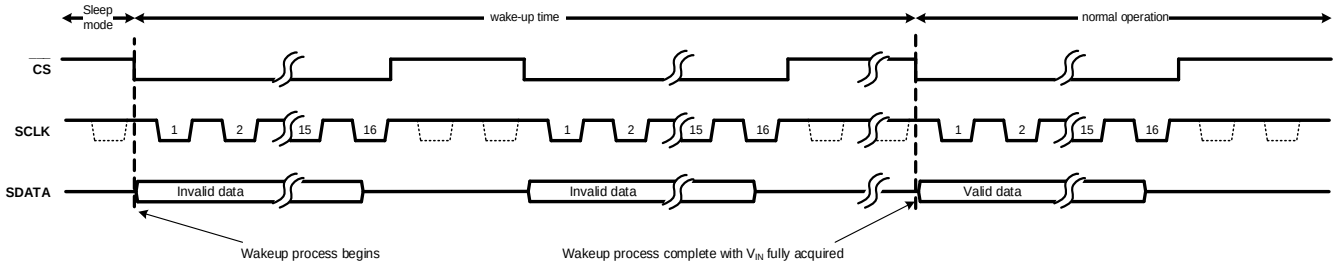


Figure 11: Entering Normal Mode

Power Up Sequence

After V_{DD} is up and stable, at least 200 cycles ($t_{clkwait}$) of stable SCLK after at least 200 µs (t_{puwait}) to MDC97476/7/8 should be provided to allow it to fully power up. This $t_{clkwait}$ period is equivalent to 10 dummy samples operating $\overline{CS}$ and SCLK in normal operation. During this time ($t_{clkwait}$), $\overline{CS}$ can be either high or low. It is recommended to

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keep $\overline{CS}$ high or operate $\overline{CS}$ in the same manner as in normal operation.

Figure 12 shows the detailed power up timing sequence.

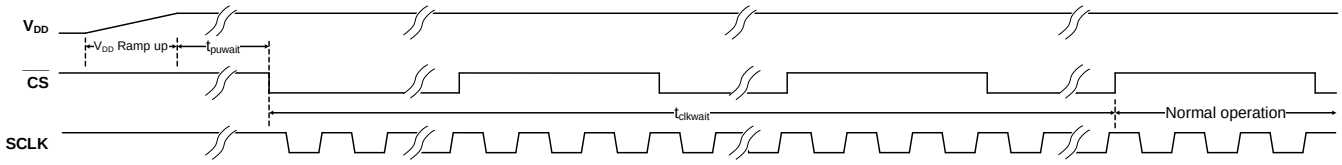


Figure 12: Power Up Sequence

Layout Guidelines

The reference voltage is critical for optimal ADC performance. A noisy reference voltage affects SNR and SINAD performance. Since MDC97476/7/8 uses V_{DD} as its reference voltage, V_{DD} must be treated carefully. A uniform ground plane and a dedicated V_{DD} plane are recommended for the MDC97476/7/8. The decoupling capacitors should be low ESR/ESL and placed next to V_{DD}/GND pins on the same side of the PCB as the chip to provide the best performance.

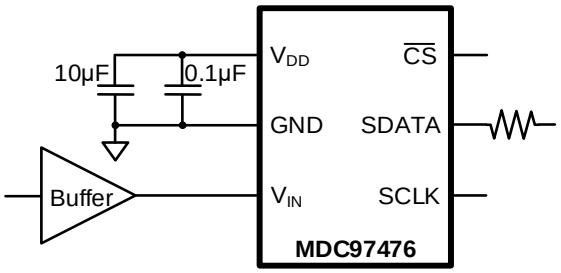
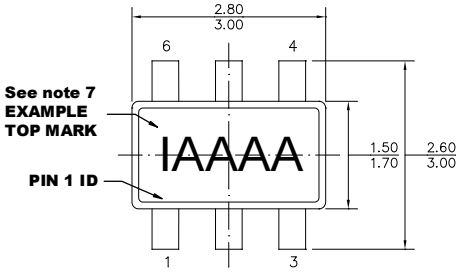


Figure 13: Schematic for typical application

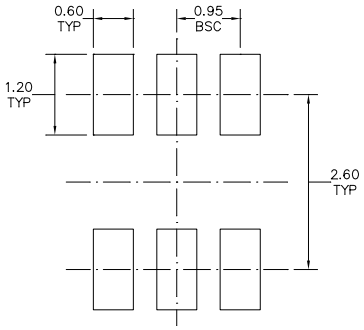
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PACKAGE INFORMATION

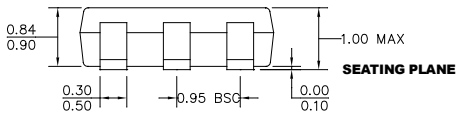
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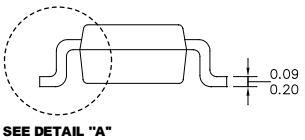
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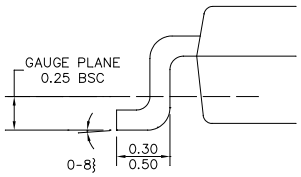
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



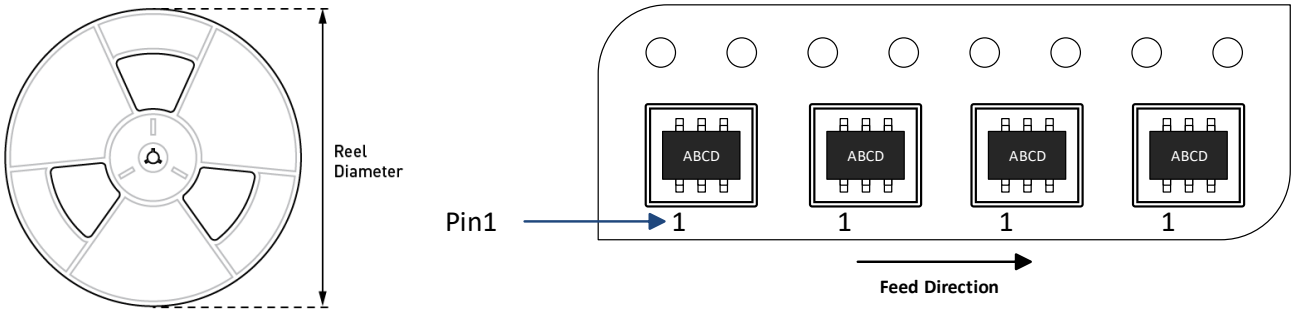
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MDC97476GJ-Z	TSOT-23-6	3000	N/A	N/A	7in.	8mm	4mm
MDC97477GJ-Z							
MDC97478GJ-Z							

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