MP6631H

35V Input, 3A Peak Phase Current, Three-Phase BLDC Motor Driver

DESCRIPTION

The MP6631H is a three-phase brushless DC (BLDC) motor driver with integrated power MOSFETs. The device supports a single external Hall sensor or triple external Hall-effect sensors to drive a three-phase BLDC motor, with up to 3A of peak phase current and an input voltage (V_{IN}) range of 3.6V to 35V.

The MP6631H controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin with closed-/open-loop control. The device features a built-in, configurable speed curve function. It also features a sinusoidal drive for maximum torque, as well as low speed ripple and noise across the full speed range.

The MP6631H provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the Hall comparator's output. Direction control is achieved via the DIR pin's input.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

The MP6631H is available in a QFN-26 (3mmx4mm) package.

FEATURES

- 3.6V to 35V Operating Input Voltage (V_{IN}) Range
- Up to 3A of Peak Phase Current
- Integrated 160mΩ High-Side MOSFETs (HS-FETs) and Low-Side MOSFETs (LS-FETs)
- Sinusoidal Drive
- Supports 0V to 1.2V DC Input or 1kHz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports Triple-Hall or Single-Hall Element Differential Input
- Closed-/Open-Loop Speed Control
- Direction/Brake Input
- Power-Save Mode
- 0.5s/4.5s Lock Protection
- Over-Current Protection (OCP)
- Single-Pulse or Triple-Pulse FG Output per Electrical Cycle
- FG Signal: Rotational Speed Indication
- Soft Start (SS) for Low Noise and Current Overshoot
- Available in a QFN-26 (3mmx4mm) Package

APPLICATIONS

- Fans
- General Three-Phase Brushless DC (BLDC) Motors
- Pumps

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION

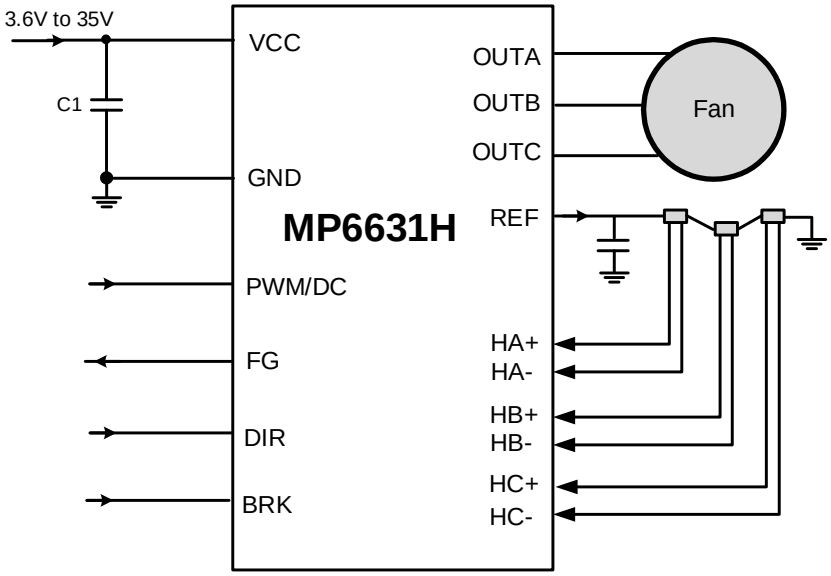


Figure 1: Triple Hall-Effect Sensor Application

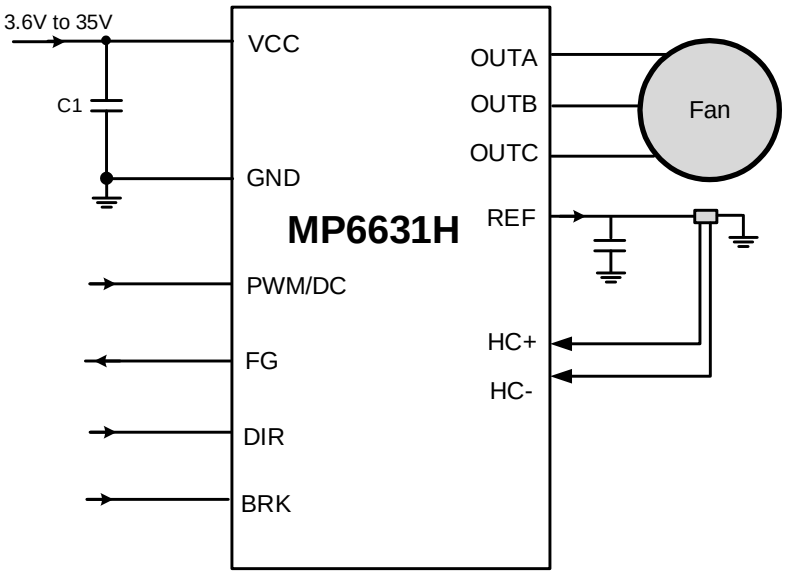


Figure 2: Single Hall-Effect Sensor Application

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Level
MP6631HGL-xxxx**	QFN-26 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6631HGL-xxxx-Z).

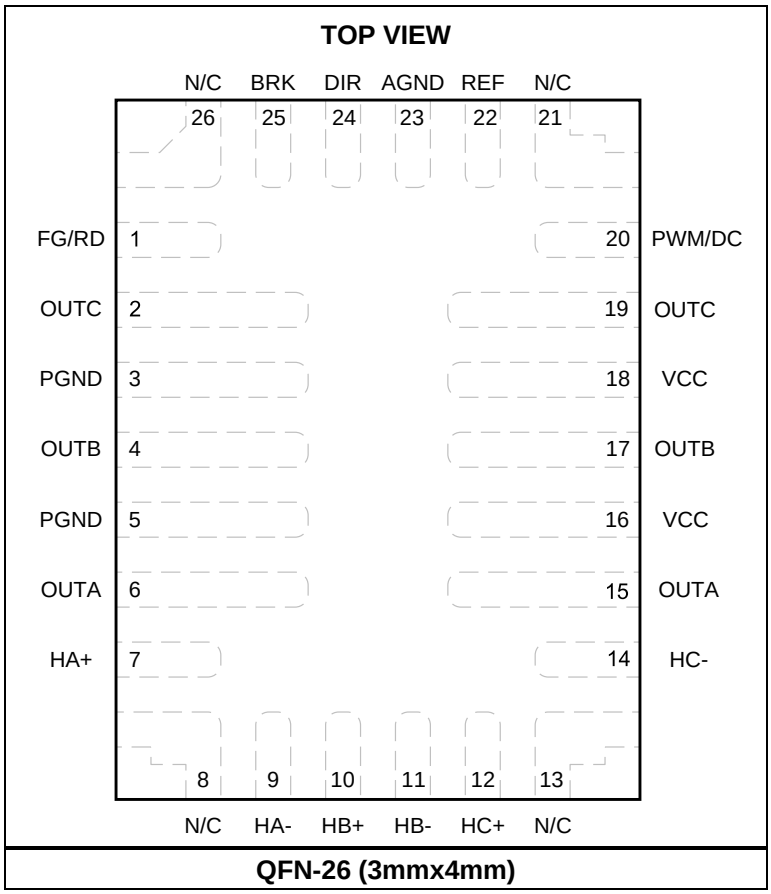
** "-xxxx" is the configuration code identifier. The first four digits of the suffix (-xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for non-default function option. -0000 is the default function value.

TOP MARKING

MPYW
6631
HLLL

MP: MPS prefix
Y: Year code
W: Week code
6631H: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-26 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	FG/RD	**Speed or rotor lock indication.** Open-drain output. FG/RD can be used for speed indication (FG) or rotor lock indication (RD). Pull up this pin externally.
2, 19,	OUTC	**Phase C terminal.**
3, 5	PGND	**Power ground.**
4, 17	OUTB	**Phase B terminal.**
6, 15	OUTA	**Phase A terminal.**
7	HA+	**Phase A positive Hall input terminal.**
9	HA-	**Phase A negative Hall input terminal.**
10	HB+	**Phase B positive Hall input terminal.**
11	HB-	**Phase B negative Hall input terminal.**
12	HC+	**Phase C positive Hall input terminal.**
14	HC-	**Phase C negative Hall input terminal.**
16, 18	VCC	**Input voltage supply pin.** The VCC pin must be locally bypassed.
20	PWM/DC	**Rotational speed control input pin.** Pull the PWM/DC pin high internally with 500kΩ resistance. When DC_PWM = 0, apply a 1kHz to 100kHz pulse-width modulation (PWM) signal for speed control. When DC_PWM = 1, apply a 0V to 1.2V DC voltage for speed control.
22	REF	**5V LDO output.** The REF pin must be locally bypassed.
23	AGND	**Analog ground.**
24	DIR	**Direction control pin.** Pull this pin low for forward rotation (A → B → C); pull it high for reverse rotation (A → C → B). Internally pull down using a resistor.
25	BRK	**Brake pin.** Pull BRK high to brake the motor, pull it low internally using a resistor.
8, 13, 21, 26	NC	

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC} .....-0.3V to +38V
OUTA, OUTB, OUTC.....-0.3V to V_{CC} + 0.3V
All other pins .....-0.3V to +5.8V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)…..
..... 2.6W
Junction temperature .....150°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM) 2kV

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....3.6V to 35V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-26 (3mmx4mm).....48..... 11... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}		3	3.3	3.5	V
Input UVLO hysteresis				360		mV
Operating supply current	I_{CC}			6.7		mA
Standby current	$I_{STANDYBY}$			130		μA
DIR input high voltage	V_{DIR_H}		1.5			V
DIR input low voltage	V_{DIR_L}				0.4	V
BRK input high voltage	V_{BRK_H}		1.5			V
BRK input low voltage	V_{BRK_L}				0.4	V
Pulse-width modulation (PWM) input high voltage	V_{PWM_H}	DC_PWM = 0	1.5			V
PWM input low voltage	V_{PWM_L}	DC_PWM = 0			0.4	V
PWM pull-up resistance	R_{PWM}	DC_PWM = 0		500		kΩ
DC input high voltage	V_{DC_H}	DC_PWM = 1	1.08	1.2	1.32	V
DC input low voltage	V_{DC_L}	DC_PWM = 1		0		V
REF output voltage	V_{REF}			5.24		V
REF load regulation	I_{REF_LO}	I_{REF} = 30mA		5.2		V
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 100mA		85		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 100mA		75		mΩ
Cycle-by-cycle current limit	I_{OCP}	OCP_SEL = 11, T_J = 25°C	2.7	3		A
PWM output frequency	f_{SW}	T_J = 25°C	24.5	25	25.8	kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA		0.2	0.4	V
Rotor-lock detection time	t_{RD}			0.5		sec
Zero-current detection (ZCD) threshold	I_{ZCD}			5		mA
Hall input low voltage, common mode	V_{HCM_LO}			1	1.06	V
Hall input high voltage, common mode	V_{HCM_HI}		4.43	4.5		V
Hall input minimum differential voltage	V_{HDM_MIN}	T_J = 25°C	60			mV_{PK-PK}
Thermal shutdown threshold (5)				160		°C
Thermal shutdown hysteresis (5)				25		°C

Notes:

5) Guaranteed by design.

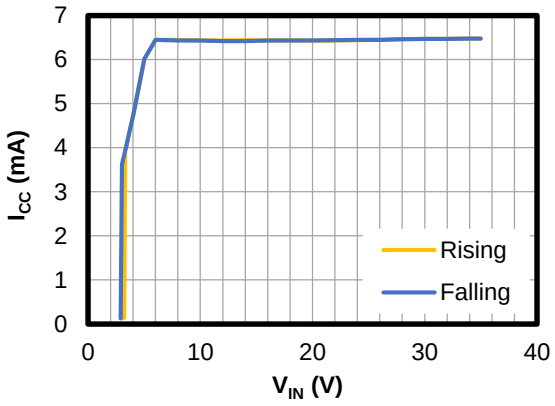
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

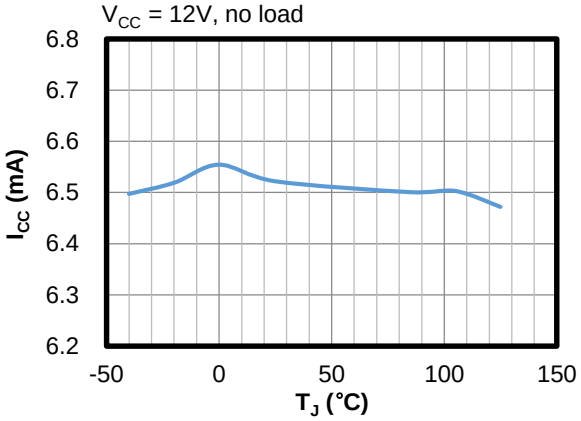
Supply Current vs. Input Voltage

V_{CC} = 2.9V to 35V, no load, T_J = 25°C

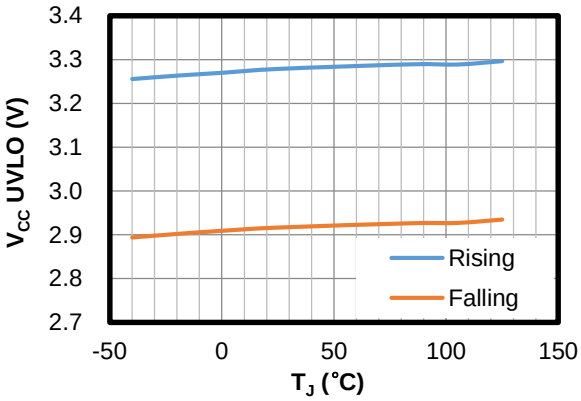


Supply Current vs. Junction Temperature

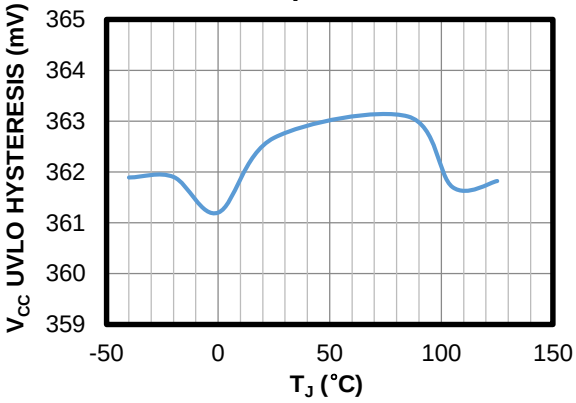
V_{CC} = 12V, no load



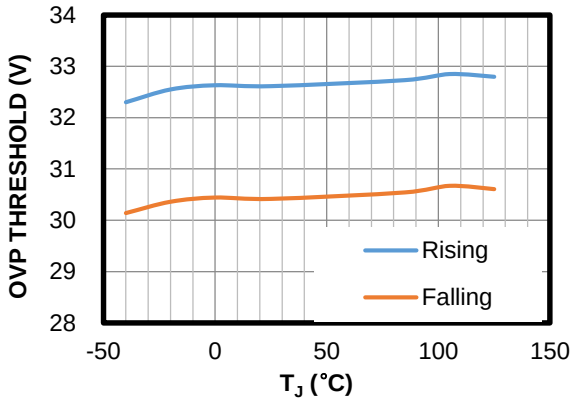
V_{CC} UVLO vs. Junction Temperature



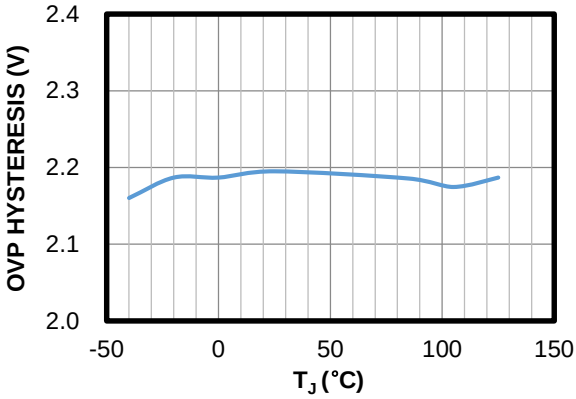
V_{CC} UVLO Hysteresis vs. Junction Temperature



OVP Threshold vs. Junction Temperature



OVP Hysteresis vs. Junction Temperature

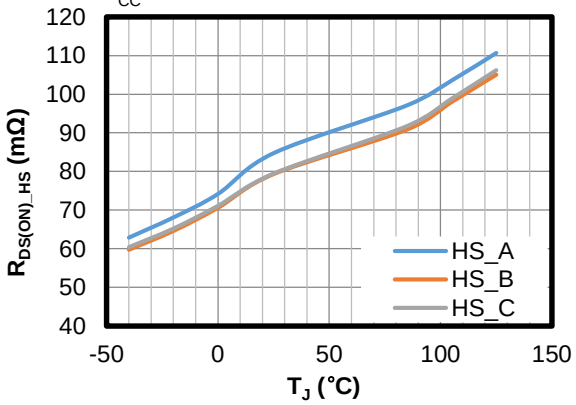


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

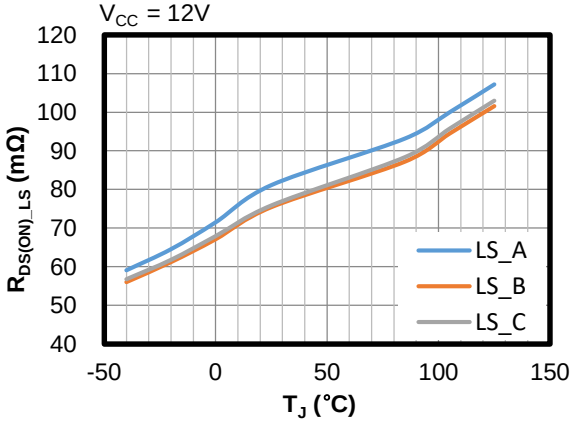
TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

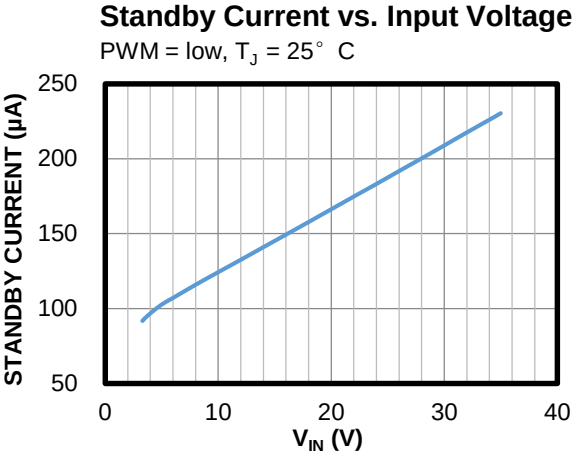
HS-FET $R_{DS(ON)}$ vs. Junction Temperature



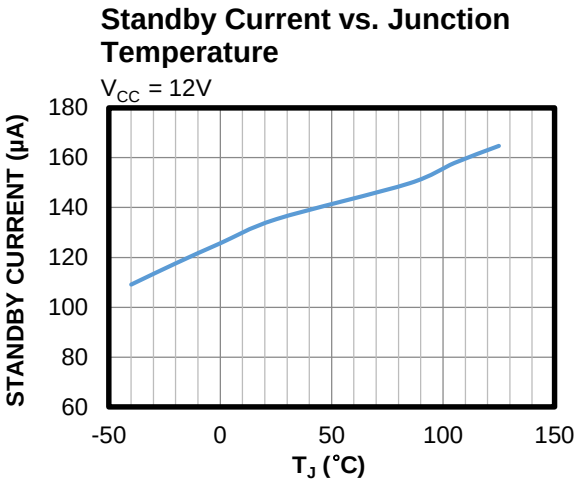
LS-FET $R_{DS(ON)}$ vs. Junction Temperature



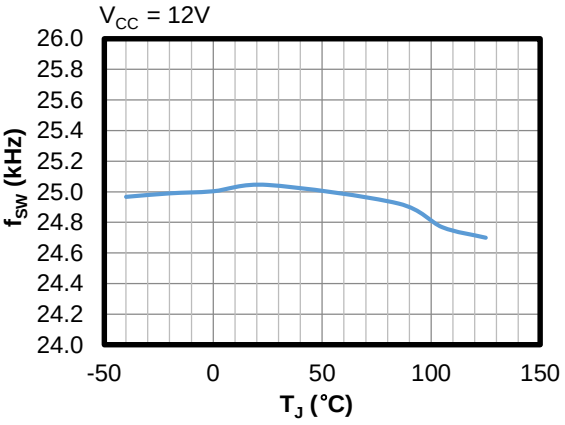
Standby Current vs. Input Voltage



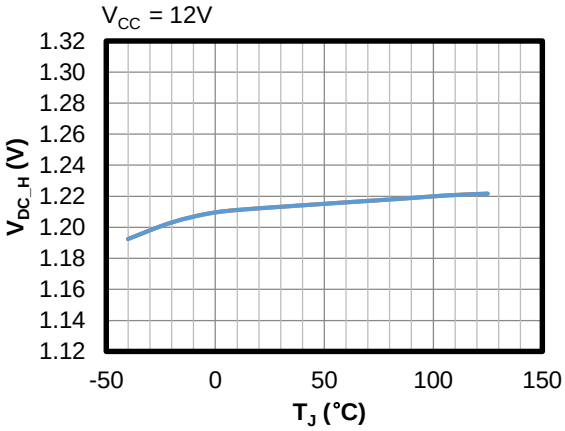
Standby Current vs. Junction Temperature



PWM Output Frequency vs. Junction Temperature



DC Input High Threshold vs. Junction Temperature



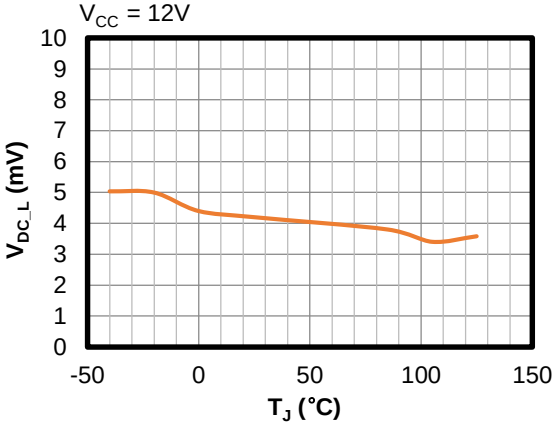
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

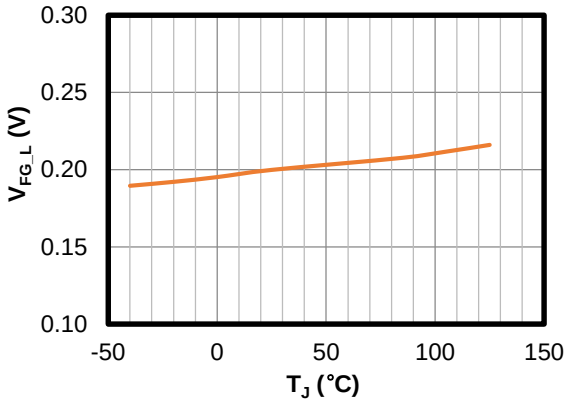
DC Input Low Threshold vs. Junction Temperature

V_{CC} = 12V



V_{FG_L} vs. Junction Temperature

V_{CC} = 12V, $I_{FG/RD}$ = 3mA



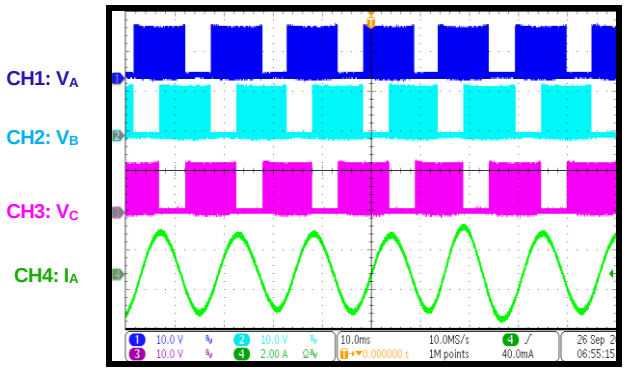
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

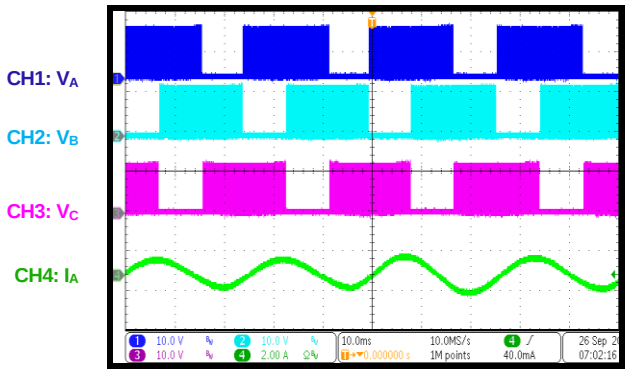
Steady State

PWM duty = 100%, DIR = low, CCW



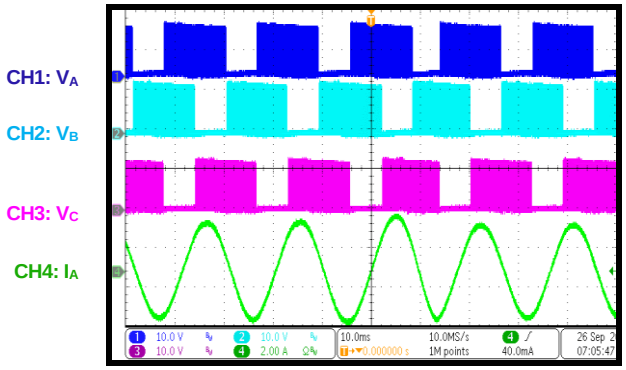
Steady State

PWM duty = 50%, DIR = low, CCW



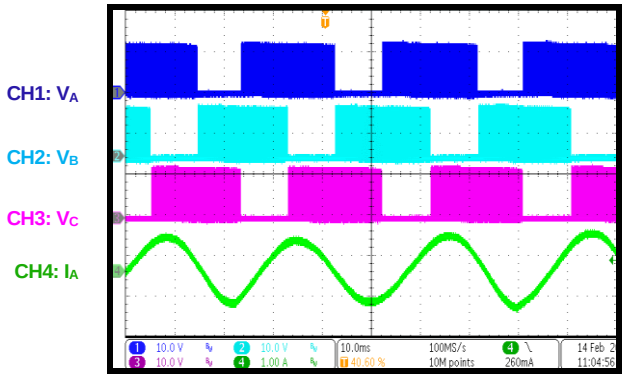
Steady State

PWM duty = 100%, DIR = high, CW



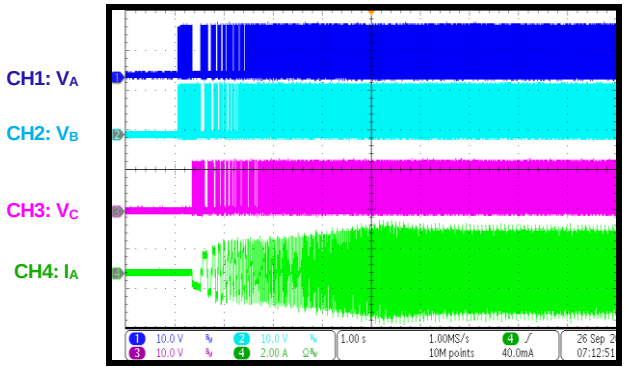
Steady State

PWM duty = 50%, DIR = high, CW



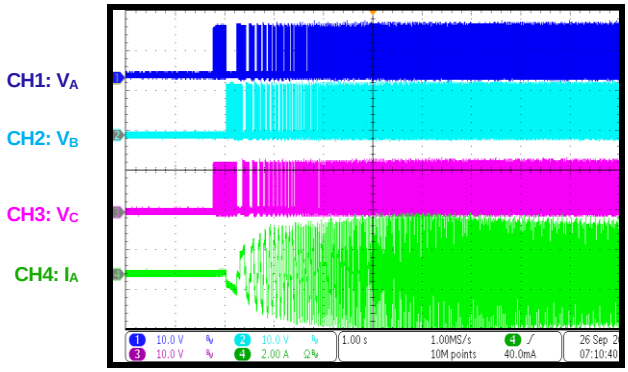
PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = low, CCW



PWM On

PWM duty = 0% to 100%, triple Hall-effect sensor, DIR = high, CW



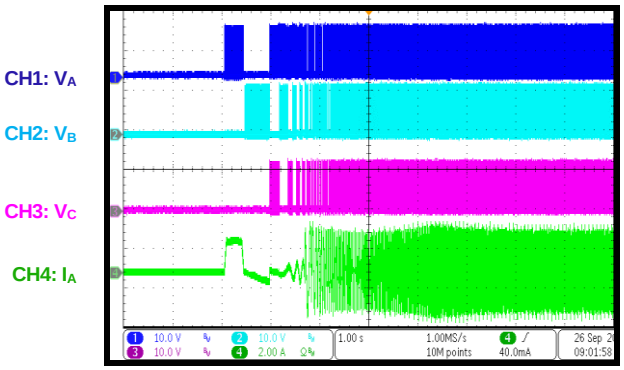
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

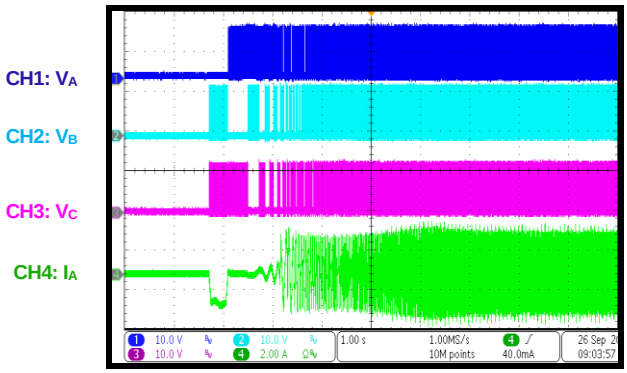
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = low, CCW



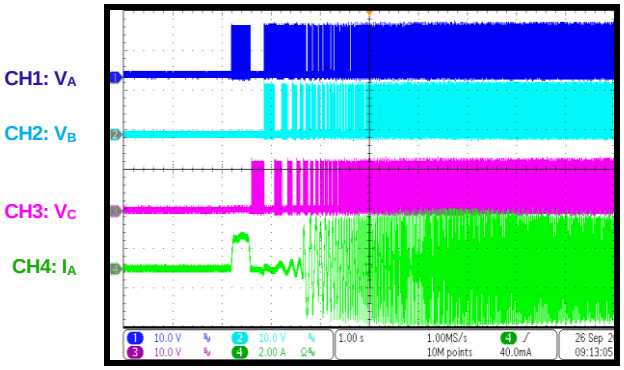
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = low, CCW



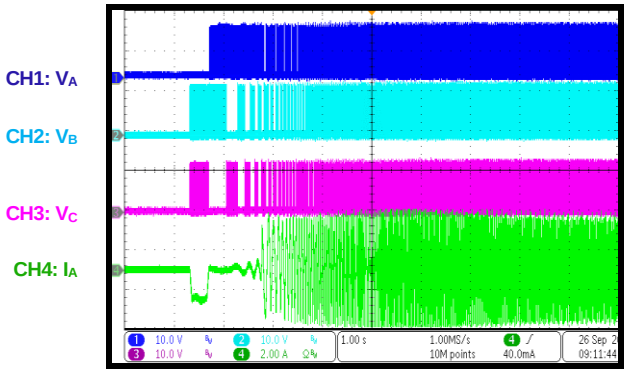
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = high, CW



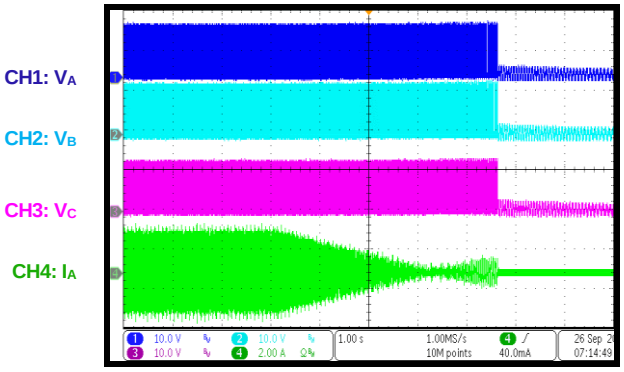
PWM On

PWM duty = 0% to 100%, single Hall sensor, DIR = high, CW



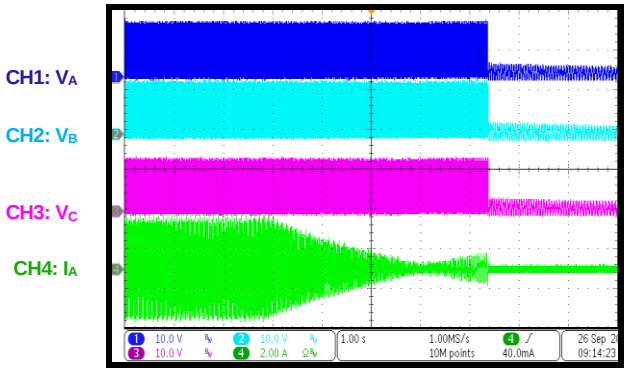
PWM Off

PWM duty = 100% to 0%, DIR = low, CCW



PWM Off

PWM duty = 100% to 0%, DIR = high, CW



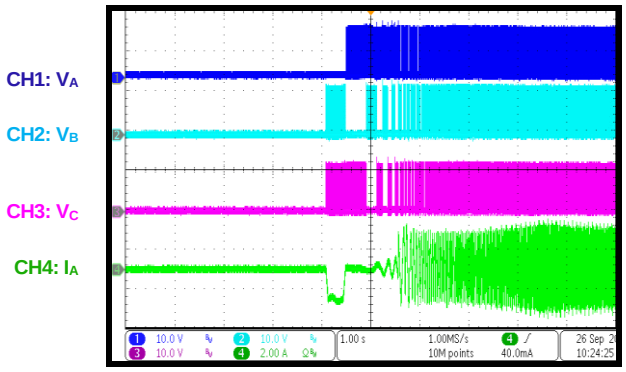
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, PWM frequency = 20kHz, with a single external Hall-effect sensor or triple external Hall-effect sensors.

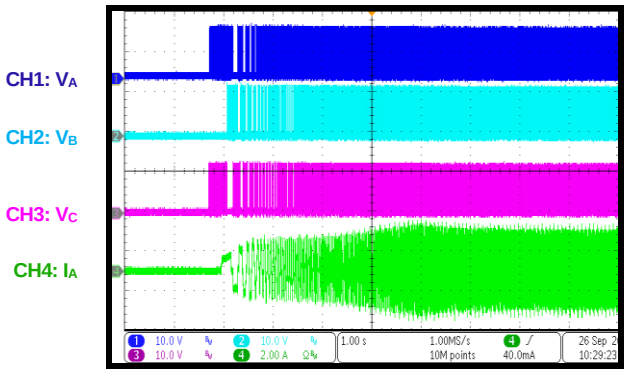
Start-Up with VCC

V_{CC} = 0V to 12V, PWM duty = 100%, single Hall sensor, DIR = low, CCW



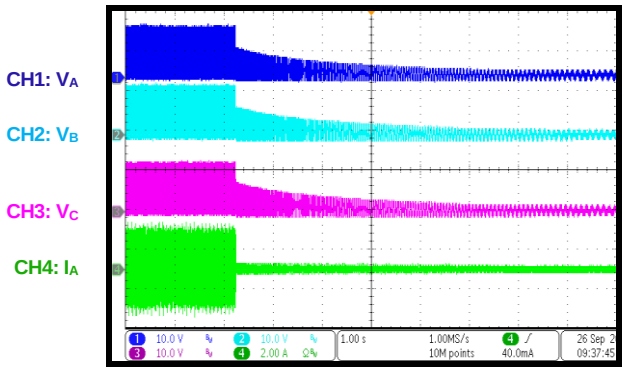
Start-Up with VCC

V_{CC} = 0V to 12V, PWM duty = 100%, triple Hall sensor, DIR = low, CCW



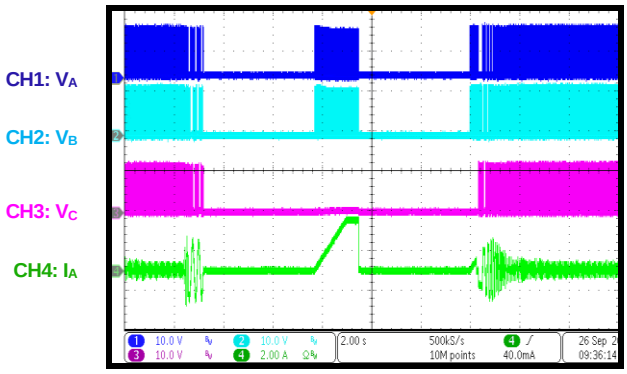
Shutdown with VCC

V_{CC} = 0V to 12V, PWM duty = 100%, DIR = low, CCW



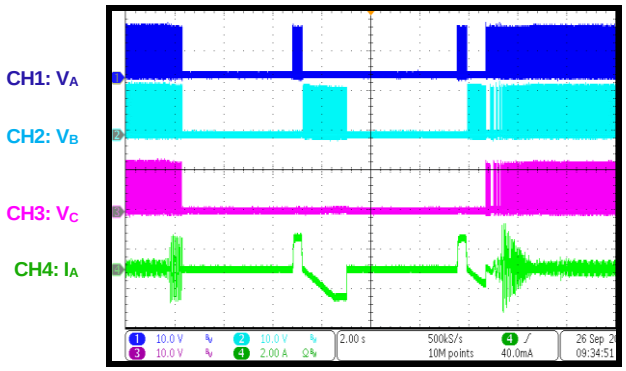
Rotor Lock and Retry

PWM duty = 25%, triple Hall sensor, lock rotor then release



Rotor Lock and Retry

PWM duty = 25%, single Hall sensor, lock rotor then release



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

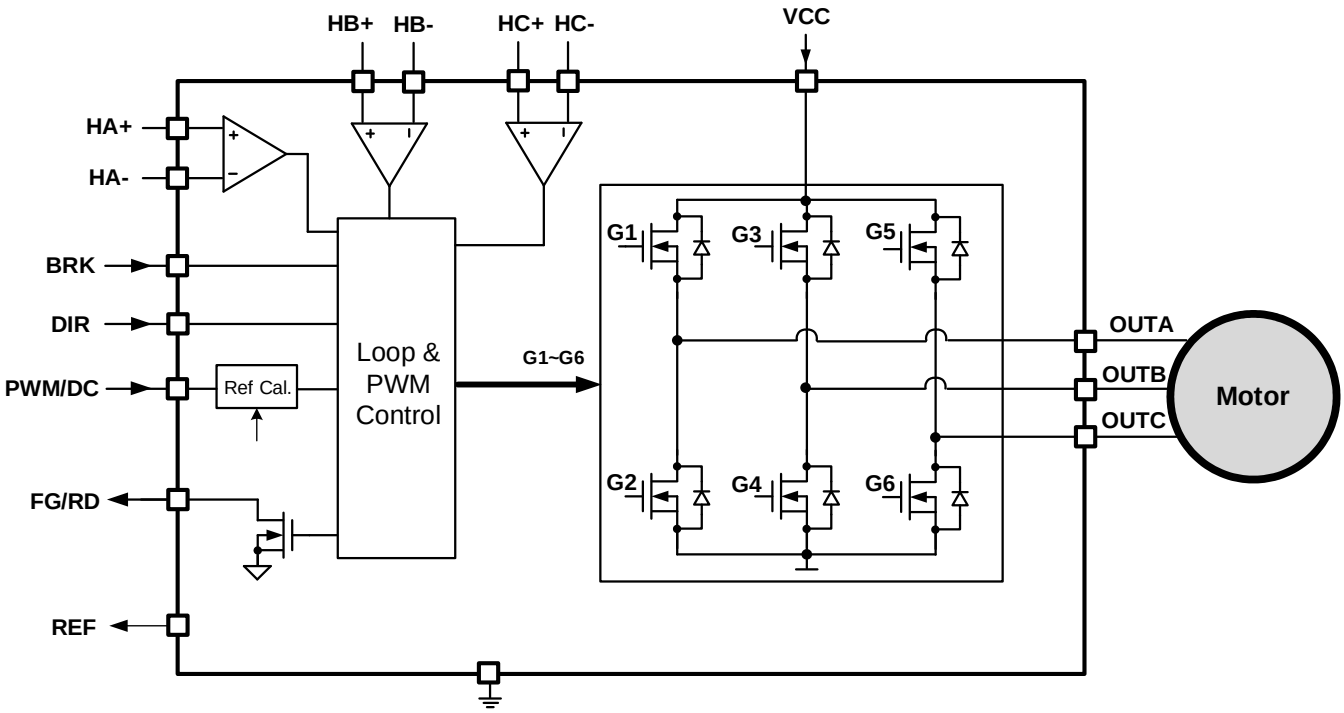


Figure 3: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

The MP6631H is a three-phase brushless DC (BLDC) motor driver with integrated power MOSFETs. The MP6631H controls the motor speed via the pulse-width modulation (PWM) signal or the DC voltage on the PWM/DC pin, with closed/open-loop speed control and a built-in, configurable speed curve function.

The MP6631H also features a rotational speed detector. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the external Hall signal. Additionally, direction control is achieved via the DIR pin's input, and the BRK pin is used to brake the motor.

Rich protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked-rotor protection, over-current protection (OCP), and thermal shutdown protection.

A sinusoidal drive is employed in the MP6631H. Figure 4 shows the MP6631H's output drive, where HA, HB, and HC are the output of Hall A, Hall B, and Hall C, respectively. OUTA, OUTB, and OUTC are the output duty of the OUTA, OUTB, and OUTC pins, respectively.

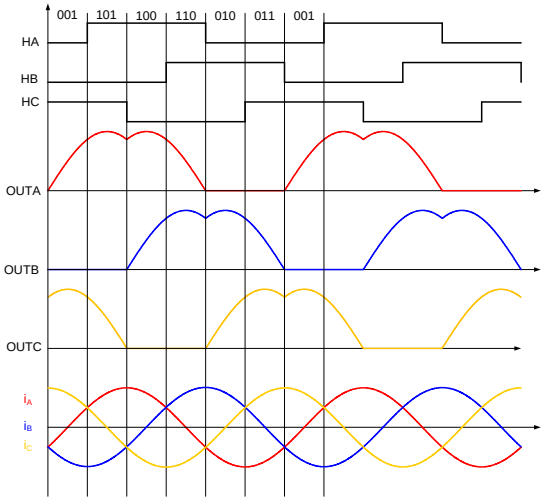


Figure 4: MP6631H Hall Output and Output Drive

Speed Control

The PWM/DC pin controls the motor speed in an open loop or closed loop via the PWM signal or the DC voltage. PWM/DC accepts a wide input frequency range (1kHz to 100kHz) or a 0V to 1.2V voltage.

If DC_PWM = 1, then the motor speed is controlled via the DC voltage on the PWM/DC pin.

If DC_PWM = 0, then the motor speed is controlled via the input PWM signal duty cycle.

Starting Duty and Minimum Speed

The starting duty is configured by the DIN_MIN bits. When PWM input duty is below the duty set by DIN_MIN, the fan speed supports two modes:

1. The speed maintains the minimum speed when SPD_ZERO is set to 0.
2. The speed is at 0 when SPD_ZERO is set to 1.

Speed Curve Configuration

The SPD_MAX registers configure the speed when the input duty is at 100%. Otherwise, the MP6631H provides a five-point curve configuration function where the output speed can be configured when the input duty is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

The DIN_MIN register sets the minimum input duty, and SPD_MIN sets the minimum output duty and minimum speed.

Figure 5 shows the curve configuration when SPD_ZERO = 1.

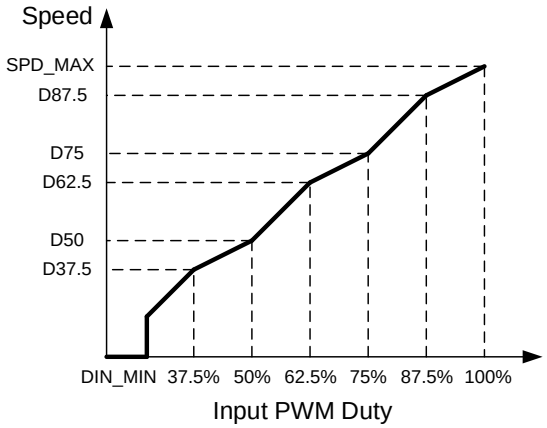


Figure 5: Curve Configuration when SPD_ZERO = 1

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

Figure 6 shows the curve configuration when SPD_ZERO = 0.

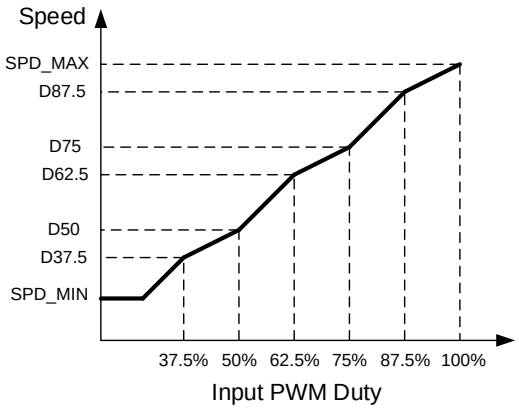


Figure 6: Curve Configuration when SPD_ZERO = 0

Speed Open-/Closed-Loop Control

In closed-loop mode (OPEN_L = 0, CLOSE_H = 1), the MP6631H internally detects the Hall signal speed and feedback to the control loop, which adjusts the output PWM duty in a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (OPEN_L = 1), the OUT1 and OUT2 output duty cycles directly depend on the PWM input duty.

In mixed mode (OPEN_L = 0, CLOSE_H = 0), the MP6631H operates in closed-loop mode when the PWM input duty is below 87.5%, and operates in open-loop mode when input duty exceeds 87.5%.

Soft-Start Time

To reduce the input inrush current during start-up, the MP6631H provides the reference speed's configurable soft-start time (t_{SS}) by setting register bits TDYN[1:0]. This time can be configured from 1.3s to 10.4s.

Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain depends on registers KI[7:0] and KP[7:0].

Higher KI and KP values lead to quick loop response. KI and KP should be adjusted according to the dynamic response and steady state operation.

Single- or Triple-Hall Input Mode

The MP6631H supports either a single or triple Hall-effect sensor. If a single Hall-effect sensor is employed, the Hall selecting bit must set the single Hall sensor, and Hall C is used as the control.

Direction Control

The direction is controlled by the DIR pin's polarity. When DIR is pulled low, the MP6631H operates in forward rotation in the following sequence: A → B → C → A…

When DIR is pulled high, the MP6631H operates in reverse rotation in the following sequence: A → C → B → A…

Standby Mode

The MP6631H provides standby mode when the VCC voltage (V_{CC}) exceeds its UVLO threshold and the SPD_ZERO bit = 1.

If the PWM/DC pin stays low (below V_{PWM_L} in PWM input mode or below V_{DC_L} in DC input mode) for 83ms and the MP6631H stops switching, then the MP6631H enters standby mode. In standby mode, the supply current decreases and the REF output is disabled. Standby mode is active in both PWM input mode and DC input mode.

If a PWM high signal (V_{PWM_H}) is detected on the PWM/DC pin in PWM input mode or in DC input mode, the MP6631H exits standby mode.

If standby mode is not needed in application, then select the MP6631HGL-0001, for which standby mode is disabled.

Alignment

At the beginning of start-up in single Hall sensor applications, the MP6631H aligns the rotor in certain positions depending on the Hall outputs. After the alignment time set by register TOPS completes, the MP6631H enters pre-startup. This function is only enabled in single Hall sensor applications.

Pre-Startup Timer

During pre-startup, the MP6631H gradually increases the output duty cycle with the timer set by the TPRE[1:0] bits. This provides sufficient torque for robust start-up and avoids current overshoot during start-up.

- TPRE = 0: Timer period is 2.5ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

- TPRE = 1: Timer period is 5ms
- TPRE = 2: Timer period is 10ms
- TPRE = 3: Timer period is 20ms

A higher timer period leads to lower soft pre-startup current, but increases pre-startup time.

Cycle-by-Cycle Over-Current Protection (OCP)

During normal switching, if the current flowing through the MOSFET exceeds the threshold set by register bits OCP_SEL[1:0] after a set blanking time, then the high-side MOSFETs (HS-FETs) turn off and the low-side MOSFETs (LS-FETs) turn on immediately. The MP6631H resumes normal switching during the next switching cycle.

Maximum Peak Current Limit

If the load current is not limited by OCP and the current exceeds the maximum peak current limit threshold (typically 6A), all MOSFETs turn off and the MP6631H tries to re-enable after a lock-retry time.

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. Different FG signal frequencies are provided. The frequencies are selected by setting the FGRD bit to 00, 01, or 10.

FG/RD is an open-drain output, and must be pulled up externally by a resistor.

Locked-Rotor Protection

If the motor rotor is locked and the Hall signal edge is not detected during the 0.5s detection time, then the MP6631H turns on all LS-FETs and auto-restarts after the recovery time (4.5s). By setting the FGRD bit to 11, the signal on FG/RD is set to rotor lock indication. During locked-rotor fault status, FG/RD remains low.

Over-Voltage Protection (OVP)

If the voltage on the VCC pin (V_{CC}) exceeds the over-voltage (OV) threshold (34V), the MP6631H turns off the HS-FETs and turns on the LS-FETs. Once V_{CC} drops below 32V, the device resumes normal operation.

Thermal Shutdown

The MP6631H also provides thermal monitoring. If the MP6631H's die temperature exceeds 160°C, then the output duty decreases to reduce power consumption until the die temperature drops below 135°C .

Under-Voltage Lockout (UVLO)

If the voltage on the VCC pin (V_{CC}) falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the device resumes normal operation.

Test Mode and Factory Mode

To configure the internal registers, the MP6631H supports test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM), which can be configured twice. Refer to the MPS Fan Driver GUI Software for easy parameter changes and memory configuration.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN[7:0]							
03h (OTP/REG)	HI_FREQ	RESERVED	DIN_MIN[5:0]					
04h (OTP/REG)	OVP_EN	WAIT_TM[1:0]		RESERVED	MAX_EN	CLOSE_H	OPEN_L	RESERVED
05h (OTP/REG)	RESERVED	TDYN[1:0]		TPRE[1:0]		SPD_ZERO	SINGLE	RESERVED
06h (OTP/REG)	RESERVED		DC_PWM	FGRD[1:0]		OCP_SEL[1:0]		TPOS
07h (OTP/REG)	RESERVED	SW_SEL	THETA_COMP[5:0]					
08h (OTP/REG)	KI[7:0]							
09h (OTP/REG)	KP[7:0]							
0Ah (OTP/REG)	RESERVED		WAIT_SEL	RESERVED		OCP_EN	OCP_BH	OVP_BH
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			DEBUG

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG00h

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	SPD_MAX[7:0]	OTP/REG	0xFF	Sets the maximum speed when the input duty is 100%. 8-bit least significant bit (LSB). Electrical speed = 7.5rpm / LSB

REG01h

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	SPD_MAX[15:8]	OTP/REG	0x08	Sets the maximum speed when the input duty is 100%. 8-bit most significant bit (MSB). Combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

REG02h

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	SPD_MIN[7:0]	OTP/REG	0x20	Sets the minimum speed or minimum output duty. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ, where: HI_FREQ = 0, 60rpm / LSB HI_FREQ = 1, 480rpm / LSB In open-loop mode, this bit sets minimum output duty, where minimum output duty = SPD_MIN[7:0] / 255 and the default is 12.5%.

REG03h

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	HI_FREQ	OTP/REG	0	High-frequency selection bit. 0: High frequency is not selected (default) 1: High frequency is selected. The SW bit must be 1 if HI_FREQ = 1.
6	RESERVED	N/A	0	Reserved.
5:0	DIN_MIN[5:0]	OTP/REG	0x10	Sets the starting duty, where the starting duty = DIN_MIN / 128 and the default is 12.5%.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG04h

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	OVP_EN	OTP/REG	0	Enables OVP. 0: Disable OVP (default) 1: Enable OVP
6:5	WAIT_TM[1:0]	OTP/REG	00	Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching or the motor speed threshold at which the IC starts driving the motor. The waiting time or speed threshold can be selected as follows: If WAIT_SEL = 1, wait for a fixed time. The time setting is WAIT_TM = 00: 1.2s, 01: 1.8s, 10: 3s, 11: 4.2s. If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed, where WAIT_TM = 00: 1000rpm (electrical speed), 01: 600rpm, 10: 150rpm, 11: 60rpm. This is active for triple Hall sensor applications.
4	Reserved	N/A	0	Reserved.
3	MAX_EN	OTP/REG	0	Enables the maximum speed when PWM input duty < DIN_MIN. 0: Disabled (default) 1: Maximum output speed or maximum output duty when PWM input duty < DIN_MIN Active only when SPD_ZERO = 0.
2	CLOSE_H	OTP/REG	0	Enables closed-loop speed control when the PWM input duty > 87.5%. 0: Open-loop speed control when the PWM input duty > 87.5% (default) 1: Closed-loop speed control when the PWM input duty > 87.5%
1	OPEN_L	OTP/REG	1	Enables open-loop speed control. 1: Open-loop speed control (default) 0: Closed-loop speed control when the PWM input duty < 87.5%
0	RESERVED	N/A	0	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG05h

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6:5	TDYN[1:0]	OTP/REG	00	Sets the soft dynamic time. The output duty reference time ranges from 0% to 100%. 00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 10.4s
4:3	TPRE[1:0]	OTP/REG	10	Pre-startup time bits. The output duty's time duration increases by 1 step. 00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms
2	SPD_ZERO	OTP/REG	1	Enables zero speed. 0: Maintains minimum speed when PWM input duty < DIN_MIN 1: Stops when PWM input duty < DIN_MIN
1	SINGLE	OTP/REG	1	Selects the number of Hall sensors. 0: Triple Hall sensor application 1: Single Hall sensor application (default)
0	RESERVED	N/A	0	Reserved.

REG06h

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	01	Reserved.
5	DC_PWM	OTP/REG	0	Selects DC input or PWM input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	FGRD[1:0]	OTP/REG	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 10: 1/4x for single Hall sensor applications, 3x for triple Hall sensor applications 11: RD
2:1	OCP_SEL[1:0]	OTP/REG	11	Sets the current limit threshold. 00: 0.7A 01: 1.5A 10: 2.2A 11: 3A (default)
0	TPOS	OTP/REG	0	Sets the alignment time. 0: 320ms (default) 1: 650ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG07h

Addr: 0x07				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6	SW_SEL	OTP/REG	0	Selects the output switching frequency (f_{SW}). 0: 25kHz (default) 1: 50kHz
5:0	THETA_COMP[5:0]	OTP/REG	0x00	Sets the leading/lag compensation angle. 0x00: Auto compensation. The non-zero value sets the fixed compensation. The MSB is the signed bit. MSB = 0: leading Compensation angle = THETA_COMP[5:0] x 15 / 8° + 0.94° MSB = 1 lag Compensation angle = 119.06° - THETA_COMP[5:0] x 15 / 8°

REG08h

Addr: 0x08				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	KI[7:0]	OTP/REG	0x01	Integral parameter for closed-loop speed control.

REG09h

Addr: 0x09				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	KP[7:0]	OTP/REG	0x01	Gain during closed-loop speed control.

REG0Ah

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	00	Reserved.
5	WAIT_SEL	OTP/REG	0	Selects the waiting function at start-up. 0: The IC keeps no drive until the speed drops below the threshold speed during start-up (default) 1: The IC keeps no drive for a fixed time during start-up
4:3	RESERVED	N/A	00	Reserved.
2	OCP	OTP/REG	0	Enables over-current protection (OCP). 0: Enabled 1: Disabled
1	OCP_BH	OTP/REG	0	Selects the OCP response. 0: Turn on the LS-FETs and resume switching during the next switching cycle (default) 1: Decrease the output duty
0	OVP_BH	OTP/REG	0	Selects the over-voltage protection (OVP) response. 0: Turn on the LS-FETs when OVP is triggered 1: Turn off all the MOSFETs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG0Bh

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D37.5[7:0]	OTP/REG	0x60	Sets the speed or output duty when the input PWM duty = 37.5%. For open-loop control, set the output duty when the input PWM duty = 37.5%. Output duty = D37.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 37.5%. Speed = D37.5[7:0] / 256 x SPD_MAX[15:0].

REG0Ch

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D50[7:0]	OTP/REG	0x80	Sets the speed or output duty when the input PWM duty = 50%. For open-loop control, set the output duty when the input PWM duty = 50%. Output duty = D50[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 50%. Speed = D50[7:0] / 256 x SPD_MAX[15:0].

REG0Dh

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D62.5[7:0]	OTP/REG	0xA0	Sets the speed or output duty when the input PWM duty = 62.5%. For open-loop control, set the output duty when the input PWM duty = 62.5%. Output duty = D62.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 62.5%. Speed = D62.5[7:0] / 256 x SPD_MAX[15:0].

REG0Eh

Addr: 0x0E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D75[7:0]	OTP/REG	0xC0	Sets the speed or output duty when the input PWM duty = 75%. For open-loop control, set output duty when the input PWM duty = 75%. Output duty = D75[7:0] / 256. In closed-loop control, set the speed reference when the input PWM duty = 75%. Speed = D75[7:0] / 256 x SPD_MAX[15:0].

REG0Fh

Addr: 0x0F				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D87.5[7:0]	OTP/REG	0xE0	Sets the speed or output duty when the input PWM duty = 87.5%. For open-loop control, set the output duty when the input PWM duty = 87.5%. Output duty = D87.5[7:0] / 256. For closed-loop control, set the speed reference when the input PWM duty = 87.5%. Speed = D87.5[7:0] / 256 x SPD_MAX[15:8].

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REG10h

Addr: 0x10				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	00	Reserved.
5:4	OTP_PAGE[1:0]	REG	0	One-time programmable (OTP) memory page indicator. 00: No OTP configured 01: OTP Page 1 is configured 10: OTP Page 2 is configured
3:1	RESERVED	N/A	000	Reserved.
0	DEBUG	REG	0	Debugging bit. Write 1 to this bit to exit debugging mode.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C_{IN}) as close to the VCC and GND pins as possible. A sufficient capacitance must be applied to maintain a stable input voltage (V_{IN}) and reduces input switching voltage noise and ripple. C_{IN}'s impedance must be low at the switching frequency (f_{SW}). Ceramic capacitors with X7R dielectrics are recommended for their low ESR characteristics.

The capacitance depends on the DC voltage applied on the capacitor. A ceramic capacitor can lose more than 50% of its capacitance when the voltage is close to the voltage rating. Leave a sufficient voltage rating margin when selecting the capacitor.

It is recommended to use an additional electrolytic capacitor to absorb chargeback back energy.

Input Clamping TVS

High voltage spikes are created when the energy stored in the motor charges back to C_{IN}. To avoid these spikes, a voltage-clamping transient voltage suppressor (TVS) diode is recommended. The maximum clamping voltage should be below the MP6631H's maximum operating V_{IN}.

Hall Placement and Connection

Hall sensors are required to operate the MP6631H, which supports Hall elements with differential inputs. When Hall elements are used, the Hall sensors can be connected in series or in parallel.

Figure 7 shows the Hall sensors connected in series.

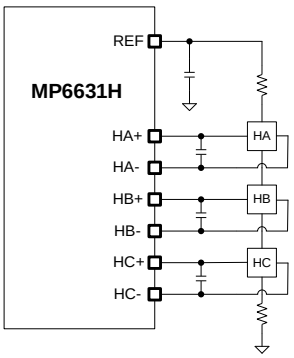


Figure 7: Series Hall Elements Connection

Figure 8 shows the Hall sensors connected in parallel.

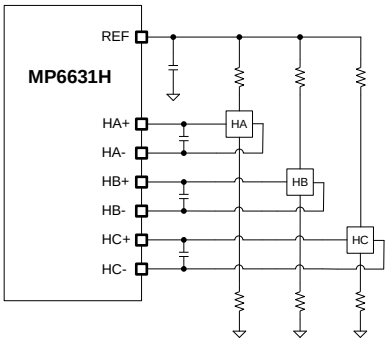


Figure 8: Parallel Hall Elements Connection

The MP6631H's Hall-sensor IC outputs logic polarity with an open-drain output, and requires an external pull-up resistor.

Figure 9 shows the Hall-sensor IC connection.

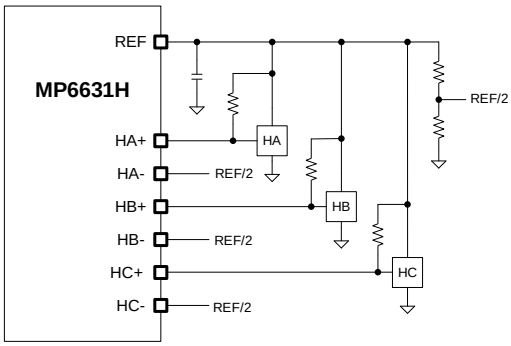


Figure 9: Hall Sensor Connection

Hall Sensor Placement Example

The MP6631H supports either a single or triple Hall-effect sensor. Consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

1. When the current flows into the stator phase winding, the north magnetic field is generated.
2. If the Hall sensor output is high when the north pole is close to the Hall sensor's branded side.

If both conditions are satisfied, then the Hall sensor placement is as follows (see Figure 10):

- Hall A is aligned with phase B's central line.
- Hall B is aligned with phase C's central line.
- Hall C is aligned with phase A's central line. In single Hall sensor applications, Hall C is the active Hall sensor.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

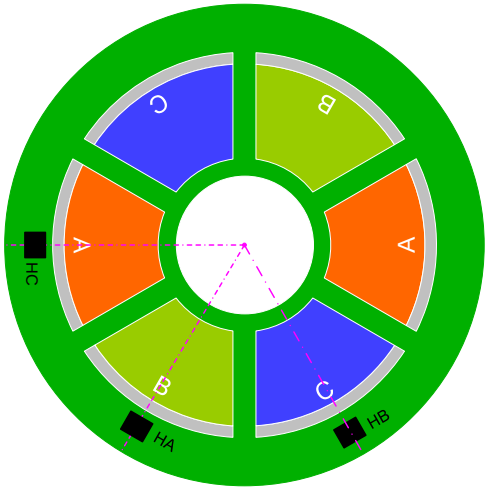


Figure 10: Hall Sensor Placement Option 1

If one of these conditions is not satisfied, then the Hall sensor placement can be shifted 180° into an electrical angle, resulting in the following Hall sensor placement (see Figure 11):

- Hall A is aligned with the central line of phase A and phase C.
- Hall B is aligned with the central line of phase A and phase B.
- Hall C is aligned with the central line of Phase B and Phase C.

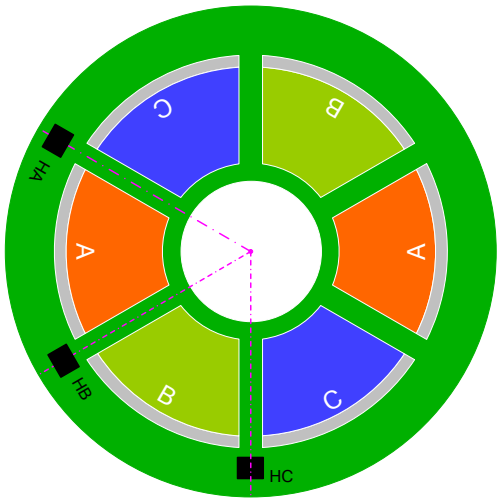


Figure 11: Hall Sensor Placement Option 2

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 12 and Figure 13, and follow the guidelines below:

1. After selecting C_{IN}, place a 100nF/X7R bypass capacitor as close to the VCC and GND pins as possible.
2. Figure 12 shows the recommended PCB layout when the MP6631H is placed on the top layer and the bypass capacitor is placed on the bottom layer.

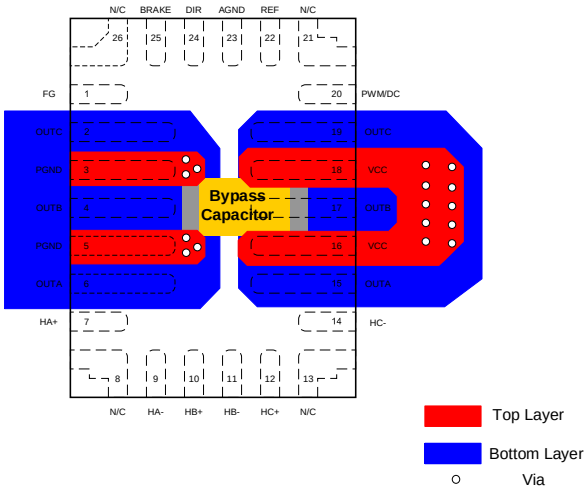


Figure 12: Recommended PCB Layout (Top View)

3. Figure 13 shows the side view of the MP6631H's recommended PCB layout.

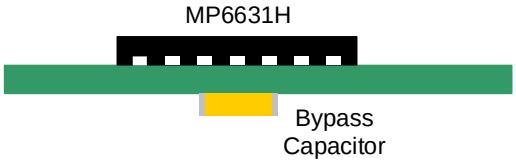


Figure 13: Recommended PCB Layout (Side View)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

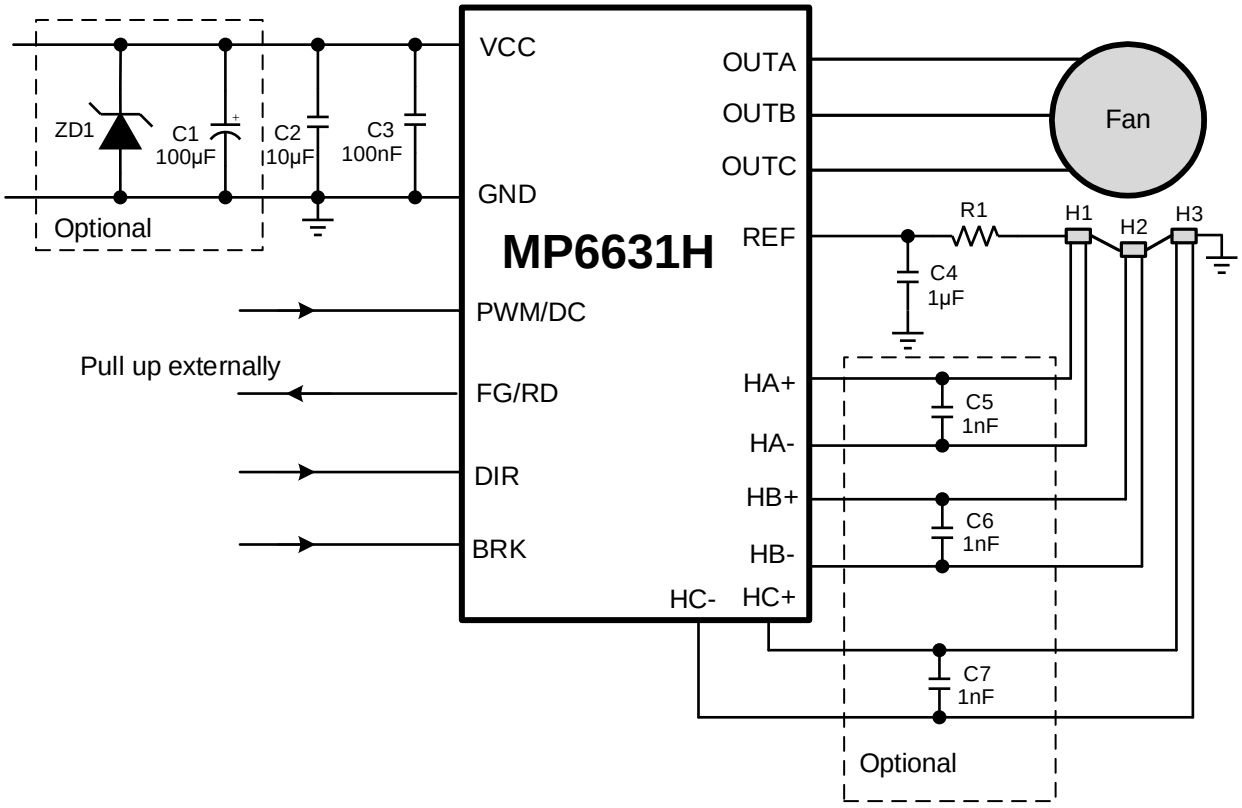
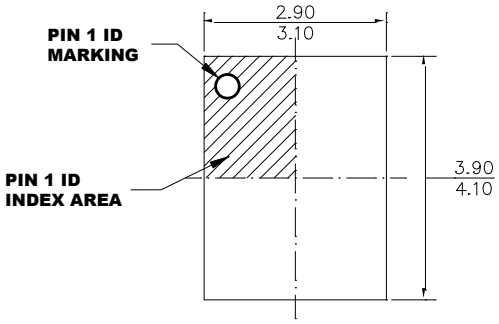


Figure 12: Triple Hall-Effect Sensor Application

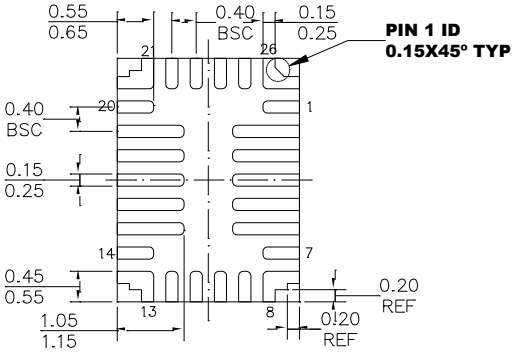
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

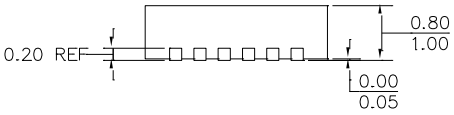
QFN-26 (3mmx4mm)



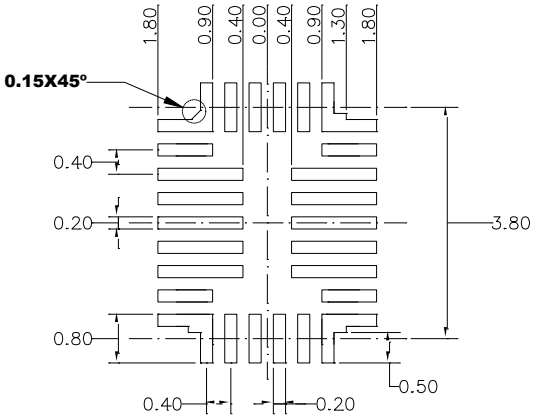
TOP VIEW



BOTTOM VIEW



SIDE VIEW



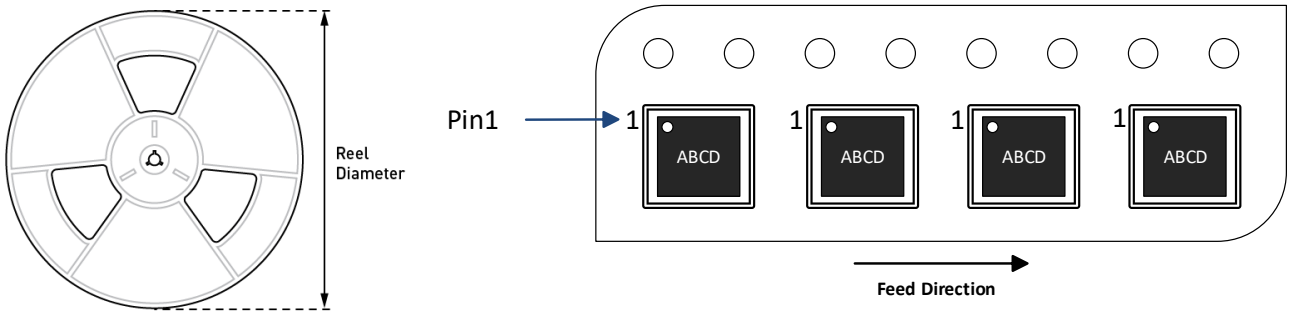
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6631HGL-xxxx-Z	QFN-26 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/17/2022	Initial Release	-
1.1	2/21/2023	Updated the Hall input low voltage, common mode parameter's maximum value to "1.06"; updated the Hall input high voltage, common mode parameter's minimum value to "4.43"; updated the Hall input minimum differential voltage parameter's name, symbol, conditions, and values	5
1.2	3/28/2025	Added the Standby Mode section	14
		Corrected the OCP threshold bit to OCP_SEL[1:0] in the Cycle-by-Cycle Over-Current Protection (OCP) section	15
		Corrected the OCP threshold bit to OCP_SEL[1:0] in the Register Map section	16
		Corrected the OCP threshold bit to OCP_SEL[1:0] in the REG06h section	19

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.