MPQ4214

40V, Synchronous Buck-Boost Controller with I²C and Adjustable OCP via IPWM, AEC-Q100 Qualified

DESCRIPTION

The MPQ4214 is a synchronous, four-switch, buck-boost controller capable of regulating different output voltages with a wide input voltage range and high efficiency. The MPQ4214 provides an I²C interface, which supports V_{OUT} voltage programmability, V_{OUT} slew-rate control, and constant output current limit programmability, making the MPQ4214 suitable for USB power delivery (PD) design in USB Type-C power supplies.

The MPQ4214 uses valley current control in buck mode and peak current control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MPQ4214 offers forced continuous conduction mode (FCCM) and a programmable average current limit, which supports flexible designs for different applications.

The MPQ4214 also features hiccup over-current protection (OCP), auto-retry over-voltage protection (OVP), programmable soft start, and programmable under-voltage lockout (UVLO).

The MPQ4214 is available in a QFN-27 (5mmx5mm) package, and it available in AEC-Q100 Grade 1.

FEATURES

- 6V to 40V Start-Up Input Voltage Range
- 5V to 40V Operation Input Voltage Range
- Flexible Reference Voltage Selection:
  - MPQ4214GU: Programmable V_{REF} Voltage
  - MPQ4214GU-12: 1.2V Fixed V_{REF} Voltage
- MPQ4214 Flexible I²C Interface Control for:
  - 0.5V to 36V Output Voltage Range
  - 0.3V to 2.047V Reference Voltage Range with 1mV Steps
  - Selectable V_{OUT} Slew Rate
  - 0.6A Step Programmable Output Constant Current Limit
- <50mA Step Output Current Limit Adjusting through IPWM Pin
- Frequency Dithering Function for EMI Optimization
- Integrated V_{OUT} Discharge Function
- Selectable 200kHz, 300kHz, 400kHz, and 600kHz Switching Frequency
- OCP, SCP, and OVP
- Output Enters High-Impedance State during EN Shutdown
- Interrupt Indicator for CC, OCP, OVP, and OTP
- Available in a QFN-27 (5mmx5mm) Package
- Available in AEC-Q100 Grade 1

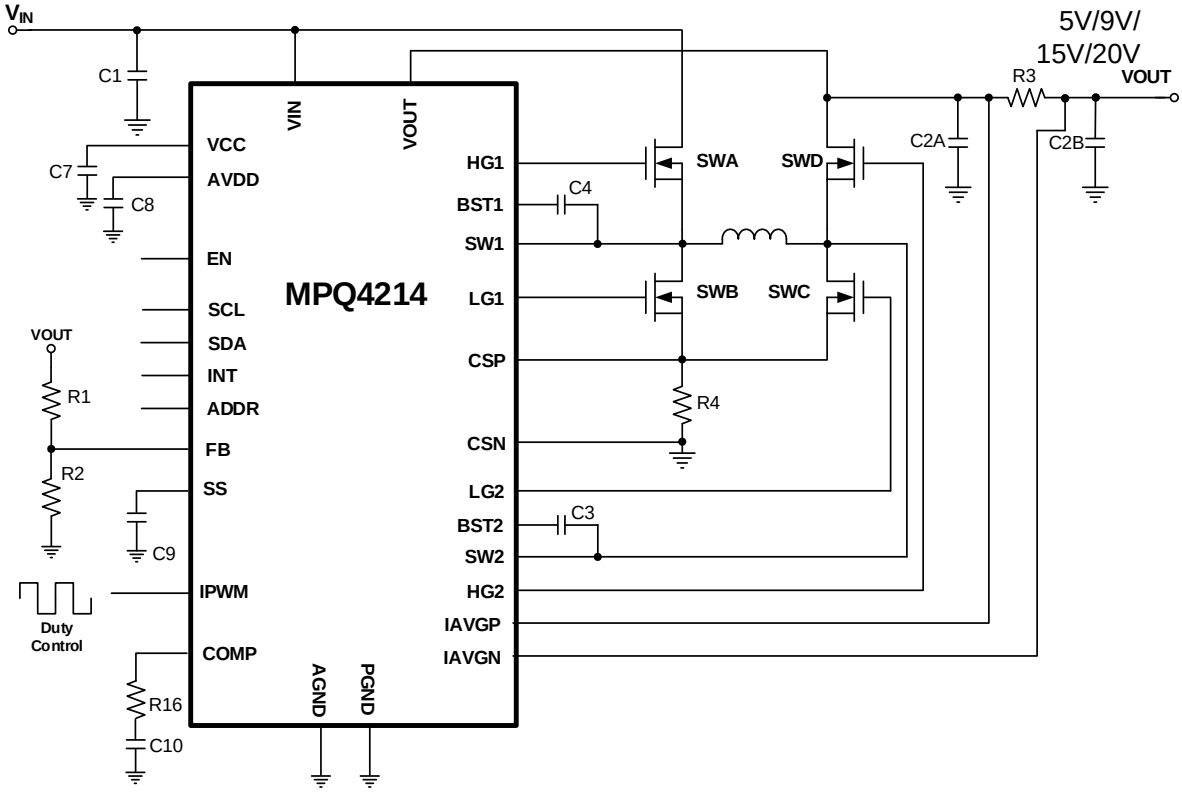
APPLICATIONS

- USB Power Delivery
- Industrial PC Power Supplies
- Wireless Charging
- High-Power LED Drivers

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ4214GU-AEC1*	QFN-27 (5mmx5mm)	*See Below*	*2*
MPQ4214GU-12-AEC1*	QFN-27 (5mmx5mm)	*See Below*	

* For Tape & Reel, add suffix –Z (e.g. MPQ4214GU–AEC1-Z).

TOP MARKING (MPQ4214GU-AEC1)

MPSYYWW
MP4214
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4214: Part number
LLLLLLL: Lot number

TOP MARKING (MPQ4214GU-12-AEC1)

MPSYYWW
MP4214
LLLLLLL
12

MPS: MPS prefix
YY: Year code
WW: Week code
MP4214: Part number
LLLLLLL: Lot number
12: Part number suffix

EVALUATION KIT EVKT-MPQ4214 CONTENTS

EVKT-MPQ4214 kit contents (items listed below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website):

#	Part Number	Item	Quantity
1	EVQ4214-U-00A	MPQ4214GU evaluation board	1
2	EVKT-USBI2C-02	Includes USB to I²C communication interface device, USB cable, and ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

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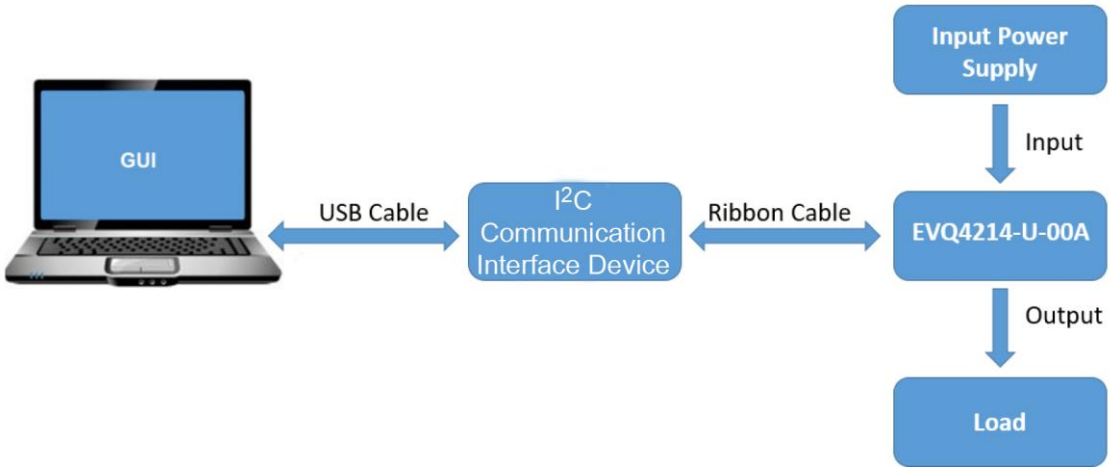
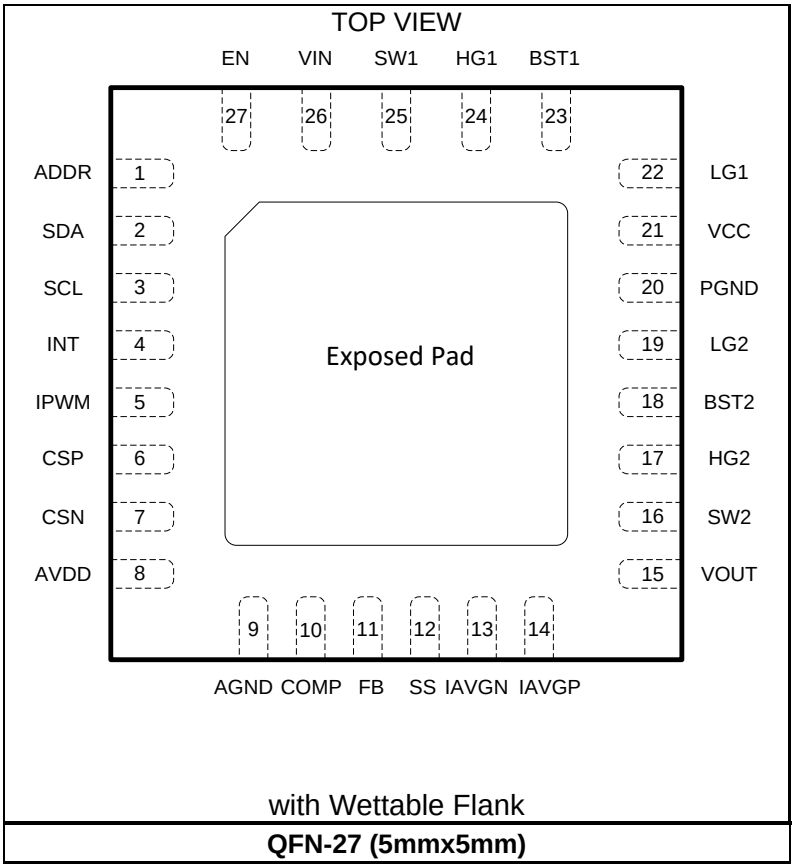


Figure 1: EVKT-MPQ4214 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-27 (5mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	ADDR	**I²C slave address set pin.**
2	SDA	**I²C data signal.**
3	SCL	**I²C clock signal.**
4	INT	**Interrupt pin for PNG, OCP, OTP, and OVP events.** In default set-up, INT is masked off for response to a PNG event. It is an open-drain output, and is pulled low when an interrupt event occurs, recovering to open drain when the fault is cleared. INT is an open drain when the IC is not enabled.
5	IPWM	**PWM signal input to continuously program the output current limit.** The I²C register can program the maximum output current limit. The IPWM can change the final current limit to the I²C setting value multiplied by the IPWM duty cycle. IPWM is internally pulled up to AVDD through a 1MΩ resistor.
6	CSP	**Positive input of the switching current-sense signal.** Connect to the high side of the current-sense resistor.
7	CSN	**Negative input of the switching current-sense signal.** Connect to the low side of the current-sense resistor.
8	AVDD	**5V internal control circuit bias supply.** Decouple with a ≥2.2μF capacitor.
9	AGND	**Analog ground.**
10	COMP	**Internal error amplifier output pin.** Connect a capacitor and resistor in series to AGND for loop compensation.
11	FB	**VOUT voltage feedback pin.** Connect a resistor divider from V_{OUT} to FB.
12	SS	**Soft start set pin.** Sets the hiccup off time period. Connect an external capacitor to SS.
13	IAVGN	**Negative terminal of average current limit sense input.** The IAVGN and IAVGP pins can only be used for output current limit setting by connecting to the positive terminal of the output rail.
14	IAVGP	**Positive terminal of average current limit sense input.** The IAVGN and IAVGP pins can only be used for output current limit setting by connecting to the positive terminal of the output rail.
15	VOUT	**V_{OUT} voltage sense input.** Supplies power to VCC based on VCC power logic. Connect to the output capacitor.
16	SW2	**Boost switch node of the converter.** Connect to the source of SWD and drain of SWC.
17	HG2	**Boost high-side MOSFET gate driver pin.** Connect directly to the gate of SWD.
18	BST2	**Bootstrap power pin for boost high-side MOSFET gate driver.** Connect one capacitor between BST2 and SW2. It is supplied by VCC or BST1.
19	LG2	**Boost high-side MOSFET gate driver pin.** Connect directly to the gate of SWC.
20	PGND	**Power ground.** Gate-driving current return pin.
21	VCC	**Driver circuit and internal bias supply.** Powered by VIN or VOUT. Decouple with a ≥2.2μF ceramic capacitor as close to this pin as possible.
22	LG1	**Buck low-side MOSFET gate driver pin.** Connect directly to the gate of the SWB.
23	BST1	**Bootstrap power pin for buck high-side MOSFET gate driver.** Supplied by VCC or BST2. Connect one capacitor between BST1 and SW1.
24	HG1	**Buck high-side MOSFET gate driver pin.** Connect directly to the gate of SWA.
25	SW1	**Buck switch node of the converter.** Connect to the source of SWA and drain of SWB.
26	VIN	**VIN power supply and voltage-sense input.**
27	EN	**Chip enable control pin.** If not used, connect EN to the input source for automatic start-up. EN can program VIN UVLO. Do not float this pin.
	Exposed pad	**Connect to ground.**

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ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .....-0.3V to +45V
VOUT, IAVGP, IAVGN .....-0.3V to +40V
VCC .....-0.3V to +8.5V
SW1, SW2 .....
.....-1V to +45V (-5V to +50V for <20ns)
LG1, LG2 .....
.....-0.3V to +10V (-2V to +11V for <20ns)
BST1, HG1 ..... -0.3V to V_{SW1} + 8.5V
BST2, HG2 ..... -0.3V to V_{SW2} + 8.5V
All other pins .....-0.3V to +6.5V
Continuous power dissipation (2) (6)..... 5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Start-Up voltage (V_{ST}) .....6V to 40V
Operation voltage (V_{IN}) (4) .....5V to 40V
Output voltage (V_{OUT}).....0.5V to 36V (5)
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVQ4214-U-00A (6) ……	25	6 °C/W
JESD51-7 (7) ……..	32	6 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Operation voltage after V_{OUT} is regulated to a voltage 5V or higher.
5) Only the MPQ4214GU can work down to 0.5V; the MPQ4214GU-12's reference voltage is fixed at 1.2V.
6) Measured on EVQ4214-U-00A, 4-layer PCB.
7) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Operating VCC voltage	V_{CC}	V_{IN} = 6V or V_{OUT} = 6V, 0mA to 20mA on VCC	5.1	5.95	6	V
		V_{IN} = 12V or V_{OUT} = 12V, 0mA to 60mA on VCC	6.7	7.2	7.7	V
VIN UVLO	VIN_{UVLO-R}	VIN rising	5	5.5	5.9	V
VCC UVLO	VCC_{UVLO-F}	VCC falling	3.8	4.3	4.8	mV
VCC power source change threshold	VINTH_VCC	V_{OUT} = 12V, ramp V_{IN} from 5V to 10V	8.1	8.8	9.5	V
	VOUTTH_VCC	V_{IN} = 12V, ramp V_{OUT} from 5V to 10V	8.1	8.8	9.5	V
AVDD voltage	V_{AVDD}	V_{IN} = 12V, 0mA to 30mA	4.7	5.2	5.6	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on the VIN and VOUT pins			5	µA
		ENPWR bit = 0, V_{IN} = 12V, V_O = 0V, measured on the VIN pin	300	450	600	µA
Enable Control (EN Pin)						
EN turn-on threshold voltage	V_{EN-ON}	V_{EN} rising (switching)	1.25	1.35	1.45	V
EN high threshold voltage	V_{EN-H}	V_{EN} rising (micro-power)			1.1	V
EN low threshold voltage	V_{EN-L}	V_{EN} falling (micro-power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	EN > V_{EN-ON}	3.2	4.7	6.2	µA
EN input current	I_{EN}	V_{EN} = 0V, 3.3V		0.01		µA
EN turn-on delay (8)		C_{SS} = 47nF		1		ms
Feedback Control						
MPQ4214GU reference voltage	V_{REF}	VREF bits = 1111 1111 111, T_J = 25°C, full V_{IN} range	-1%	2.047	+1%	V
		VREF bits = 1111 1111 111, T_J = -40°C to +125°C, full V_{IN} range	-2%	2.047	+2%	V
		VREF bits = 0011 1110 100, T_J = 25°C, full V_{IN} range	-2%	0.5	+2%	V
		VREF bits = 0011 1110 100, T_J = -40°C to +125°C, full V_{IN} range	-3%	0.5	+3%	V
MPQ4214GU-12 Reference voltage	V_{REF-12}	T_J = 25°C, full V_{IN} range	-2%	1.2	+2%	V
FB pin input current	I_{FB}	V_{FB} = 0.52V			200	nA
Error amp transconductance	G_{EA}			1220		µA/V
Comp to current-sense gain	Gcs	ΔV_{CS} / ΔV_{COMP}		200		mV/V
SS charge current	I_{CHG_SS}	During soft start and overload recovery	2	6	10	µA
SS discharge current (8)	I_{DSG_SS}	After trigger hiccup protection		1		µA
VREF change slew rate	t_{REF}	SR = 00	25	38	51	mV/ ms
		SR = 11	130	150	170	mV/ ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Limit and IPWM Control						
Buck valley current limit	I_{LIMIT_BUCK}		113	133	153	mV
Boost peak current limit	I_{LIMIT_BOOST}		130	150	170	mV
OCP hiccup threshold (8)	V_{TH_OCP}			60%		V_{REF}
Average constant current limit (IAVGP - IAVGN)	I_{AV_LIMIT}	ILIM bits = 011, IAVGN = 12V, ramp IAVGP voltage up	40	45	50	mV
		ILIM bits = 111, IAVGN = 12V, ramp IAVGP voltage up	62.5	68	73.5	mV
		ILIM bits = 111, IAVGN = 12V, ramp IAVGP voltage up, T_J = 25°C	-5%	68	+5%	mV
IPWM input high threshold	V_{H_IPWM}				1.2	V
IPWM input low threshold	V_{L_IPWM}		0.4			V
IPWM to AVDD internal pull-up resistor	R_{IPWM}			1		MΩ
Average current limit dimming	$I_{AV_DIMMING}$	IPWM duty = 48%, 20kHz signal, ILIM bits = 111, measure load current limit, T_J = 25°C	33	37	41	mV
		IPWM duty = 71.5%, 20kHz signal, ILIM bits = 111, measure load current limit, T_J = 25°C	48	52.5	57	mV
CSP and CSN bias current	I_{CS_BIAS}	V_{CSP} = V_{CSN} = 0V		70		µA
IAVGP and IAVGN bias current	I_{AV_BIAS}	IAVGN = 5V		55		µA
		IAVGN = 20V				
		IAVGP - IAVGN = 40mV				
Switching Frequency						
Switching frequency	f_{SW}	f_{SW} bits = 10, V_{OUT} = 5V	300	400	500	kHz
		f_{SW} bits = 00, V_{OUT} = 5V	140	200	260	kHz
Frequency spread span (8)	f_{SS}	Dither bit = 1		±6%		f_{SW}
Dither modulation frequency (8)	$f_{MODULATION}$	Dither bit = 1		2		kHz
Gate Driver						
Gate source current capability (8)	I_{HG_SO}	V_{CC} = 7.2V, 4.7nF load		0.7		A
	I_{LG_SO}			0.85		A
Gate sink current capability (8)	I_{HG_SI}	V_{CC} = 7.2V, 4.7nF load		1.6		A
	I_{LG_SI}			2		A
Low-side gate output high voltage	V_{LS_HIGN}		V_{CC} - 0.05			V
Low-side gate output low voltage	V_{LS_LOW}				0.05	V
High-side gate output high voltage	V_{HS_HIGN}		$V_{BST\ SW}$ - 0.05			V
High-side gate output low voltage	V_{HS_LOW}				0.05	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Dead-time between high-side gate and low-side gate (8)	t_{DEAD}			30		ns
OVP Protection						
FB feedback OVP trigger threshold	V_{OVP_RISING}		119%	127%	135%	V_{REF}
FB feedback OVP recovery threshold	$V_{OVP_FALLING}$		104%	111%	118%	V_{REF}
Power Good						
Power good upper trip threshold	$PG_{H_FALLING}$	PNG bit sets to 1, and INT pin pulls low	110%	117%	124%	V_{REF}
	PG_{H_RISING}	PNG bit resets to 0, and INT pin rises to high	101%	106.5%	112%	V_{REF}
Power good upper trip threshold	$PG_{L_FALLING}$	PNG bit sets to 1, and INT pin pulls low	80%	85.5%	91%	V_{REF}
	PG_{L_RISING}	PNG bit resets to 0, and INT pin rises to high	85%	91%	97%	V_{REF}
Power-good delay (INT pin response to PNG event)	PG_{DELAY}	Low to high		10		µs
		VOUT UV, high to low		2		µs
		VOUT OV, high to low		6.5		µs
INT pin sink current capability	I_{SINK_INT}	Sink 4mA		0.1	0.4	V
INT pin leakage current	I_{LKG_INT}	V_{INT} = 5V			1	µA
I²C Interface						
Input logic low voltage	V_{LI}	SCL, SDA			0.8	V
Input logic high voltage	V_{HI}	SCL, SDA	2			V
Logic input current		SCL, SDA, 5V	-1		+1	µA
Open-drain output logic low voltage	V_{LO}	SDA, sink 4mA			0.4	V
ADDR Pin Setting Threshold						
Setting voltage level 1	ADDR1	Set I²C address 60H			0.23	AVDD
Setting voltage level 2	ADDR2	Set I²C address 62H	0.27		0.47	AVDD
Setting voltage level 3	ADDR3	Set I²C address 63H	0.51		0.68	AVDD
Setting voltage level 4	ADDR4	Set I²C address 66H	0.74			AVDD
ADDR to GND internal pull-down resistor	R_{ADDR}			2		MΩ
Thermal Protection						
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD-HYS}			25		°C

Note:

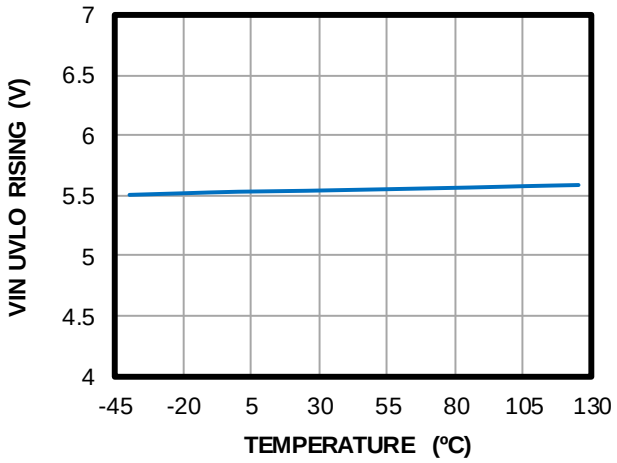
8) Guaranteed by characterization; not tested in production.

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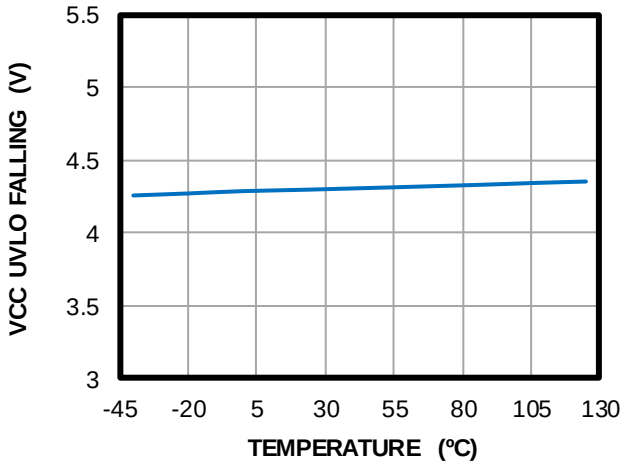
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

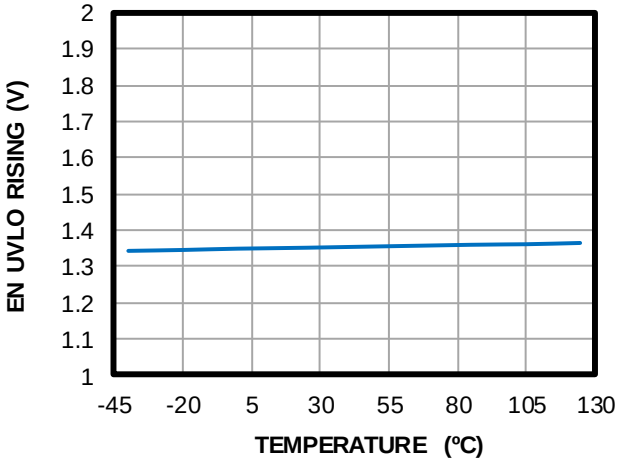
VIN UVLO Rising vs. Temperature



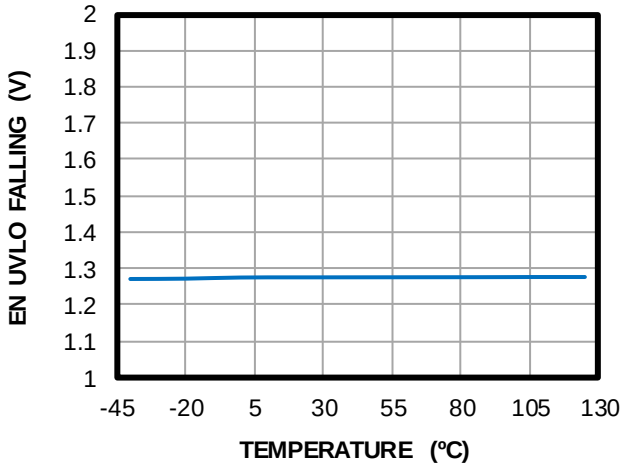
VCC UVLO Falling vs. Temperature



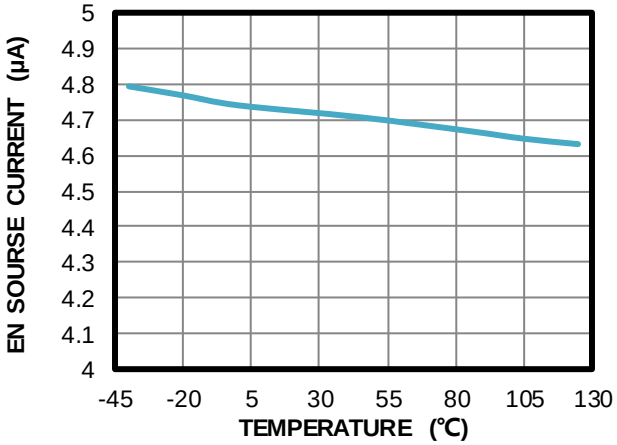
EN UVLO Rising vs. Temperature



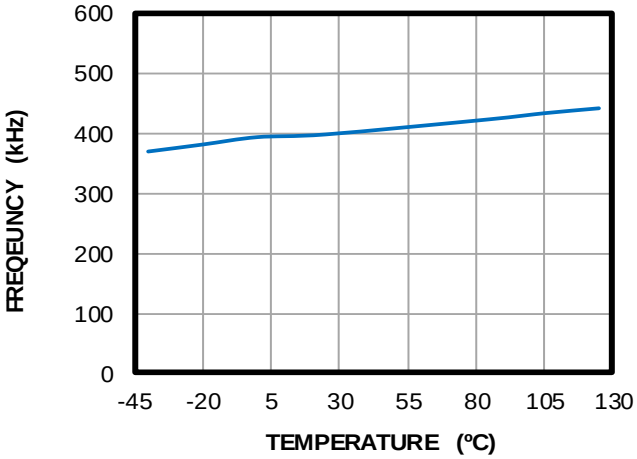
EN UVLO Falling vs. Temperature



EN Source Current vs. Temperature



Frequency vs. Temperature

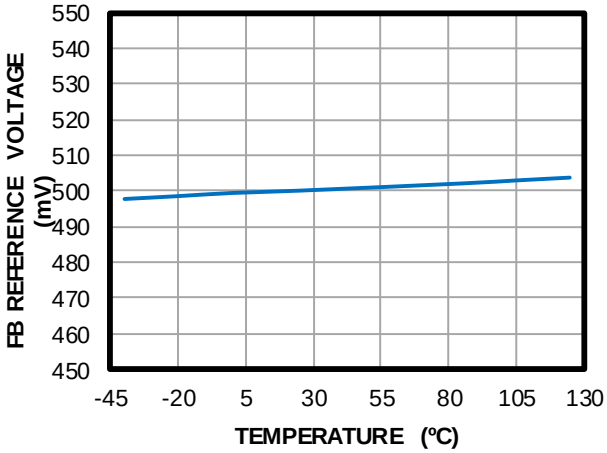


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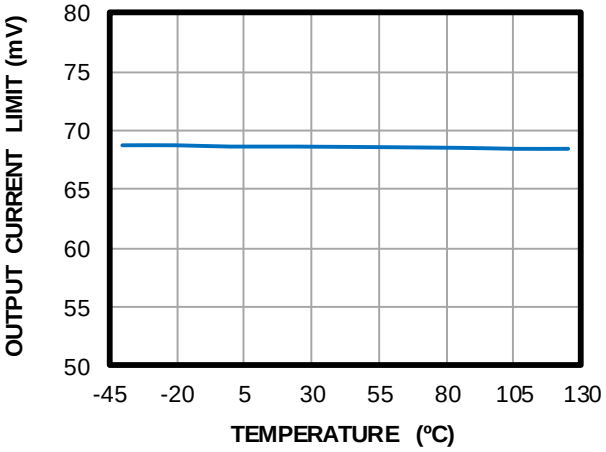
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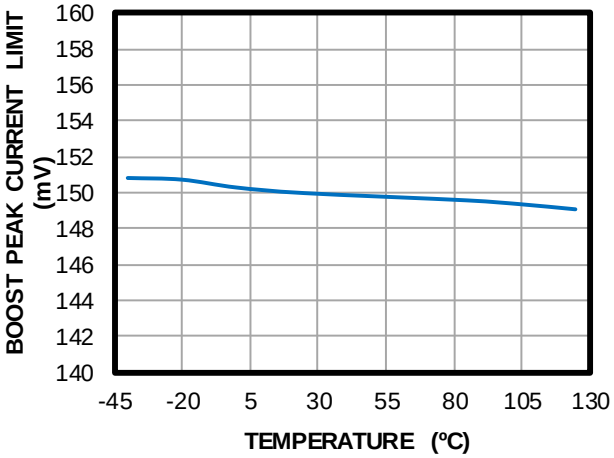
FB Reference Voltage vs. Temperature



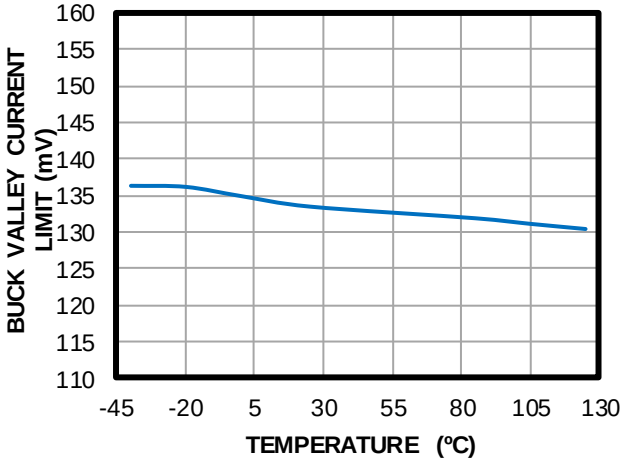
Output Current Limit vs. Temperature, I_{LIM} = 111b



Boost Peak Current Limit vs. Temperature, I_{LIM} = 111b

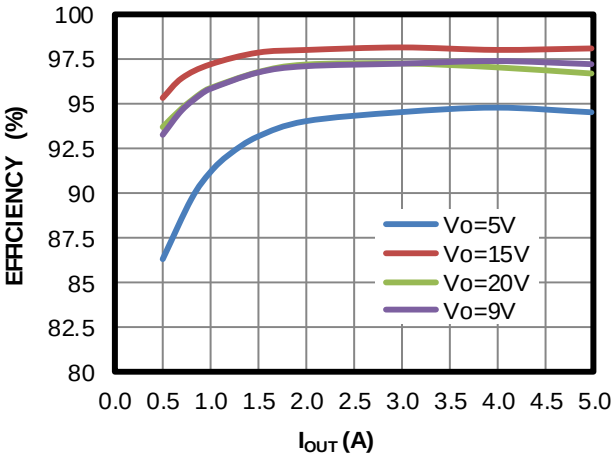


Buck Valley Current Limit vs. Temperature, I_{LIM} = 111b



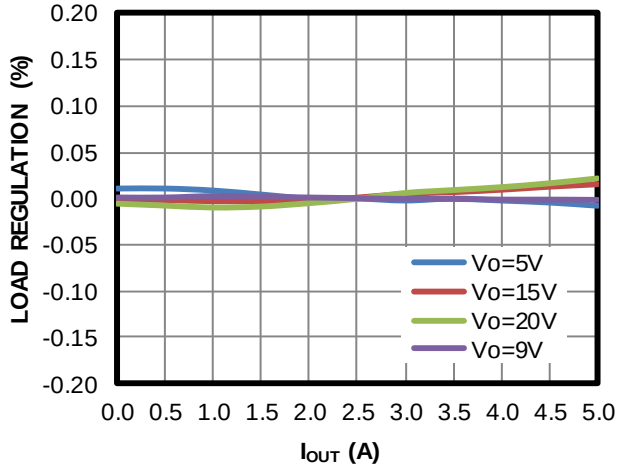
Efficiency vs. Load

V_{IN} = 12V



Load Regulation

V_{IN} = 12V

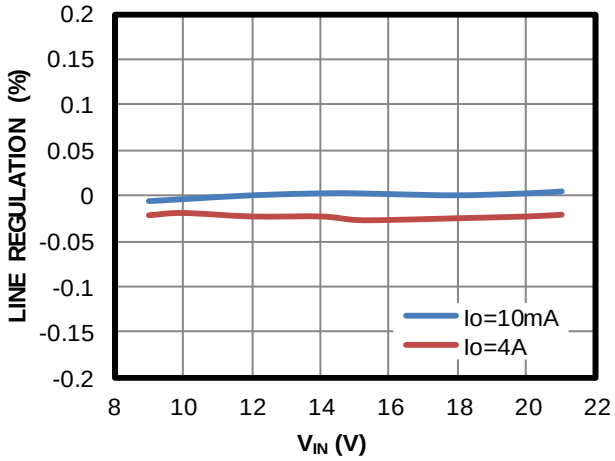


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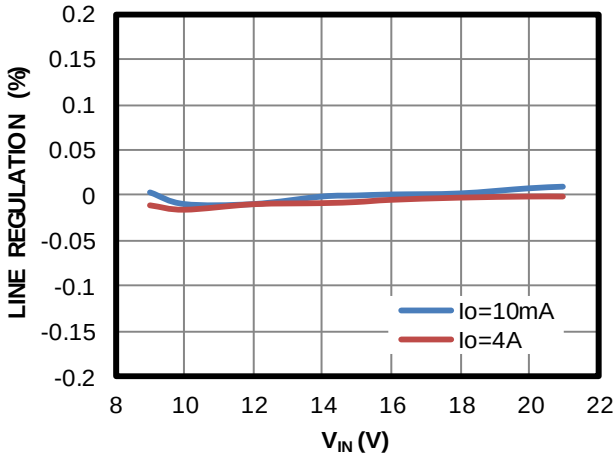
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

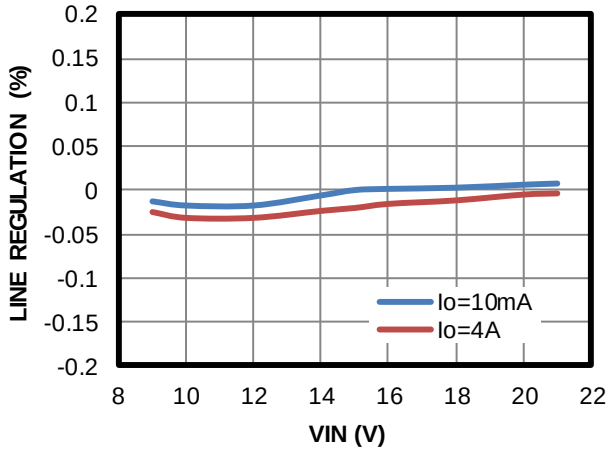
Line Regulation
V_{OUT} = 5V



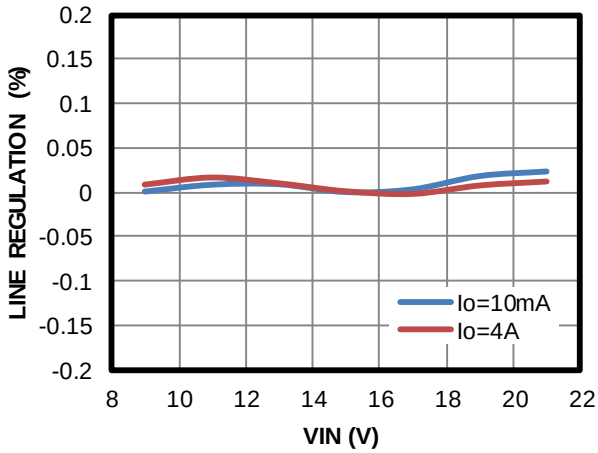
Line Regulation
V_{OUT} = 9V



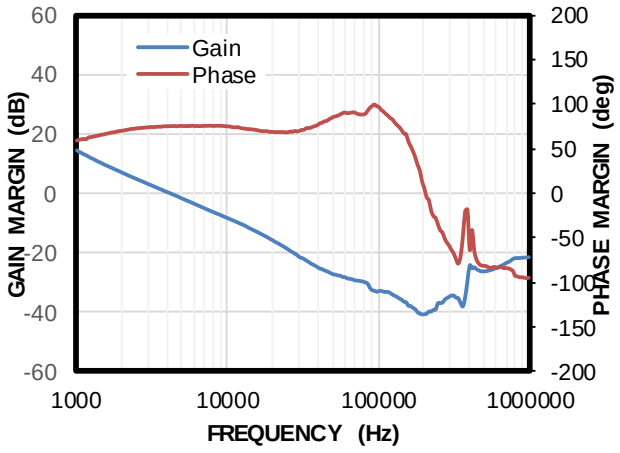
Line Regulation
V_{OUT} = 15V



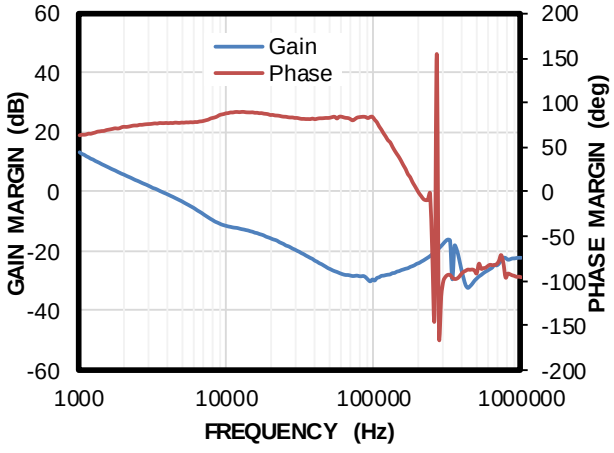
Line Regulation
V_{OUT} = 20V



Bode Plot
V_{OUT} = 5V, I_{OUT} = 5A, BW = 2.82kHz,
PM = 75deg, based on Figure 15 circuitry



Bode Plot
V_{OUT} = 20V, I_{OUT} = 5A, BW = 2kHz,
PM = 70deg, based on Figure 15 circuitry



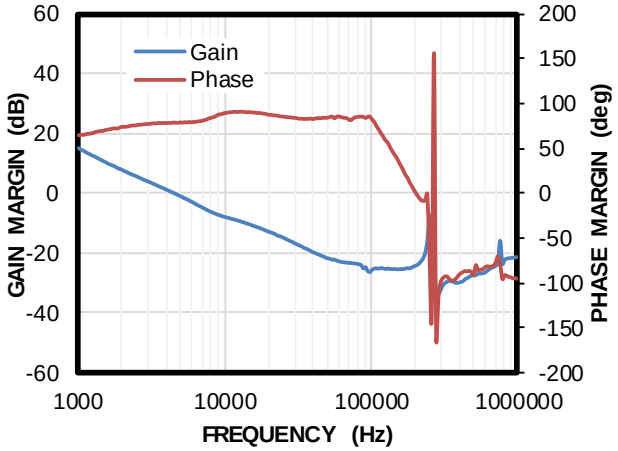
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

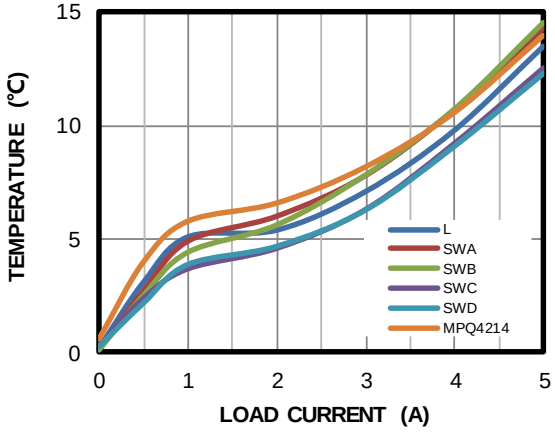
Bode Plot

V_{OUT} = 12V, I_{OUT} = 5A, BW = 2.74kHz,
PM = 78.5deg, based on Figure 15 circuitry



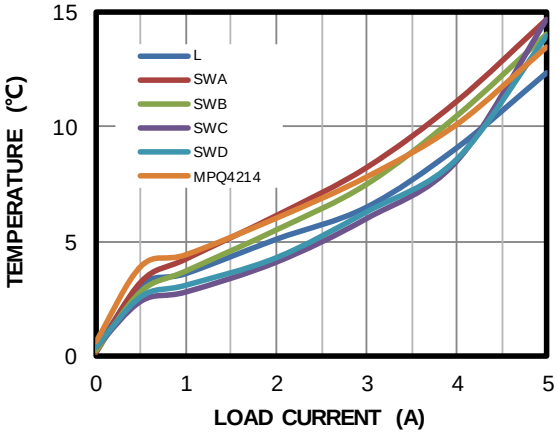
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 400kHz,
based on EVQ4214-U-00A



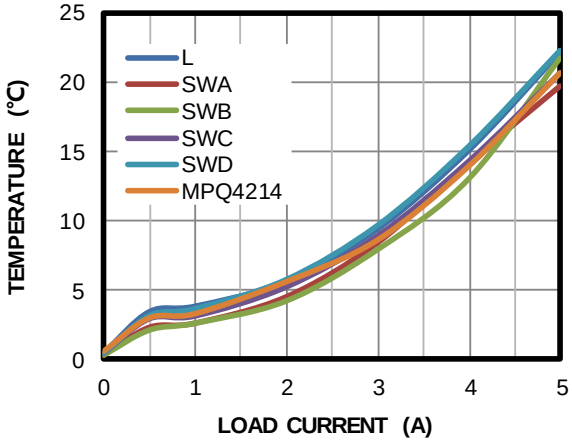
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 9V, f_{SW} = 400kHz,
based on EVQ4214-U-00A



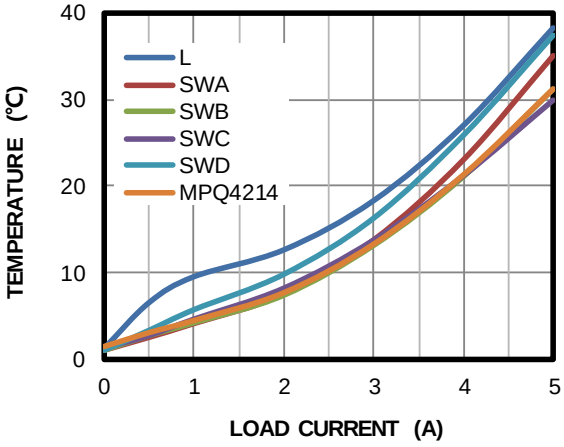
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 15V, f_{SW} = 400kHz,
based on EVQ4214-U-00A



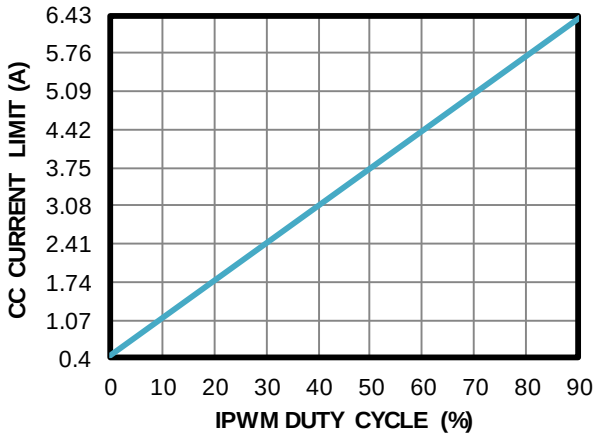
Case Temperature Rise

V_{IN} = 12V, V_{OUT} = 20V, f_{SW} = 400kHz,
based on EVQ4214-U-00A



CC Current limit vs. IPWM Duty Cycle

ILIM = 111, R_{SENSE} = 10mΩ

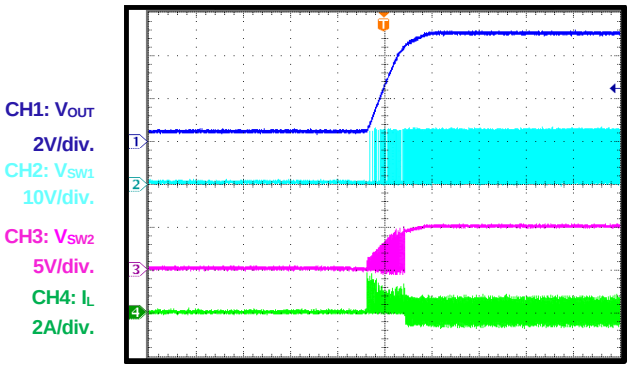


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

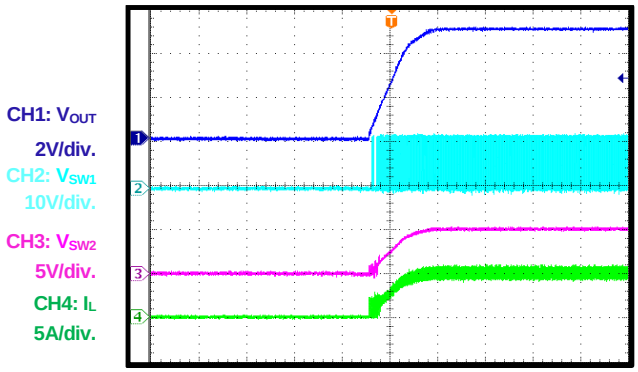
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

ENPWR Bit Enable through I²C Command, Load = 0A



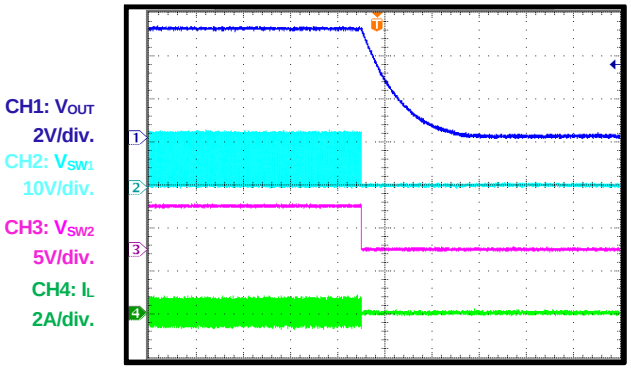
4ms/div.

ENPWR Bit Enable through I²C Command, Load = 5A



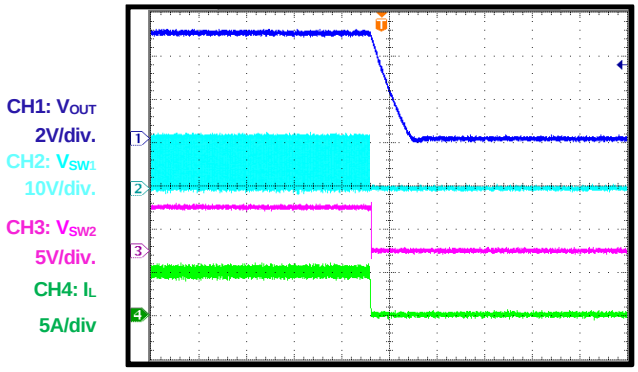
4ms/div.

ENPWR Bit Disable through I²C Command, Load = 0A



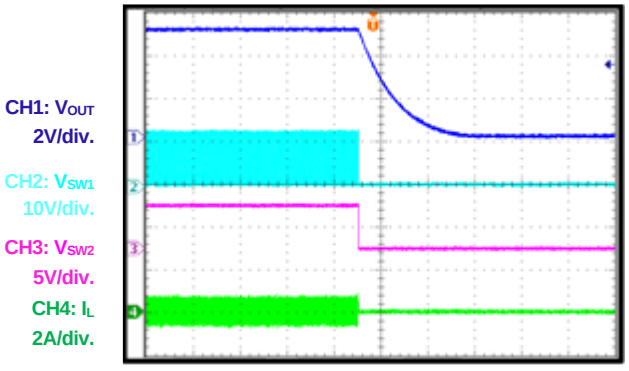
10ms/div.

ENPWR Bit Disable through I²C Command, Load = 5A



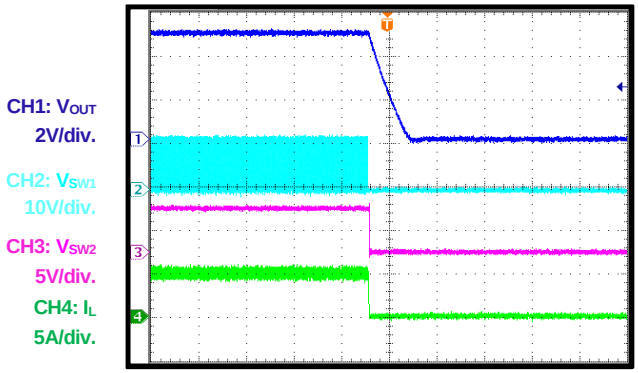
200µs/div.

EN Pin Disable, Load = 10mA



10ms/div.

EN Pin Disable, Load = 5A



200µs/div.

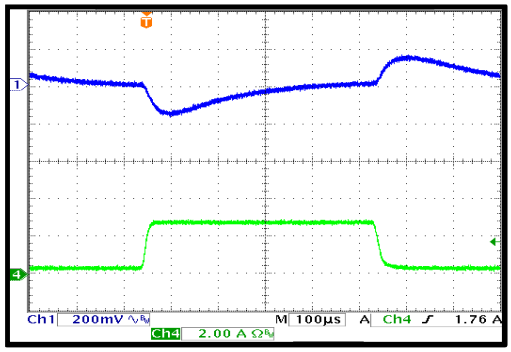
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

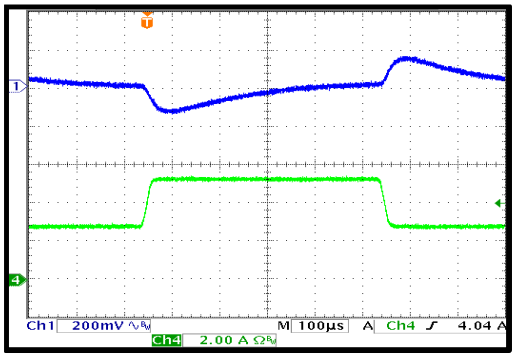
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A to 2.5A, 150mA/µs



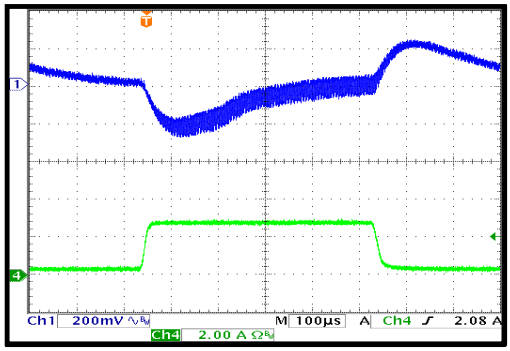
Load Transient

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.5A to 5A, 150mA/µs



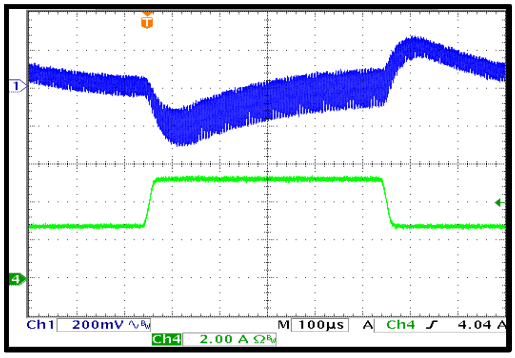
Load Transient

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A to 2.5A, 150mA/µs



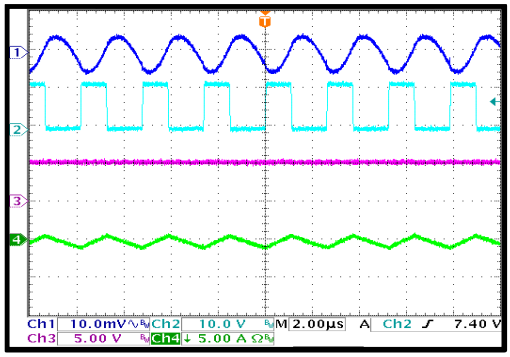
Load Transient

V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 2.5A to 5A, 150mA/µs



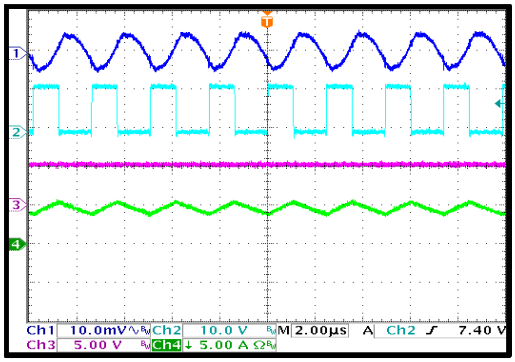
Steady State

V_{OUT} = 5V, I_{OUT} = 0A



Steady State

V_{OUT} = 5V, I_{OUT} = 5A



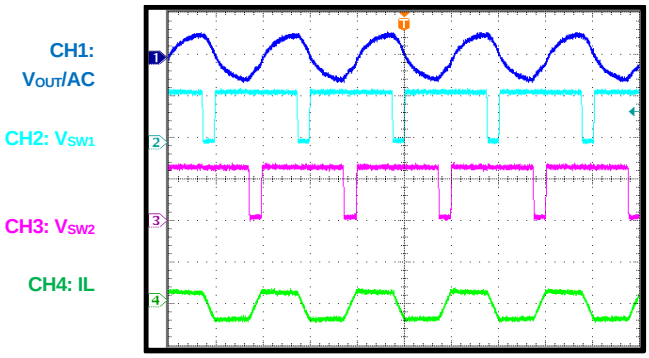
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

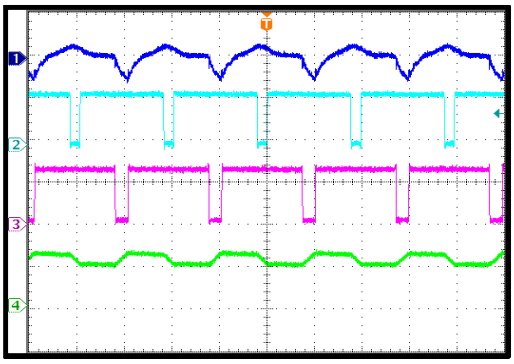
Steady State

V_{OUT} = 12V, I_{OUT} = 0A



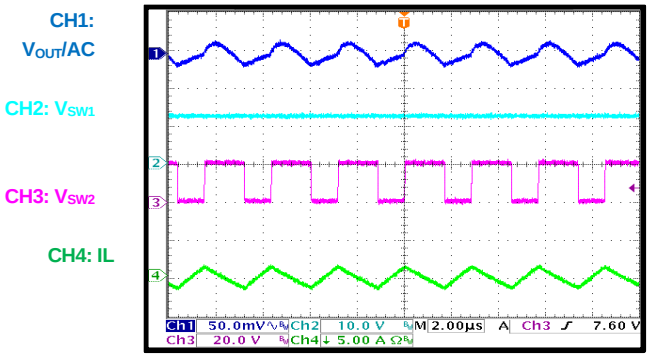
Steady State

V_{OUT} = 12V, I_{OUT} = 5A



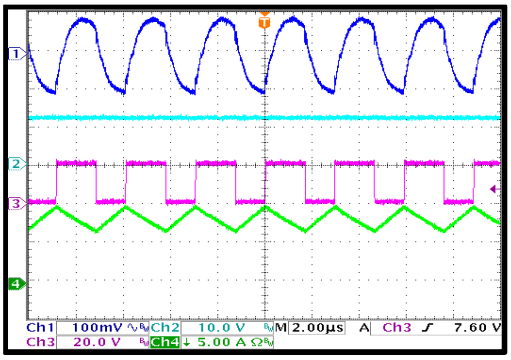
Steady State

V_{OUT} = 20V, I_{OUT} = 0A



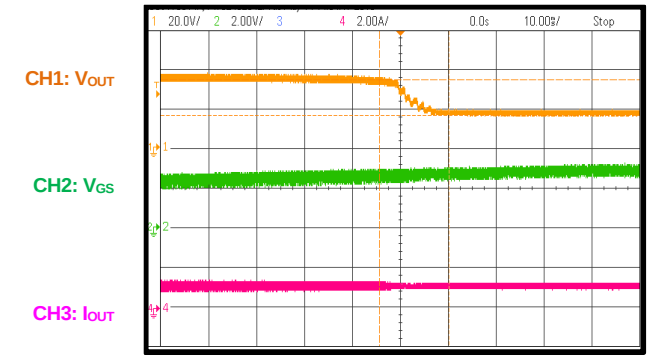
Steady State

V_{OUT} = 20V, I_{OUT} = 5A



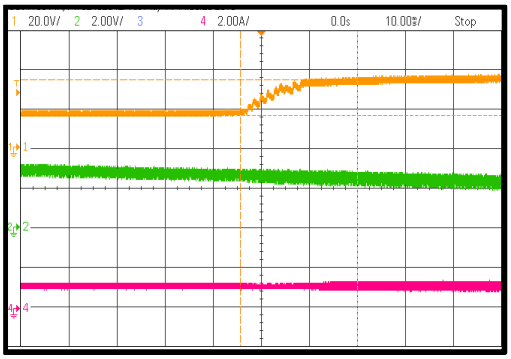
LED Transient

V_{IN} = 12V, short half of LED string, CC current limit = 1.2A



LED Transient

V_{IN} = 12V, LED switches from half to full string, CC current limit = 1.2A



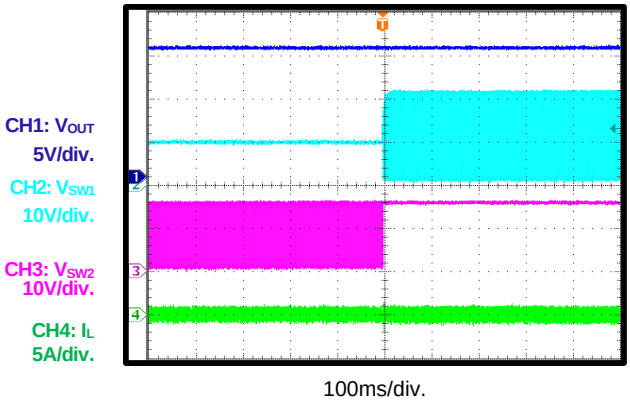
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

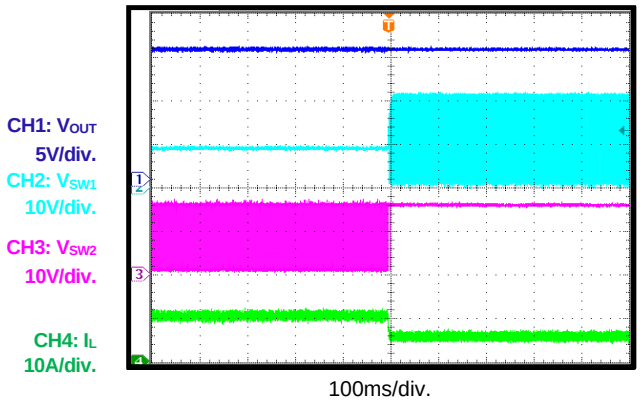
Input Voltage Transient

V_{IN} = 9V to 20V, V_{OUT} = 15V, load = 0A



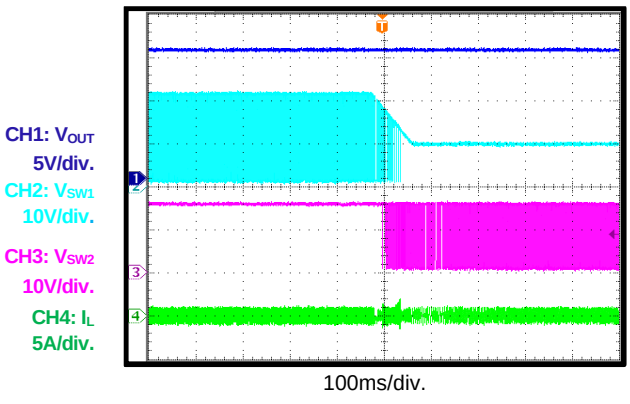
Input Voltage Transient

V_{IN} = 9V to 20V, V_{OUT} = 15V, load = 5A



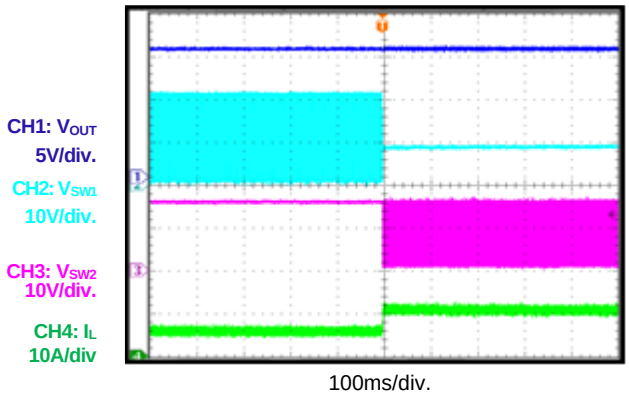
Input Voltage Transient

V_{IN} = 20V to 9V, V_{OUT} = 15V, load = 0A



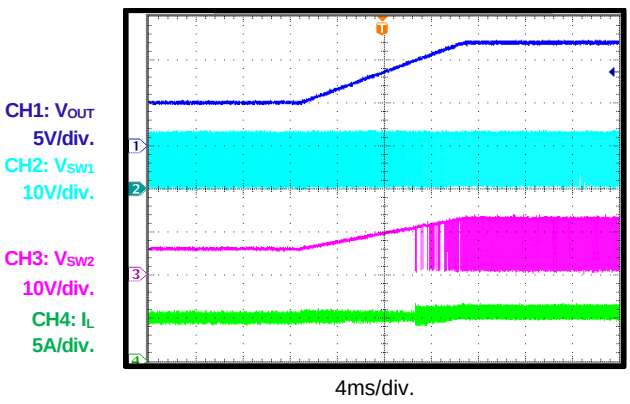
Input Voltage Transient

V_{IN} = 20V to 9V, V_{OUT} = 15V, load = 5A



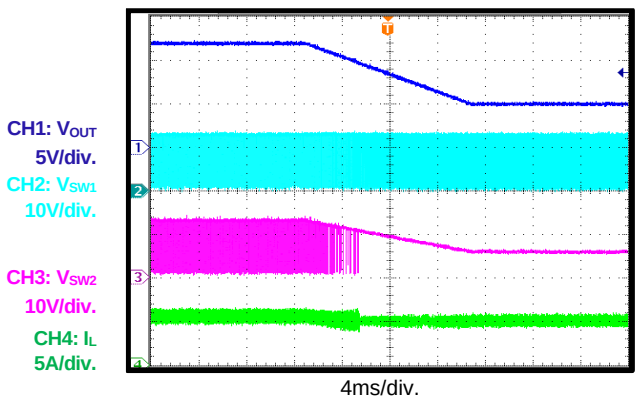
Output Voltage Transient

V_{OUT} = 5V to 12V, I_{OUT} = 5A



Output Voltage Transient

V_{OUT} = 12V to 5V, load = 5A



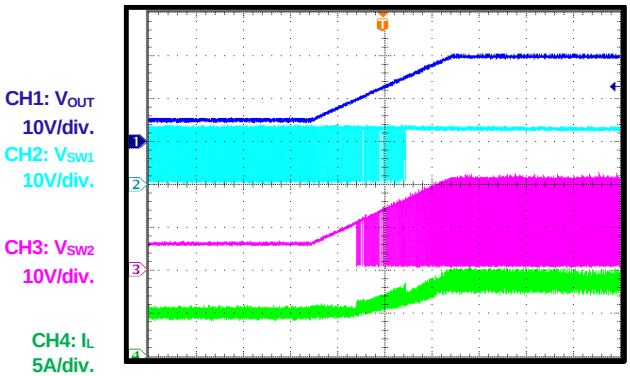
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

Output Voltage Transient

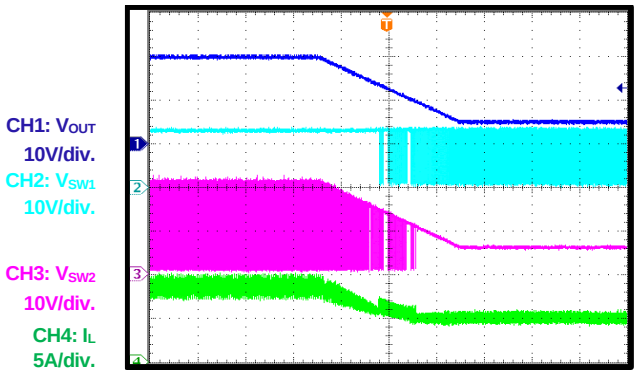
V_{OUT} = 5V to 20V, load = 5A



10ms/div.

Output Voltage Transient

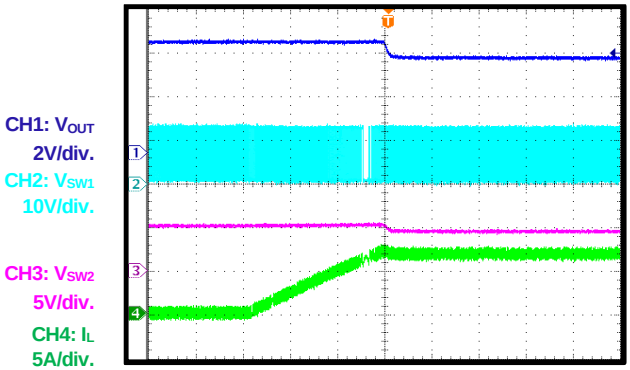
V_{OUT} = 20V to 5V, load = 5A



10ms/div.

OCP Entry

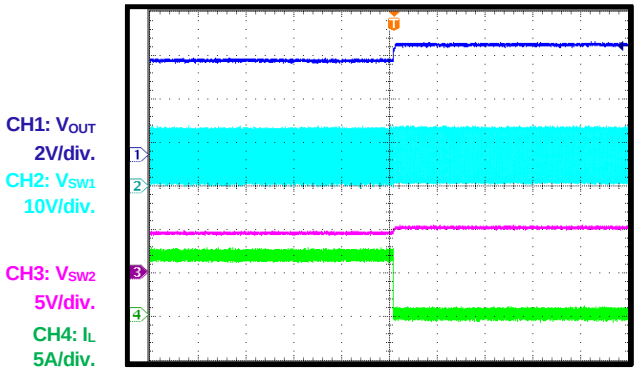
Ramp up load current slowly



40ms/div.

OCP Recovery

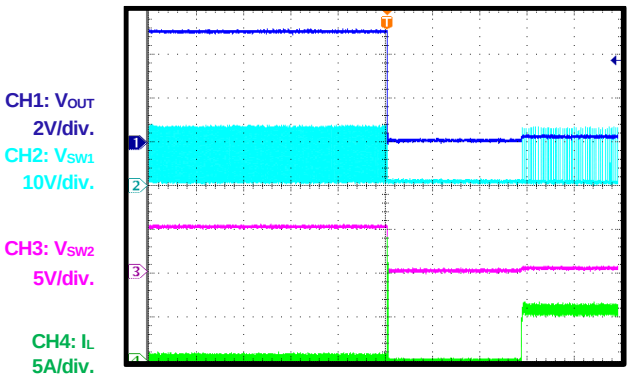
Remove load current



40ms/div.

SCP Entry

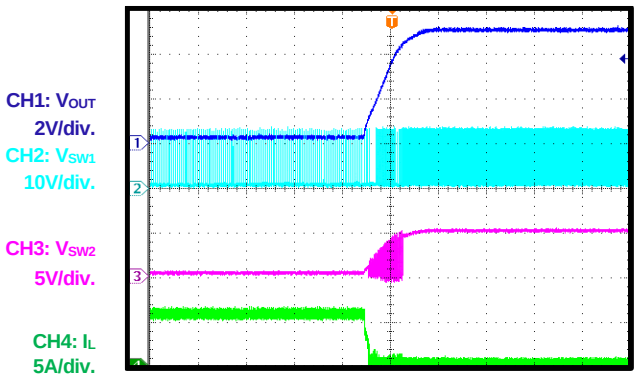
Short output to ground, R_{CC} = 10mΩ



20ms/div.

SCP Recovery

Remove short circuit, R_{CC} = 10mΩ



4ms/div.

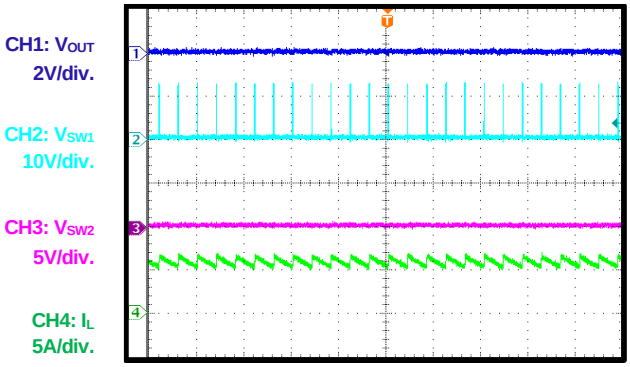
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

SCP Steady State

Short output to ground, R_{CC} = 10mΩ



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FUNCTIONAL BLOCK DIAGRAM

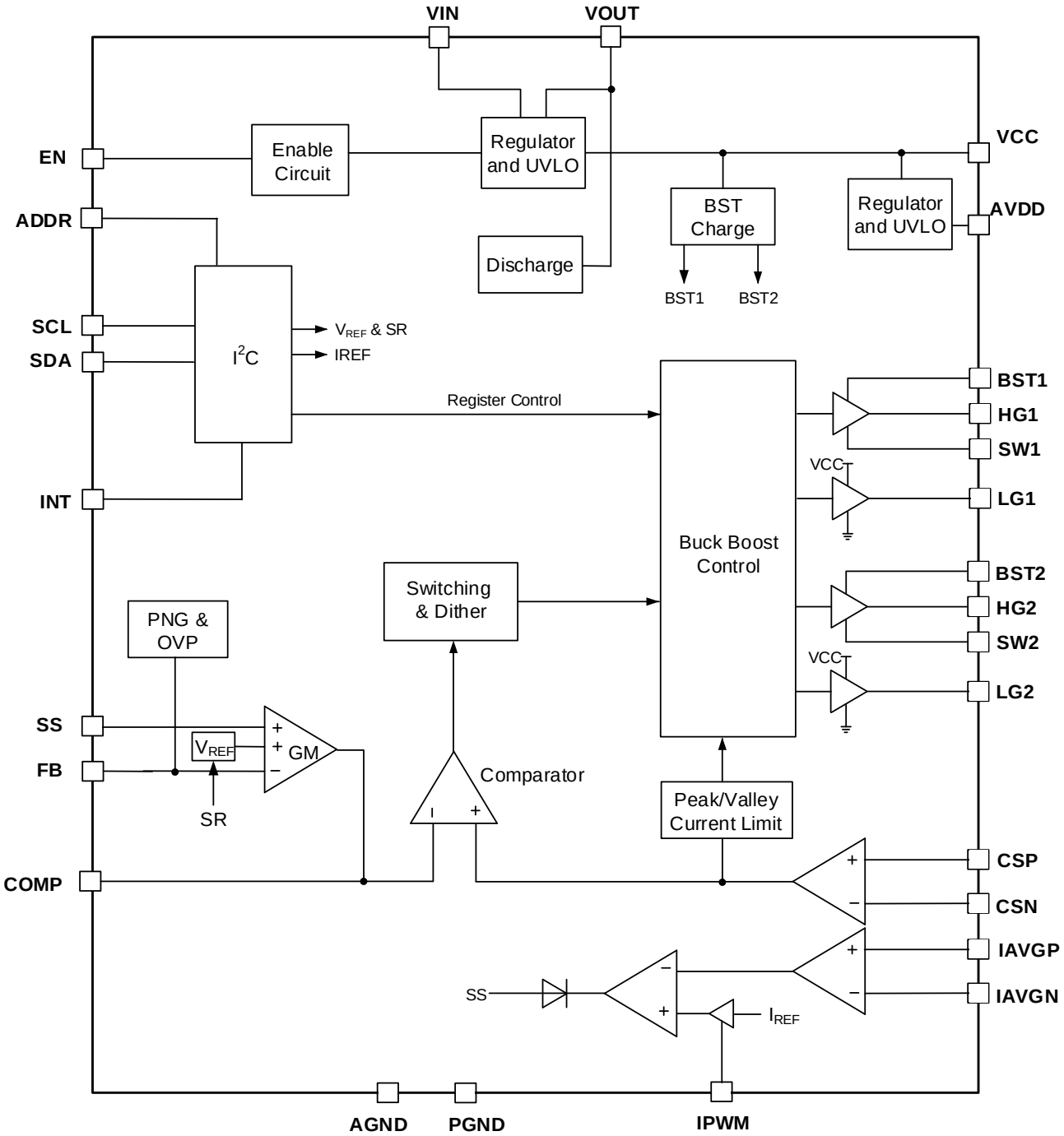


Figure 2: Functional Block Diagram

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OPERATION

The MPQ4214 is a four-switch, buck-boost controller. It works with fixed frequency in buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency over the full input range and smooth transient between different modes. Figure 2 shows the internal block diagram, and the sections below describe the device functions.

Buck-Boost Operation

The MPQ4214 can regulate the output above, equal to, or below the input voltage. Based on the one-inductor, four-switch power structure (see Figure 3), it operates in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 4).

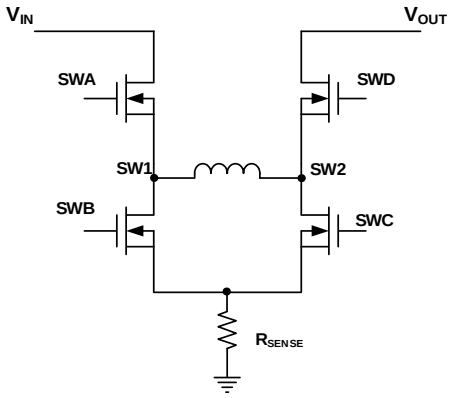


Figure 3: Buck-Boost Topology

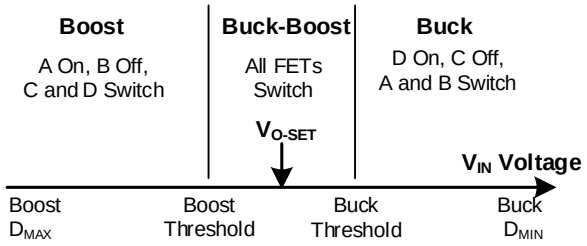


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} is significantly higher than the output voltage (V_{OUT}), the MPQ4214 works in buck mode. SWA and SWB switch for the buck regulation period, while SWC is off and SWD remains on to conduct the inductor current.

In each cycle of buck mode, SWA turns on first when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). After SWA turns off, SWB turns on to conduct the inductor current until it triggers the COMP control signal. By repeating operation this way, the converter regulates the output voltage.

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly below V_{OUT}, the MPQ4214 works in boost mode. In boost mode, SWC and SWD switch for the boost regulation period, while SWB is off and SWA remains on to conduct the inductor current.

In each cycle of boost mode, SWC turns on to conduct the inductor current. When the inductor current rises and triggers the control signal on the COMP pin, SWC turns off and SWD turns on for the current freewheel. Then SWC turns on and off repeatedly to regulate V_{OUT} in boost mode.

Buck-Boost Mode (V_{IN} ≈ V_{OUT})

If V_{IN} is close to V_{OUT}, the converter is unable to provide enough energy to the load in buck mode due to SWA's minimum off time, or the converter supplies more power to the load in boost mode due to SWC's minimum on time, the MPQ4214 adopts buck-boost control to regulate the output.

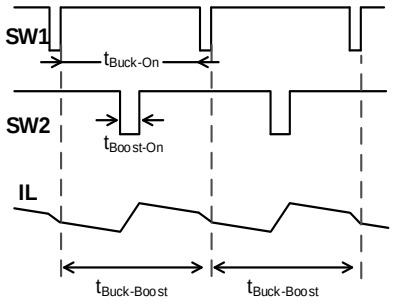


Figure 5: Buck-Boost Waveform

If V_{IN} is close to V_{OUT}, buck-boost mode engages, and one boost switching period is inserted into each buck switching period. The MOSFET turn-on sequence is then SWA & SWD → SWA & SWC → SWA & SWD → SWB & SWD. This way, the inductor current can meet the COMP voltage requirement, and supply enough current to the output.

Power Supply

The MPQ4214 internal circuit is powered by 5.2V AVDD, while the gate drivers are powered by 7.2V VCC. VCC is regulated from V_{IN} and V_{OUT}, while AVDD is powered by VCC.

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When V_{IN} power is supplied and EN is high, the MPQ4214 tries to regulate V_{CC} at 7.2V. At the same time, AVDD is regulated to 5.2V. When AVDD rises above the UVLO voltage, the device starts switching and regulates V_{OUT} with soft-start control. If V_{IN} and V_{OUT} are both above 8.8V, the MPQ4214 powers V_{CC} from the lower voltage source to reduce power loss. Otherwise, the device powers V_{CC} from the higher voltage power source of V_{IN} and V_{OUT} to get enough V_{CC} voltage. VCC and BST have separate UVLO thresholds, which keep the gate signal off. Both VCC and BST should have enough voltage to enable switching, except for the AVDD UVLO.

The MPQ4214 can start working in a 6V to 40V input voltage range. When VCC is powered from VOUT after start-up, the MPQ4214 can work until V_{IN} drops below 5V.

When the MPQ4214 is powered off by AVDD_UVLO or the EN signal, the I²C interface cannot respond to the host, and COMP is immediately pulled low. The VCC, AVDD, and BST voltages drop slowly with leakage, but all logic is off.

Start-Up

When the MPQ4214 is enabled, it starts switching with soft-start (SS) control. The SS circuit charges current to the SS pin and ramps the SS voltage up from 0V. It then feeds to the error amplifier to control output voltage. After the SS signal rises to the programmed reference voltage (set by the VREF bits), soft start completes and closed-loop regulation starts. The SS voltage rises and clamps at 0.6V above V_{REF} in steady state, unless a protection is triggered.

Normally the MPQ4214 starts with buck switching after start-up because V_{OUT} is much lower than V_{IN}. If there is some bias voltage on VOUT, the part will not switch until the SS signal rises above V_{FB}, which is proportional to the VOUT bias voltage. During SS, the IC works in auto-PFM mode. OVP and hiccup OCP do not work during the SS period.

Enable (EN) and Programmable UVLO

The EN pin enables and disables the MPQ4214. When applying a voltage greater than the EN high threshold (>1.1V), the part starts up some of the internal circuits (micro-power mode). If the EN voltage exceeds the turn-on threshold (1.35V), the MPQ4214 enables all functions and starts switching operation. Switching operation is disabled when the EN voltage falls below its lower threshold (<1.28V).

If V_{EN} < 0.4V, the MPQ4214 completely shuts down. After shutdown, the part sinks a small amount of current from the input power (typically <1μA). EN is compatible with voltages up to 40V. For automatic start-up, connect EN directly to VIN. During EN shutdown, the I²C resets to its default value after a 200ms discharge time.

The MPQ4214 features a programmable UVLO hysteresis. When powering up, EN sources a 4.7μA current out of the EN pin once the EN voltage exceeds 1.35V (see Figure 6). VIN must decrease to overcome the current source and stop switching after the IC starts. The VIN start and stop switching thresholds are determined with Equation (1) and Equation (2), respectively:

$$V_{IN_ON}(V)=V_{EN_ON}(V)\times(1+\frac{R_{TOP}}{R_{BOT}})=5.95V \quad (1)$$

$$V_{IN_OFF}(V)=V_{EN_OFF}(V)\times(1+\frac{R_{TOP}}{R_{BOT}})-4.7\mu A\times R_{TOP}(k\Omega)\div 1000=5.16V \quad (2)$$

Where V_{EN_ON} is typically about 1.35V, and V_{EN_OFF} is about 1.28V.

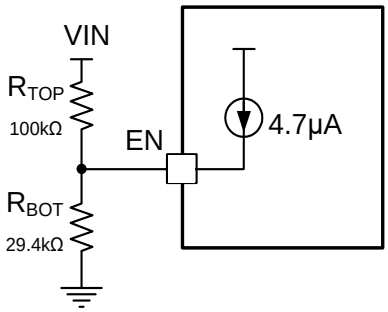


Figure 6: V_{IN} UVLO Program

FCCM Mode

The MPQ4214 works in forced continuous conduction mode (FCCM). The buck on time and boost off time are determined by the internal circuit to get a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current drops and the inductor current may go negative from V_{OUT} to V_{IN} during the SWD on period. This forces the inductor current to work in continuous mode with a fixed frequency, producing a low V_{OUT} ripple.

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Switching Current Limit

The MPQ4214 senses the LS-FET current in the loop control. It provides the valley current limit in buck mode and peak current limit in boost mode in each cycle-by-cycle switching. In buck mode, the next period will not start before IL drops to the valley current limit, so it may fold back the frequency when the valley current limit is triggered. The switching current limit can be programmed with an external sense resistor. The SWB & SWC current signal is blanked for about 180ns internally to enhance noise rejection.

In an over-current condition, the MPQ4214 runs in cycle-by-cycle current limit. It may run into hiccup protection or latch-off protection based on the OCP_MODE bit's setting. In hiccup mode, the IC turns off once V_{FB} drops below 60% of V_{REF}, and triggers the switching current limit after the SS period. It recovers after a fixed off time, which is programmed by the SS capacitor discharge period. In latch-off mode, the IC turns off if V_{FB} drops below 60% of V_{REF}, and triggers switching current limit after the SS period. It does not recover until a new power cycle is initiated. If hiccup and latch-off protection are disabled, the IC continues switching with cycle-by-cycle current limiting. Hiccup mode and the latch-off protection are masked during the SS period.

Average Current Limit

The IAVGP and IAVGN pins are used to sense the output current in the MPQ4214. The sense resistor can be connected to the VOUT line for average output current limit control. Once the sensed signal exceeds the current limit reference voltage, one internal EA pulls down the SS pin voltage. Finally, SS replaces V_{REF} to control COMP, and the inductor current is limited by COMP to transfer less energy to the output. SS regulates the output low until the average load current drops.

If the switching current is regulated by the average current limit and does not trigger the cycle-by-cycle current limit, the MPQ4214 will not allow hiccup mode or a latch-off protection even if the average current limit is triggered. This feature provides the most constant current charge possible.

The ILIM bits can provide 8 level current limits, and one external IPWM pin provides high-resolution current limit adjusting. The average output current limit is determined by the ILM bit setting, multiplied by the IPWM duty cycle.

When the ILIM bits = 111 and the current limit is programmed by the IPWM pin, the current limit threshold can be calculated with Equation (3):

$$OCP_LIMIT(mV) = 65.8mV \times Duty + 4.49mV \quad (3)$$

Where OCP_LIMIT is the average load current limit programmed by the IPWM pin when the ILIM bits = 111, and "Duty" is the IPWM pin input signal duty cycle (varies from 0 to 0.9).

For example, if the IPWM signal duty cycle is 48%, the final average output current limit is about 36mV. The IPWM signal frequency can be between 5kHz and 100kHz. A 20kHz frequency signal is typically recommended.

Overload and Short-Circuit Protection

When an overload or short circuit occurs, the MPQ4214 limits the output current with average current limit loop regulation. If the average current limit loop is disabled, the cycle-by-cycle switching current limit works.

In a cycle-by-cycle current limit condition, if the IC works in boost mode, the SWC peak current is limited. If the IC works in buck mode due to a high V_{IN} or V_{OUT} drop in overload, the MPQ4214 keeps SWB on until IL drops to the buck valley current limit level; then the next cycle can kick in. This way, the inductor current can be controlled in all work modes.

Output Voltage Regulation

The MPQ4214 regulates V_{OUT} with the feedback on the FB pin. V_{FB} is compared to the internal reference, which is from 300mV to 2.047V based on the VREF register bit's setting (fixed at 1.2V VREF in the MPQ4214GU-12). The EA output on the COMP pin controls the inductor current to supply the output voltage.

Switching Frequency and Dither Function

The MPQ4214 programs the switching frequency with a 2-bit FSW register. The frequency is selectable at 200kHz, 300kHz, 400kHz, and 600kHz. Typically, a 400kHz switching frequency is recommended.

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The MPQ4214 has a frequency spread spectrum function (see Figure 7). Set the Dither bit = 1 (0x02, D[4]) to enable this function. Set the Dither bit = 0 to disable the function. The purpose of the spread spectrum is to minimize the peak emissions at certain frequencies.

The MPQ4214 uses a 2kHz triangle wave to modulate the internal oscillator. The frequency span of the spread spectrum operation is ±6%.

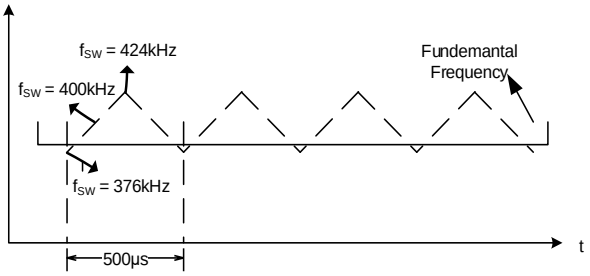


Figure 7: Frequency Spread Spectrum

The MPQ4214 frequency spread spectrum can be enabled for a 200kHz, 300kHz, 400kHz, or 600kHz switching frequency.

Gate Driver and BST Power

The MPQ4214 provides four N-channel MOSFET gate drivers for the H-bridge MOSFETs (see Figure 2). Each driver is capable of sourcing and sinking current. In buck operation, LG1 and HG1 switch while HG2 remains on. In boost operation, LG2 and HG2 switch while HG1 remains on. LG1 and LG2 are powered by VCC power, while HG1 and HG2 are powered by BST1 and BST2 power.

Capacitors from BST1 to SW1 and from BST2 to SW2 are necessary to supply the power, which is powered by an internal diode from VCC or can charge each other.

Over-Voltage Protection

The MPQ4214 monitors the FB pin. If the feedback voltage is 27% above reference voltage and the OVP_MODE bits = 01, the IC discharges the V_{OUT} capacitor through one internal discharge resistor. It stops discharging when the FB voltage drops to 111% of the regulation voltage. If the OVP_MODE bits = 00, the IC will not stop switching even if V_{FB} is above the OVP threshold. If the OVP_MODE bits = 10, the IC latches off when V_{OUT} rises to 127% of the reference voltage.

Interrupt Pin

The MPQ4214 has one interrupt pin for the following fault events: OCP, OVP, and OTP reporting.

When the switching peak cycle-by-cycle current limit (OCP), output over-voltage (FB OVP), or over-temperature protection (OTP) is triggered, the corresponding register bit sets to 1. At the same time, INT pulls low to indicate an interrupt signal, depending on the related mask register setting.

INT is an open-drain output. When the MPQ4214 is disabled, INT is an open drain.

Slew-Rate Control and Output Discharge

The MPQ4214 sets the output voltage change slew rate via internal SR bits. V_{REF} changes 1mV in each step when V_{REF} is between 0.3V and 2.047V. The SR bits can set each step interval at 6.7µs, 14µs, 20µs, or 26µs. Based on the V_{REF} change speed, the V_{OUT} slew rate can be controlled. The MPQ4214GU-12 cannot program V_{REF} or the output change slew rate.

When VOUT ramps down from a high voltage to low voltage with light load, some internal or external discharge load is necessary to discharge C_{OUT} at the set slew rate. During voltage transient, the discharge function works when GO_BIT = 1, and the discharge function is disabled automatically after GO_BIT resets to 0 (which means the VREF change completes). If V_{OUT} has not been discharged to the goal voltage while the VREF change completes due to too large of an output capacitor, the OVP discharge function or DISCHG bit can be used to continue discharging C_{OUT}.

The output discharge function can be enabled by any of the conditions below:

1. GO_BIT = 1. Discharge works until after a 20ms delay once GO_BIT resets to 0.
2. DISCHG bit = 1.
3. OVP_MODE bits = 01, and V_{FB} is 127% greater than V_{REF}.
4. ENPWR bit powers off, plus a 200ms discharge.
5. EN pin is off, plus a 200ms discharge.

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6. If VIN_UVLO is triggered, but AVDD has residual voltage, the MPQ4214 discharges for 200ms. This discharge function may halt if the AVDD voltage drops.

Soft-Start Time Programmable (SS)

The MPQ4214 has a soft-start pin to program the soft-start time. The SS charge current is typically about 6μA. The soft-start time can be estimated with Equation (4):

$$t_{SS}(ms) = C_{SS}(nF) \times V_{REF}(V) \div I_{SS}(\mu A) \quad (4)$$

Typically, the I_{SS} charge current is about 6μA, C_{SS} = 47nF, and V_{REF} = 0.5V. The soft-start time is typically about 3.9ms.

Thermal Protection

The MPQ4214 integrates one temperature monitor circuit. If the junction temperature exceeds 150°C, the device shuts down. After the temperature drops below 125°C, it resumes operation.

I²C Interface

The MPQ4214 integrates one I²C interface. The device address is defined as 1100xxx, set by the ADDR pin resister divider from AVDD (see Figure 8).

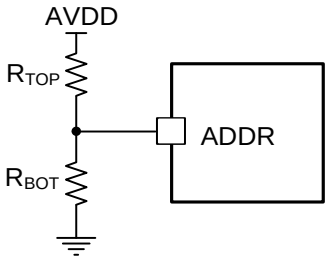


Figure 8: ADDR Set-Up

One R/W bit follows the 7-bit address, which is 0 for a write command and 1 for a read command. It works as a slave and supports both standard mode (100kbps) and fast mode (400kbps) communication. Table 1 details the I²C slave address selection. The ADDR pin setting also affects the default value of the ENPWR bit.

Table 1: I²C Slave Address

Device Address	R_{TOP}	R_{BOT}	ENPWR Default Value
60H	NS	0	1
62H	100kΩ	59kΩ	1
64H	68kΩ	100kΩ	0
66H	0	NS	0

I²C Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable (low) during the high period of this clock pulse.

Figure 9 shows the format that data transfers follow. A start command (S) sends a slave address. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command (P), generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

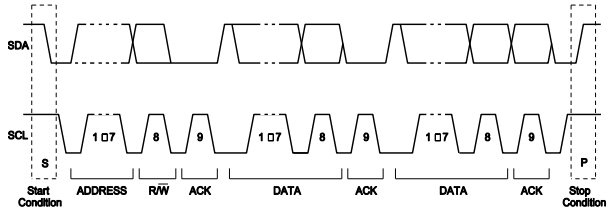
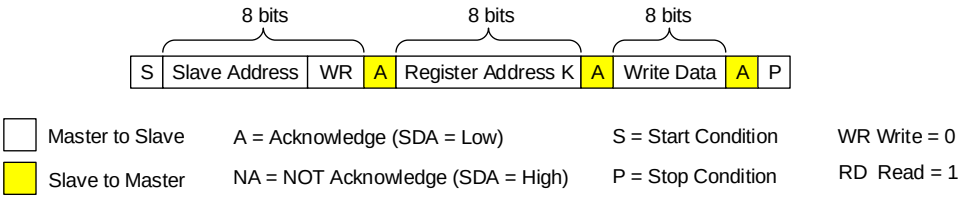


Figure 9: Complete Data Transfer

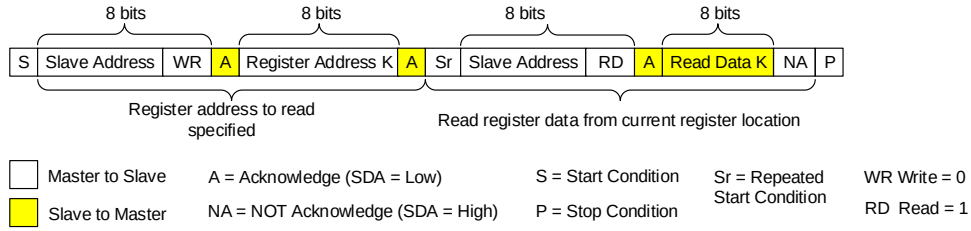
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The MPQ4214 includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPQ4214 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MPQ4214. The MPQ4214 performs an update on the falling edge of the LSB byte.

Figure 10 shows an example of the I²C read and write command.



(a) I²C Write Example



(b) I²C Read Example

Figure 10: I²C Read and Write

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APPLICATION INFORMATION

Output Voltage Setting

The default output voltage is set using a resistor divider to FB. The default reference voltage (V_{REF}) is 0.5V. The bottom resistor in the resistor divider is typically between 1kΩ and 100kΩ.

The top resistor in the feedback resistor divider is determined using Equation (5):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (5)$$

It is possible to use the I²C interface to select the FB V_{REF} and get another output voltage.

Inductor Selection

The inductor selection is based on the work mode. The inductance for buck mode is calculated with Equation (6):

$$L_{Buck} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Where ΔI_L is the peak-to-peak inductor ripple current, and is about 30% to 50% of the maximum load current.

In boost mode, the inductor selection is based on limiting ΔI_L to about 30% to 50% of the maximum input current. The target inductance for boost mode is calculated with Equation (7) and Equation (8):

$$L_{Boost} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (7)$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(max)})}{V_{IN} \times \eta} \quad (8)$$

Where $I_{LOAD(max)}$ is the maximum load current, ΔI_L is the peak-to-peak ripple current (about 30% to 50% of the maximum input current), and η is the efficiency.

Choosing a larger inductance reduces the ripple current, but also increases the size of the inductor and reduces the achievable bandwidth of the converter by moving the right half-plane zero to lower frequencies. The appropriate balance should be chosen based on the application requirements.

Input Capacitor Selection

In buck mode, the MPQ4214 has a discontinuous input current (boost mode is continuous), and requires a capacitor to supply the AC current while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance, and should be placed as close to VIN as possible. Capacitors with X5R or X7R ceramic dielectrics are recommended because of their stable temperature characteristics. The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The buck mode input ripple current can be estimated with Equation (9):

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition in buck mode occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (10):

$$I_{CIN_RMS} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

In buck mode, the input voltage ripple can be estimated with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (12)$$

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Output Capacitor Selection

In boost mode, the output current is discontinuous, so C_{OUT} must be capable of reducing the output voltage ripple.

A higher capacitance value may be required to lower the output ripple and transient response. Low-ESR capacitors, such as X5R or X7R ceramic capacitors, are recommended. If using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is independent of the ESR. The output voltage ripple is estimated with Equation (13):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} \quad (13)$$

Where V_{RIPPLE} is the output ripple voltage, and C_{OUT} is the capacitance of the output capacitor.

If using hybrid, polymer, or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output ripple is estimated using Equation (14):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (14)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

For a 100W USB PD application, one 330µF electrolytic capacitor and four 10µF ceramic capacitors are recommended.

Choose output capacitors to satisfy the output ripple and load transient requirements of the design. Capacitance derating should be taken into consideration when designing high-output voltage applications.

External MOSFET Selection

The MPQ4214 requires four external N-channel power MOSFETs. Figure 11 shows two for the top switches (switches A and D) and two for the bottom switches (switches B and C). In buck mode, SWA and SWB switch while SWD remains on. In boost mode, SWC and SWD switch while SWA remains on.

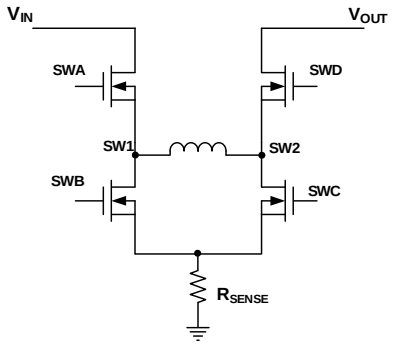


Figure 11: Buck-Boost Topology

The critical parameters of selecting a MOSFET are:

1. Maximum drain-to-source voltage ($V_{DS(MAX)}$)

   SWA and SWB need to withstand the maximum input voltage and the transient spikes at SW1 during switching. Therefore, it is recommended to select $V_{DS(MAX)}$ for SWA and SWB at 1.5 times the input voltage.

   SWC and SWD see output voltage and transient spikes at SW2 during switching. Therefore, it is recommended that SWC and SWD be ≥1.5 times the output voltage.

2. Maximum current ($I_{D(MAX)}$)
3. V_{TH}: The driver voltages of the MPQ4214 are supplied by VCC. The gate plateau voltages of the MOSFETs should be less than the minimum VCC voltage of the converter, otherwise the MOSFETs may not fully enhance during start-up or overload conditions.
4. On resistance ($R_{DS(ON)}$)
5. Total gate charge (Q_G)

   For the MPQ4214, all switches (Q_G) should be less than 50nC (at a 7.2V gate condition). If there are two MOSFETs in parallel, each MOSFET Q_G must be less than 25nC.

MOSFET SWA

When the MPQ4214 works in boost mode, SWA is on consistently. Its conduction power loss can be calculated with Equation (15):

$$P_{C_Loss(SWA)} = (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWA)} \quad (15)$$

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Assume that the MOSFET junction-to-ambient thermal resistance is 50°C/W (this is determined by the board power dissipation), and that the maximum acceptant temperature rise is 50°C. Therefore, the maximum power loss is 1W, calculated with Equation (16):

$$P_{C_Loss(SWA)} < 1W \quad (16)$$

Based on this equation, we can select the MOSFET R_{ON}.

When the MPQ4214 works in buck mode, the conduction and switching loss of SWA can be calculated with Equation (17) and Equation (18), respectively:

$$P_{C_Loss(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_o^2 \times R_{DSON(SWA)} \quad (17)$$

$$P_{SW_Loss(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{on} + t_{off}) \times f_{sw} \quad (18)$$

The switch on time (t_{on}) and the switch off time (t_{off}) are based on the MOSFET datasheet information (see Figure 12).

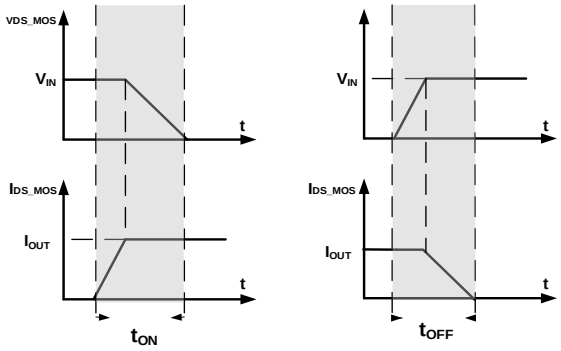


Figure 12: Switch On Time and Switch Off Time

MOSFET SWB

When the MPQ4214 works in buck mode, its conduction loss can be calculated with Equation (19):

$$P_{C_Loss(SWB)} = (1 - \frac{V_{OUT}}{V_{IN}}) \times I_o^2 \times R_{DSON(SWB)} \quad (19)$$

MOSFET SWC

When the MPQ4214 works in boost mode, SWB is always off. Its conduction loss in boost mode can be calculated with Equation (20):

$$P_{C_Loss(SWC)} = (1 - \frac{V_{IN}}{V_{OUT}}) \times (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWC)} \quad (20)$$

When the MPQ4214 works in boost mode, the SWC switching loss can be calculated with Equation (21):

$$P_{SW_Loss(SWC)} = \frac{1}{2} \times V_{OUT} \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}}) \times (t_{on} + t_{off}) \times f_{sw} \quad (21)$$

MOSFET SWD

When the MPQ4214 works in buck mode, SWD is on consistently. Its power loss can be calculated with Equation (22):

$$P_{C_Loss(SWD)} = I_o^2 \times R_{DSON(SWD)} \quad (22)$$

When the MPQ4214 works in boost mode, the SWD conduction loss can be calculated with Equation (23):

$$P_{C_Loss(SWD)} = (\frac{V_{IN}}{V_{OUT}}) \times (I_o \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DSON(SWD)} \quad (23)$$

Dead time and the low-side MOSFET switching loss can be ignored.

Compensation Components

The COMP pin controls system stability and transient response. COMP is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics.

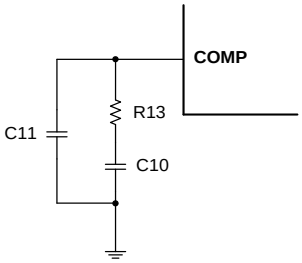


Figure 13: COMP External Compensation

The COMP external compensation sets one pole f_{P1} and one zero f_{Z1} (see Figure 13). These are determined by Equation (24) and Equation (25):

$$f_{P1} = \frac{1}{2\pi \times C11 \times R13} \quad (24)$$

$$f_{Z1} = \frac{1}{2\pi \times C10 \times R13} \quad (25)$$

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When the MPQ4214 works in buck mode, the DC gain of the voltage feedback loop is calculated with Equation (26):

$$A_{VDC} = R_{LOAD} \times \frac{G_{CS}}{R_{SENSE}} \times A_{V-EA} \times \frac{V_{FB}}{V_{OUT}} \quad (26)$$

Where A_{V-EA} is the error amplifier voltage gain (300V/V), G_{CS} is the COMP to current-sense gain, R_{SENSE} is the current-sense resistor, and R_{LOAD} is the load resistor value.

The system has two important poles: one is from the compensation capacitor (C10) and the output resistor of the error amplifier, and the other is from the output capacitor and the load resistor. These poles can be calculated with Equation (27) and Equation (28), respectively:

$$f_{P2} = \frac{G_{EA}}{2\pi \times C10 \times A_{V-EA}} \quad (27)$$

$$f_{P3} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (28)$$

Where G_{EA} is the error-amplifier transconductance (1220μA/V), and C_{OUT} is the output capacitor.

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value. This zero can be determined with Equation (29):

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (29)$$

When the MPQ4214 works in boost mode, the DC gain of the voltage feedback loop is calculated with Equation (30):

$$A_{VDC} = \frac{V_{IN} \times A_{V-EA} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R13}{2 \times V_{OUT}^2 \times R_{SENSE}} \quad (30)$$

There is also a right half-plane zero (f_{RHPZ}) that exists in boost mode. The frequency of the right half-plane zero is determined with Equation (31):

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 \quad (31)$$

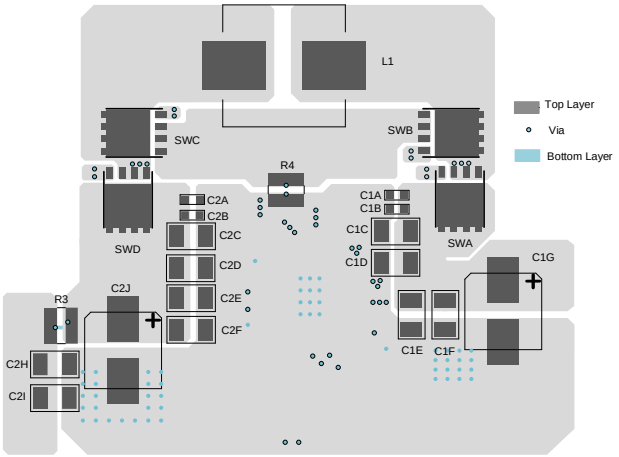
The right half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase and gain margin. The worst-case condition occurs when the input voltage is at its minimum and the output power is at its maximum.

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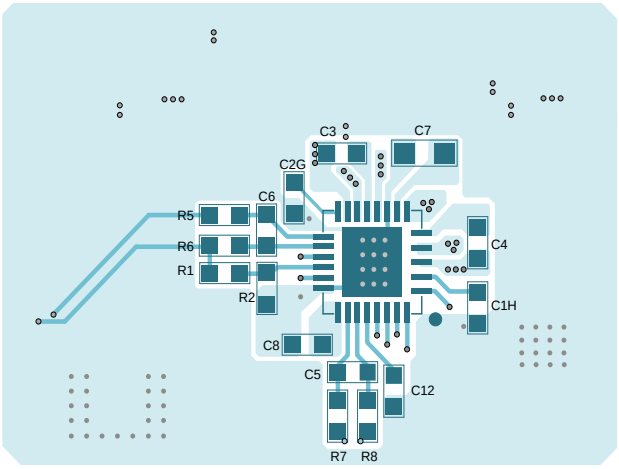
PCB Layout Guidelines

Efficient layout is a critical step in designing a buck-boost controller. Improper layout may result in reduced performance, EMI problems, resistive loss, and even system instability. For best results, refer to Figure 14 and follow the guidelines below:

1. In buck mode, place the input power loop — including the input filter capacitor (C_{IN}), the power MOSFETs (SWA and SWB), and the cycle-by-cycle current-sense resistor (R4) — as close as possible.
2. In boost mode, place the output power loop — including the output filter capacitor (C_{OUT}), the power MOSFETs (SWC and SWD), and the cycle-by-cycle current-sense resistor (R4) — as close as possible.
3. Use wide copper traces and power loop vias to help thermal dissipation.
4. Connect the exposed pad to GND, and place vias on the exposed pad for IC thermal dissipation.
5. Place small decoupling capacitors close to VIN, VOUT, and AGND.
6. Lay out the gate drive traces and return paths as directly as possible.
7. Lay out the forward and return traces close together to minimize the inductance of the gate drive path. They can run side by side, or on top of each other on adjacent layers.
8. Use Kelvin connections to R3 (for the average current sense) and R4 (for the cycle-by-cycle current), and run lines in parallel from the R3/R4 terminals to the IC pins.
9. Avoid crossing noisy areas, such as SW1 and SW2, or gate drive traces.
10. Place the filter capacitor for the current-sense signal as close to the IC pins as possible.
11. Place the VCC and AVDD capacitors as close as possible to the VCC and AVDD pins.
12. Place the BST1 bootstrap capacitor close to the IC, and connect it directly to the BST1 and SW1 pins.
13. Place the BST2 bootstrap capacitor close to the IC, and connect it directly to the BST2 and SW2 pins.
14. The feedback loop should be far away from any noise source, so place the FB dividers (R1 and R2) as close as possible to the FB and AGND pins.
15. Separate the power and signal paths so that no power or switching current flows through the AGND connections.
16. Connect the PGND and AGND traces near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the cycle-by-cycle current-sense resistor (R4).



Top Layer



Bottom Layer

Figure 14: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

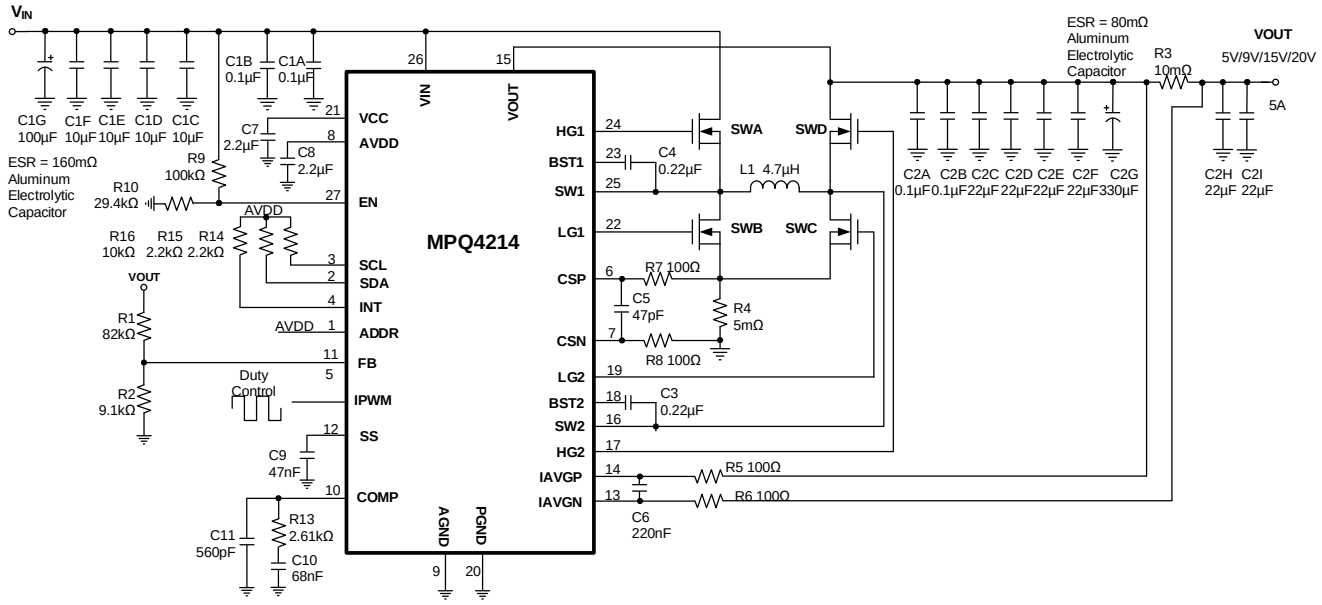


Figure 15: Typical Application Circuitry

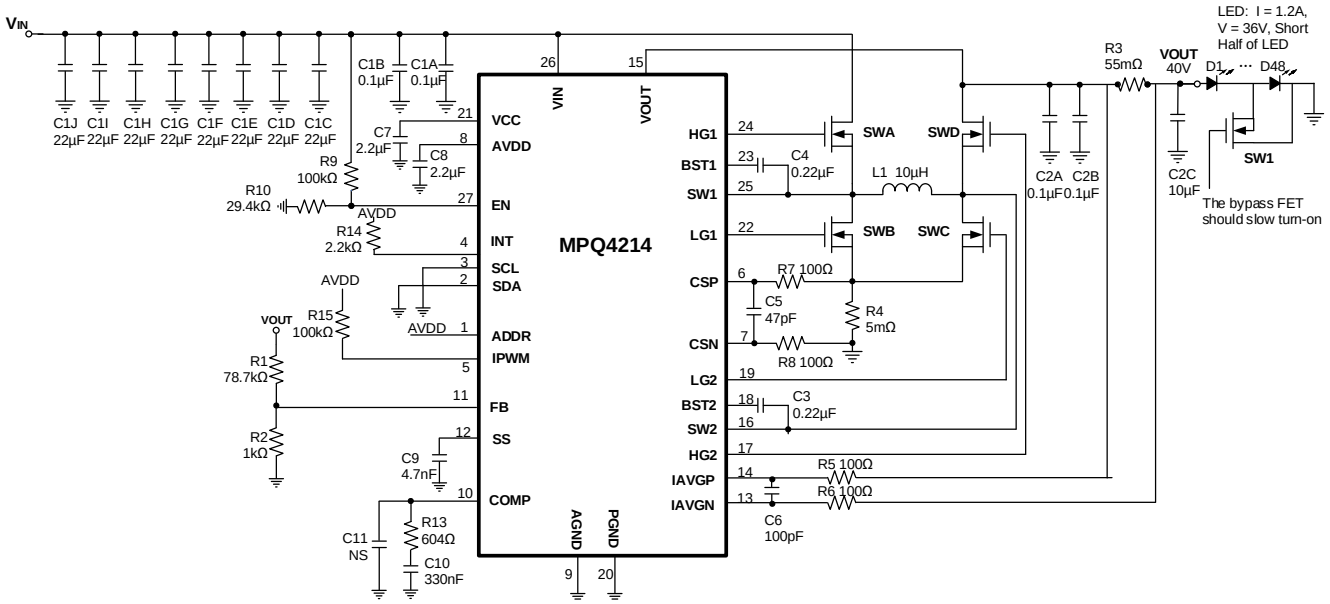


Figure 16: High-Power LED Driver Application

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REGISER DESCRIPTION

Register Map

Addr	Register	Type	D7	D6	D5	D4	D3	D2	D1	D0	Reset State
0x00	REF_LSB	R/W	-	-	-	-	-	VREF_L [bit 2:0] (10)			0000 0100
0x01	REF_ MSB	R/W	VREF_H [bit 10:3] (10)								0011 1110
0x02	Control 1	R/W	SR (10)		DISCHG	Dither	PNG_ Latch	Reserve (11)	GO_BIT (10)	ENPWR	0100 010x (9)
0x03	Control 2	R/W	FSW		-	BB_FSW	OCP_MODE		OVP_MODE		1000 0101
0x04	ILIM	R/W	-	-	-	-	-	ILIM			0000 1111
0x05	Interrupt Status	R/W	-	-	-	OTP	CC	OVP	OCP	PNG	0000 0000
0x06	Interrupt Mask	R/W	-	-	-	M_OTP	M_CC	M_OVP	M_OCP	M_PNG	0000 0001

Notes:

9) The “x” default value is determined by the device address setting (ADDR pin setting). See Table 1 for details.
10) The MPQ4214GU can program these bits, but the MPQ4214GU-12 cannot program V_{REF} or the output change slew rate.
11) Reserved bits. Do not write different value to these bits in application.

Register Name: REF_LSB, 00h (Read/Write)

Name	Bits	Default Value	Description
VREF_L	D[2:0]	100	Feedback VREF low 3 bits. LSB = 1mV.

Register Name: REF_MSB, 01h (Read/Write)

Name	Bits	Default Value	Description
VREF_H	D[7:0]	0011 1110	Feedback VREF high 8 bits. LSB = 8mV.

See below for FB reference data format.

Name	VREF															
Format	Direct, unsigned binary integer															
Register Name	N/A					VREF_H D[7:0]								VREF_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high								Data bit low		
Default Value (0.5V)	N/A					500 integer										

Total 11 bits to set reference voltage. If V is an 11-bit, unsigned binary integer of VREF [10:0], then V_{FB} (V) = V / 1000.

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Register Name: Control 1, 02h (Read/Write)

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td rowspan="6">SR</td><td rowspan="6">D[7:6]</td><td rowspan="6">01</td><td colspan="3">Programs the V_{REF} changing slew rate. This SR control only works after SS finishes. During the SS period, the VOUT slew rate is controlled by SS.
V_{OUT} slew rate = VREF slew rate × feedback ratio of (R1 + R2) / R2</td></tr>
<tr><td>SR bits value</td><td>V_{REF} step interval</td><td>V_{REF} slew rate</td></tr>
<tr><td>00</td><td>26µs / step</td><td>38mV/ms</td></tr>
<tr><td>01</td><td>20µs / step</td><td>50mV/ms</td></tr>
<tr><td>10</td><td>14µs / step</td><td>72mV/ms</td></tr>
<tr><td>11</td><td>6.7µs / step</td><td>150mV/ms</td></tr>
<tr><td>DISCHG</td><td>D[5]</td><td>0</td><td colspan="3">Turns on or turns off the output-to-ground discharge path. Write DISCHG bit = 1 to always turn on the internal discharge resistor. Write DISCHG bit = 0 to turn off output discharge resistor. The DISCHG bit function works even when the ENPWR bit is low.
This bit does not affect the output discharge behavior in the following cases:
1. VOUT voltage changed by the I²C
2. ENPWR power off
3. EN pin power off
4. Output OVP (When OVP_MODE enables discharge)
5. VIN UVLO
When GO_BIT = 1, the VOUT discharge automatically turns on. After GO_BIT resets to 0 with an 20ms extra delay, the VOUT discharge path turns off.
Normally, it is recommended to set the slew rate low so V_{OUT} can follow the V_{REF} change with this internal discharge current. If V_{OUT} cannot follow the V_{REF} change even with the discharge due to a large COUT capacitor, there is an additional 20ms discharge.</td></tr>
<tr><td>Dither</td><td>D[4]</td><td>0</td><td colspan="3">Frequency dither function enable bit.
0 = Dither disabled
1 = Dither enabled</td></tr>
<tr><td>PNG_Latch</td><td>D[3]</td><td>0</td><td colspan="3">PNG status bit reset control bit.
0 = PNG bit status recovers to 0 once V_{OUT} returns to its normal voltage range
1 = PNG bit status latches to 1 once V_{OUT} exits power good voltage range. The host writing 1 to the PNG bit can reset the bit</td></tr>
<tr><td>Reserved</td><td>D[2]</td><td>1</td><td colspan="3">This bit should be always set to 1.</td></tr>
</table>

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GO_BIT	D[1]	0	Reference voltage change function enable bit. Set GO_BIT = 1 to enable the output change based on the VREF register. When the command completes (the internal reference voltage steps to the goal of VREF), GO_BIT auto-resets to 0. It prevents false operation of VOUT scaling. Write the VREF registers (00h and 01h) first, then write GO_BIT = 1. The reference and output voltage will change based on the new V_{REF}. GO_BIT resets to 0 when the reference voltage reaches the new level. The host reads GO_BIT to determine whether the VREF scaling is finished or not. The V_{OUT} discharge path enables when GO_BIT = 1, no matter what the DISCHG bit is. This can help pull V_{OUT} from high to low in light-load conditions. After GO_BIT resets to 0, the discharge continues and turns off after a 20ms delay. 0 = V_{OUT} cannot be changed 1 = V_{OUT} changes based on the VREF registers. After V_{REF} reaches the new level set by the VREF bits, GO_BIT resets to 0 automatically
ENPWR	D[0]	x	Power switching enable bit. The default value is determined by the ADDR set-up. 1 = Enables power switching. 0 = Disables power switching, but other internal control circuits work. Recommended ENPWR start-up sequence: Step 1: Set VREF, ENPWR = 0 Step 2: Set GO_BIT = 1, ENPWR still = 0 Step 3: Set ENPWR = 1 to enable V_{OUT}

I²C VREF Changing Sequence for USB PD Application

When the sink device is unplugged, the PD controller should set ENPWR = 0 to turn off the V_{BUS} voltage. Next time the sink device is attached, the PD controller should follow the sequence below to set V_{BUS} to 5V:

1. Write V_{REF}.
2. Write GO_BIT = 1, but keep ENPWR = 0, as this can set V_{REF} to the target.
3. Write ENPWR = 1 to enable V_{OUT}.

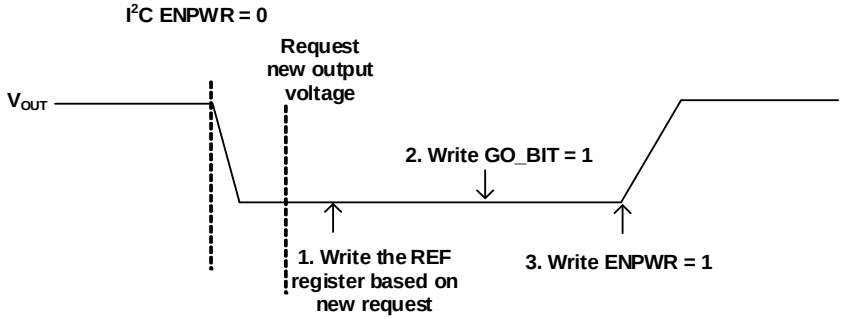


Figure 17: New Output Voltage Request Sequence

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Register Name: Control 2, 03h (Read/Write)

<table>
<tr><th>Name</th><th>Bits</th><th>Default Value</th><th>Description</th></tr>
<tr><td rowspan="3">FSW</td><td rowspan="3">D[7:6]</td><td rowspan="3">10</td><td colspan="5">Switching frequency setting bit.
It is writable during both ENPWR = 0 and ENPWR = 1 conditions. The switching frequency changes smoothly after the I²C writes these bits.</td></tr>
<tr><td>FSW bits</td><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><td>Frequency</td><td>200kHz</td><td>300kHz</td><td>400kHz</td><td>600kHz</td></tr>
<tr><td>BB_FSW</td><td>D[4]</td><td>0</td><td colspan="5">Buck-boost region switching frequency set bit.
0 = Higher switching frequency in buck-boost region. The higher buck-boost switching frequency is 62.5% of the base switching frequency
1 = Lower switching frequency in buck-boost region. The lower buck-boost switching frequency is 37.5% of the base switching frequency</td></tr>
<tr><td>OCP_MODE</td><td>D[3:2]</td><td>01</td><td colspan="5">Sets OCP protection mode after triggering the cycle-by-cycle switching current limit (valley current limit in buck or peak current limit in boost).
00 = No hiccup or latch-off protection. Inductor current is limited by the cycle-by-cycle current limit
01 = Hiccup protection after triggering the switching current limit and V_{FB} < 60% of V_{REF}. The off period is controlled by the SS discharge
10 = Latch-off protection. The IC must be re-powered or re-enabled for the device to start up again
11 = Reserved</td></tr>
<tr><td>OVP_MODE</td><td>D[1:0]</td><td>01</td><td colspan="5">Sets OVP protection mode after triggering the 127% V_{REF} threshold.
00 = No protection after OVP, V_{OUT} is regulated by COMP. No discharge after OVP
01 = Discharges V_{OUT} through the internal resistor and stops switching when V_{OUT} triggers 127% of V_{REF}. Recovers when V_{OUT} drops to 111% of V_{REF}
10 = Latch-off protection. No discharge after OVP
11 = Reserved</td></tr>
</table>

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Register Name: ILIM, 04h (Read/Write)

Name	Bits	Default Value	Description		
ILIM	D[2:0]	111	Average current limit. It can be used to program the output current limit.		
			ILIM bits	Current limit threshold	Current limit with 10mΩ R_{SENSE}
			000	26mV	2.6A
			001	32mV	3.2A
			010	38mV	3.8A
			011	45mV	4.5A
			100	50mV	5.0A
			101	56mV	5.6A
			110	62mV	6.2A
			111	68mV	6.8A

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Register Name: Interrupt Status, 05h (Read/Write)

Name	Bits	Default Value	Description	Reset Condition
OTP	D[4]	0	Over-temperature protection indication. 0: Normal state 1: Chip is in over-temperature protection state	This bit is latched once triggered. Write 0xFF to this register to reset the interrupt status and INT's state.
CC	D[3]	0	Output average current limit indicator. 0: Normal state 1: The output current is higher than the average current limit reference, and V_{OUT} drops	
OVP	D[2]	0	V_{OUT} OVP indicator. 0: Normal state 1: Chip is in over-temperature protection state	
OCP	D[1]	0	Cycle-by-cycle switching current limit indication. 0: Normal state 1: Cycle-by-cycle current limit is triggered, V_{FB} < 60% of V_{REF}, and soft start is finished	Related to the PNG_Latch setting: PNG_Latch = 0: This bit indicates instantaneous value. INT indicates the instantaneous state. PNG_Latch = 1: This bit is latched once triggered. Write 0xFF to reset the interrupt status and INT's state.
PNG	D[0]	0	VOUT power not good indicator. 0: Normal state 1: Output power is not good. It indicates when V_{OUT} is out of both its upper and lower thresholds The PNG_Latch bit controls the PNG reset behavior.	

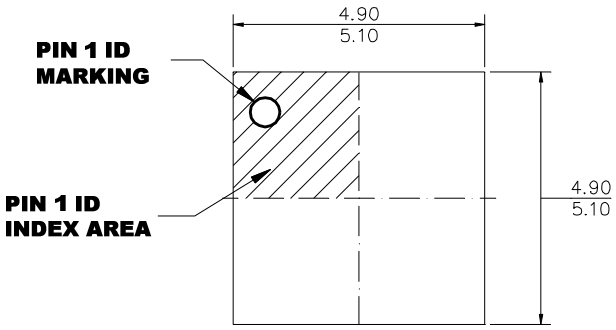
Register Name: Interrupt Mask, 06h (Read/Write)

Name	Bits	Default Value	Description
M_OTP	D[4]	0	OTP mask bit. Set 1 to mask the OTP interrupt, but the OTP bit cannot be masked.
M_CC	D[3]	0	CC mask bit. Set 1 to mask the CC interrupt, but the CC bit cannot be masked.
M_OVP	D[2]	0	OVP mask bit. Set 1 to mask off the OVP alert. M_OVP = 1 only masks INT's output.
M_OCP	D[1]	0	OCP mask bit. Set 1 to mask off the OCP alert. M_OCP = 1 only masks INT's output.
M_PNG	D[0]	1	PNG mask bit. Set 1 to mask off the PNG alert. M_PNG = 1 only masks INT's output.

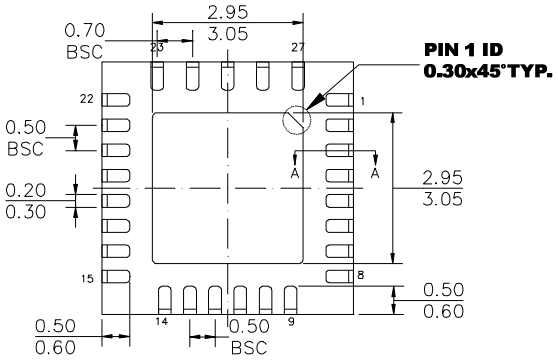
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PACKAGE INFORMATION

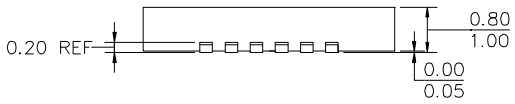
QFN-27 (5mmx5mm)



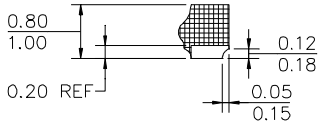
TOP VIEW



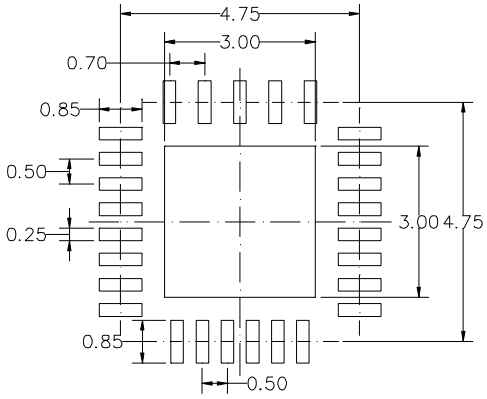
BOTTOM VIEW



SIDE VIEW



SECTION A-A



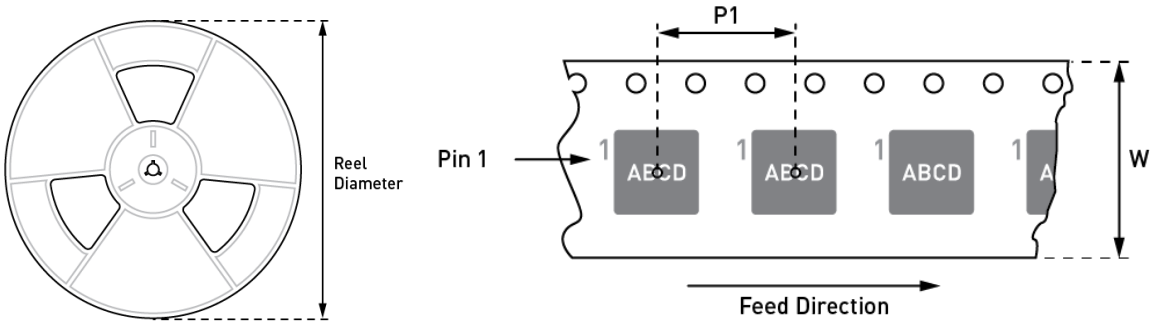
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING REFERENCE TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4214GU-AEC1-Z	QFN (5mmx5mm)	5000	N/A	13 in.	12mm	8mm
MPQ4214GU-12-AEC1-Z	QFN (5mmx5mm)	5000	N/A	13 in.	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/19/2019	Initial Release	-
1.1	8/17/2020	Updated POD	39
1.2	5/26/2023	• Updated header by adding “AEC-Q100 Qualified” • Updated Description section with AEC-Q100 qualification • Updated “AEC-Q100 Qualification in Process” in Features section to “Available in AEC-Q100 Grade 1”	1
		Updated header to add “AEC-Q100”	2–41
		Updated shutdown current max value from 2μA to 5μA	7

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