MPQ1923-AEC1

100V, 8A, High-Frequency, Half-Bridge Gate Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ1923-AEC1 is a high-frequency, N-channel MOSFET, half-bridge gate driver. The device's low-side MOSFET (LS-FET) and high-side MOSFET (HS-FET) driver channels are controlled independently, and are matched with <5ns in time delay.

In the case of an insufficient supply, the device's HS-FET and LS-FET under-voltage lockout (UVLO) protection forces the outputs low. The MPQ1923-AEC1 also features an integrated bootstrap (BST) diode to reduce the external component count.

The MPQ1923-AEC1 is available in QFN-10 (4mmx4mm) and QFN-8 (4mmx4mm) packages.

FEATURES

- Drives an N-Channel MOSFET Half-Bridge
- Low Dropout with 4.5V Under-Voltage Lockout (UVLO) Falling Threshold
- 120V Bootstrap Voltage (V_{BST}) Range
- On-Chip Bootstrap Diode
- 20ns Typical Propagation Delay
- 8A Sink Current, 7A Source Current at 12V V_{DD}
- <5ns Gate Driver Matching Time Delay
- Drives a 1nF Load with 7.2ns Rise Time (t_{RISE}) and 5.5ns Fall Time (t_{FALL}) at 12V V_{DD}
- TTL-Compatible Input
- <300µA Quiescent Current (I_Q)
- UVLO Protection for the HS-FET and LS-FET Gate Drivers
- Available in QFN-10 (4mmx4mm) and QFN-8 (4mmx4mm) Packages
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Motor Drivers
- Telecom Half-Bridge Power Supplies
- Avionics DC/DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters

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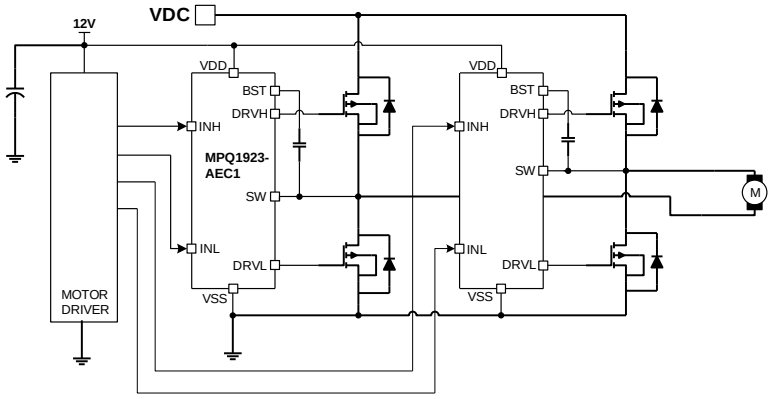
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ1923GRE-AEC1	QFN-10 (4mmx4mm)	*See Below*	1
MPQ1923GR-AEC1	QFN-8 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ1923GRE-AEC1-Z).

TOP MARKING

MPSYWW
MP1923
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP1923: Part number
LLLLLL: Lot number
E: MPQ1923GRE-AEC1

TOP MARKING

MPSYWW
MP1923
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
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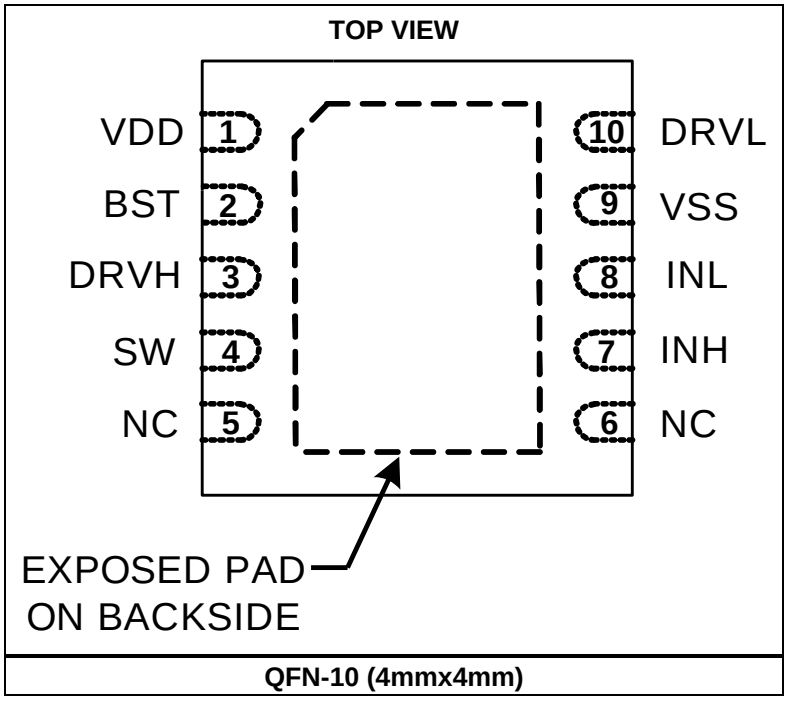
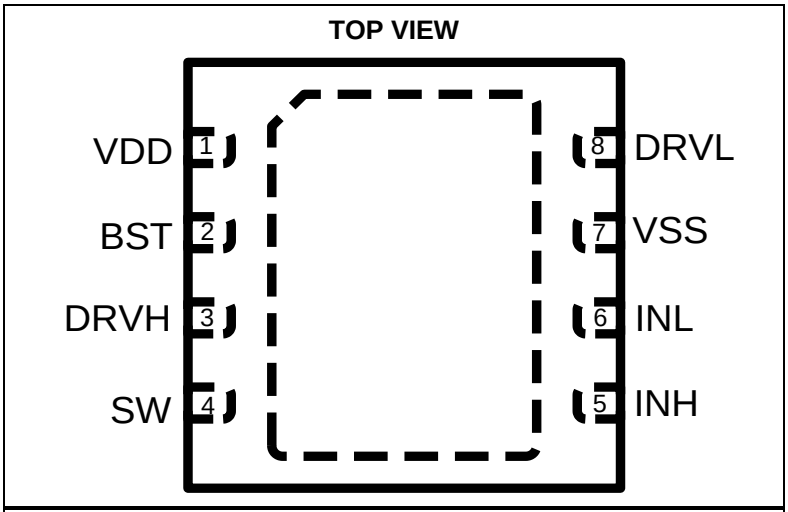
PACKAGE REFERENCE (MPQ1923GRE-AEC1)



QFN-10 (4mmx4mm)

PACKAGE REFERENCE (MPQ1923GR-AEC1)



QFN-8 (4mmx4mm)

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PIN FUNCTIONS

Pin #		Name	Description
QFN-10	QFN-8		
1	1	VDD	**Supply voltage.** The VDD pin supplies power to the internal circuitry. Connect a decoupling capacitor between VDD and ground to ensure a stable and clean supply.
2	2	BST	**Bootstrap.** The BST pin is the positive power supply for the internal floating high-side MOSFET (HS-FET) driver. Connect a bypass capacitor between the BST and SW pins.
3	3	DRVH	**Floating HS-FET driver output.**
4	4	SW	**Switching node.**
5, 6		NC	**Not connected.**
7	5	INH	**Control signal input for the floating HS-FET driver.**
8	6	INL	**Control signal input for the LS-FET driver.**
9	7	VSS	**Chip ground.**
10	8	DRVL	**LS-FET driver output.**
Pad	Pad	Exposed pad	**Exposed pad.** Connect the exposed pad to the VSS pin to improve thermal operation.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{DD}) .....-0.3V to +18V
SW voltage (V_{SW}) .....-5V to +120V
V_{SW} (<2µs) .....-18V to +120V
BST voltage (V_{BST}) .....-0.3V to +120V
BST to SW .....-0.3V to +18V
DRVH voltage (V_{DRVH})…….
……. V_{SW} - 0.3V to V_{BST} + 0.3V
V_{DRVH} (<2µs).....V_{SW} - 2V to V_{BST} + 0.3V
DRVL voltage (V_{DRVL}).....-0.3V to V_{DD} + 0.3V
V_{DRVL} (<2µs) .....-2V to V_{DD} + 0.3V
All other pins to VSS.....-0.3V to +10V
Continuous power dissipation (2) .....
QFN-10 (4mmx4mm) 2.66W
QFN-8 (4mmx4mm) 2.66W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±500V

Recommended Operating Conditions (3)

Supply voltage (V_{DD}) .....5V to 17V
SW voltage (V_{SW}) .....-1V to +100V
SW slew rate..... <50V/ns
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-10 (4mmx4mm)…….47……7…°C/W
QFN-8 (4mmx4mm)……..47……7…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_A = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I_{DD_Q}	V_{INL} = V_{INH} = 0V		130	300	µA
VDD operating current	I_{DD_OP}	f_{SW} = 500kHz, C_{LOAD} = 0nF		2.6	6	mA
Floating driver quiescent current	I_{BST_Q}	V_{INL} = V_{INH} = 0V		60	150	µA
Floating driver operating current	I_{BST_OP}	fsw = 500kHz, C_{LOAD} = 0nF		2.6	6	mA
BST to VSS quiescent current	I_{BST-SS_Q}	V_{BST} = V_{SW} = 115V		0.05	1	µA
BST to VSS operating current	I_{BST-SS_OP}	f_{SW} = 500kHz, C_{LOAD} = 0nF		2.3	5.5	mA
Leakage current	I_{LKG}	V_{BST} = V_{SW} = 100V		0.05	1	µA
Inputs						
INL and INH high voltage				2	2.4	V
INL and INH low voltage			0.8	1.2		V
Input voltage hysteresis				600		mV
INL and INH internal pull-down resistance	R_{INL}			155		kΩ
	R_{INH}			155		kΩ
Under-Voltage Protection (UVLO) Protection						
VDD rising threshold	V_{DD_RISING}		4.6	5	5.4	V
VDD falling threshold	$V_{DD_FALLING}$		4.1	4.5	4.9	V
(BST - SW) rising threshold	V_{BST_RISING}		1.6	3.7	4.9	V
(BST - SW) falling threshold	$V_{BST_FALLING}$		1.4	3.2	4.6	V
Bootstrap Diode						
Bootstrap diode VF at 100µA	V_{F1}			0.5	0.9	V
Bootstrap diode VF at 100mA	V_{F2}			1	1.2	V
Bootstrap diode dynamic R	R_D	$I_{VDD-BST}$ = 100mA and 80mA		3.1	6.5	Ω
Low-Side MOSFET (LS-FET) Gate Driver						
Low-level output voltage	V_{OLL}	I_{OUT} = 100mA	0.02	0.07	0.2	V
High-level output voltage to rail	V_{OHL}	I_{OUT} = -100mA	0.02	0.07	0.3	V
Source current (5)	I_{OHL}	V_{DRVL} = 0V, V_{DD} = 12V		7		A
		V_{DRVL} = 0V, V_{DD} = 16V		9		A
Sink current (5)	I_{OLL}	V_{DRVL} = V_{DD} = 12V		8		A
		V_{DRVL} = V_{DD} = 16V		10		A
Floating High-Side MOSFET (HS-FET) Gate Driver						
Low level output voltage	V_{OLH}	I_{OUT} = 100mA	0.02	0.07	0.2	V
High level output voltage to rail	V_{OHH}	I_{OUT} = -100mA	0.02	0.07	0.3	V
Source current (5)	I_{OHH}	V_{DRVH} = 0V, V_{DD} = 12V		7		A
		V_{DRVH} = 0V, V_{DD} = 16V		9		A
Sink current (5)	I_{OLH}	V_{DRVH} = V_{DD} = 12V		8		A
		V_{DRVH} = V_{DD} = 16V		10		A
Switching Specifications (LS-FET Gate Driver)						
Turn-off propagation delay	t_{DLFF}	C_{LOAD} = 0nF, INL falling to DRVL falling	5	20	50	ns
Turn-on propagation delay	t_{DLRR}	C_{LOAD} = 0nF, INL rising to DRVL rising	5	20	50	ns
DRVL rise time	t_{RISE_LS}	C_{LOAD} = 1nF, from 10% to 90%		7.2		ns
		C_{LOAD} = 0.1µF, from 3V to 9V		0.2	0.6	µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD} = V_{BST} - V_{SW} = 12V, V_{SS} = V_{SW} = 0V, no load at DRVH and DRVL, T_A = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DRVL fall time	t_{FALL_LS}	C_{LOAD} = 1nF, from 90% to 10%		5.5		ns
		C_{LOAD} = 0.1μF, from 9V to 3V		0.15	0.4	μs
Switching Specifications (Floating HS-FET Gate Driver)						
Turn-off propagation delay	t_{DHFF}	C_{LOAD} = 0nF, INH falling to DRVH falling	5	20	50	ns
Turn-on propagation delay	t_{DHRR}	C_{LOAD} = 0nF, INH rising to DRVH rising	5	20	50	ns
DRVH rise time	t_{RISE_HS}	C_{LOAD} = 1nF, from 10% to 90%		7.2		ns
		C_{LOAD} = 0.1μF, (3V to 9V)		0.2	0.6	μs
DRVH fall time	t_{FALL_HS}	C_{LOAD} = 1nF, from 90% to 10%		5.5		ns
		C_{LOAD} = 0.1μF, (9V to 3V)		0.15	0.4	μs
Switching Specifications (Matching)						
HS-FET driver turn-off to LS-FET driver turn-on time (5)	t_{MON}			1	5	ns
LS-FET driver turn-off to HS-FET driver turn-on time (5)	t_{MOFF}			1	5	ns
Minimum input pulse width to change the output (5)	t_{PW}				50	ns
Bootstrap (BST) diode turn-on or turn-off time (5)	t_{BST}			10		ns
Thermal shutdown				165		°C
Thermal shutdown hysteresis				25		°C

Note:

5) Guaranteed by design.

TIMING DIAGRAM

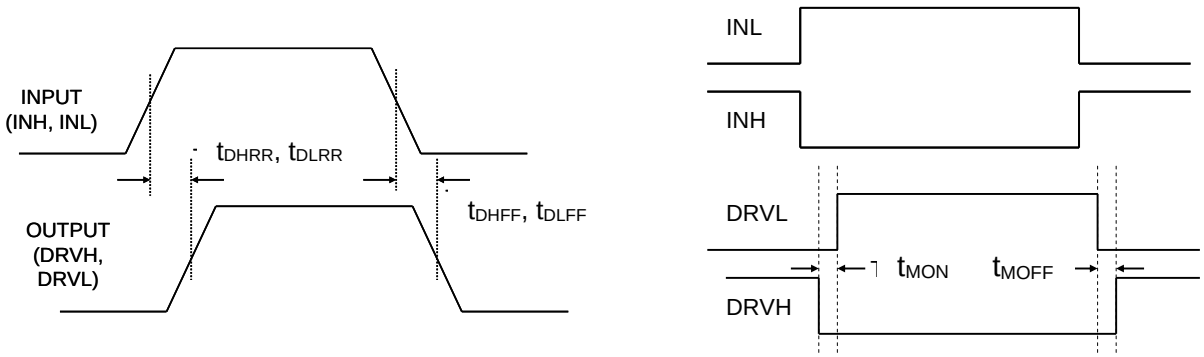

Figure 1: Timing Diagram

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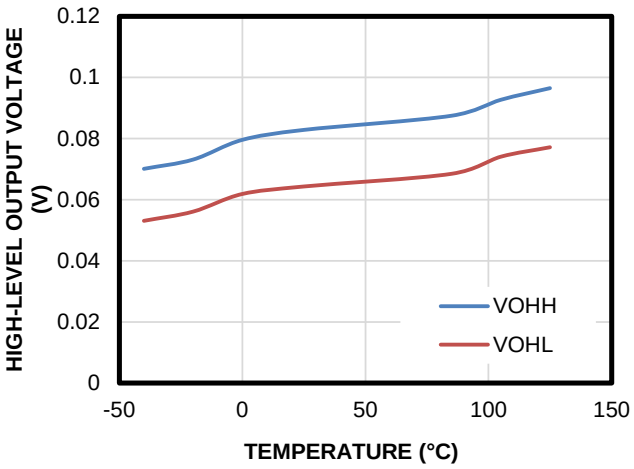
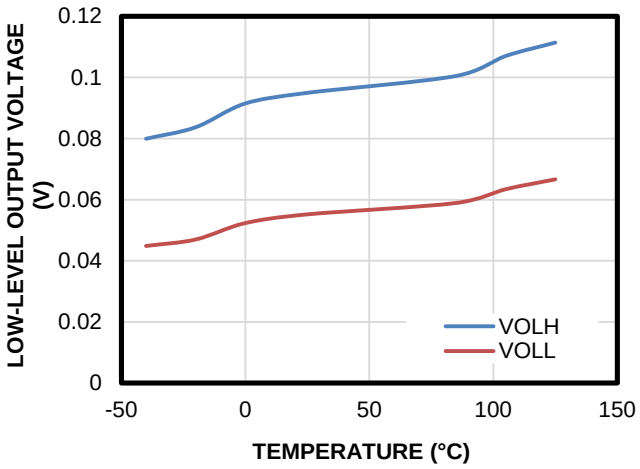
TYPICAL CHARACTERISTICS

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

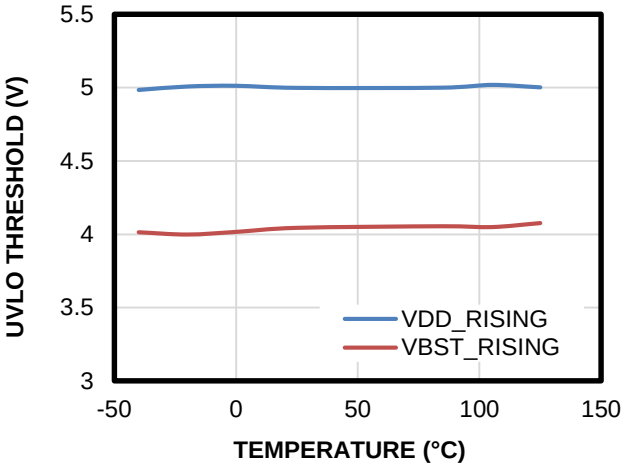
High-Level Output Voltage vs. Temperature



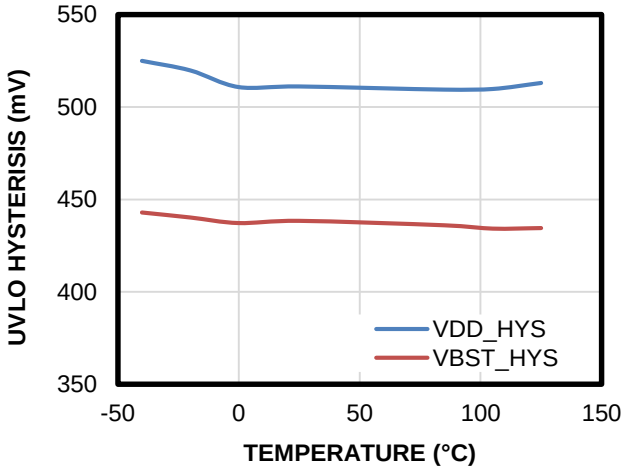
Low-Level Output Voltage vs. Temperature



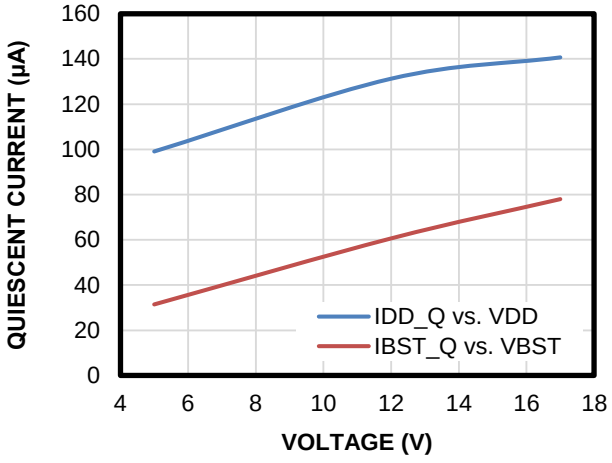
UVLO Threshold vs. Temperature



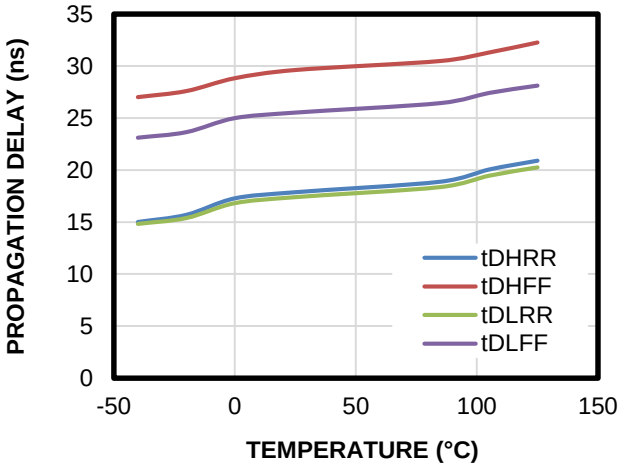
UVLO Hysteresis vs. Temperature



Quiescent Current vs. Voltage



Propagation Delay vs. Temperature



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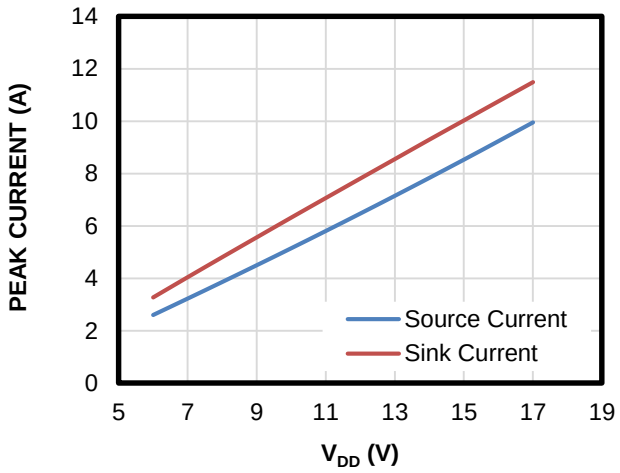
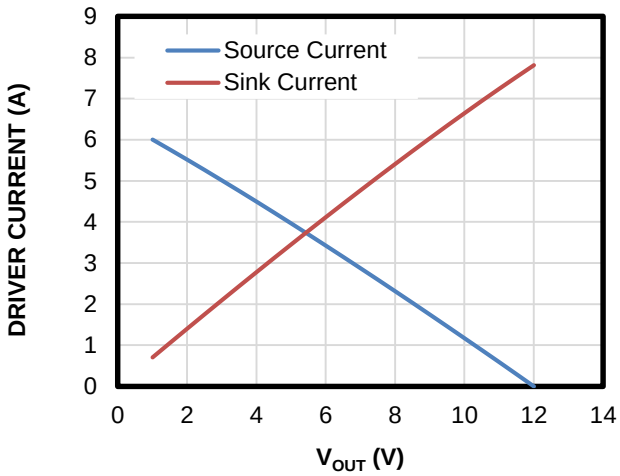
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

Peak Current vs. V_{DD}



Driver Current vs. Output Voltage



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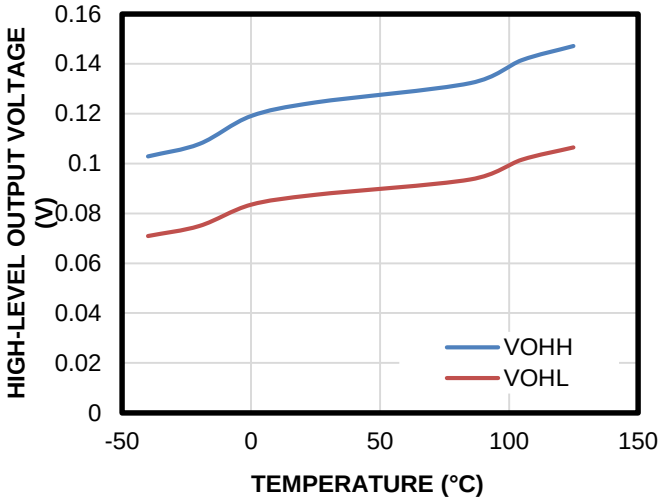
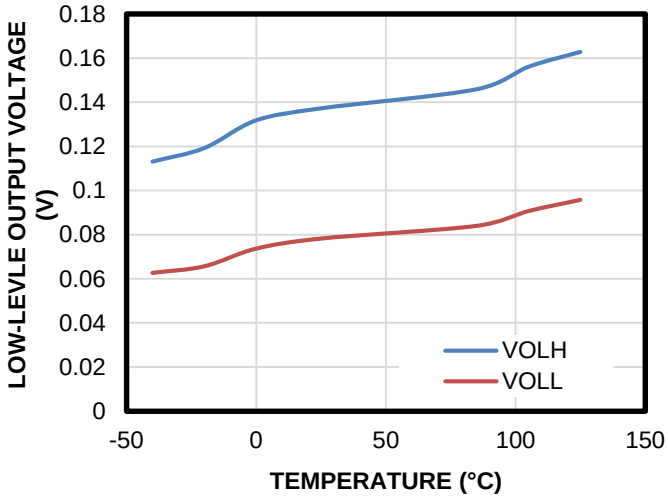
TYPICAL CHARACTERISTICS *(continued)*

V_{DD} = 5V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

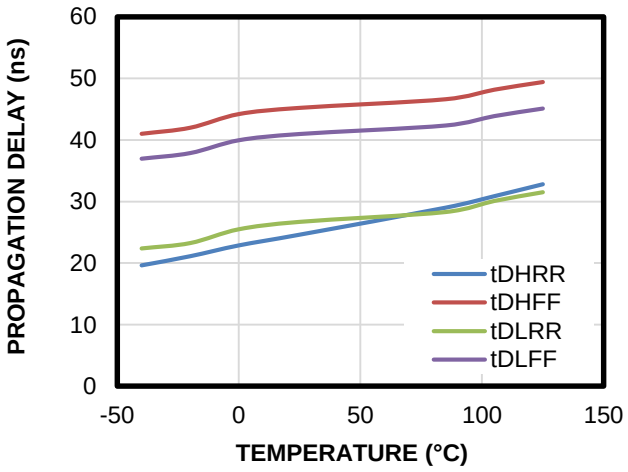
High-Level Output Voltage vs. Temperature



Low-Level Output Voltage vs. Temperature



Propagation Delay vs. Temperature



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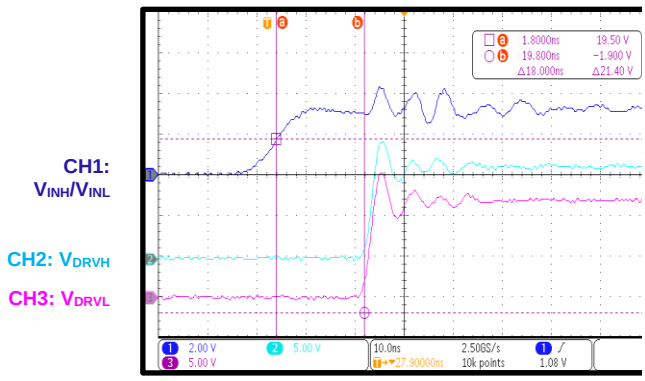
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 12V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

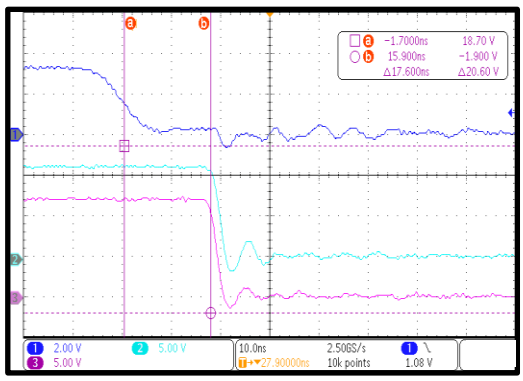
Turn-On Propagation Delay

C_{LOAD} = 0nF, SW is connected to ground



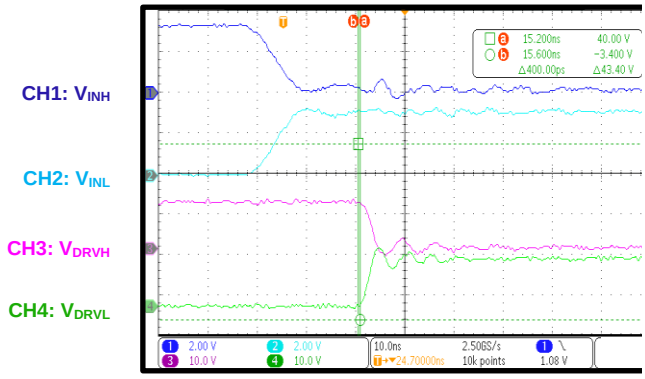
Turn-Off Propagation Delay

C_{LOAD} = 0nF, SW is connected to ground



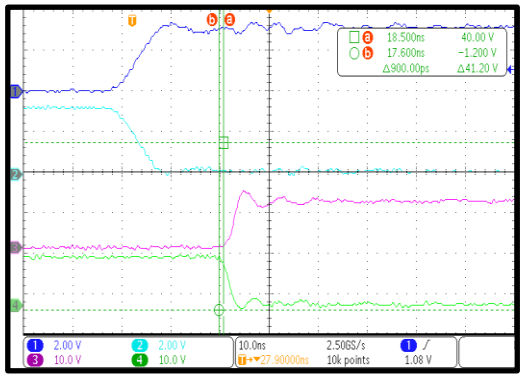
Gate Driver Matching (t_{MON})

C_{LOAD} = 0nF, SW is connected to ground



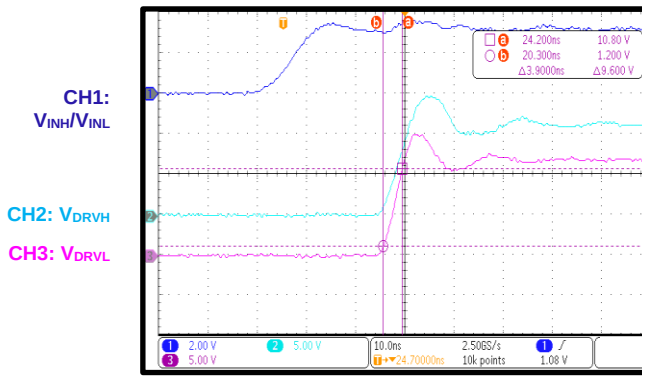
Gate Driver Matching (t_{MOFF})

C_{LOAD} = 0nF, SW is connected to ground



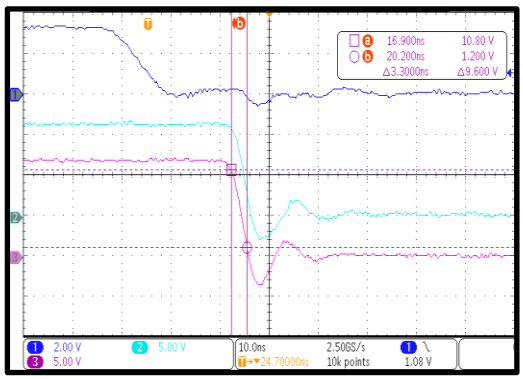
Gate Driver Rise Time

C_{LOAD} = 1nF, SW is connected to ground



Gate Driver Fall Time

C_{LOAD} = 1nF, SW is connected to ground



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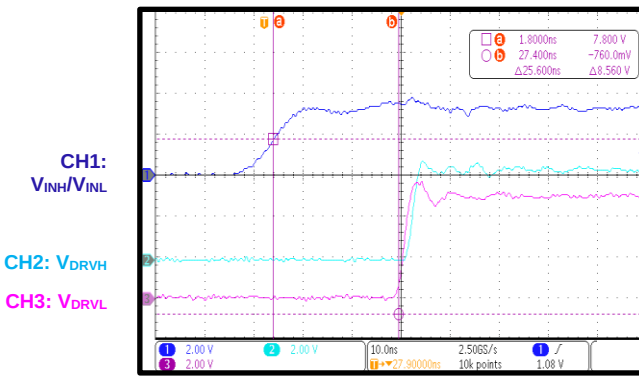
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{DD} = 5V, V_{SS} = V_{SW} = 0V, T_A = 25°C, unless otherwise noted.

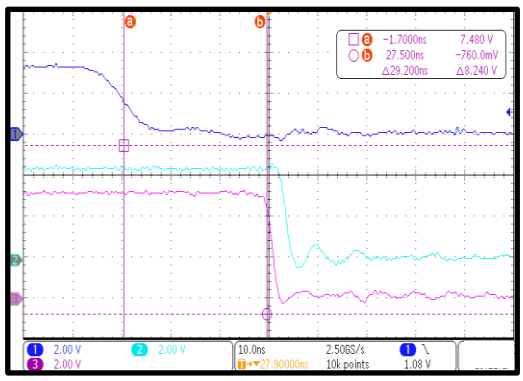
Turn-On Propagation Delay

C_{LOAD} = 0nF, SW is connected to ground



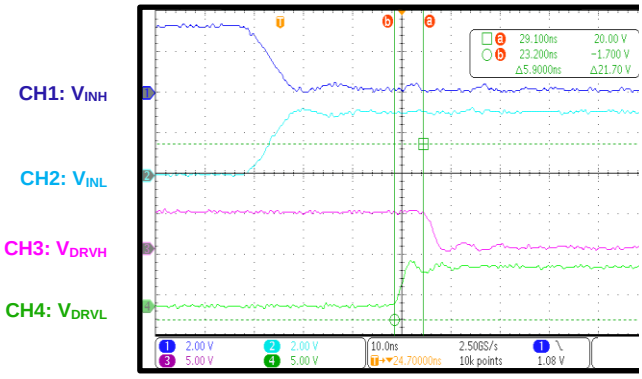
Turn-Off Propagation Delay

C_{LOAD} = 0nF, SW is connected to ground



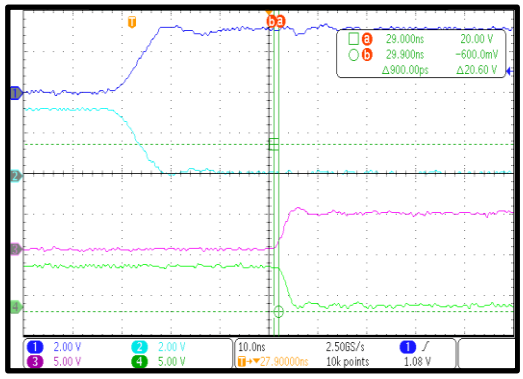
Gate Driver Matching (t_{MON})

C_{LOAD} = 0nF, SW is connected to ground



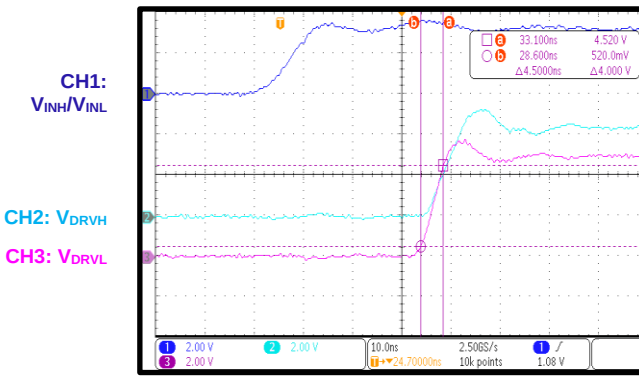
Gate Driver Matching (t_{MOFF})

C_{LOAD} = 0nF, SW is connected to ground



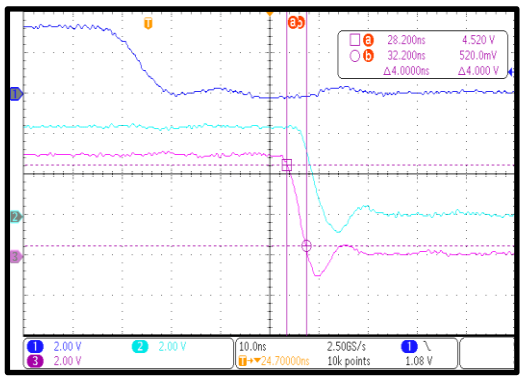
Gate Driver Rise Time

C_{LOAD} = 1nF, SW is connected to ground



Gate Driver Fall Time

C_{LOAD} = 1nF, SW is connected to ground



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FUNCTIONAL BLOCK DIAGRAM

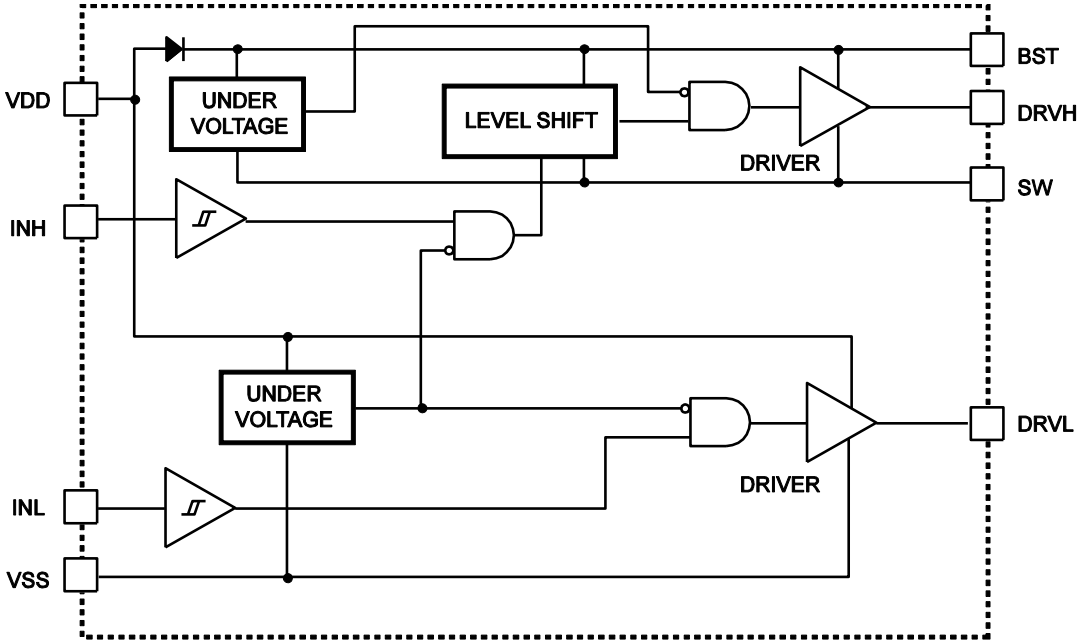

Figure 2: Functional Block Diagram

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REFERENCE DESIGN CIRCUITS

Half-Bridge Converter

In a half-bridge converter topology, the high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are driven alternately with a dead time (DT) inserted between their respective on periods. INT and INL are driven with alternating signals via the pulse-width modulation (PWM) controller. The input voltage (V_{IN}) can rise up to 100V when in a half-bridge topology (see Figure 5 in the Typical Application Circuits section on page 16).

Two-Switch Forward Converter

In a two-switch forward converter topology, the HS-FET and LS-FET start up and shutdown simultaneously. During current-mode control, the INH and INL input signals sense the output voltage (V_{OUT}) and output current (I_{OUT}) via a PWM controller. The Schottky diodes clamp the power transformer's reverse swing, and should be rated for V_{IN}, which can rise up to 100V (see Figure 6 in the Typical Application Circuits section on page 16).

Active-Clamp Forward Converter

In an active-clamp forward converter topology, the HS-FET and LS-FET are driven alternately. The HS-FET and the reset capacitor (C_{RESET}) reset the power transformer without loss.

Active-clamp forward converter topologies are optimal for duty cycles exceeding 50%. The MPQ1923-AEC1 may not be able to operate at 100V in an active-clamp forward topology (see Figure 7 in the Typical Application Circuits section on page 16).

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APPLICATION INFORMATION

The INH and INL input signals can be controlled independently. If both INH and INL control the HS-FET and LS-FET of the same bridge, set a sufficient DT between the low INH and INL signals (and vice versa) to avoid shoot-through. DT is the time interval between low INH and low INL. Figure 3 shows the shoot-through timing diagram.

PCB Mounting

To comply with IPC-2221 or IPC-9592 standards, conformal coating is required after mounting the device on the PCB.

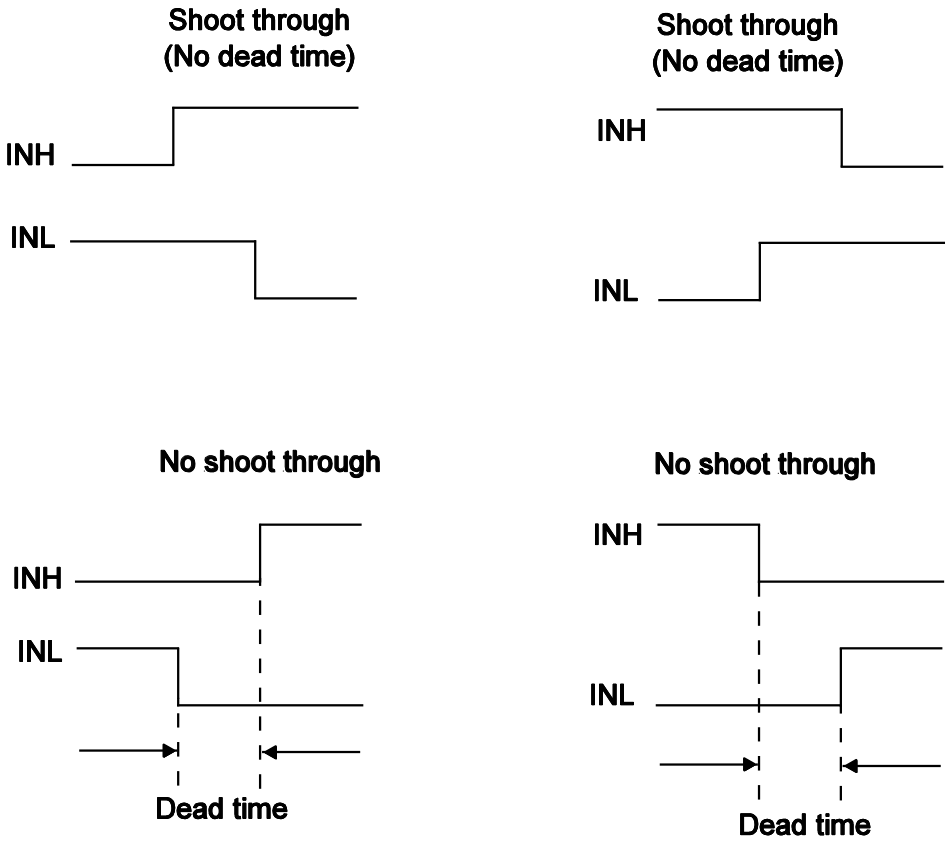

Figure 3: Shoot-Through Timing Diagram

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. The MPQ1923-AEC1 is designed to accommodate negative undershoot; however, excessive undershoot can lead to unpredictable operation or damage to the IC. For the best results, refer to Figure 4 and follow the guidelines below:

1. Connect the HS-FET source and the LS-FET drain using a short and direct trace to avoid negative undershoot on the phase node due to parasitic inductance.
2. Use surface-mount N-channel MOSFETs that allow for a very short connection between the HS-FETs and LS-FETs.
3. Place the bootstrap capacitor (C3) and the supply bypass capacitor (C2) as close to the IC as possible.
4. Connect the ground side of C3 and C2 to both the GND pin and the exposed pad using multiple vias. The ground side of the capacitors are connected to a solid ground plane.
5. Route the high-current ground path between the input supply, the input bulk capacitor (C6), and the MOSFETs. Route this path away from the IC.

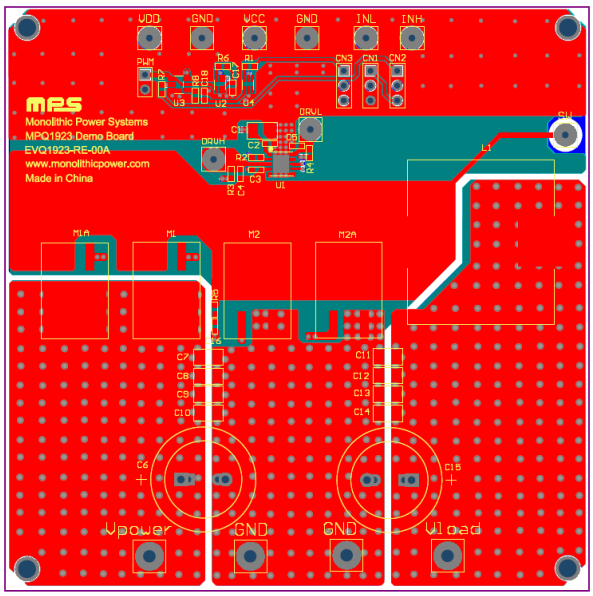

Figure 4: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

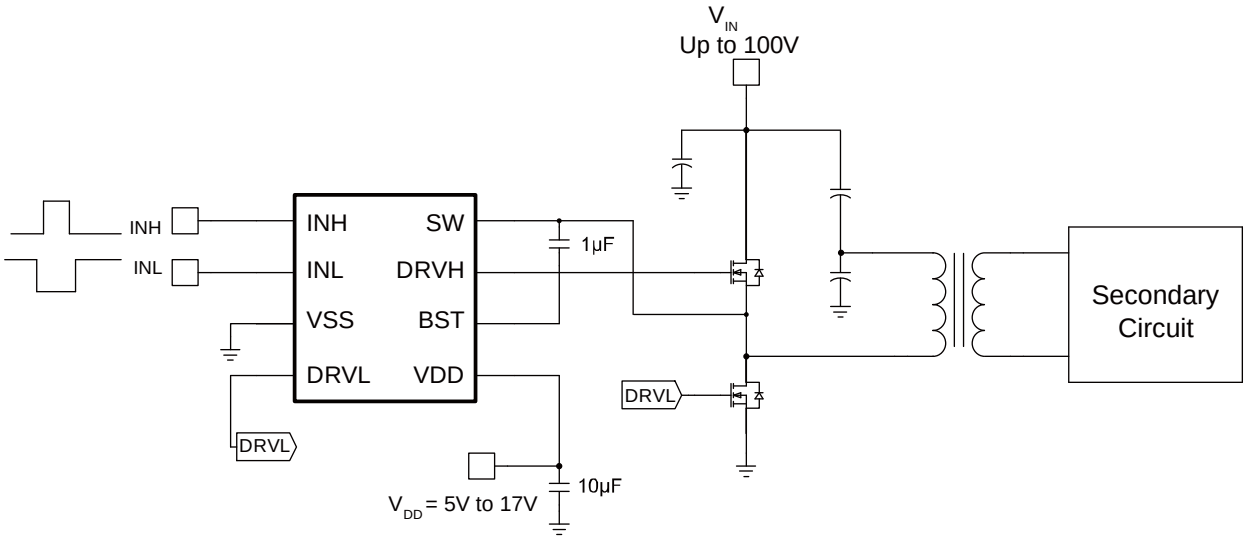

Figure 5: Typical Application Circuit (Half-Bridge Converter Topology)

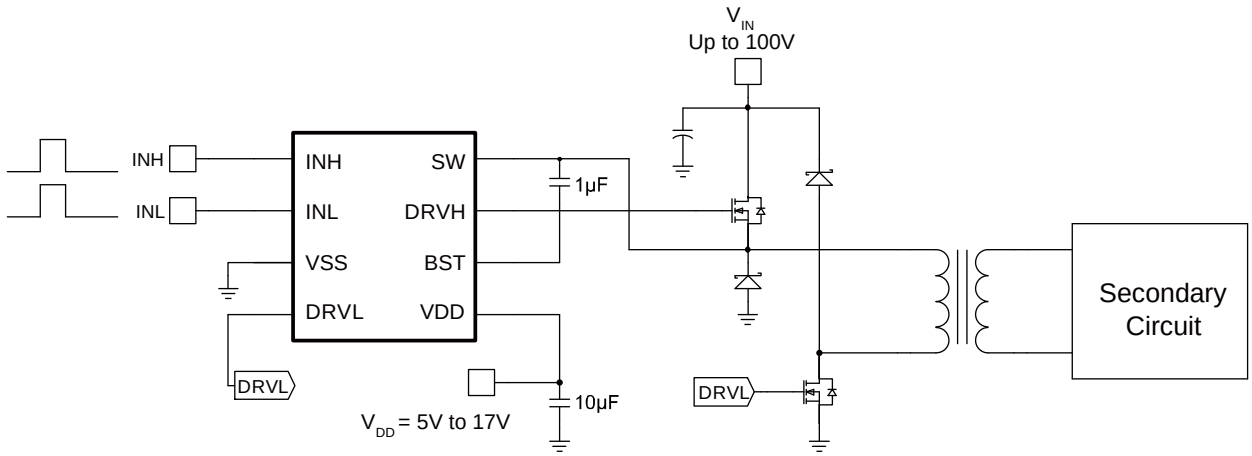

Figure 6: Typical Application Circuit (Two-Switch Forward Converter Topology)

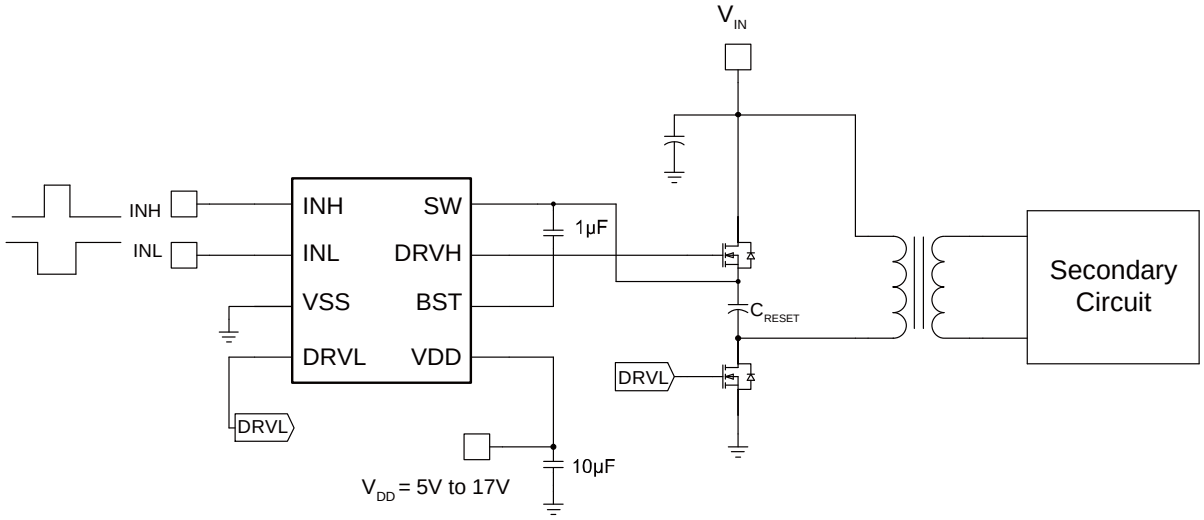

Figure 7: Typical Application Circuit (Active-Clamp Forward Converter Topology)

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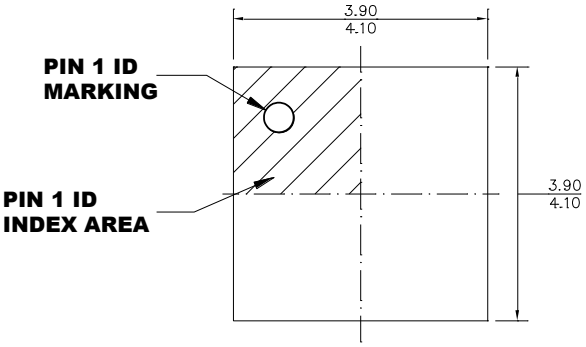
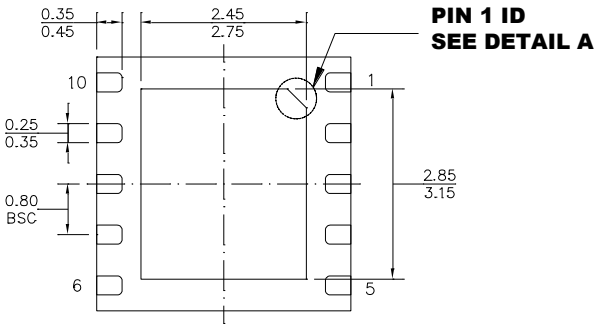
PACKAGE INFORMATION

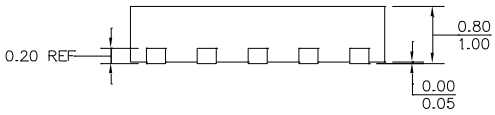
QFN-10 (4mmx4mm)



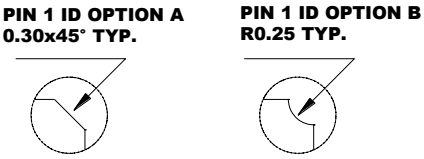
TOP VIEW



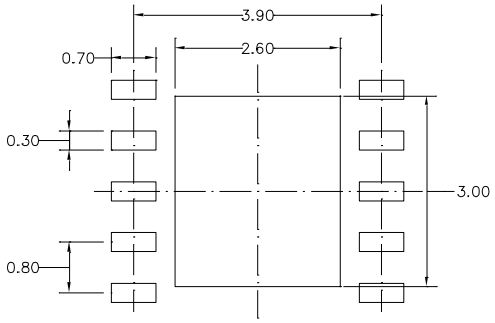
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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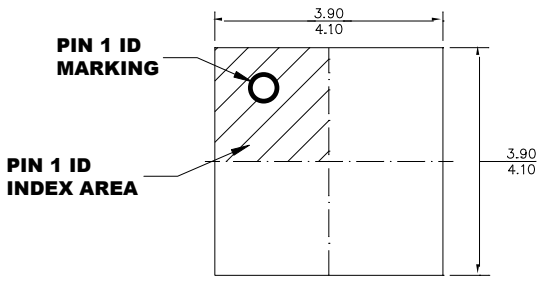
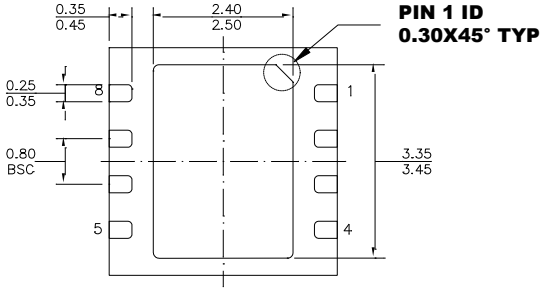
PACKAGE INFORMATION *(continued)*

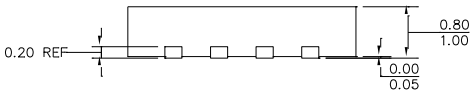
QFN-8 (4mmx4mm)



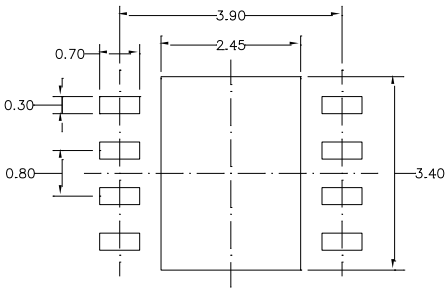
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
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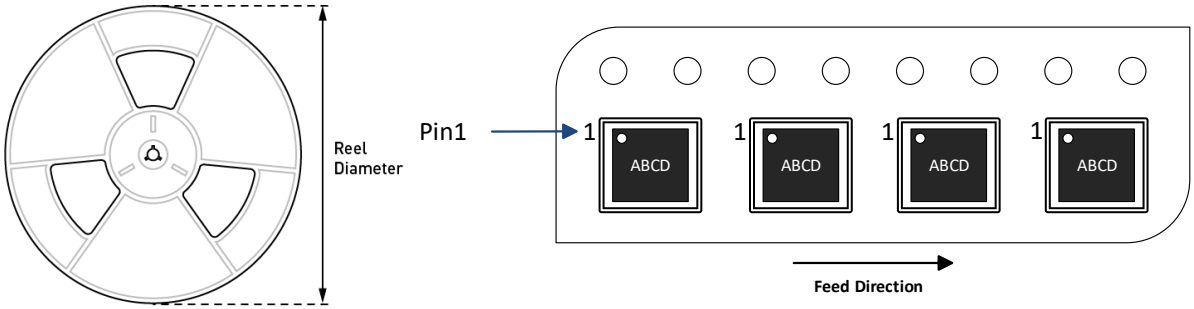
CARRIER INFORMATION

QFN-10 and QFN-8



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ1923GRE-AEC1-Z	QFN-10 (4mmx4mm)	5000	N/A	13in	12mm	8mm
MPQ1923GR-AEC1-Z	QFN-8 (4mmx4mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	8/19/2022	Initial Release	-
1.1	7/18/2023	Updated all headers with AEC-Q100; formatting updates	All
		Updated footers with MPQ1923-AEC1	All
		Updated all mentions of MPQ1923 to MPQ1923-AEC1	All
		• Updated the Ordering Information section • Updated the Top Marking section	2
		Updated the Carrier Information section	19

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