MPM3808C

6V, 3A, 2.4MHz, Synchronous Step-Down Module, AEC-Q100 Qualified

DESCRIPTION

The MPM3808C is an easy-to-use, fully integrated, synchronous step-down power module with a built-in inductor and MOSFET switches. It can achieve up to 3A of continuous output current (I_{OUT}), with excellent load and line regulation.

The constant-on-time (COT) control scheme provides fast transient response and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown. An open-drain power good (PG) signal indicates whether the output voltage (V_{OUT}) exceeds 90% of its nominal voltage.

The MPM3808C is well-suited for a wide range of applications, including high-performance digital signal processors (DSPs), advanced driver assistance system (ADAS) sensors, portable and mobile devices, and other low-power systems with constrained areas.

The MPM3808C requires a minimal number of readily available, standard external components, and is available in a small QFN-15 (3mmx4mmx1.6mm) package.

FEATURES

- **Designed for Automotive Applications**
  - Wide 2.5V to 6V Operating V_{IN} Range
  - Up to 3A Output Current (I_{OUT})
  - 1% Feedback (FB) Accuracy
  - -40°C to +150°C Operating T_J Range
  - Available in AEC-Q100 Grade 1
- **High Performance for Improved Thermals**
  - 50mΩ and 26mΩ Integrated Internal Power MOSFETs
- **Optimized for EMC and EMI**
  - FCCM Across the Full Load Range
  - 2.4MHz Switching Frequency (f_{SW})
  - MeshConnect™ Flip-Chip Package
- **Optimized for Board Size and BOM**
  - Integrated Internal Power MOSFETs
  - Integrated Compensation Network
  - Available in a QFN-15 (3mmx4mmx1.6mm) Package
  - Fixed Output Options (1): 0.8V, 1V, 1.1V, 1.2V, 1.25V, 1.5V, 1.8V, 2.5V, 2.8V, and 3.3V
- **Additional Features**
  - Enable (EN) for Power Sequencing
  - Power Good (PG)
  - 100% Duty Cycle
  - External Soft Start (SS) Control
  - Output Discharge
  - Output Over-Voltage Protection (OVP)
  - Short-Circuit Protection (SCP) with Hiccup Mode
  - Available in a Wettable Flank Package

APPLICATIONS

- Camera Modules
- ADAS Sensors
- Automotive Infotainment
- Automotive V2X

Note:

1) See the Ordering Information section on page 3 for the availability of each fixed output version. Contact MPS for details on additional output voltages that may be available.

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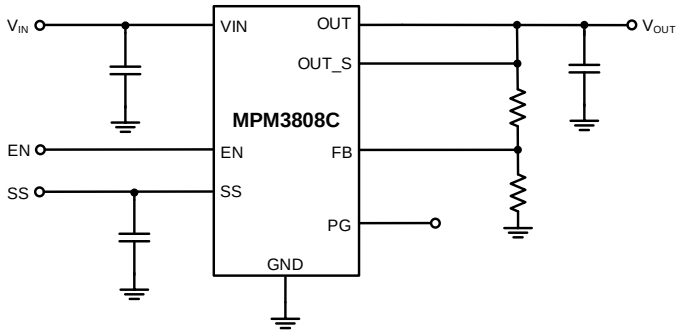
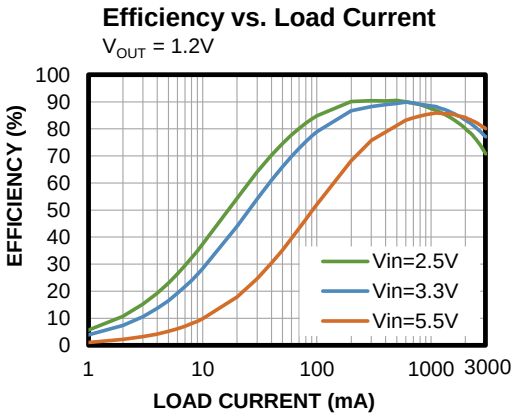
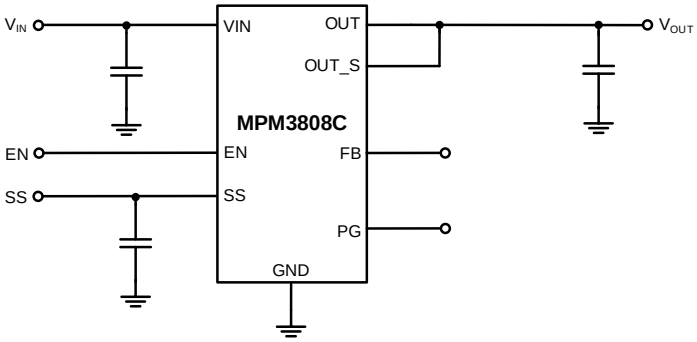
TYPICAL APPLICATION



Typical Application (Adjustable Output)





Typical Application (Fixed Output)

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ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPM3808CGLE-AEC1***	Adjustable	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3808CGLE-08-AEC1***	Fixed 0.8V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3808CGLE-12-AEC1***	Fixed 1.2V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1
MPM3808CGLE-18-AEC1***	Fixed 1.8V	QFN-15 (3mmx4mmx1.6mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPM3808CGLE-AEC1-Z).

** Moisture Sensitivity Level Rating

*** Wettable flank

Note:

2) Contact MPS for details on additional output voltages that may be available.

TOP MARKING (MPM3808CGLE-AEC1)

MPYW
3808
CLLL
ME

MP: MPS prefix
Y: Year code
W: Week code
3808: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame

TOP MARKING (MPM3808CGLE-08-AEC1)

MPYW
3808
CLLL
ME08

MP: MPS prefix
Y: Year code
W: Week code
3808: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame
08: 0.8V fixed-output version of the MPM3808C

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TOP MARKING (MPM3808CGLE-12-AEC1)

MPYW
3808
CLLL
ME12

MP: MPS prefix
Y: Year code
W: Week code
3808: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame
12: 1.2V fixed-output version of the MPM3808C

TOP MARKING (MPM3808CGLE-18-AEC1)

MPYW
3808
CLLL
ME18

MP: MPS prefix
Y: Year code
W: Week code
3808: First four digits of the part number
C: FCCM
LLL: Lot number
M: Module
E: Wettable flank frame
18: 1.8V fixed-output version of the MPM3808C

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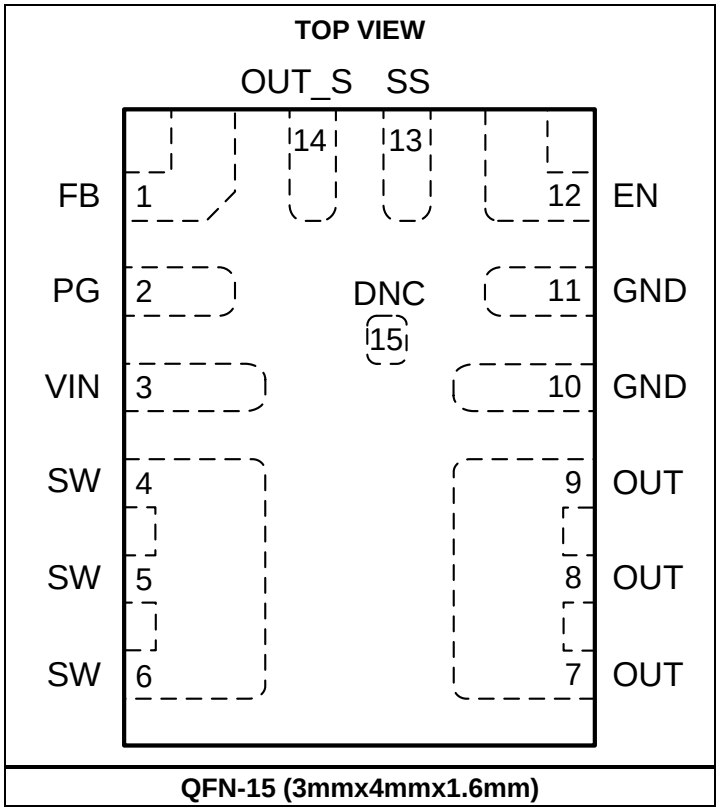
PACKAGE REFERENCE



QFN-15 (3mmx4mmx1.6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	FB	**Feedback.** In the adjustable-output version of the MPM3808C, connect the FB pin to an external resistor divider from the output to GND to set the output voltage (V_{OUT}). To set the regulation voltage, the FB voltage (V_{FB}) is compared to the 0.6V internal reference voltage (V_{REF}). In the fixed-output version of the MPM3808C, float this pin.
2	PG	**Power good indicator.** The PG pin is an open-drain output. Connect PG to a voltage source using an external resistor. When V_{FB} exceeds 90% of V_{REF}, PG is pulled high. If V_{FB} drops below 85% of V_{REF}, PG is pulled low to GND. Float this pin if it is not used.
3	VIN	**Input supply.** The MPM3808C operates across a 2.5V to 6V input voltage (V_{IN}) range. A decoupling capacitor is required to prevent large voltage spikes at the input.
4, 5, 6	SW	**Switch output.** The SW pin is the internal, high-side P-channel MOSFET drain, and is connected internally to the power inductor.
7, 8, 9	OUT	**Power output.** Connect the OUT pin to the load. An output capacitor (C_{OUT}) is required to reduce the voltage ripple.
10, 11	GND	**IC ground.** Connect the GND pin to the negative terminals of the input and output capacitors using large copper areas. Use several vias to connect GND to the ground plane.
12	EN	**Enable.** Pull EN below the 0.65V falling threshold to shut down the chip. Pull EN above the 0.9V rising threshold to enable the chip. There is an internal 2MΩ resistor from EN to ground.
13	SS	**Soft start.** Connect a capacitor between SS and GND to set the soft-start (SS) timer to avoid start-up inrush current. The minimum recommended soft-start capacitance (C_{SS}) is 1nF (for a typical SS current of 3μA) or 6.8nF (for a typical SS current of 16μA).
14	OUT_S	**Output sense.** OUT_S is the sensing pin for V_{OUT} and the discharge path to the 120Ω resistor load.
15	DNC	**Do not connect.** This pad is connected internally to SW. Do not route or place vias under this area.

ABSOLUTE MAXIMUM RATINGS (3)

All pins……-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (4) (8)
QFN-15 (3mmx4mmx1.6mm) 2.4W
Operating junction temperature .....150°C
Lead temperature…….....260°C
Storage temperature……...-65°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (5)
Charged device model (CDM).....Class 2b (6)

Recommended Operating Conditions

Input voltage (V_{IN})…….....2.5V to 6V
Output voltage (V_{OUT})…….0.6V to V_{IN} - 0.5V
Load current range……..…..0A to 3A
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (3mmx4mmx1.6mm)
JESD51-7…..…..……...65……14..°C/W (7)
EVM3808C-LE-00A.....53.....10..°C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom.
8) Measured on the standard EVB, a 4-layer, 2oz, copper PCB (6.3cmx6.3cm). The θ_{JC} value shows the thermal resistance from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO_RISING}			2.3	2.45	V
V_{IN} UVLO falling threshold	$V_{UVLO_FALLING}$			2.1		V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			0.2		V
V_{IN} quiescent current	I_Q	V_{EN} = 2V, V_{FB} = 0.63V, V_{IN} = 3.6V, T_J = 25°C		460	650	µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V, T_J = 25°C		0.01	1	µA
		V_{EN} = 0V, T_J = -40°C to +125°C (9)			3	
		V_{EN} = 0V, T_J = -40°C to +150°C			20	
V_{IN} over-voltage protection (OVP) rising threshold	$V_{IN_OVP_RISING}$	After V_{OUT}, OVP is enabled		6.15		V
V_{IN} OVP falling threshold	$V_{IN_OVP_FALLING}$			5.95		V
V_{IN} OVP hysteresis	$V_{IN_OVP_HYS}$			0.2		V
Frequency, Switches, and Inductors						
Switching frequency	f_{SW}		2000	2400	2700	kHz
Minimum on time (9)	t_{ON_MIN}	V_{IN} = 5V		50		ns
Minimum off time (9)	t_{OFF_MIN}	V_{IN} = 5V		80		ns
Maximum duty cycle	D_{MAX}			100		%
Switch leakage current	I_{SW_LKG}	V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = 25°C		0	1	µA
		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V or 6V, T_J = -40°C to +125°C (9)			30	
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{IN} = 5V		50	85	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{IN} = 5V		26	55	mΩ
Integrated inductor value (9)	L		376	470	564	nH
Integrated inductor DC resistance	R_L			25	65	mΩ
Integrated inductor saturation current (9)	I_{L_SAT}		4.8	5.4		A
Output and Regulation						
FB voltage (adjustable output)	V_{FB}	T_J = 25°C	0.594	0.6	0.606	V
		T_J = -40°C to +150°C	0.591	0.6	0.609	V
Output regulation voltage (fixed output)	V_{OUT_REG}	0.8V fixed output	0.784	0.8	0.816	V
		1.2V fixed output	1.176	1.2	1.224	V
		1.8V fixed output	1.764	1.8	1.836	V
FB input current	I_{FB}	Adjustable output		50	100	nA
		0.8V fixed output		2	5	µA
		1.2V fixed output		3	8	
		1.8V fixed output		5	10	
V_{OUT} discharge resistance	R_{DIS}	V_{EN} = 0V, V_{OUT} = 1.2V		120		Ω

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Enable (EN)						
EN rising threshold	V_{EN_RISING}			0.9	1.2	V
EN falling threshold	$V_{EN_FALLING}$		0.4	0.65		V
EN threshold hysteresis	V_{EN_HYS}			0.25		V
EN turn-on delay		Pull EN high to enable SW		100		µs
EN turn-off delay		Pull EN low to stop switching		11		µs
EN pull-down resistor				2		MΩ
EN input current	I_{EN}	V_{EN} = 2V		1.2		µA
		V_{EN} = 0V		0		µA
Soft Start (SS)						
Soft-start current	I_{SS}	Adjustable output, 1.2V fixed output, and 1.8V fixed output	1.5	3	4.5	µA
		0.8V fixed output	12	16	20	µA
Power Good (PG)						
PG rising threshold	PG_{VTH_RISING}	FB rising edge	87	90	93	% of V_{FB}
PG falling threshold	$PG_{VTH_FALLING}$	FB falling edge	82	85	88	% of V_{FB}
PG logic high voltage	V_{PG_HIGH}	V_{IN} = 5V, V_{FB} = 0.6V	4.9			V
PG sink current capability	V_{PG_LOW}	Sink 1mA			0.4	V
PG rising deglitch	t_{PGOOD_R}			70		µs
PG falling deglitch	t_{PGOOD_F}			70		µs
PG leakage current (high)		5V logic high			100	nA
PG self-bias		V_{IN} = 0V, V_{EN} = 0V, PG is pulled up between 3V and 6V via a 100kΩ resistor			0.7	V
Protections						
High-side (HS) peak current limit	I_{LIMIT_HS}		4	5	6	A
Low-side (LS) valley current limit	I_{LIMIT_LS}		2	3	4	A
LS reverse current limit		Current flows from SW to GND		1.2		A
Thermal shutdown (9)	T_{SD}			170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C
Output over-voltage (OV) threshold	V_{OVP}		110	115	120	% of V_{FB}
Output OVP hysteresis	V_{OVP_HYS}			10		% of V_{FB}
OVP delay				2		µs

Note:

9) Not tested in production. Guaranteed by design and characterization.

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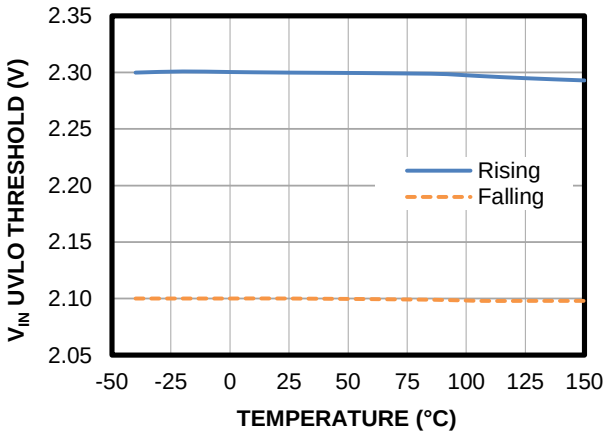
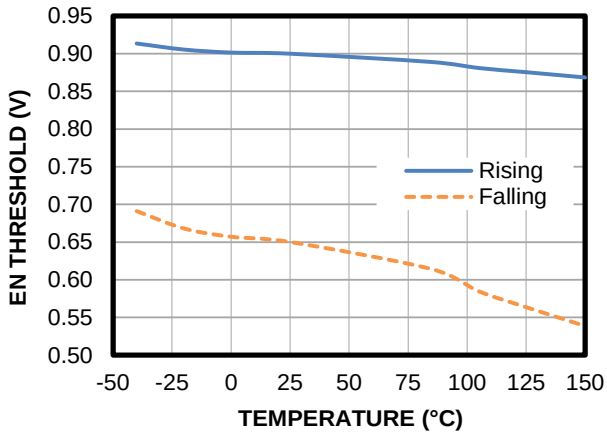
TYPICAL CHARACTERISTICS

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

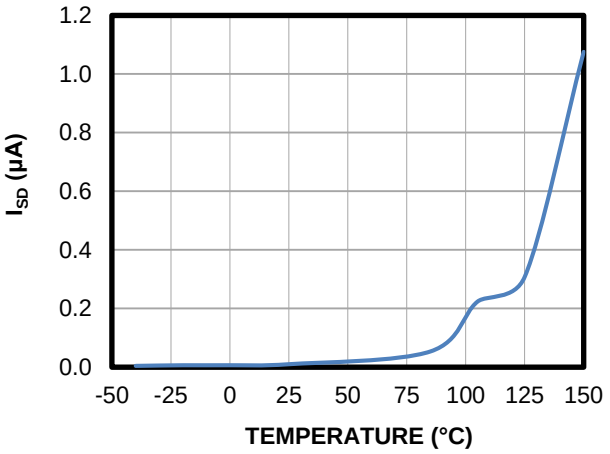
V_{IN} UVLO Threshold vs. Temperature



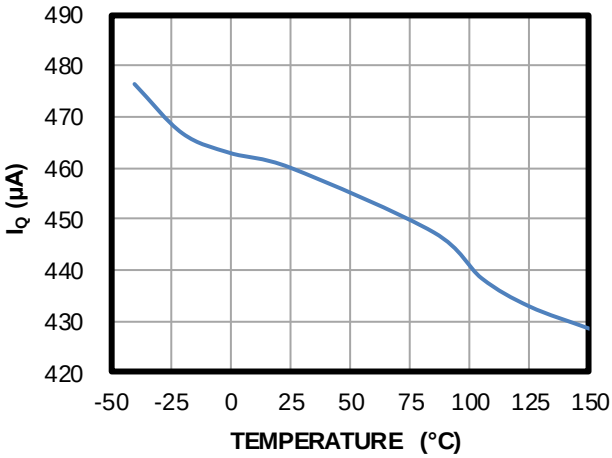
EN Threshold vs. Temperature



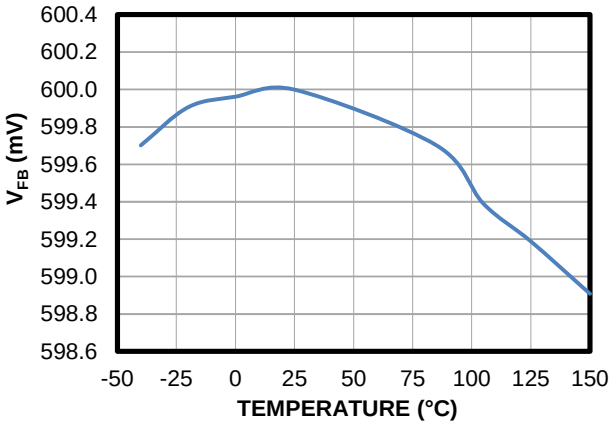
Shutdown Current vs. Temperature



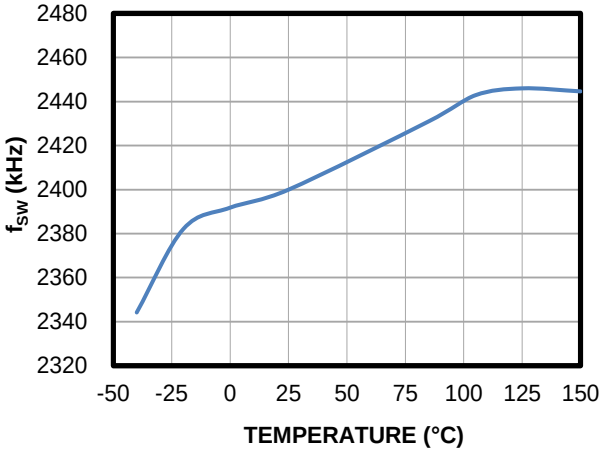
Quiescent Current vs. Temperature



Feedback Voltage vs. Temperature



Switching Frequency vs. Temperature



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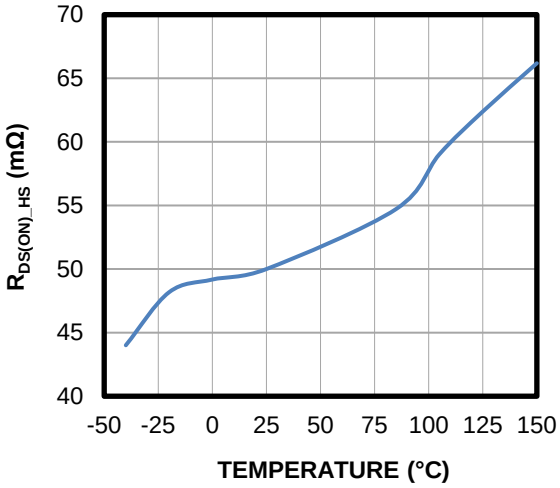
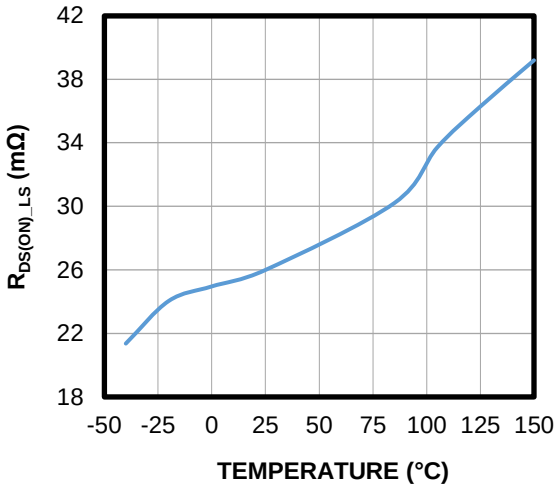
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

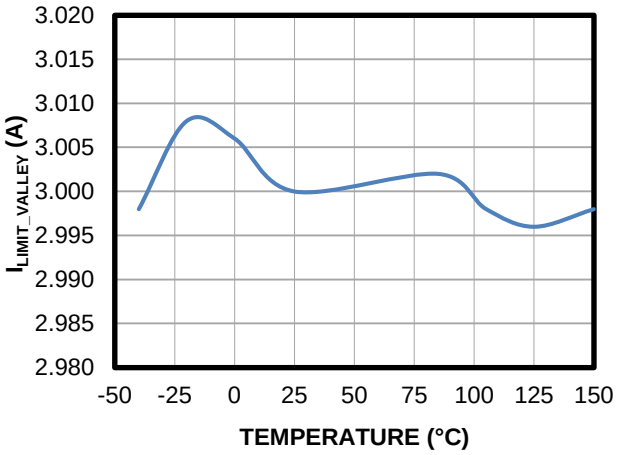
HS-FET On Resistance vs. Temperature



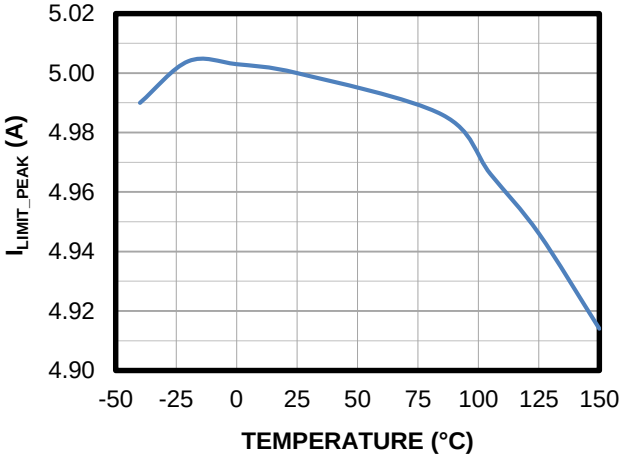
LS-FET On Resistance vs. Temperature



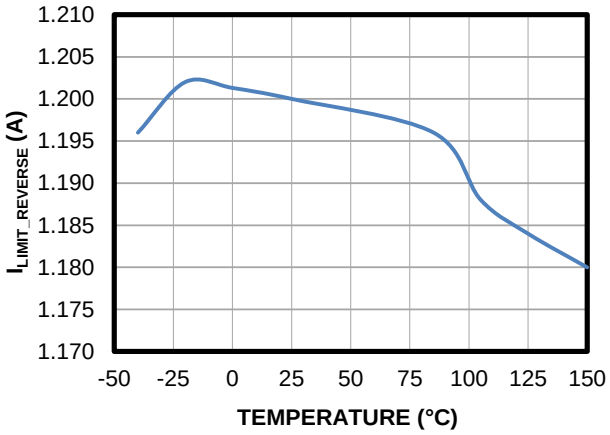
N-Channel MOSFET Valley Current Limit vs. Temperature



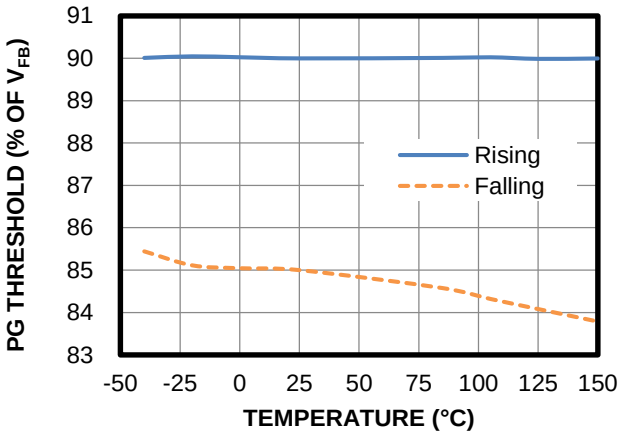
P-Channel MOSFET Peak Current Limit vs. Temperature



LS-FET Reverse Current Limit vs. Temperature



PG Threshold vs. Temperature



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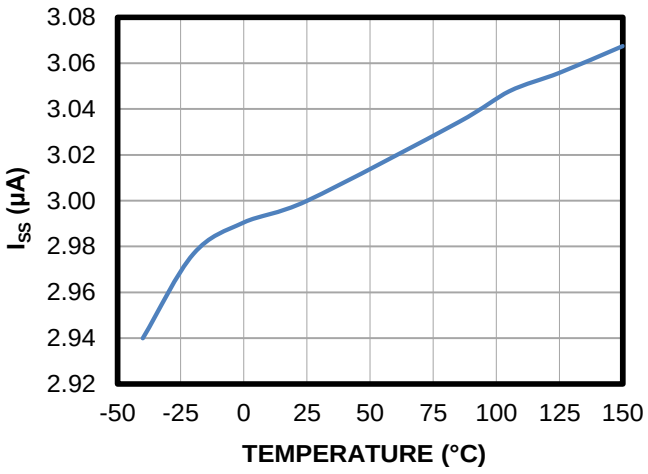
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 3.6V, T_J = -40°C to +150°C, unless otherwise noted.

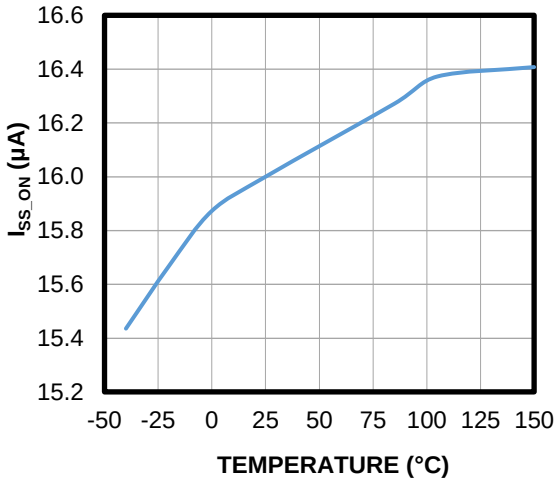
Soft-Start Current vs. Temperature

MPM3808C, MPM3808C-12, and MPM3808C-18



Soft-Start Current vs. Temperature

MPM3808C-08



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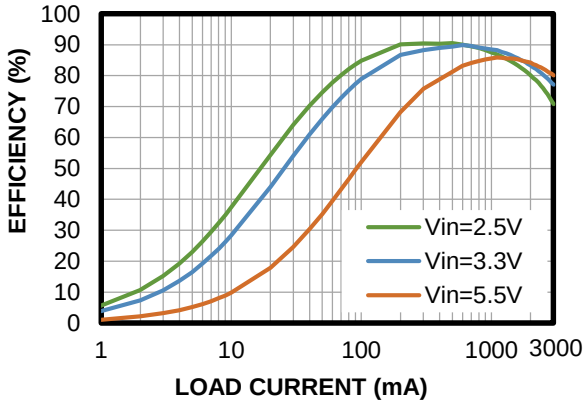
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

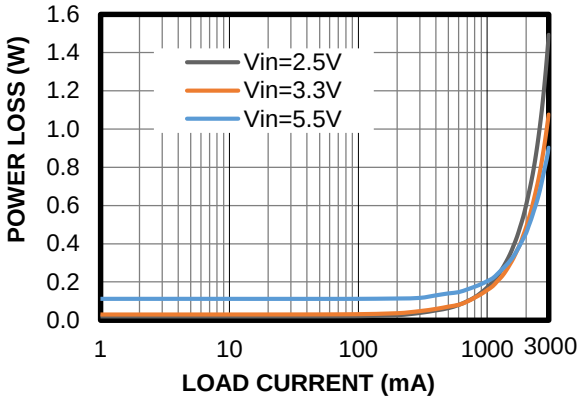
Efficiency vs. Load Current

V_{OUT} = 1.2V



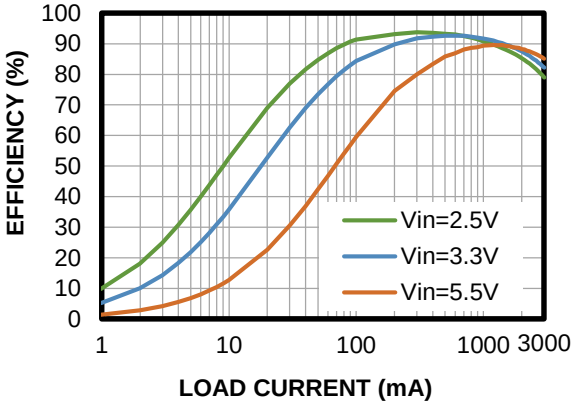
Power Loss vs. Load Current

V_{OUT} = 1.2V



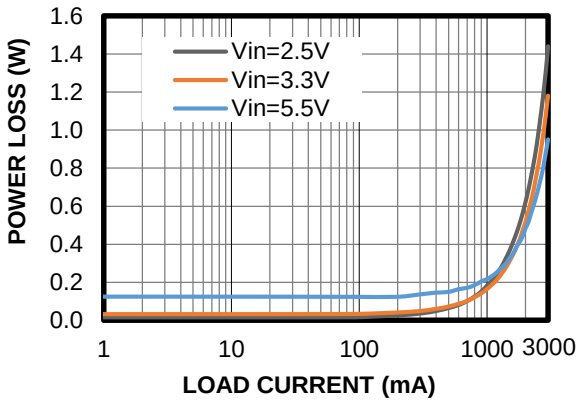
Efficiency vs. Load Current

V_{OUT} = 1.8V



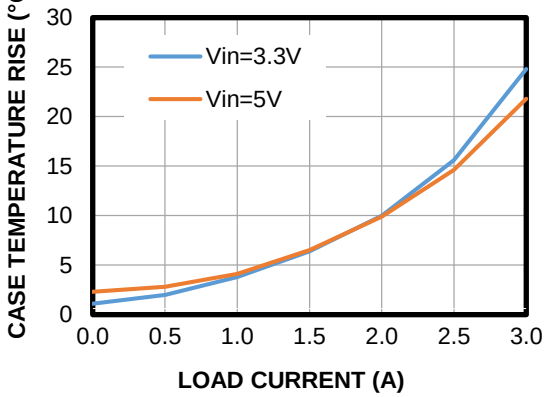
Power Loss vs. Load Current

V_{OUT} = 1.8V



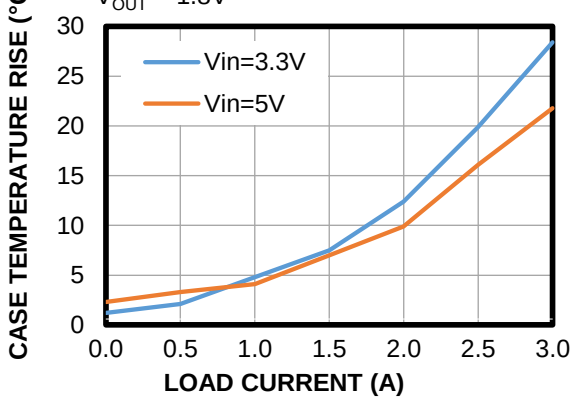
Case Temperature Rise

V_{OUT} = 1.2V



Case Temperature Rise

V_{OUT} = 1.8V



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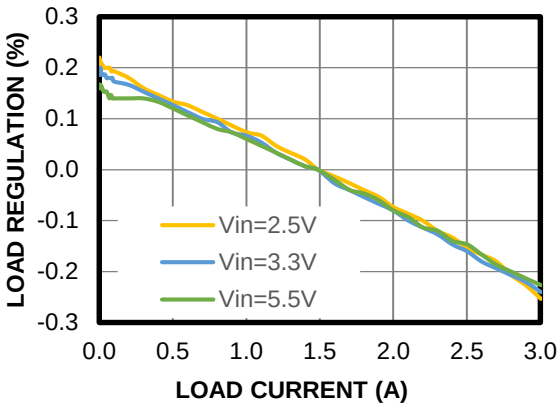
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

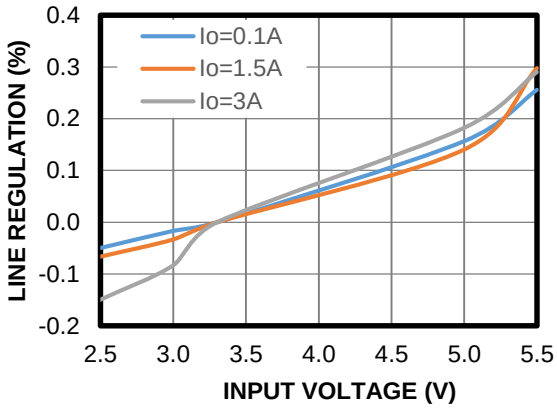
Load Regulation

V_{OUT} = 1.2V



Line Regulation

V_{OUT} = 1.2V



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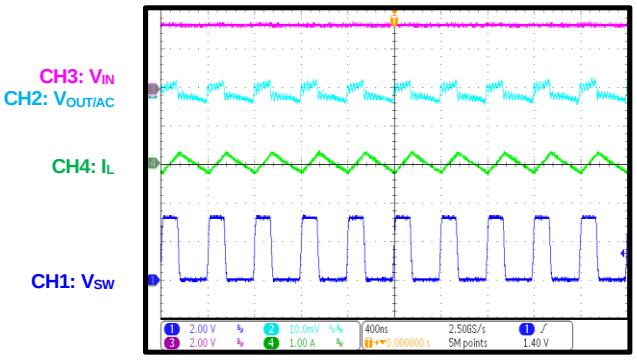
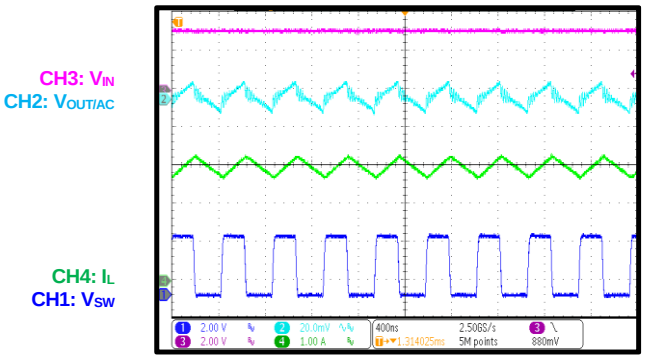
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

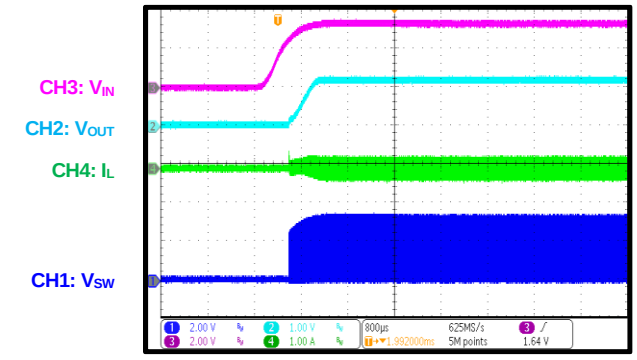
Steady State
I_{OUT} = 0A



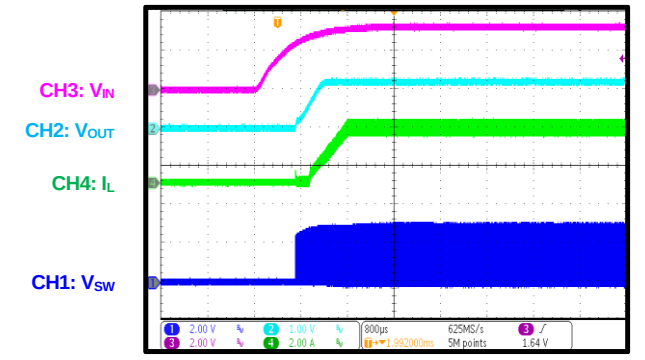
Steady State
I_{OUT} = 3A



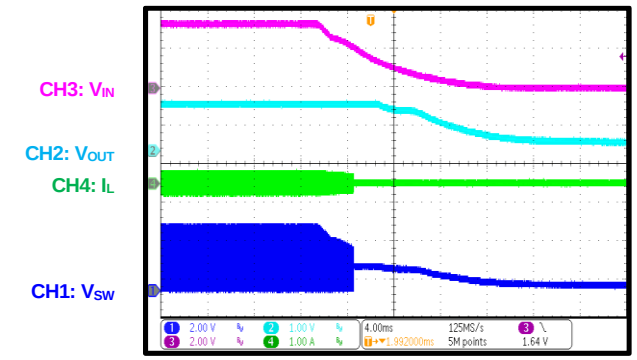
Start-Up through VIN
I_{OUT} = 0A



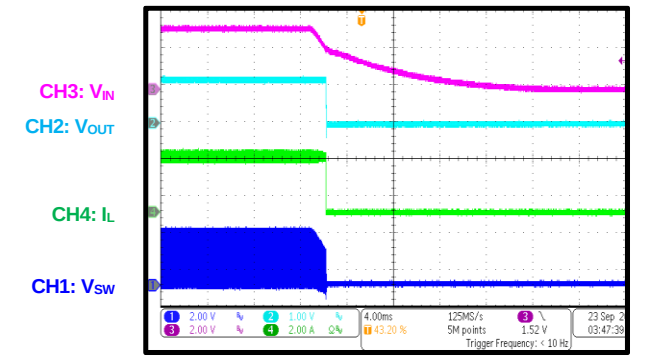
Start-Up through VIN
I_{OUT} = 3A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 3A



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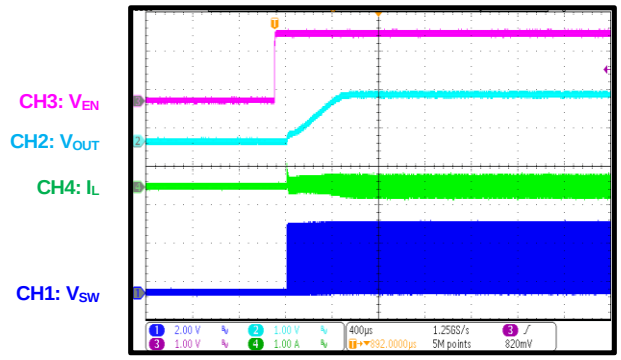
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

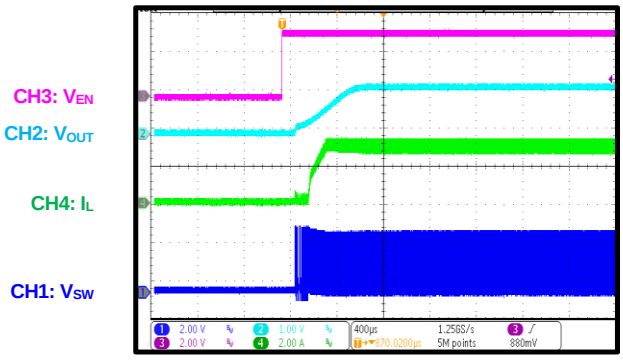
Start-Up through EN

I_{OUT} = 0A



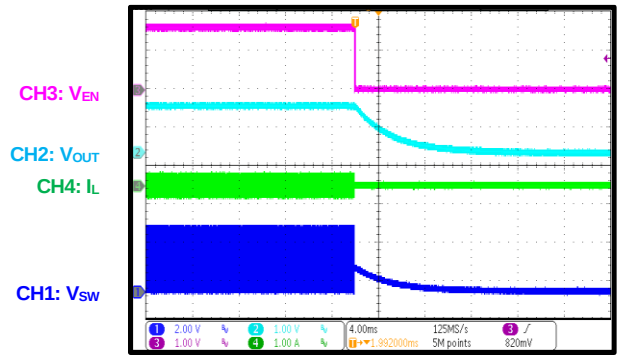
Start-Up through EN

I_{OUT} = 3A



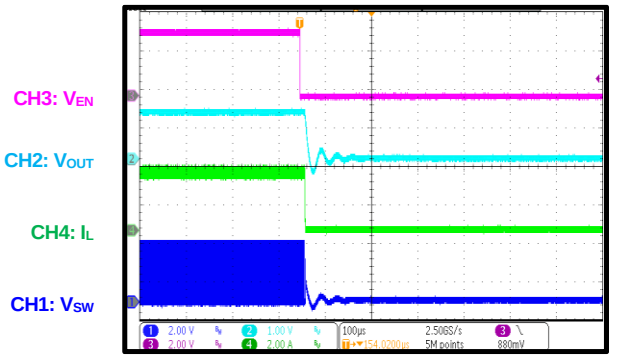
Shutdown through EN

I_{OUT} = 0A



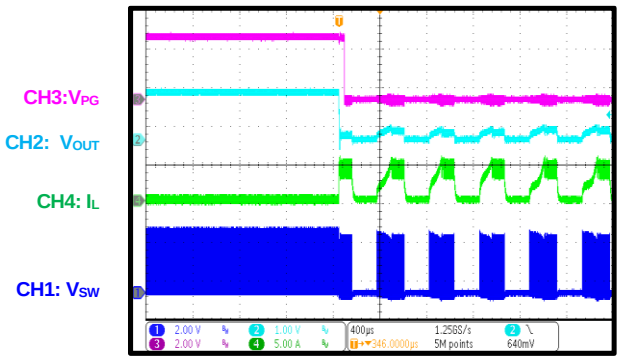
Shutdown through EN

I_{OUT} = 3A



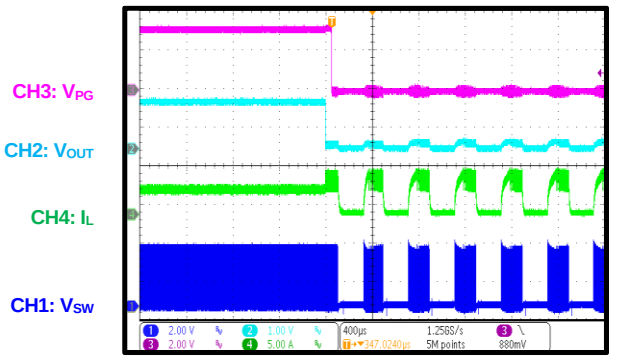
SCP Entry

I_{OUT} = 0A



SCP Entry

I_{OUT} = 3A



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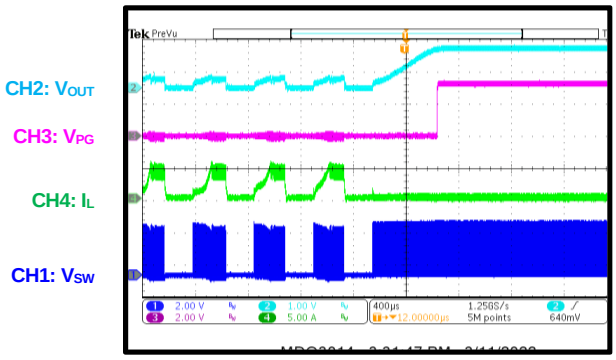
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

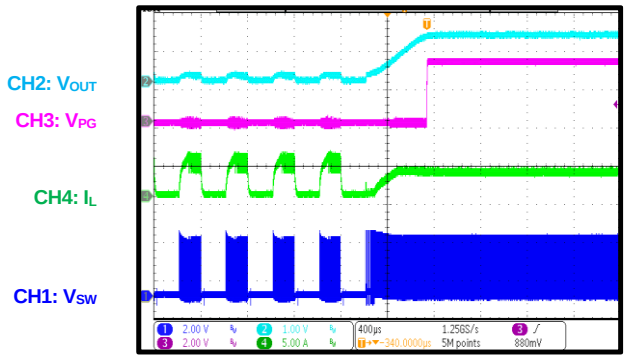
SCP Recovery

I_{OUT} = 0A



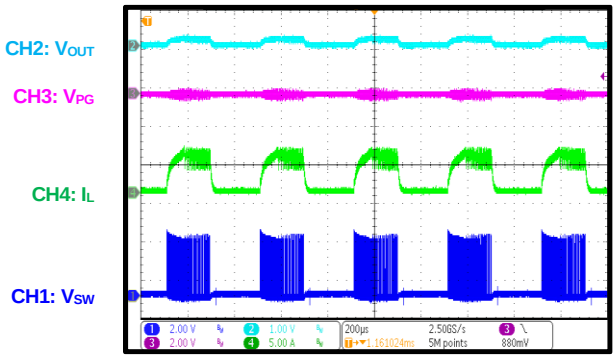
SCP Recovery

I_{OUT} = 3A



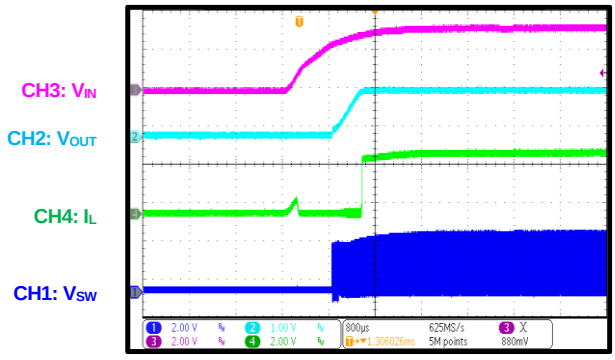
Short-Circuit Protection

I_{OUT} = 0A



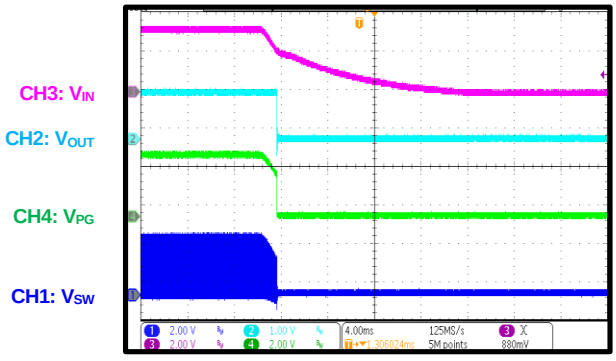
PG Start-Up through VIN

I_{OUT} = 3A



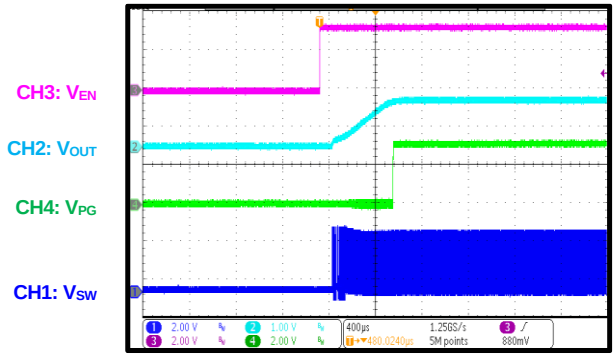
PG Shutdown through VIN

I_{OUT} = 3A



PG Start-Up through EN

I_{OUT} = 3A



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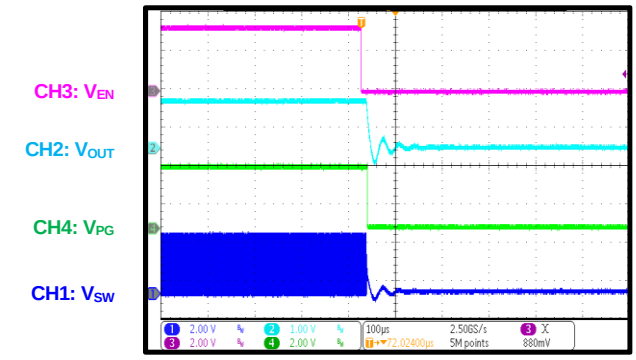
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 22µF, T_A = 25°C, unless otherwise noted.

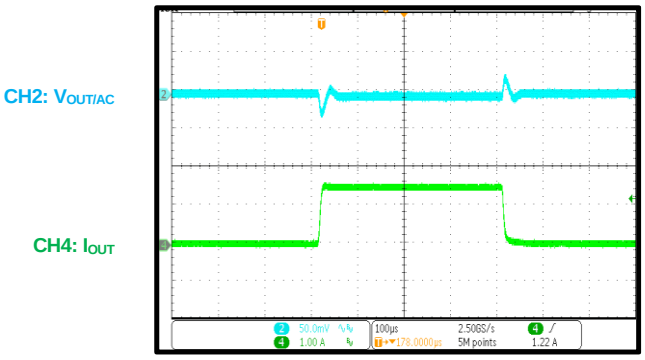
PG Shutdown through EN

I_{OUT} = 3A



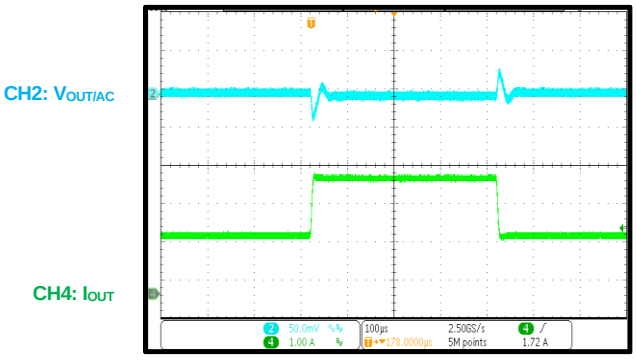
Load Transient Response

I_{OUT} = 0A to 1.5A, 1A/µs



Load Transient Response

I_{OUT} = 1.5 to 3A, 1A/µs



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FUNCTIONAL BLOCK DIAGRAM

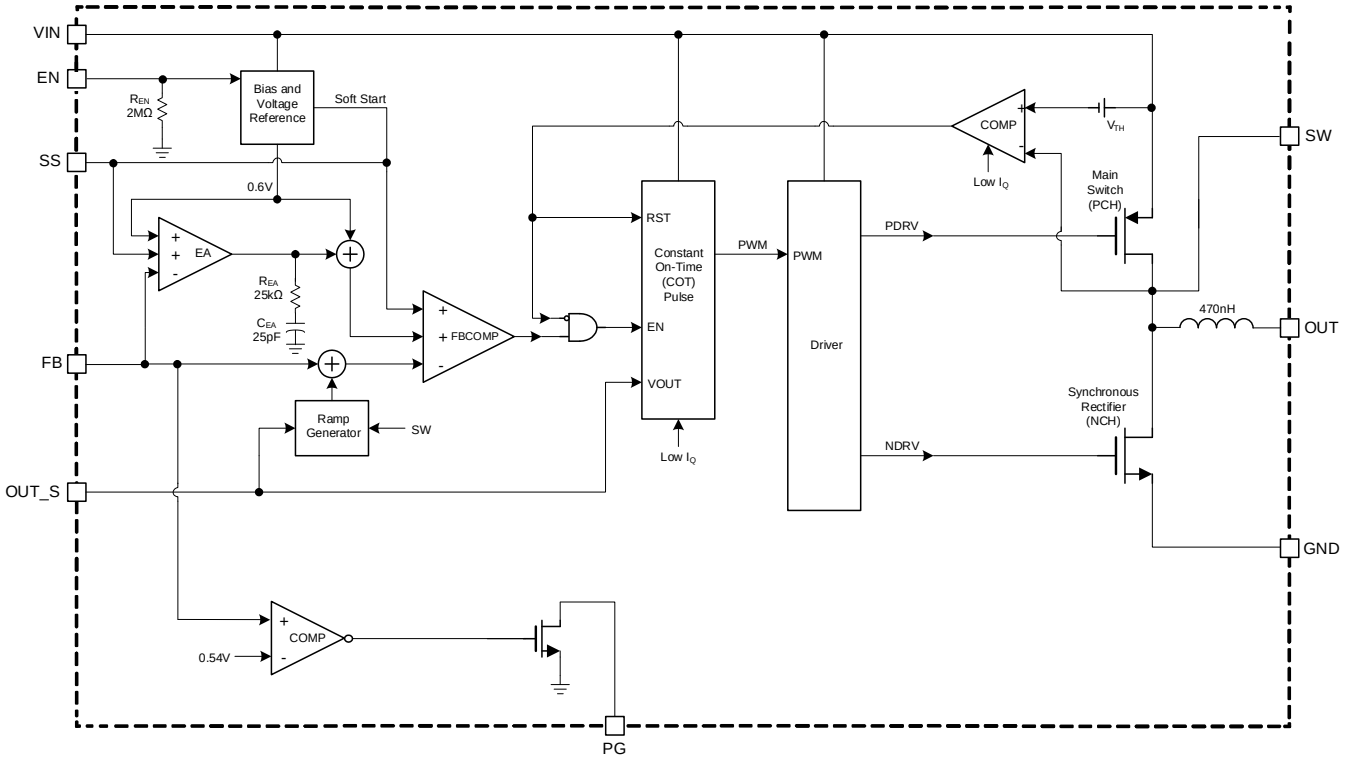

Figure 1: Functional Block Diagram (Adjustable Output)

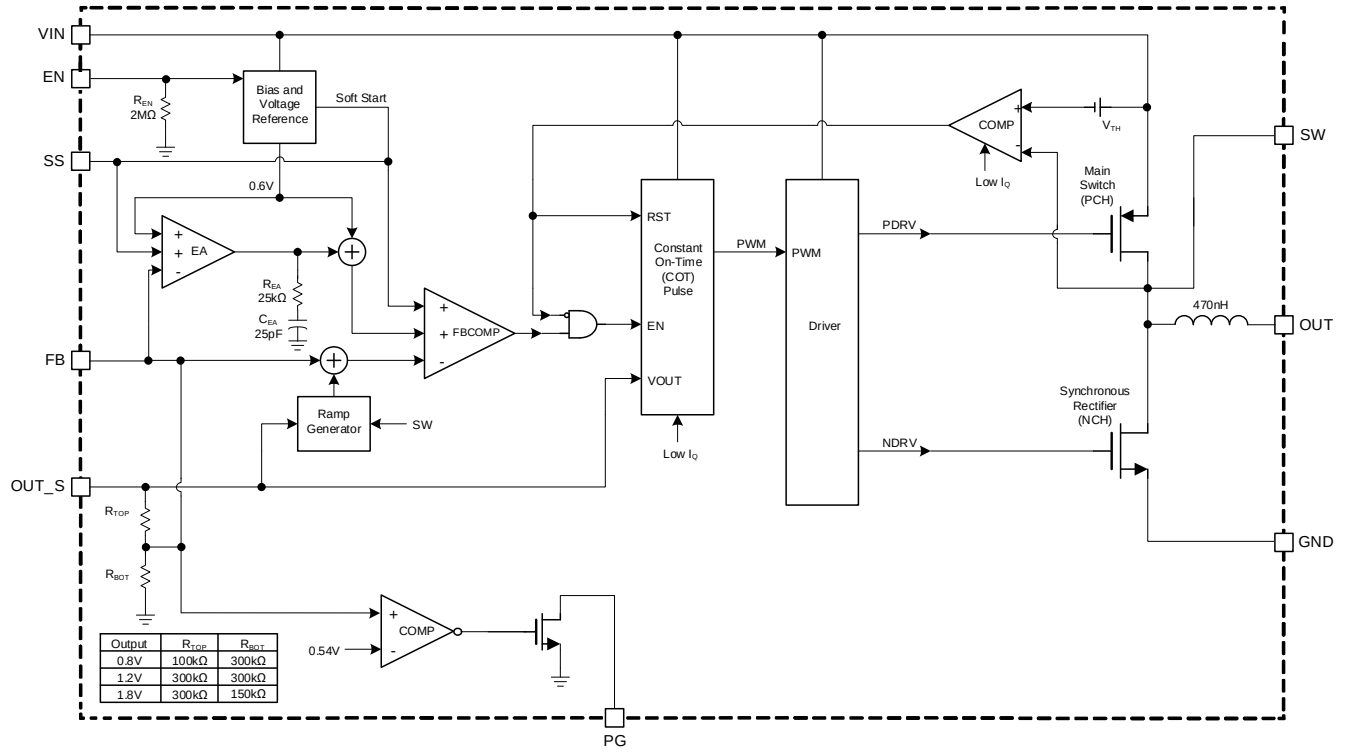

Figure 2: Functional Block Diagram (Fixed Output)

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OPERATION

The MPM3808C employs input voltage (V_{IN}) feed-forward and constant-on-time (COT) control to stabilize the switching frequency (f_{SW}) across the entire V_{IN} range. The device can achieve 3A of output current (I_{OUT}) across a 2.5V to 6V V_{IN} range, with excellent load and line regulation. The output voltage (V_{OUT}) can be regulated to as low as 0.6V. A 100% maximum duty cycle can be reached in low-dropout (LDO) mode.

Constant-On-Time (COT) Control and Forced Continuous Conduction Mode (FCCM)

The MPM3808C's COT control provides a simpler control loop and faster transient response. The switching cycles have a fixed minimum off time (t_{OFF_MIN}) to prevent inductor current (I_L) runaway during load transients. If the low-side MOSFET (LS-FET) turns on, it remains on for at least t_{MIN_OFF} (typically 80ns). The high-side MOSFET (HS-FET) turns on once the feedback (FB) voltage (V_{FB}) drops below the reference voltage (V_{REF}). This indicates an insufficient V_{OUT}. V_{IN} feed-forward allows the device to maintain a nearly constant f_{SW} across the input range and load range. The f_{SW} on time (t_{ON}) can be calculated with Equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 400ns \quad (1)$$

To improve frequency stability and reduce output voltage ripple, the MPM3808C operates in forced continuous conduction mode (FCCM), which has a constant f_{SW} (see Figure 3).

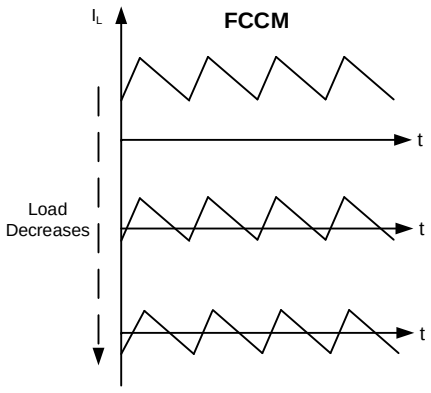

Figure 3: FCCM

Enable (EN) Control

The enable (EN) pin is a digital control pin that turns the MPM3808C on and off. Pull EN above 0.9V to turn the converter on; pull EN below 0.65V or float EN to turn it off. Pulling EN to GND also disables the device. There is an internal 2MΩ resistor connected between EN and GND.

Output Discharge

If the MPM3808C shuts down, the device initiates output discharge mode. The internal discharge MOSFET provides a resistive discharge path for the output capacitor (C2) between the OUT pin and GND. To block the output discharge path, add an external capacitor between V_{OUT} and the OUT pin.

Soft Start (SS)

The MPM3808C features external soft start (SS). To avoid overshoot during start-up, the SS pin ramps up V_{OUT} at a controlled slew rate. SS's charge current is typically 3μA (typically 16μA for the MPM3808C-08). The soft-start time (t_{SS}) is determined by the external SS capacitor (C_{SS}). t_{SS} can be calculated with Equation (2):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times 0.6V}{I_{SS}(\mu A)} \quad (2)$$

Where I_{SS} is the internal SS charge current (3μA or 16μA).

The minimum C_{SS} is recommended to be 1nF or 6.8nF.

The MPM3808C has a pre-biased start-up function. Once EN is pulled above 0.9V, the converter starts up regardless of any pre-biased voltage on the output. Pre-biased start-up works even while the output discharge path is blocked.

Peak Current Limit and Valley Current Limit

Both the HS-FET and LS-FET feature current-limit protection. If I_L reaches the HS-FET's peak current limit (I_{LIMIT_PEAK}) threshold (typically 5A), the HS-FET turns off and the LS-FET turns on to discharge the energy. The HS-FET does not turn on again until I_L drops below the valley current limit (I_{LIMIT_VALLEY}) threshold (typically 3A). This prevents current runaway during overload and short-circuit events. The valley current limit is blocked unless the HS-FET turns off due to the triggered peak current limit.

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Short-Circuit Protection (SCP) and Recovery

If a short-circuit condition occurs, the MPM3808C reaches its current limit immediately. Meanwhile, V_{OUT} drops until V_{FB} falls below 50% of V_{REF}, which is considered an output dead short. Short-circuit protection (SCP) with hiccup mode is triggered to periodically restart the part. In hiccup mode, the output power stage is disabled, and the SS voltage (V_{SS}) is discharged. Once V_{SS} is discharged completely, the device initiates a new SS. This process repeats until the fault condition is removed.

Over-Voltage Protection (OVP)

The MPM3808C monitors V_{FB} to detect over-voltage (OV) conditions. If V_{FB} exceeds 115% of V_{REF}, then the converter enters its dynamic regulation period. During this period, the LS-FET remains on until its current reaches -1.2A. This process discharges V_{OUT} to keep it within its normal range. If the OV condition still remains after this process, there is a 1.5µs delay before the LS-FET turns on again. Once V_{FB} falls below 105% of V_{REF}, the converter exits the regulation period.

If the dynamic regulation period cannot prevent V_{OUT} from increasing, and a 6.1V V_{IN} is detected, then over-voltage protection (OVP) is triggered. The device stops switching until V_{IN} drops below 6V. Once V_{IN} drops below 6V, the MPM3808C resumes normal operation.

Power Good (PG) Indicator

The MPM3808C has a power good (PG) output to indicate whether the converter is operating normally after start-up. PG is the open drain of an internal MOSFET. It is recommended that this MOSFET's maximum on resistance ($R_{DS(ON)}$) be below 400Ω. PG can be connected to V_{IN} or an external voltage source via an external resistor (10kΩ to 100kΩ). Once V_{IN} is applied, the MOSFET turns on and PG is pulled to GND before SS is ready. After V_{FB} reaches 90% of V_{REF}, PG is pulled high by the external voltage source. If V_{FB} drops to 85% of V_{REF}, then the PG voltage (V_{PG}) is pulled to GND to indicate an output failure.

If VIN and EN are not available, and PG is pulled up via an external power supply, then PG self-biases and asserts. If a 100kΩ pull-up resistor is being used, then V_{PG} should be below 0.7V.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the MPM3808C's adjustable V_{OUT}, which can be set from 0.6V to V_{IN} - 0.5V. Select a feedback (FB) resistor (R1) to reduce the V_{OUT} leakage current (typically between 10kΩ and 100kΩ). R2 can then be calculated with Equation (3):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6} - 1} \quad (3)$$

Figure 4 shows the FB network.

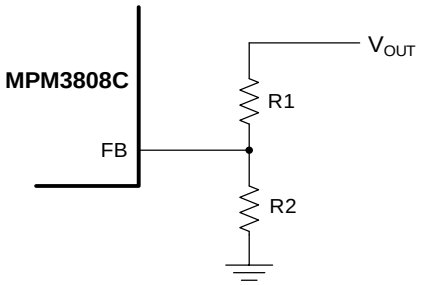

Figure 4: Feedback Network

Table 1 shows the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1	30.9 (1%)	47 (1%)
1.2	100 (1%)	100 (1%)
1.8	36 (1%)	18 (1%)
2.5	51 (1%)	16 (1%)
3.3	68 (1%)	15 (1%)

For the fixed-output version of the MPM3808C, it is not necessary to connect the external divider resistor. FB can be floated.

Frequency Scaling at Low Input Voltages

Under heavy-load conditions, the HS-FET voltage decreases as t_{ON} increases, and the duty cycle is extended. If t_{OFF_MIN} is reached at a low V_{IN} and under heavy-load conditions, then f_{SW} scales down. To maintain a constant f_{SW} during heavy-load operation, a larger V_{OUT} is required for a larger V_{IN}. For a 1.8V V_{OUT} at a 3A load, V_{IN} should exceed 2.9V to keep f_{SW} above 2MHz.

If the frequency begins to scale down, V_{IN} can be estimated with Equation (4):

$$V_{IN} = \frac{V_{OUT} + R_{DS(ON)_HS} \times I_{OUT}}{1 - \frac{t_{OFF_MIN}}{400 \times 10^{-9}}} \quad (4)$$

Where the maximum t_{OFF_MIN} is 125ns. (10)

Note:

10) Guaranteed by design and bench characterization. Not tested in production.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended due to their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. Higher output voltages may require a 22µF capacitor to increase system stability.

The input capacitor (C1) requires an adequate ripple current rating to absorb the switching I_{IN}.

C1's RMS current rating (I_{C1}) can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case scenario occurs at $V_{IN} = 2 \times V_{OUT}$, which can be calculated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half of the maximum load current.

C1 can be an electrolytic, tantalum, or ceramic capacitor. When using electrolytic or tantalum capacitors, place a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that the capacitor has sufficient capacitance to prevent excessive voltage ripple at the input.

The V_{IN} ripple (ΔV_{IN}) can be estimated with Equation (7):

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$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC V_{OUT}. It is recommended to use ceramic capacitors for C2. Low-ESR capacitors are recommended to effectively limit the V_{OUT} ripple (ΔV_{OUT}). ΔV_{OUT} can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductance, and R_{ESR} is C2's equivalent series resistance (ESR).

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Ceramic capacitors with X7R or X5R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

C2's characteristics can also affect the stability of the regulation system.

Output Discharge Blocking

If the device is disabled, an internal resistive discharge path between the OUT_S pin and GND is enabled to discharge C2. The discharge path can be blocked by adding an external capacitor between V_{OUT} and the OUT_S pin (see Figure 5).

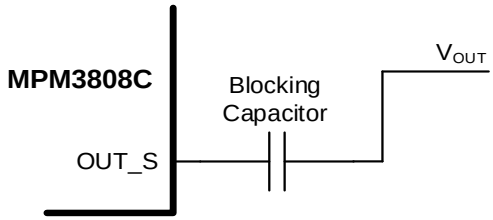

Figure 5: Circuit with V_{OUT} Discharge Blocking

Discharge blocking is supported by the adjustable-output version. For the fixed-output versions, the OUT_S pin should be directly connected to the output to regulate V_{OUT}.

To avoid influencing the loop and load transient, select a ≥10nF blocking capacitor. It is recommended to use a 10nF to 100nF blocking capacitor. A larger-value blocking capacitor does not have an impact on loop performance, but it is physically larger and is typically unnecessary for the best results.

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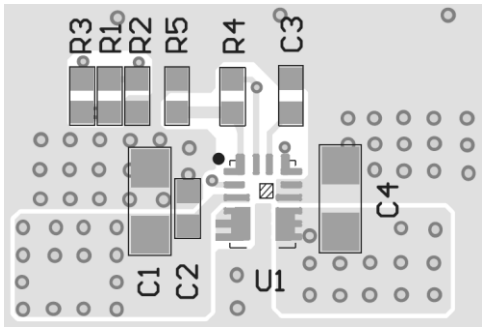
PCB Layout Guidelines (11)

The MPM3808C's integrated inductor simplifies the PCB layout design, but some considerations must still be taken to ensure proper operation. A 4-layer layout is recommended to improve EMC and thermal performance, although the device can operate sufficiently in a 2-layer layout. For the best results, refer to Figure 6 and follow the guidelines below:

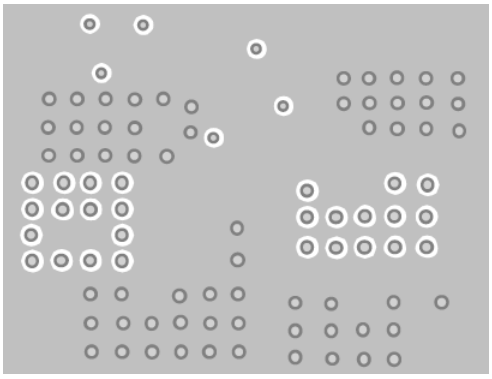
1. Place the high-current paths (GND and VIN) very close to the device using short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to VIN as possible.
4. Place several vias close to the capacitor's GND terminal and the GND pin on the IC to minimize high-frequency noise.
5. Place the FB resistors as close as possible to the FB pin to ensure that the trace connected to FB is as short as possible.
6. Use multiple vias to connect the power planes to the internal layer.

Note:

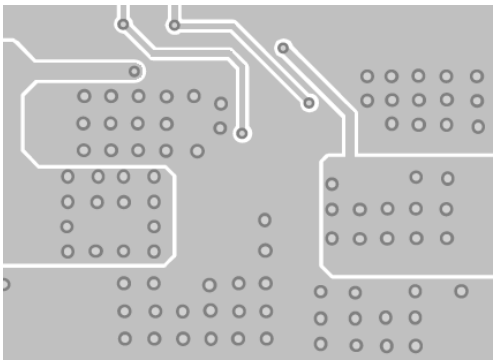
11) The recommended PCB layout is based on Figure 7 on page 24.



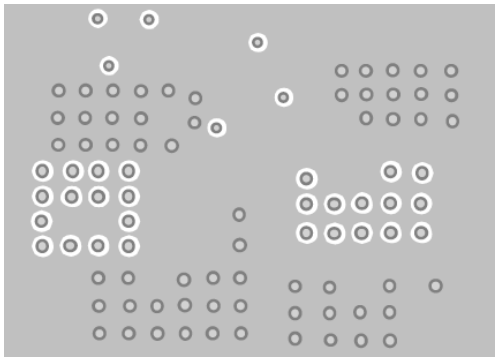
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer and Bottom Silk

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

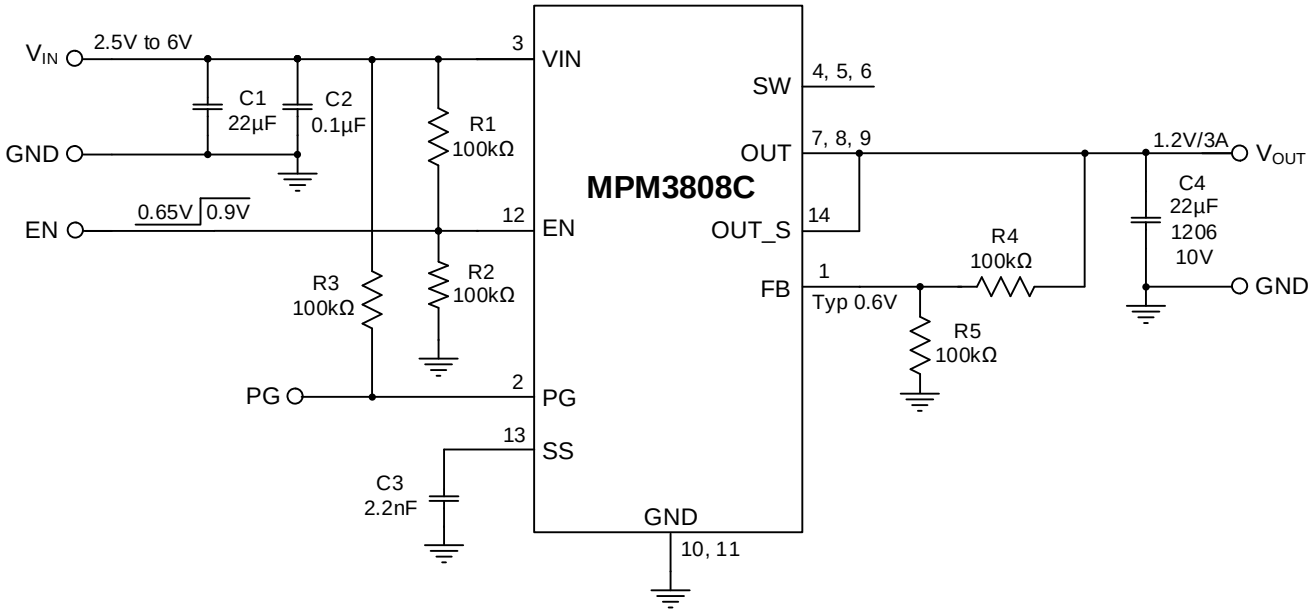

Figure 7: Typical Application (Adjustable Output, V_{OUT} = 1.2V)

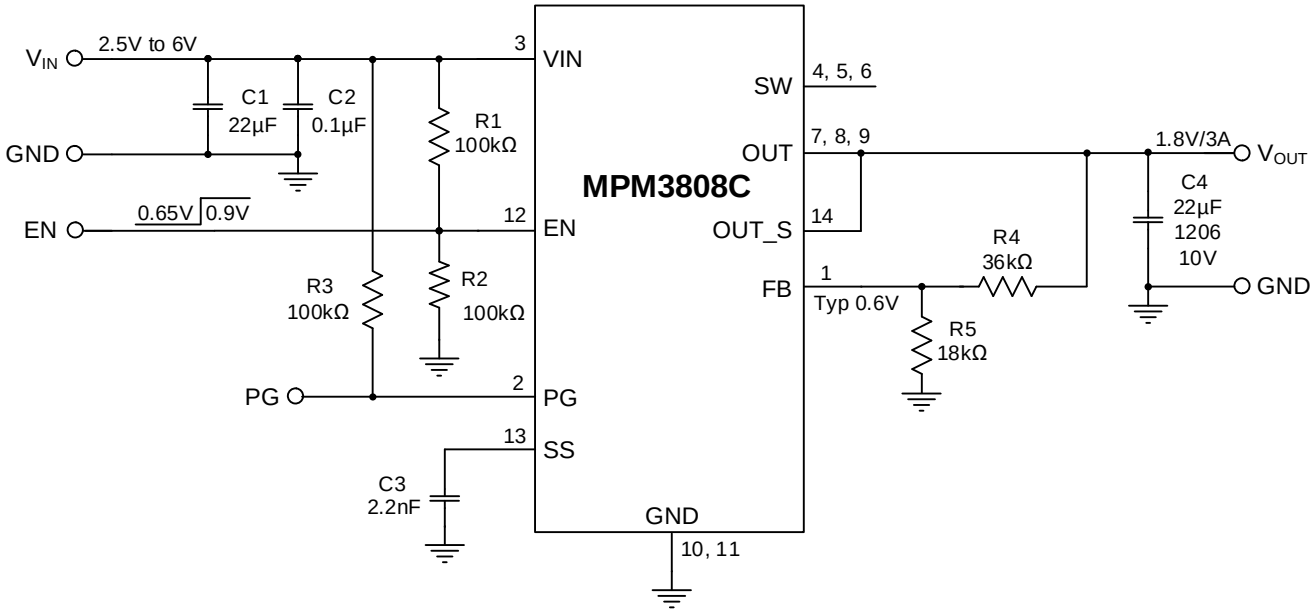

Figure 8: Typical Application (Adjustable Output, V_{OUT} = 1.8V)

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TYPICAL APPLICATION CIRCUITS *(continued)*

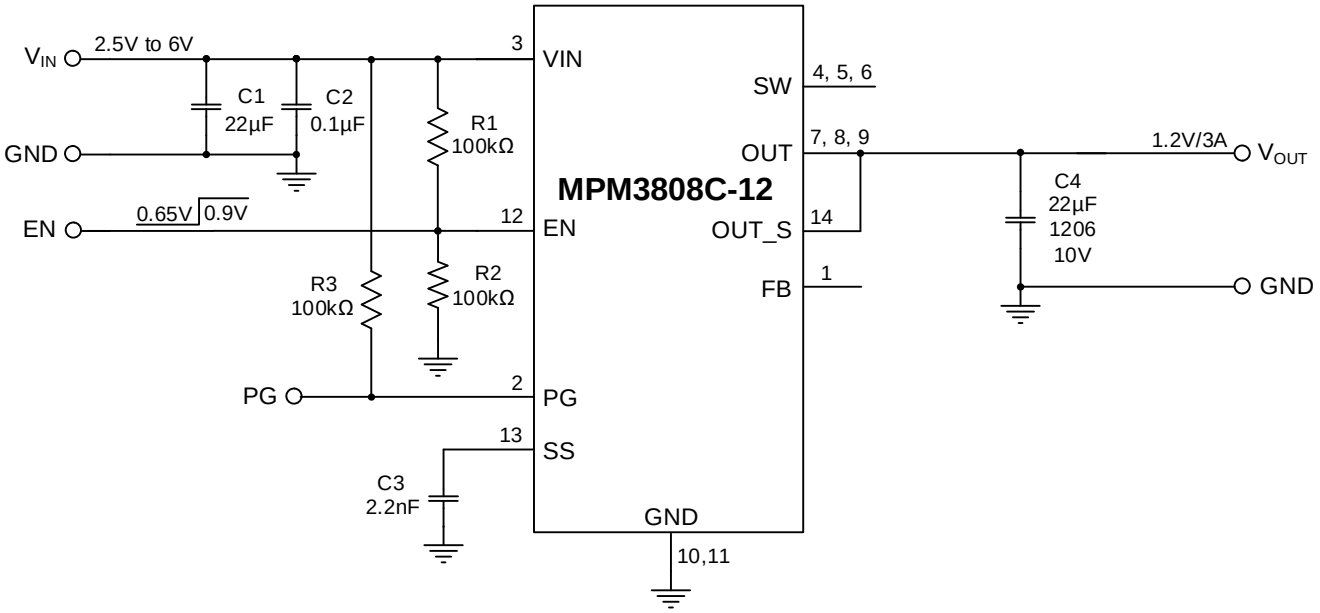

Figure 9: Typical Application (Fixed Output, V_{OUT} = 1.2V)

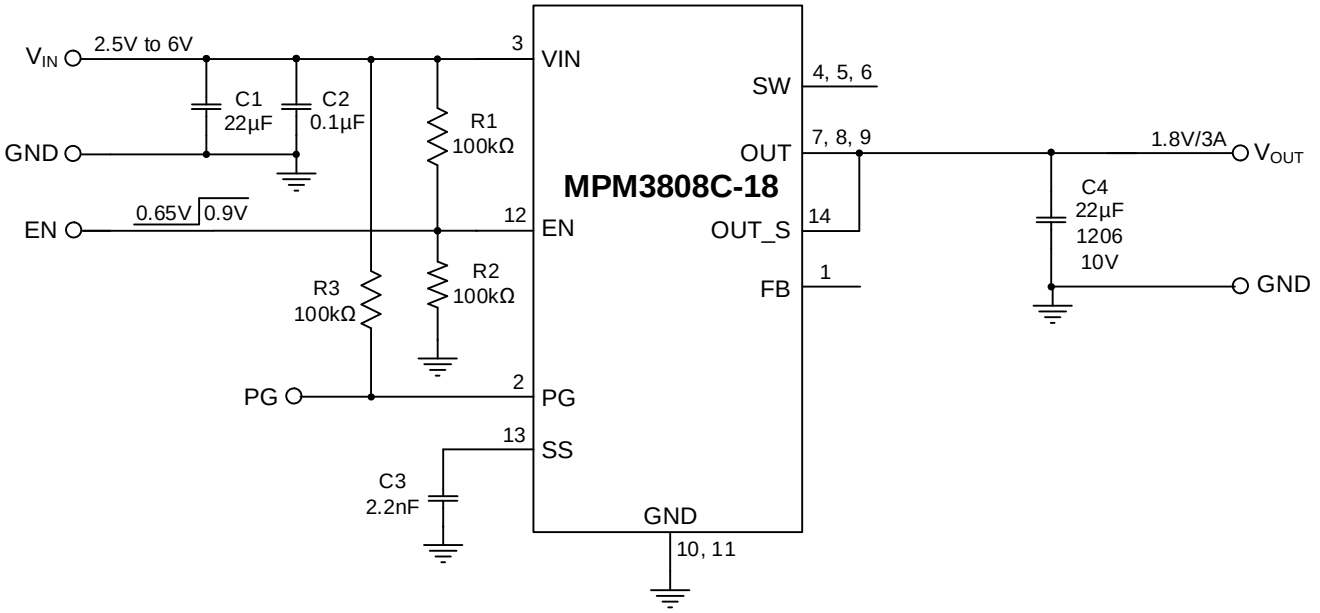

Figure 10: Typical Application (Fixed Output, V_{OUT} = 1.8V)

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TYPICAL APPLICATION CIRCUITS *(continued)*

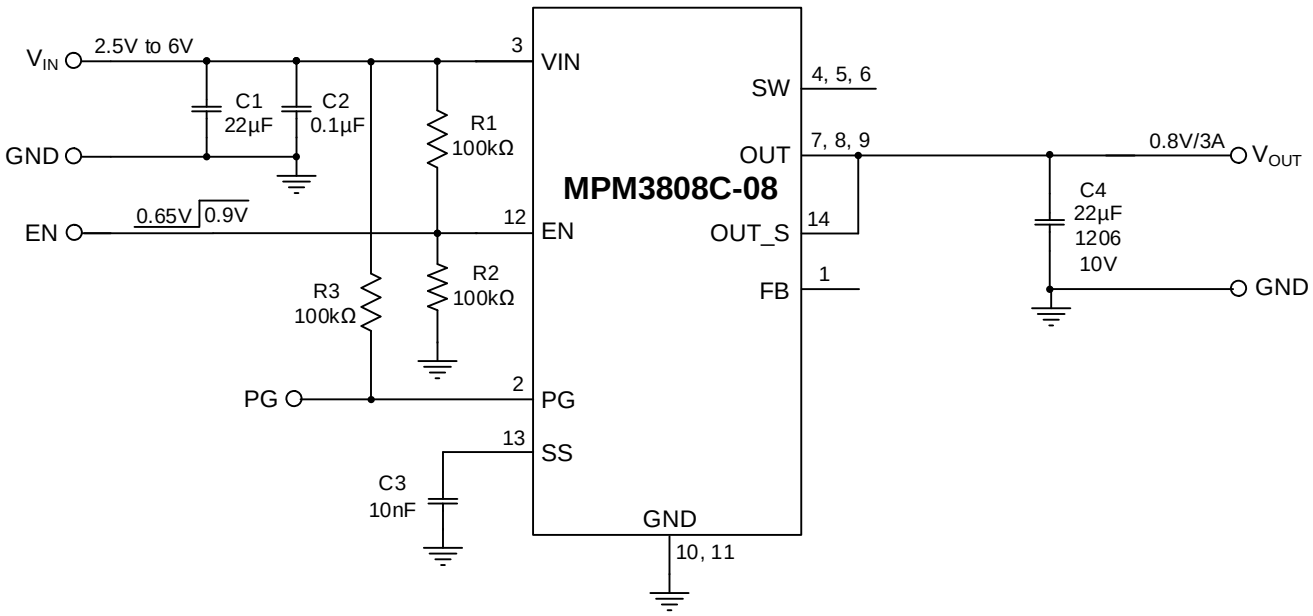

Figure 11: Typical Application (Fixed Output, V_{OUT} = 0.8V)

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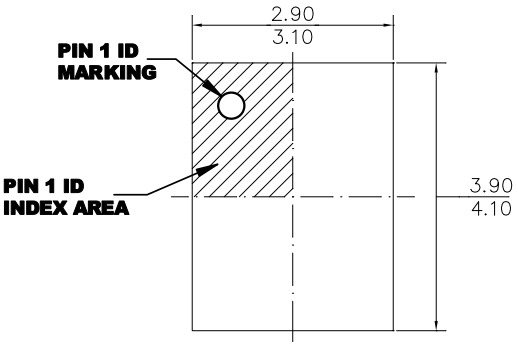
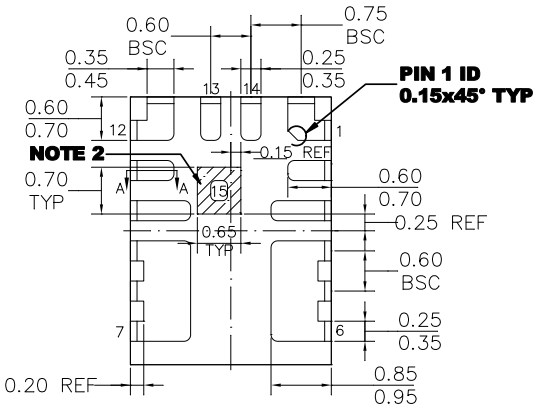
PACKAGE INFORMATION

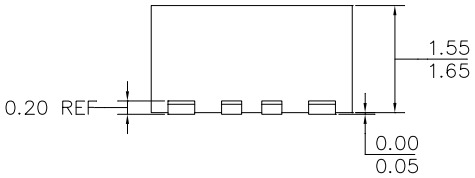
QFN-15 (3mmx4mmx1.6mm)
Wettable Flank



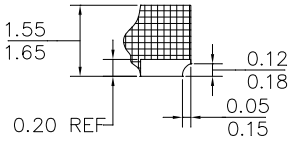
TOP VIEW



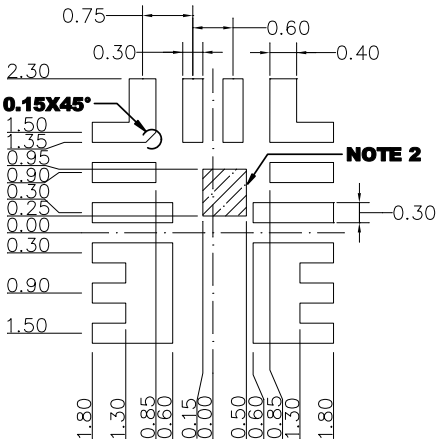
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) THE LEAD SIDE IS WETTABLE.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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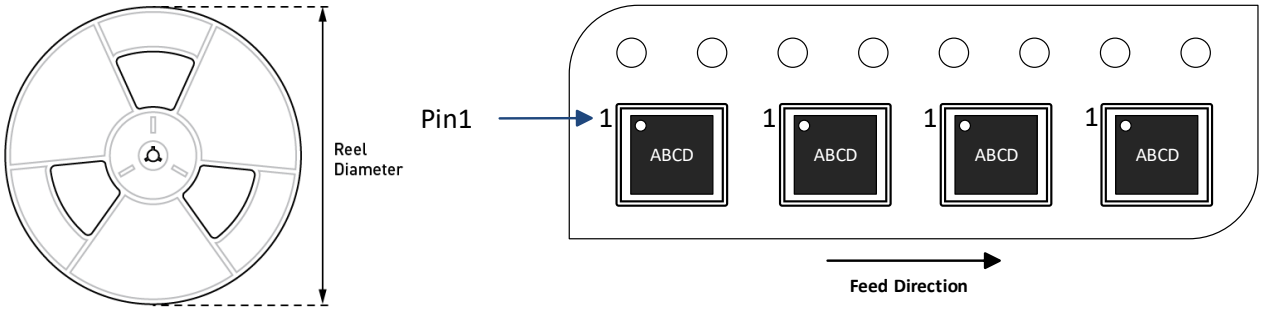
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3808CGLE-AEC1-Z	QFN-15 (3mmx 4mmx 1.6mm)	2500	N/A	N/A	13in	12mm	8mm
MPM3808CGLE-08-AEC1-Z							
MPM3808CGLE-12-AEC1-Z							
MPM3808CGLE-18-AEC1-Z							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/8/2022	Initial Release	-
1.1	3/8/2024	Updated the maximum V_{IN} from 5.5V to 6V, updated the integrated internal power MOSFETs' $R_{DS(ON)}$ from 65mΩ and 35mΩ to 50mΩ and 26mΩ, and removed the colon in the Features section.	1
		Updated the maximum V_{IN} from 5.5V to 6V in the header.	1–29
		Added the MPM3808CGLE-08-AEC1 orderable SKU to the Ordering Information and Top Marking sections.	3
		Updated the description of the VIN, SS, and OUT_S pins in the Pin Functions section; updated the max V_{IN} from 5.5V to 6V in the Absolute Maximum Ratings section.	6
		Updated the following values in the Electrical Characteristics section: • Switching frequency: Updated the max value from 2640kHz to 2700kHz • High-Side MOSFET (HS-FET) on resistance: Updated the typical value from 65mΩ to 50mΩ • Low-Side MOSFET (LS-FET) on resistance: Updated the typical value from 35mΩ to 26mΩ • V_{OUT} discharge resistance: Updated the typical value from 150Ω to 120Ω • EN turn-off delay: Updated the typical value from 30μs to 11μs • PG rising deglitch and PG falling deglitch: Updated the typical values from 80μs to 70μs • Low-side (LS) valley current limit: Updated the min value from 1.5A to 2A, and updated the max value from 4.5A to 4A • Output regulation voltage (fixed output), FB input current, and soft-start current: Added the values for the 0.8V fixed output option	7–8
		Updated the HS-FET On Resistance vs. Temperature and LS-FET On Resistance vs. Temperature curves, added conditions to the Soft-Start Current vs. Temperature curve, and added the Soft-Start Current vs. Temperature curve for the MPM3808C-08 in the Typical Characteristics section.	10–11
		Added the R_{TOP} and R_{BOT} table to Figure 2 in the Functional Block Diagram section.	18
		Updated the max V_{IN} from 5.5V to 6V in the Operation section; added the typical I_{SS} as well as C_{SS} of the MPM3808C-08 in the Soft Start (SS) section.	19
		Updated the page reference in note 11.	23
		Updated the max V_{IN} from 5.5V to 6V for Figure 7 to Figure 10.	24–25
		Added Figure 11 to the Typical Application Circuit section for the MPM3808C-08.	26

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REVISION HISTORY *(continued)*

Revision #	Revision Date	Description	Pages Updated
		Added the MPM3808CGLE-08-AEC1 orderable SKU and made general formatting edits to the Carrier Information section.	28

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