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FAIRCHILD SEMICONDUCTOR®

February 2011

# FAN3989
# USB/Charger Detection Device with Load Switch

## Features

- Charger/USB Detection Device with Load Switch
- Charger/USB Device Detection Flag
- Over/Under-Voltage Detection Flag
- Load Switch Output, Up to 1.5A Charge Current
- $V_{BUS}$ Supply: 2.7V to 20V
- $C_{ON}$: 1.5pF
- Package: 8-Lead MLP

## Applications

- Mobile Phones
- Handheld Devices

## Related Resources

- *AN-5067 — PCB Land Pattern Design and Surface Mount Guidelines for MLP Packages*

## Description

The FAN3989 is a USB connection monitoring device used to determine if a standard USB device is connected or a battery-charging device is connected.

The FAN3989 sets the FLAG1 pin to logic HIGH or LOW as an indicator to the system controller that a standard USB device or a charger is connected to the USB port. The FAN3989 also monitors the $V_{BUS}$ for over- or under-voltage conditions. The FLAG2 pin is set LOW if $V_{BUS}$ is less than 3.3V or greater than 6.0V. The internal load switch control pin is set HIGH if $V_{BUS}$ is less than 3.3V or greater than 6.0V, turning off the PMOS switch.

The FAN3989 is available in a very small 8-lead MLP package suitable for small board space applications, like mobile phones.

## Ordering Information

| Part Number | Operating Temperature Range | Package | Packing Method | Quantity |
|---|---|---|---|---|
| FAN3989MLP8X | -40°C to +85°C | 8-Lead Molded Leadless Package (MLP) | Reel | 3000 |

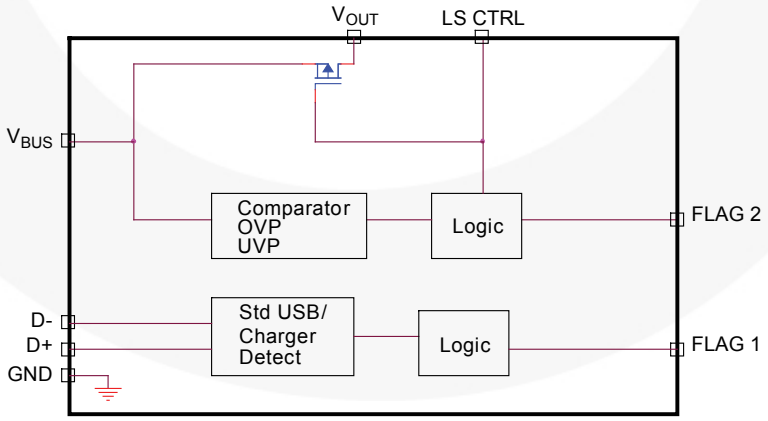



**Figure 1. Block Diagram**

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## Pin Configuration

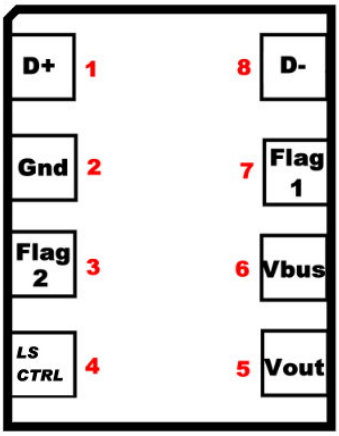



**Figure 2. Pin Configuration (Top View)**

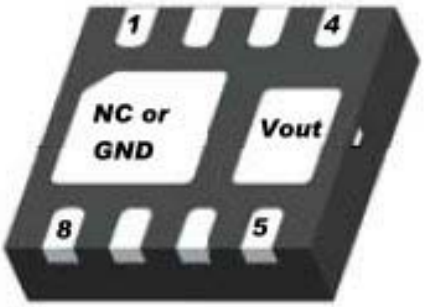



**Figure 3. Pin Configuration (Bottom View)**

## Pin Definitions

| Pin# | Name | Type | Description |
|---|---|---|---|
| 1 | D+ | Input | USB Data Input |
| 2 | GND | Input | Device Ground |
| 3 | Flag2 | Output | Over-/Under-Voltage Flag Output |
| 4 | LSCTRL | Output | PMOS Switch Control – Pull-Up Connection to $V_{BUS}$ |
| 5 | $V_{OUT}$ | Output | Voltage Out – Connection also on Package DAP *(see PCB Layout Guideline section)* |
| 6 | $V_{BUS}$ | Input | Power Input from Charger, USB Device, or Handheld Battery |
| 7 | Flag1 | Output | Charger / Standard USB Device Detect Flag |
| 8 | D- | Input | USB Data Input |

## Truth Table

| Connection State | $V_{BUS}$ | D- | D+ | FLAG1 | FLAG2 | LS CTRL | Description |
|---|---|---|---|---|---|---|---|
| STD USB Device | 0V | R to GND | R to VDD | LOW | LOW | HIGH | Load switch open |
| STD USB Device | 5V | R to GND | R to VDD | LOW | HIGH | LOW | Load switch closed |
| USB Charger | 5V | Short to D+ | Short to D- | HIGH | HIGH | LOW | Normal state, load switch closed |
| $V_{BUS}$ GT 6V | GT 6V | Short to D+ | Short to D- | HIGH | LOW | HIGH | Load switch open |
| $V_{BUS}$ LT 3.3V | LT 3.3V | Short to D+ | Short to D- | HIGH | LOW | HIGH | Load switch open |
| PC Charger | 5V | Open | Open | LOW | HIGH | LOW | Load switch closed |

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_S$ | DC Supply Voltage | -0.3 | 20.0 | V |
| $V_{IO}$ | Analog and Digital I/O | -0.3 | $V_{CC}$+0.3 | V |

## Reliability Information

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_J$ | Junction Temperature | | | +150 | °C |
| $T_{STG}$ | Storage Temperature Range | -65 | | +150 | °C |
| $\Theta_{JA}$ | Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air | | 41 | | °C/W |

## Electrostatic Discharge Information

| Symbol | Parameter | Max. | Unit |
|---|---|---|---|
| ESD | Human Body Model, JESD22-A114 | 3 | kV |
| | Charged Device Model, JESD22-C101 | 1 | |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_A$ | Operating Temperature Range | -40 | | +85 | °C |
| $V_{CC}$ | Supply Voltage Range | 2.7 | 5.0 | 20.0 | V |

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## DC Electrical Characteristics

$T_A$ = 25°C, $V_{CC}$ = 5.0V, unless otherwise noted.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_S$ | Supply Voltage Range | $V_S$ Range | 2.7 | 5.0 | 20.0 | V |
| $I_{CC}$ | Quiescent Supply Current | $V_S$ = +5.0V, D+ D- Shorted | | 1.2 | 2.0 | mA |
| $t_{SUPPLY}$ | Power-Up Stabilization Time | $V_S$ = +5.0V, D+ D- Shorted | | 10 | | ms |
| **Input Characteristics** | | | | | | |
| $C_{D+}$ | Input Capacitance | | | 1.5 | 2.0 | pF |
| $C_{D-}$ | Input Capacitance | | | 1.5 | 2.0 | pF |
| $I_{off}$ D+ | Off Leakage Current | $V_{BUS}$ = 0V or 5V $V_{IN}$ on D+ = 5V | | 1 | | µA |
| $I_{off}$ D- | Off Leakage Current | $V_{BUS}$ = 0V or 5V $V_{IN}$ on D- = 5V | | 1 | | µA |
| **Output Characteristics** | | | | | | |
| $OV_{DETECT}$ | Over-Voltage Threshold Detect | $V_S$ = +5.0V, Flag2 = LOW | 5.8 | 6.2 | 6.5 | V |
| $OV_{HYST}$ | Over-Voltage Hysteresis | Voltage Sweep through Upper and Lower Trip Points | | 100 | | mV |
| $UV_{DETECT}$ | Under-Voltage Threshold Detect | $V_S$ = +5.0V, Flag2 = LOW | 3.0 | 3.3 | 3.6 | V |
| $UV_{HYST}$ | Under-Voltage Hysteresis | Voltage Sweep through Upper and Lower Trip Points | | 100 | | mV |
| $V_{OH}$ FLAG1/ FLAG2 | Minimum HIGH Output Voltage | $V_S$ = +5.0V, $I_{OH}$ = -20µA | 2.4 | | | V |
| $V_{OL}$ FLAG1/ FLAG2 | Maximum LOW Output Voltage | $V_S$ = +5.0V, $I_{OL}$ = 20µA | | | 0.3 | V |
| $V_{OL}$ LS_CTRL | Maximum LOW Output Voltage | $V_S$ = +5.0V, $I_{OL}$ = 100µA | | | 0.3 | V |
| $VB_{DSS}$ | Drain Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = -250µA | -20 | | | V |
| $R_{DSON}$ | Static Drain-Source On Resistance | $V_{GS}$ = -5.0V, $I_P$ = 1A | | 186 | | mΩ |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -10V, $V_{GS}$ = 0V, f = 1.0MHz | | 330 | | pF |
| $C_{oss}$ | Output Capacitance | | | 80 | | pF |
| $t_{d(on)}$ | PMOS Turn-On Delay Time | $V_{DD}$ = -5V, $I_P$ = -0.5A, $V_{GS}$ = -4.5V, $R_{GEN}$ = 6Ω | | 5 | | µs |
| $t_{d(off)}$ | PMOS Turn-Off Delay Time | | | 14 | | µs |

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## Typical Performance Characteristics

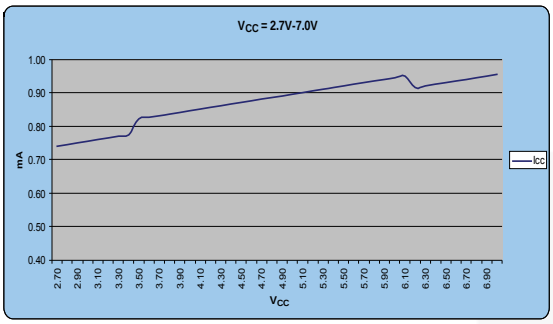



**Figure 4. $I_{CC}$ vs. $V_{CC}$ (2.7V-7.0V) No Load**

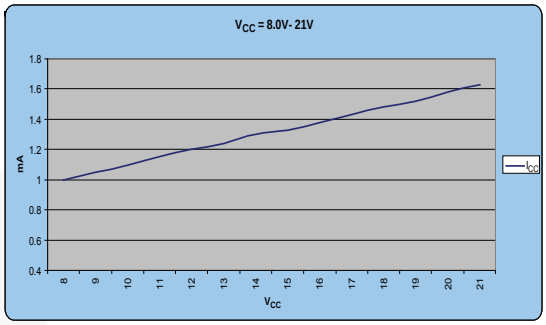



**Figure 5. $I_{CC}$ vs. $V_{CC}$ (8.0V-21V) No Load**

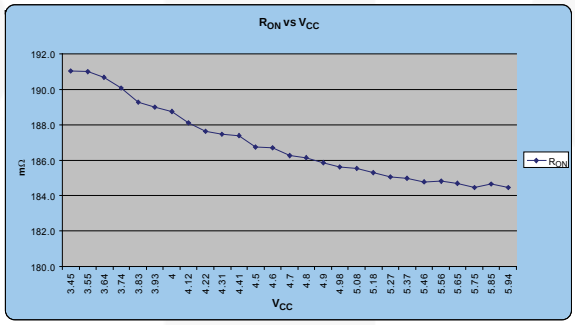



**Figure 6. $R_{ON}$ vs. $V_{CC}$ (10Ω Load)**

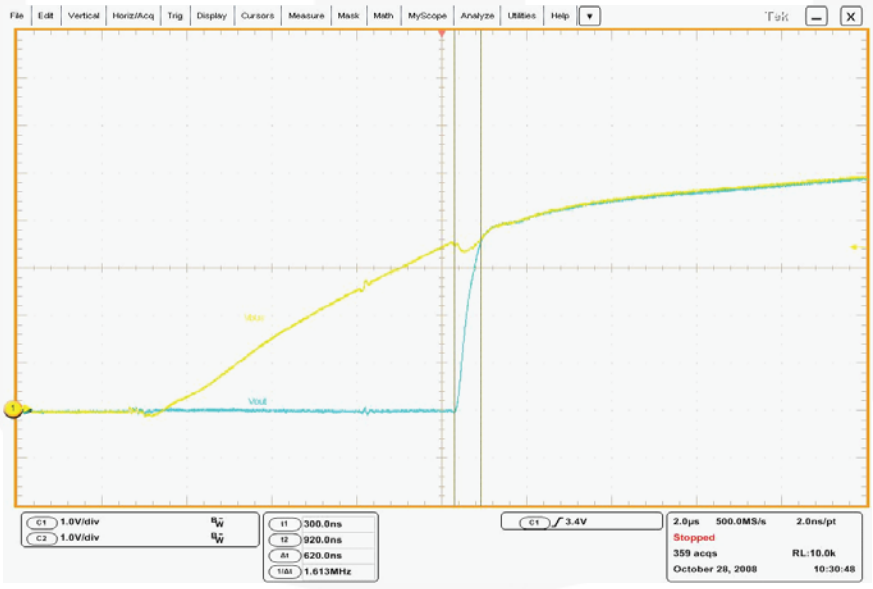



**Figure 7. Turn-On Time**

## Typical Performance Characteristics (Continued)

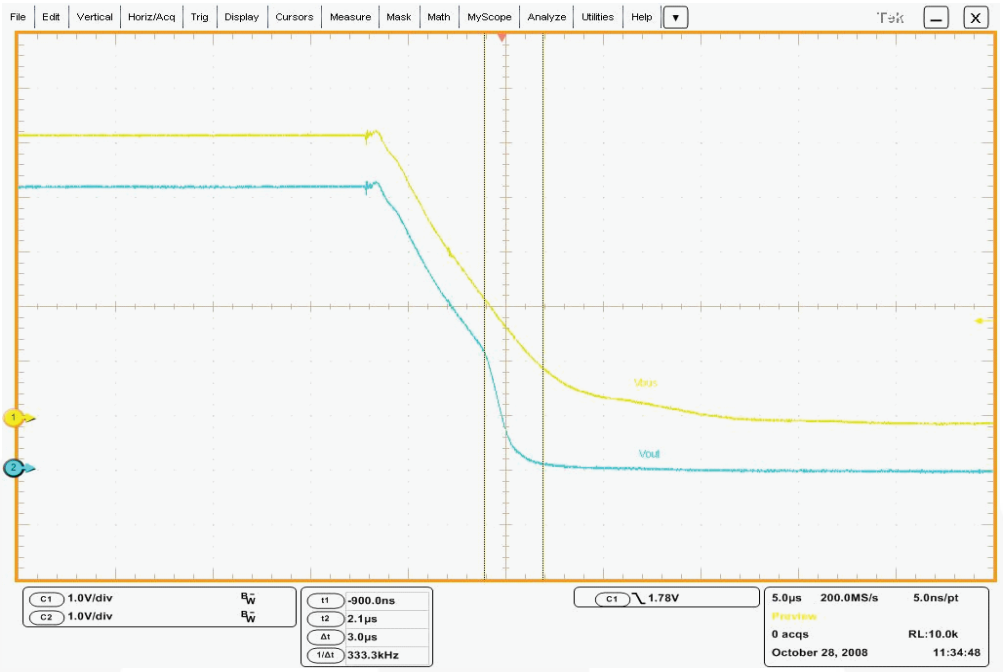



**Figure 8. Turn-Off Time**

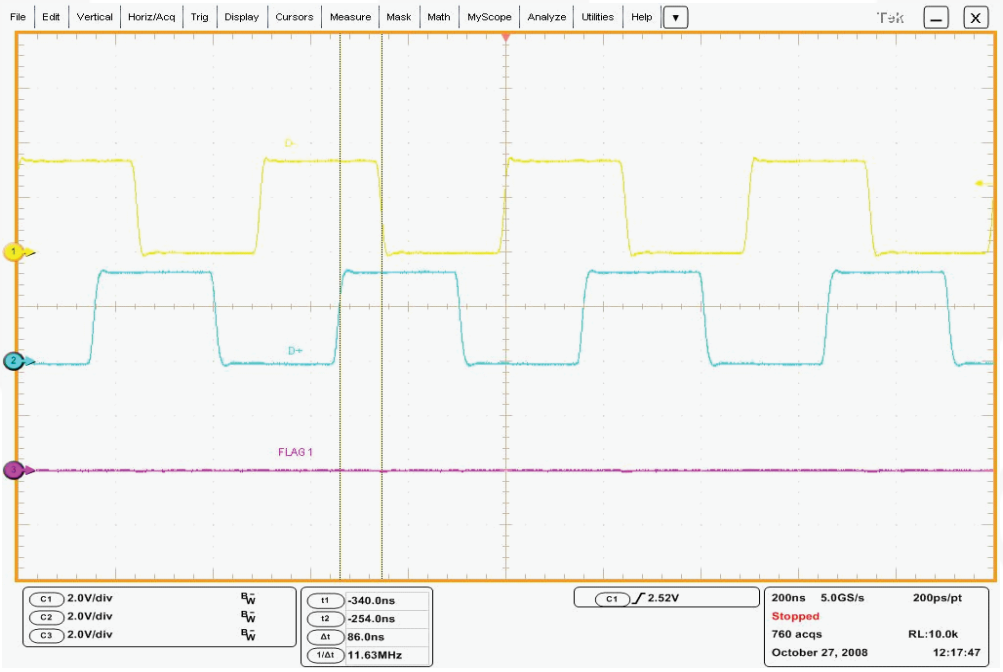



**Figure 9. No Fault on Flag 1, Skew=65ns**

## Typical Performance Characteristics (Continued)

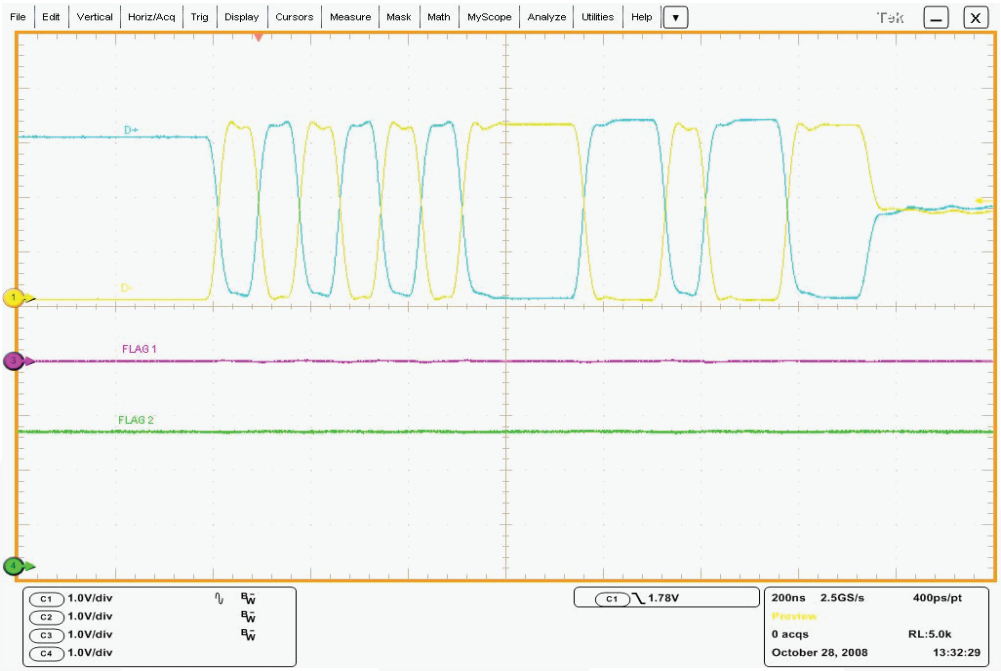



**Figure 10. PC Data Running D+/D- (Flag 1 and Flag 2 at Correct Levels)**




**Figure 11. Standard USB Charger Plug-In**

## Applications Information

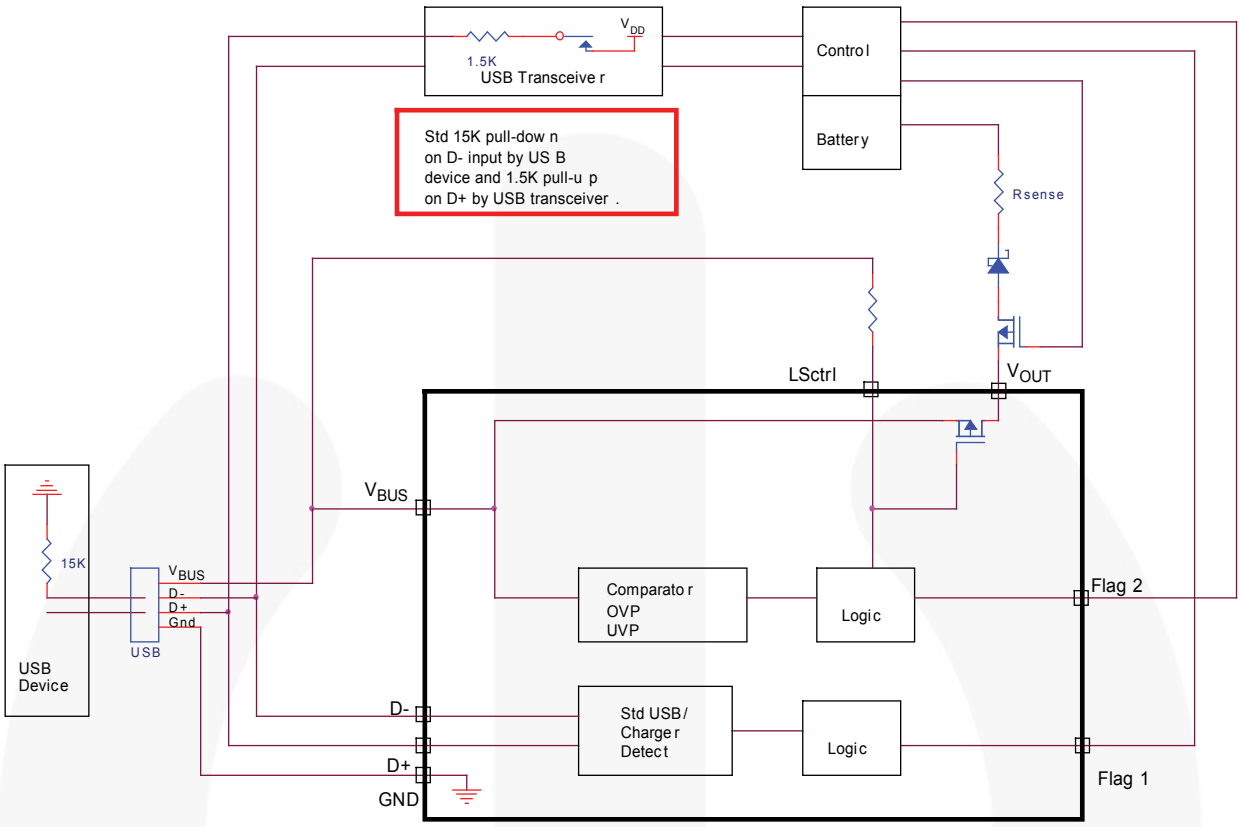



**Figure 12. Mobile Phone Battery Charging System with USB Interface**

The FAN3989 sets the FLAG1 pin to logic HIGH or LOW as an indicator to the system controller that a standard USB device or a charger is connected to the USB port. The FAN3989 also monitors the $V_{BUS}$ for over- or under-voltage conditions. If $V_{BUS}$ is less than 3.3V or greater than 6.0V, the FLAG2 pin is set LOW and the internal load switch control pin is set HIGH, turning off the PMOS switch.

In a standard USB configuration, there is a switch in the USB transceiver that is always on in full-speed mode. It is on during the transition from full-speed to high-speed mode and turned off after enumeration is complete. If D+ and D- are shorted when a charger is plugged into the USB port, the USB switch is on and pulled to $V_{DD}$, which is about 3V, making both D+ and D- HIGH. Flag1 is also set HIGH, indicating that a charging device is connected to the port. If D+ and D- are connected to a standard USB device, the D+ is pulled to $V_{DD}$ and D- is set low (due to the 15KΩ pull-down resistor on the USB device) and flag1 is LOW. If D+ and D- are open (floating), D+ is pulled to $V_{DD}$ and D- floats LOW, which makes flag1 LOW.

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## Applications Information (Continued)

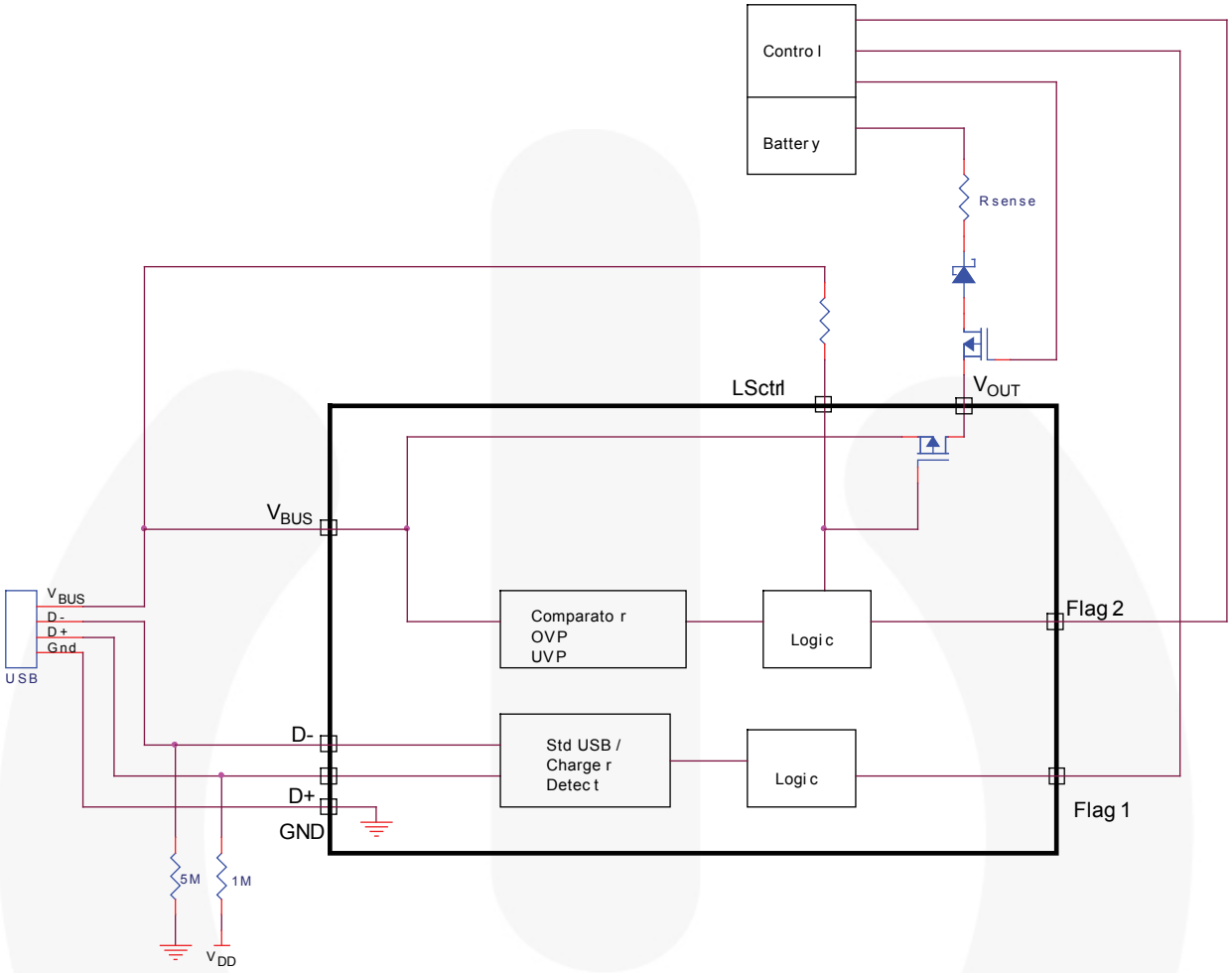



**Figure 13. Mobile Phone Battery Charging System without USB Interface**

The FAN3989 sets the FLAG1 pin to logic HIGH or LOW as an indicator to the system controller that a standard USB device or a charger is connected to the USB port. The FAN3989 also monitors the $V_{BUS}$ for over- or under-voltage conditions. If $V_{BUS}$ is less than 3.3V or greater than 6.0V, the FLAG2 pin is set LOW and the internal load switch control pin is set HIGH, turning off the PMOS switch.

Where a USB transceiver is not incorporated or there is a switch between the USB port and the FAN3989, external resistors are used to set the correct input logic states on the D+ and D- inputs. A 5MΩ pull-down on the D- line and a 1MΩ pull-up to $V_{DD}$ on the D+ line are recommended. If a charger is plugged into the USB port (D+ and D- shorted), the voltage divider of 1M and 5M put a voltage of 2.3V on the D+D- inputs and flag1 is HIGH, indicating a charger is connected to port.

If the USB port is connected to a standard USB device, the D+ input is pulled up to $V_{DD}$ and is in parallel with the 1.5KΩ on a USB transceiver with a parallel R value of 1.497KΩ. The D- input is connected to a 15KΩ pull-down by the USB device and in parallel with 5MΩ with a parallel R value of 14.955KΩ. This condition forces flag1 LOW. If D+ and D- are open (floating), D+ is pulled to $V_{DD}$ and D- floats LOW, which forces flag1 LOW.

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## PCB Layout Guidelines

*Please also see Fairchild Semiconductor applications note AN-5067 — PCB Land Pattern Design and Surface Mount Guidelines for MLP Packages*

**Pad1**
This exposed DAP is connected to the internal FET drain and labeled $V_{OUT}$ on the device. The pad should be connected to $V_{OUT}$ pin of the device or left floating. It should never be connected to the ground, power plane, or Pad2.

**Pad2**
This exposed DAP is connected to an internal die substrate that is at a ground potential. The pad should be left floating or can be connected to ground plane. This pad should never be connected to Pad1 or the power plane.

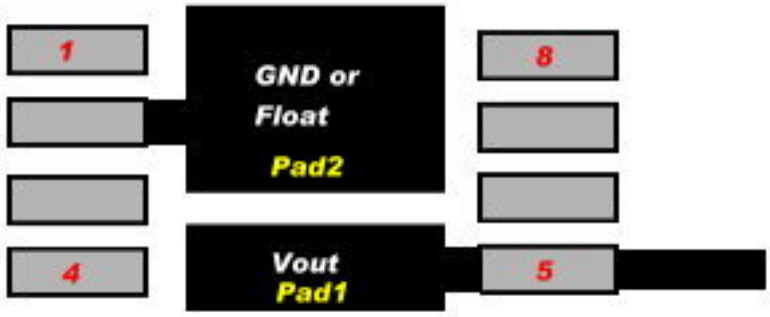
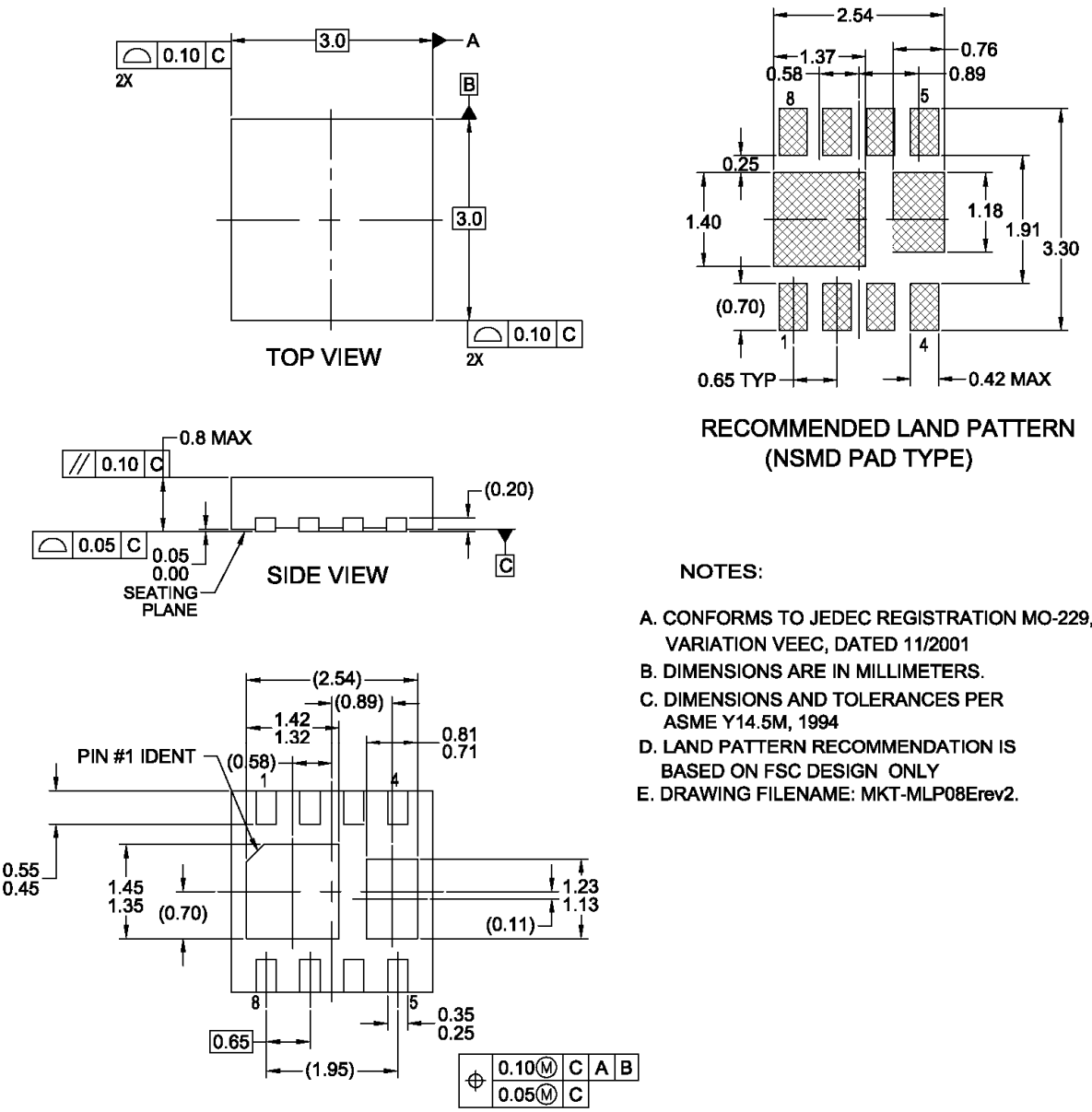



**Figure 14. PCD / Pad Layout**

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## Physical Dimensions




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VEEC, DATED 11/2001
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY
E. DRAWING FILENAME: MKT-MLP08Erev2.

**Figure 15. 8-Lead Molded Leadless Package (MLP)**

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### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative / In Design | Datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design. |
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