MPM3864

2.75V to 7V, 6A, 1.2MHz, Synchronous Power Module

DESCRIPTION

The MPM3864 is a fully integrated, high-frequency, synchronous, rectified, step-down power module with an internal inductor. This device is a compact solution that achieves 6A of continuous output current (I_{OUT}) across a wide input voltage (V_{IN}) range with excellent load and line regulation. The MPM3864 has synchronous mode operation for higher efficiency across the I_{OUT} load range.

Constant-on-time (COT) control provides very fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage lockout (UVLO), and thermal shutdown.

The MPM3864 requires a minimal number of readily available, standard external components, and it is available in a space-saving ECLGA-19 (3mmx3mmx1.85mm) package.

FEATURES

- Wide 2.75V to 7V Operating Input Voltage (V_{IN}) Range
- 6A Output Current (I_{OUT})
- Internal Power MOSFETs
- Output Voltage (V_{OUT}) Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Forced Continuous Conduction Mode (FCCM) for Low V_{OUT} Ripple
- Fixed 1200kHz Switching Frequency (f_{SW})
- Configurable, External Soft-Start Time (t_{SS})
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Available in an ECLGA-19 (3mmx3mmx1.85mm) Package

APPLICATIONS

- Field-Programmable Gate Array (FPGA) Power Systems
- Optical Modules
- Telecom
- Networking
- Industrial Equipment

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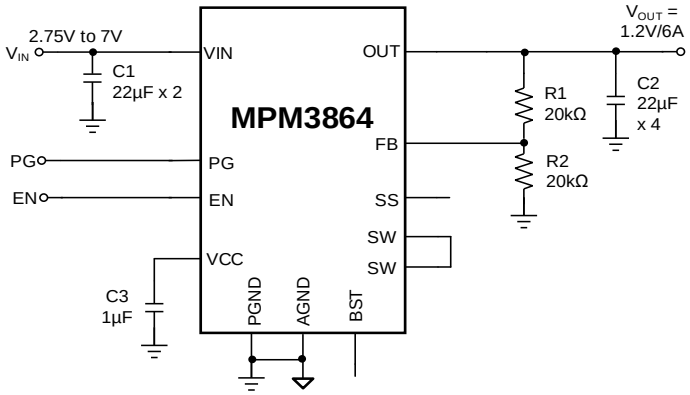
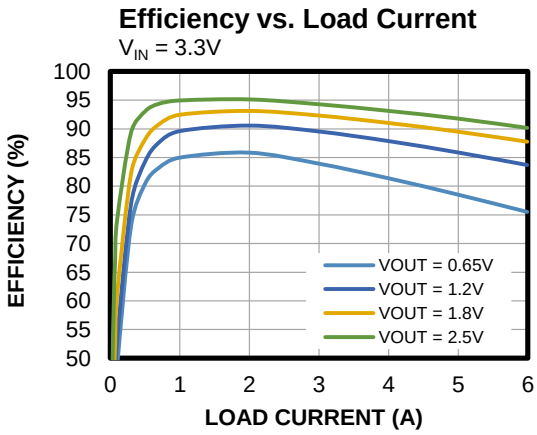
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3864GPQ	ECLGA-19 (3mmx3mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPM3864GPQ-Z).

TOP MARKING

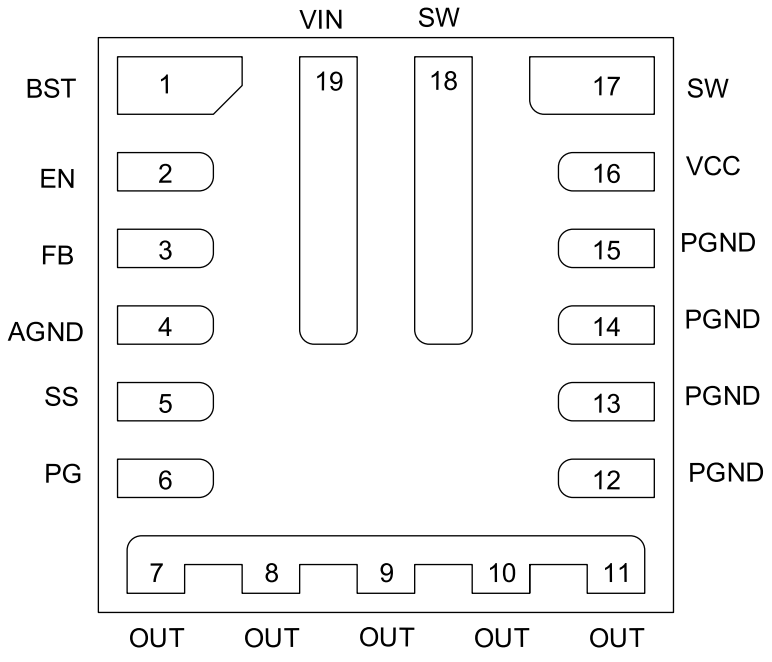
BUUY

LLL

BUU: Product code of MPM3864GPQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



ECLGA-19 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** The internal capacitor connected between the SW and BST pins forms a floating supply across the high-side MOSFET (HS-FET). This pin is a test pin, and it can be floated when designing the layout.
2	EN	**Enable.** Pull the EN pin high to enable the part. When floating, EN is pulled down to GND by an internal 1.2MΩ resistor, so the MPM3864 is disabled.
3	FB	**Feedback.** Set the output voltage (V_{OUT}) when the FB pin connected to the tap of an external resistor divider, which is connected between the output and GND.
4	AGND	**Signal ground.** The AGND pin is not internally connected to power ground (PGND), so ensure that AGND is connected to the PGND pin in the PCB layout.
5	SS	**Soft start.** Connect a capacitor across the SS and GND pins to set the soft-start time and avoid inrush current at start-up. This pin includes an internal 22nF soft-start (SS) capacitor.
6	PG	**Power good output.** The output of the PG pin is an open-drain output. The PG pin changes its state if under-voltage lockout (UVLO), over-current protection (OCP), over-temperature protection (OTP), or an over-voltage (OV) condition occurs.
7, 8, 9, 10, 11	OUT	**Power output.** Connect the OUT pin to the output capacitor (C_{OUT}).
12, 13, 14, 15	PGND	**Power ground.** The PGND pin is the reference ground of the regulated V_{OUT}. Because of this, there are additional considerations to take when designing the PCB layout. It is recommended to connect this pin to GND with copper pours and vias.
16	VCC	**Internal biased supply output.** Decouple the VCC pin with a 1µF capacitor. Place the VCC capacitor close to VCC and GND.
17, 18	SW	**Switch output.** Use a wide PCB trace to connect the two SW pins together.
19	VIN	**Supply voltage.** The MPM3864 operates from a 2.75V to 7V input rail. Use a 0402-sized, 0.1µF input capacitor to decouple the input rail. Use wide PCB traces to make the connection.

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +8V
V_{SW}.....-0.3V (-5V for <10ns) to + V_{IN} + 0.7V (+10V for <10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
V_{OUT}..... V_{IN}
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) 4.5W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +125°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....2.75V to 7V
Output voltage (V_{OUT})….0.6V to V_{IN} x D_{MAX} x η (4)
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5) (6) (7) (8)

ECLGA-19 (3mmx3mm)
θ_{JA} ..... 27.5°C/W
θ_{JC_TOP} ..... 3.8°C/W
θ_{JB} ..... 15.3°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation on the EVM3864-PQ-01A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) η is the efficiency.
5) θ_{JA} is the junction-to-ambient thermal resistance, θ_{JC_TOP} is junction-to-case top thermal characterization parameter, and θ_{JB} is the junction-to-board thermal characterization parameter.
6) The thermal parameter is based on tests on the MPS evaluation board EVM3864-PQ-01A under no airflow cooling conditions in a standard enclosure. The board size is 5.1cmx5.1cm, and 4 layers, of which the top and bottom layer copper thickness is 2oz, while the inner layer is 1oz.
7) The junction-to-case top thermal characterization parameter, θ_{JC_TOP}, estimates the junction temperature in the real system, based on the equation $T_J = \theta_{JC_TOP} \times P_{LOSS} + T_{CASE_TOP}$, where P_{LOSS} is the entire loss of the module under real applications, and T_{CASE_TOP} is the case top temperature
8) The junction-to-board thermal characterization parameter, θ_{JB}, is the estimate the junction temperature in the real system, based on the equation $T_J = \theta_{JB} \times P_{LOSS} + T_{BOARD}$, where P_{LOSS} is the entire loss of module at real application, and T_{BOARD} is board temperature.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C [9], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		2.75		7	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		2	5	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		105	150	µA
MOSFET						
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 7V			5	µA
Current Limit						
Valley current limit	I_{LIMIT_VY}		6	7		A
Short hiccup mode duty cycle [10]	D_{HICCUP}			10		%
Switching Frequency (f_{SW}) and Minimum On/Off Time						
Switching frequency	f_{SW}		0.9	1.2	1.6	MHz
Minimum on time [10]	t_{ON_MIN}			50		ns
Minimum off time [10]	t_{OFF_MIN}			100		ns
Reference and Soft Start (SS)						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
SS current	I_{SS_START}		4	6	8	µA
Enable (EN) and Under-Voltage Lockout (UVLO)						
EN rising threshold	V_{EN_RISING}		1.19	1.23	1.27	V
EN falling threshold	$V_{EN_FALLING}$		0.96	1	1.04	V
EN pin pull-down resistor	R_{EN_PD}			1.2		MΩ
Supply Current (V_{CC})						
V_{CC} UVLO rising threshold	V_{CC_VTH}		2.4	2.55	2.7	V
V_{CC} UVLO threshold	V_{CC_HYS}			300		mV
V_{CC} regulator	V_{CC}	V_{IN} = 5V		3.4		V
V_{CC} load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%
Power Good (PG)						
PG under-voltage (UV) rising threshold	$V_{PGUVVTH_HI}$		85%	90%	95%	V_{FB}
PG UV falling threshold	$V_{PGUVVTH_LO}$		75%	80%	85%	V_{FB}
PG over-voltage (OV) rising threshold	$V_{PGOVVTH_HI}$		115%	120%	125%	V_{FB}
PG OV falling threshold	$V_{PGOVVTH_LO}$		105%	110%	115%	V_{FB}
PG delay	t_{PGTD}	Both edges		50		µs
PG sink current capability	V_{PG}	Sink 4mA			0.4	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to +125°C (9), typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal shutdown (10)	T_{SD}			150		°C
Thermal hysteresis (10)	T_{SD-HYS}			20		°C

Notes:

9) Not tested in production. Guaranteed by over-temperature correlation.
10) Guaranteed by design and engineering sample characterization.

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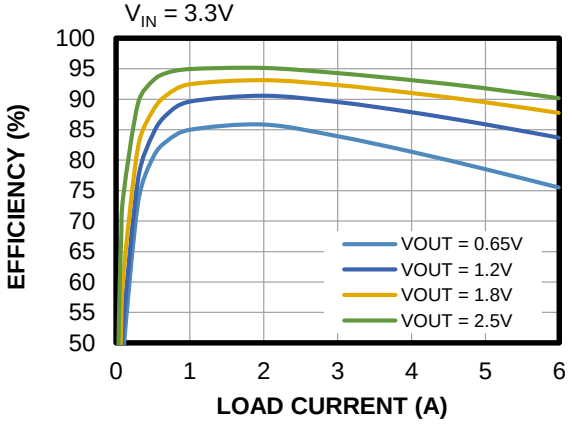
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

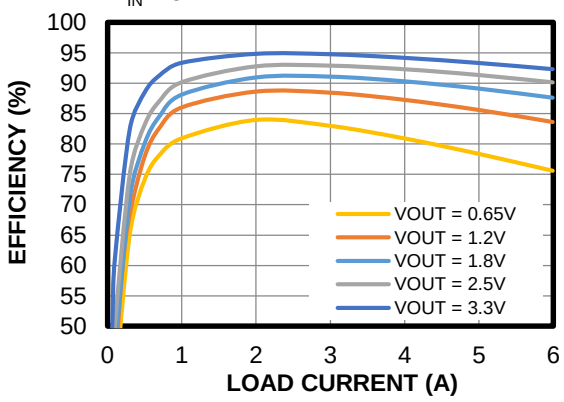
Efficiency vs. Load Current

V_{IN} = 3.3V



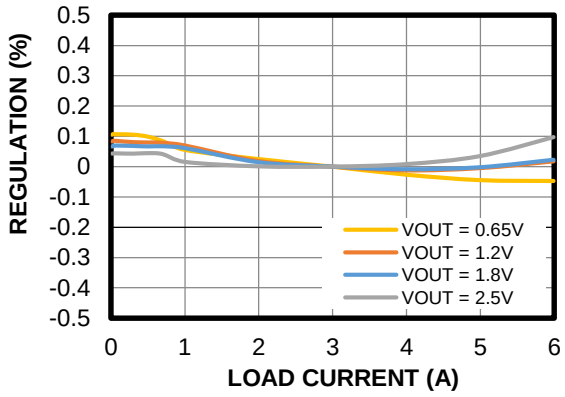
Efficiency vs. Load Current

V_{IN} = 5V



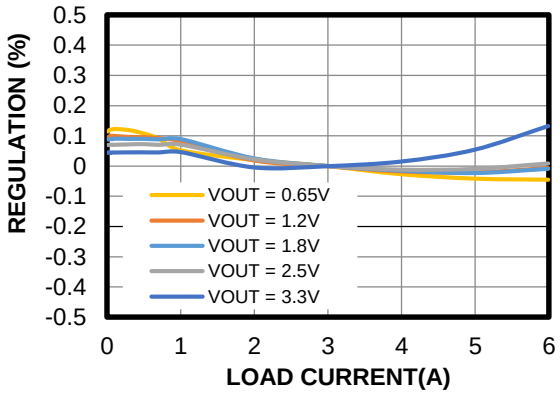
Load Regulation

V_{IN} = 3.3V

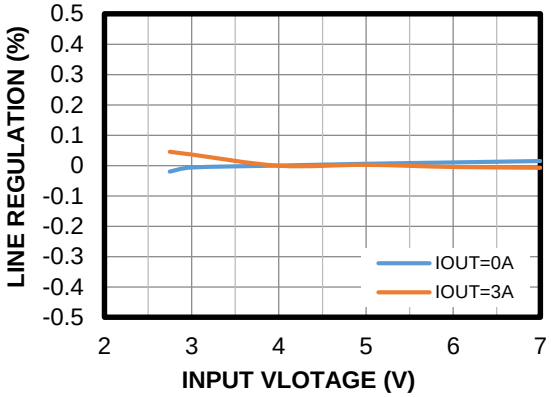


Load Regulation

V_{IN} = 5V

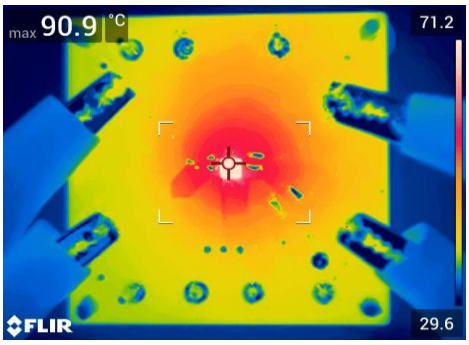


Line Regulation



Thermal Rise

I_{OUT} = 6A, T_A = 29.6°C



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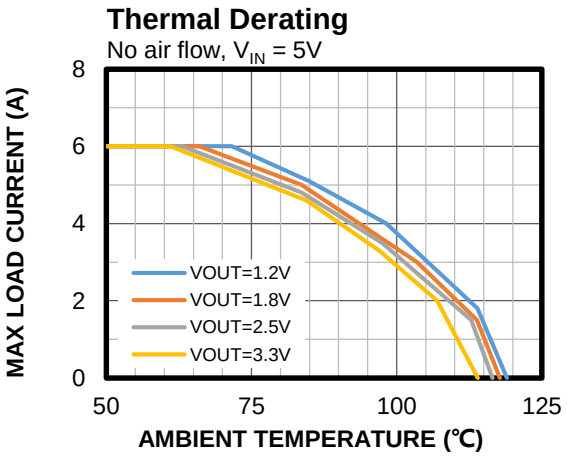
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.



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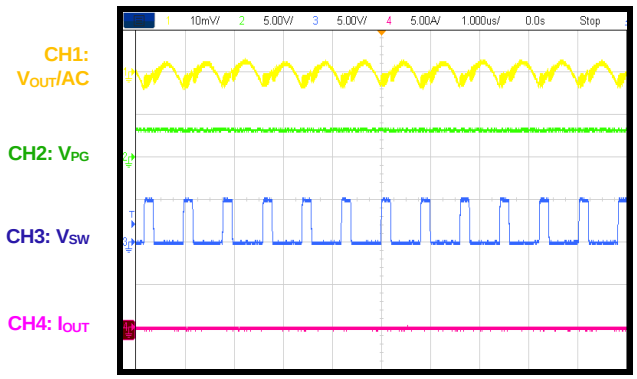
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

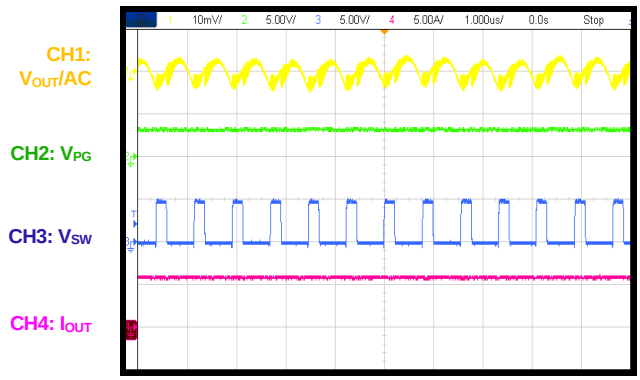
Output Voltage Ripple

I_{OUT} = 0A



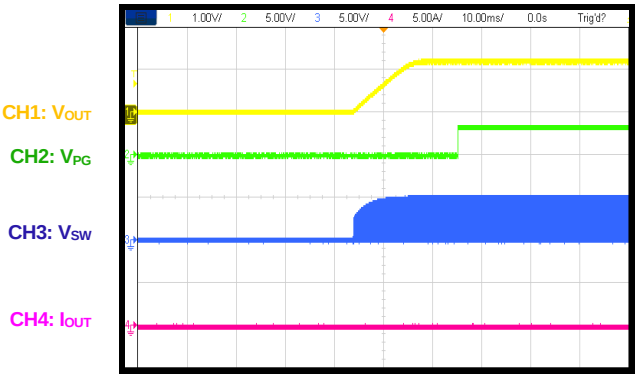
Output Voltage Ripple

I_{OUT} = 6A



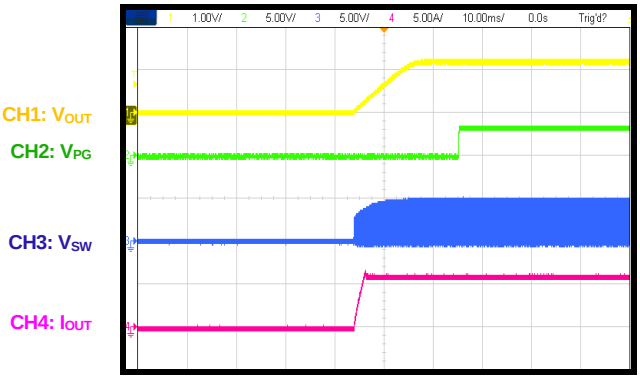
Start-Up through VIN

I_{OUT} = 0A



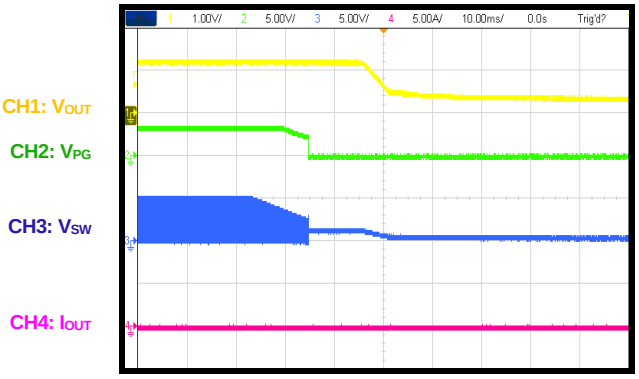
Start-Up through VIN

I_{OUT} = 6A



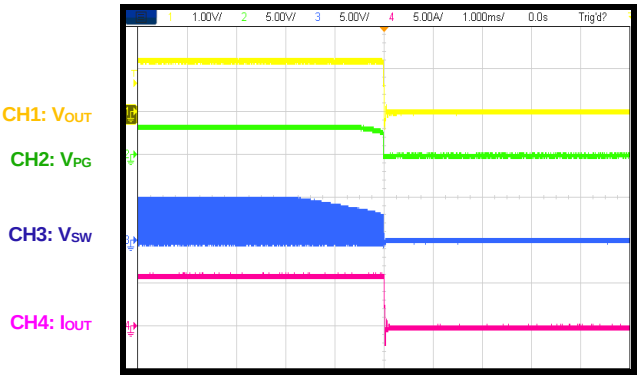
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 6A



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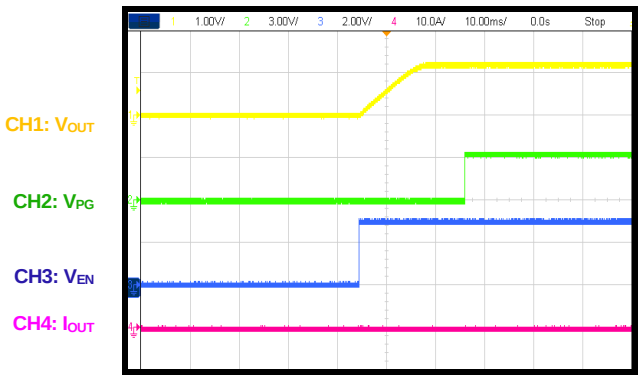
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

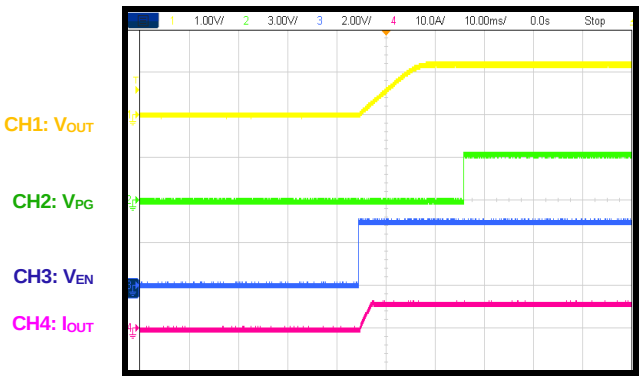
Start-Up through EN

I_{OUT} = 0A



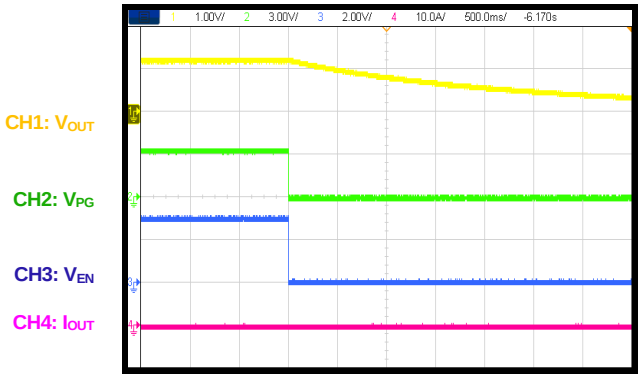
Start-Up through EN

I_{OUT} = 6A



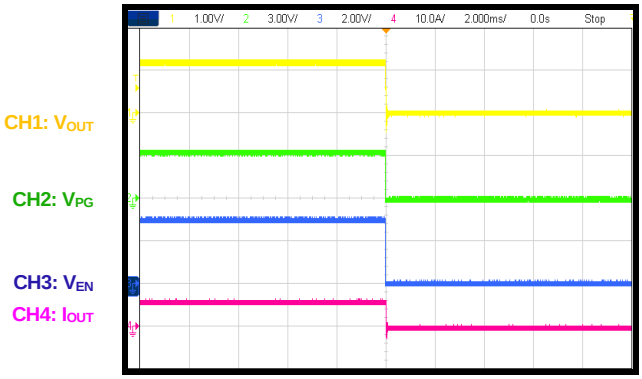
Shutdown through EN

I_{OUT} = 0A



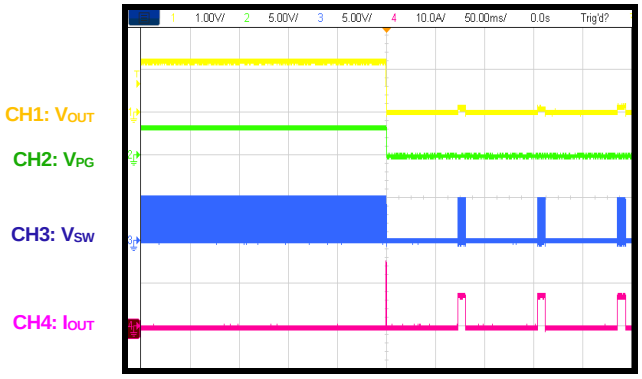
Shutdown through EN

I_{OUT} = 6A



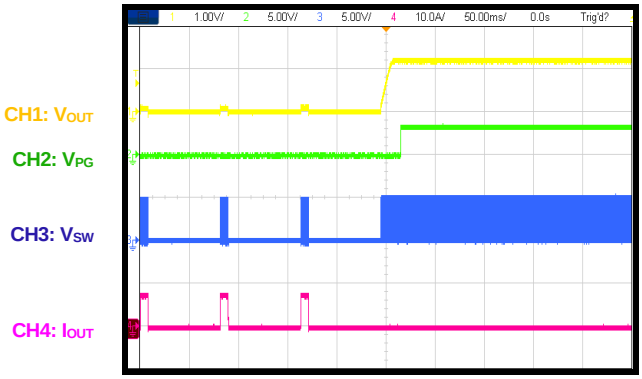
SCP Entry

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 0A



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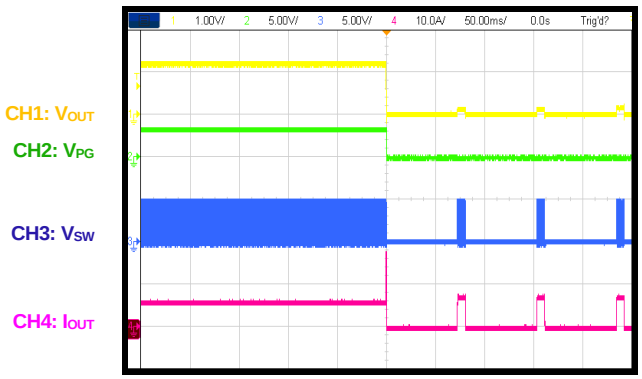
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, T_A = 25°C, unless otherwise noted.

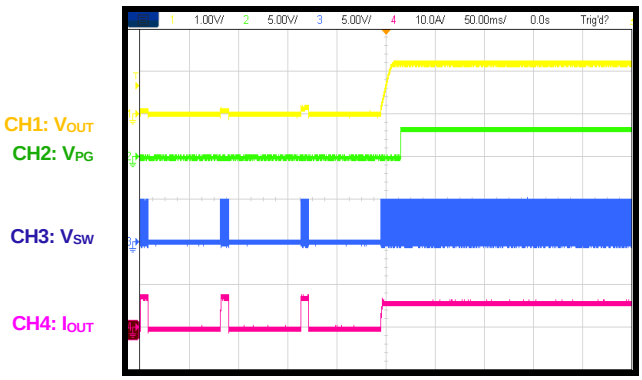
SCP Entry

I_{OUT} = 6A

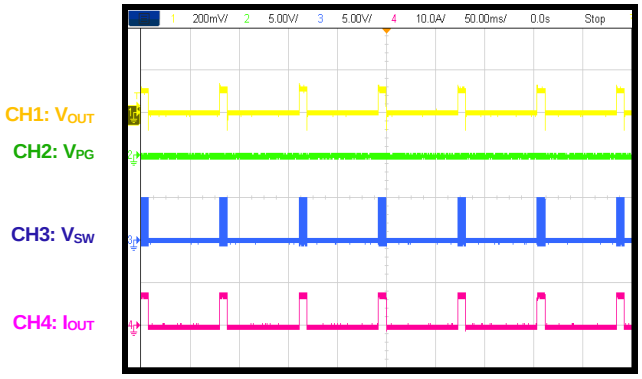


SCP Recovery

I_{OUT} = 6A

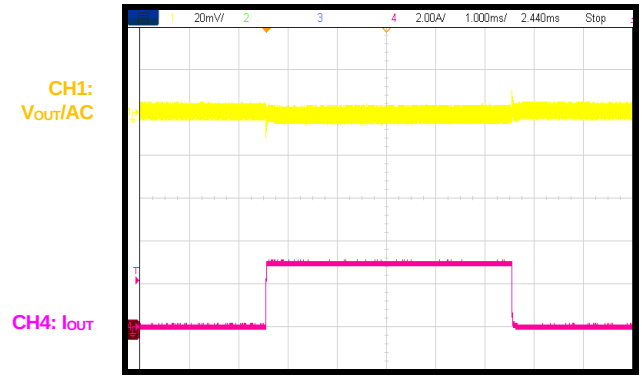


SCP Steady State



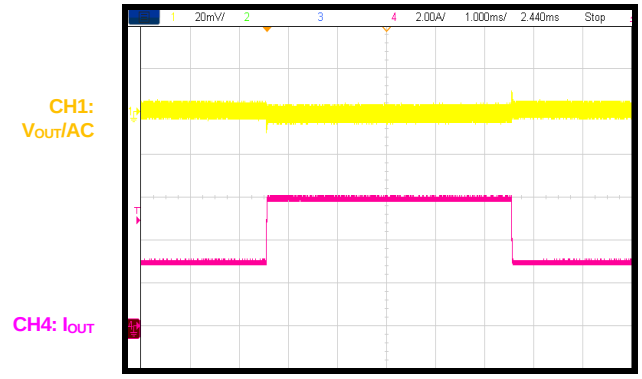
Load Transient Response

I_{OUT} = 0A to 3A, 2.5A/µs e-load



Load Transient Response

I_{OUT} = 3A to 6A, 2.5A/µs e-load



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FUNCTIONAL BLOCK DIAGRAM

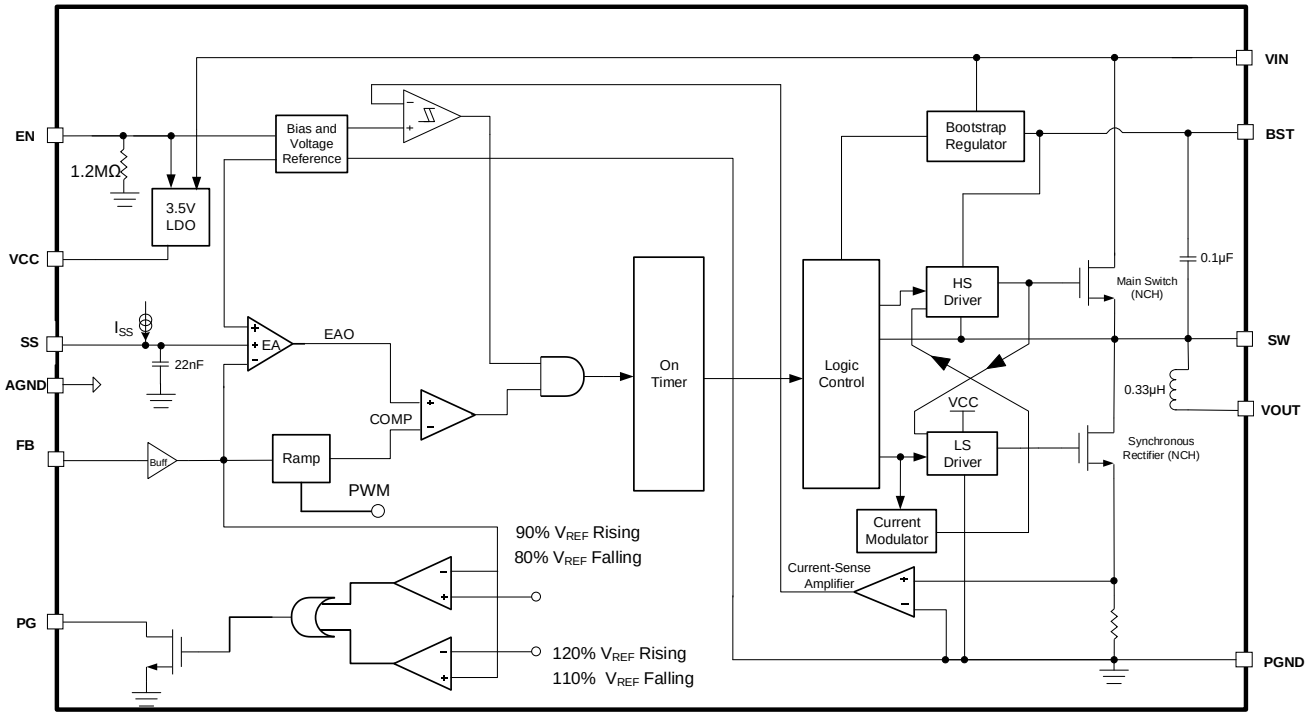

Figure 1: Functional Block Diagram

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OPERATION

The MPM3864 is a fully integrated, synchronous, rectified, step-down switch-mode power module. Constant-on-time (COT) control provides fast transient response and easy loop stabilization.

Figure 2 shows the MPM3864's simplified ramp compensation block.

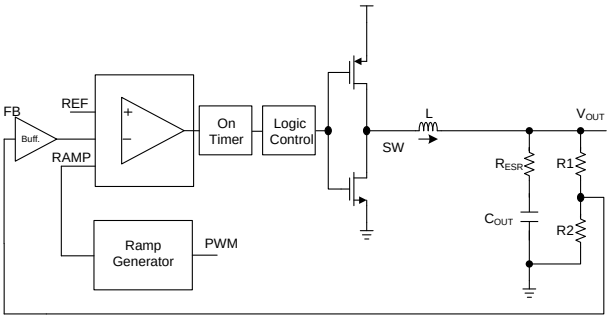

Figure 2: Simplified Ramp Compensation Block

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates there is an insufficient output voltage (V_{OUT}). The on period is determined by both V_{OUT} and the input voltage (V_{IN}) to make the switching frequency (f_{SW}) fairly constant across the V_{IN} range.

After the on period elapses, the HS-FET turns on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates V_{OUT}. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET turn on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is internally generated between the HS-FET off period and LS-FET on period, and vice versa.

Internal compensation is applied for COT control to stabilize operation. Internal compensation improves jitter performance without affecting the line or load regulation, even if ceramic capacitors are used.

Forced Continuous Conduction Mode (FCCM)

The MPM3864 works in forced continuous conduction mode (FCCM). Figure 3 shows FCCM. If the control signal ($V_{FB+RAMP}$) drops below the error amplifier output (V_{EAO}), then the HS-FET turns on for a fixed interval, which is determined by the one-shot on-timer. When the HS-FET turns off, the LS-FET turns on until the next period.

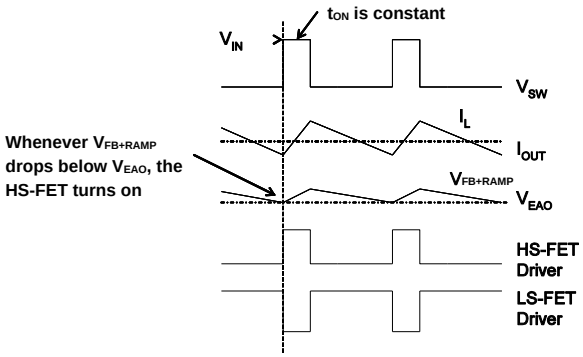

Figure 3: FCCM

During FCCM, f_{SW} is fairly constant. This is called pulse-width modulation (PWM) mode.

V_{CC} Regulator

The internal regulator powers most of the internal circuitries. This regulator takes the VIN input and operates across the full V_{IN} range. If V_{IN} exceeds 3.5V, the regulator's output is in full regulation. If V_{IN} falls below 3.5V, the regulator's output drops following the changes in V_{IN}.

Enable (EN)

EN is a digital control pin that turns the power module on and off. Drive EN above 1.23V to turn the device on; drive EN below 1V to turn it off.

When floating EN, pull it down to GND using an internal 1.2MΩ resistor. EN can be connected directly to VIN, and supports a maximum 7V input.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPM3864 UVLO comparator monitors the output voltage of the internal regulator (V_{CC}). The V_{CC} UVLO rising threshold is about 2.55V, and its falling threshold is 2.25V.

If V_{IN} exceeds the UVLO rising threshold, the MPM3864 starts up. The device shuts down when V_{IN} drops below its UVLO falling threshold. This is a non-latch protection.

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Soft Start (SS)

The MPM3864 employs a soft start (SS) mechanism to ensure that the output smoothly ramps up during start-up. When the EN pin goes high, an internal current source (6μA) charges up the SS capacitor. When the device starts up, the SS capacitor voltage (V_{SS}) is below V_{REF}, and the PWM comparator uses V_{SS} as its reference. Then V_{OUT} smoothly ramps up with V_{SS}. Once V_{SS} exceeds V_{REF}, the PWM comparator uses V_{REF} as its reference, and the SS capacitor continues to be charged until V_{SS} = V_{CC}. Then soft start finishes, and the MPM3864 enters steady state operation.

The SS capacitance (C_{SS}) can be calculated with Equation (1):

$$C_{SS}(nF) = 0.83 \times \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \quad (1)$$

The MPM3864 has an internal 22nF SS capacitor.

If the output capacitor has a large capacitance, ensure that the SS time (t_{SS}) is sufficiently long. Otherwise, the device may reach its current limit during soft start.

Power Good (PG) Indication

The PG pin is the open drain of a MOSFET that connects to VCC or a voltage source through a resistor (e.g. 100kΩ). The MOSFET turns on when V_{IN} is applied, and the PG pin pulls to GND before soft start completes. The PG pin pulls high after a 50μs delay when soft start completes. When V_{FB} drops below 80% of V_{REF}, the PG pin pulls low.

If UVLO or over-temperature protection (OTP) occurs, the PG pin immediately pulls low. If an over-current (OC) condition occurs, the PG pin immediately pulls low if the device enters hiccup mode. If an over-voltage (OV) condition occurs, the PG pin pulls low if V_{FB} exceeds 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls below 110% of V_{REF}, the PG pin pulls high after a 0.05ms delay.

If the input supply fails to power the MPM3864, PG clamps low, even if PG is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

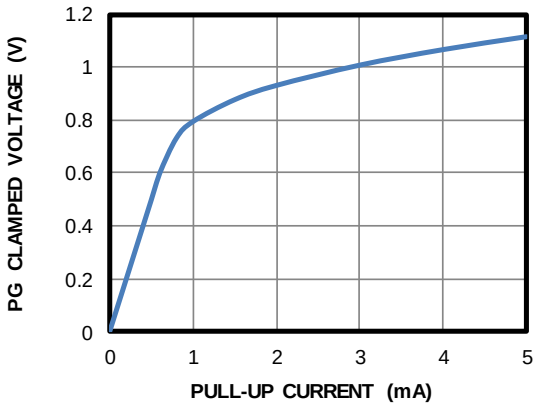

Figure 4: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MPM3864 has valley limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET does not turn on again until the valley current limit disappears. Meanwhile, V_{OUT} drops until V_{FB} falls below the under-voltage (UV) threshold (typically 50% of V_{REF}). Once a UV condition is triggered, the MPM3864 enters hiccup mode to periodically restart the part.

During over-current protection (OCP), the device tries to recover from the OC fault with hiccup mode. This means that the MPM3864 disables the output power stage, discharges the SS capacitor, then automatically tries to reinitiate soft start. If the OC condition remains after soft start ends, the device repeats this operation until the OC condition disappears, and the output rises back to its regulation level. OCP is a non-latch protection.

Pre-Biased Start-Up

The MPM3864 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor also charges. If the BST voltage exceeds its rising threshold and the SS capacitor voltage exceeds the sensed output voltage at the FB pin, the MPM3864 begins operating normally.

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Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C), the chip is re-enabled.

Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the MPM3864 starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry.

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APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT}. First, choose a value for R2. R2 should be chosen carefully, as a small resistance leads to significant quiescent current (I_Q) loss, while a larger-value resistor can make FB noise-sensitive. It is recommended to choose a value between 2kΩ and 100kΩ for R2. Typically, setting the current through R2 to below 250μA provides a good balance between system stability and minimal load loss. Then R1 can be calculated with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

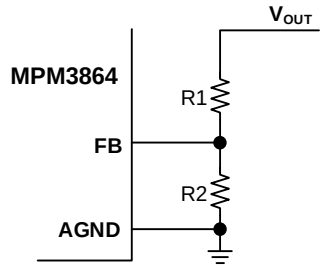

Figure 5: Feedback Network

Table 1 shows the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	20	30
1.2	20	20
1.5	20	13
1.8	20	10
2.5	20	6.34
3.3	20	4.42

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and they should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable across temperature fluctuations.

The capacitors must also have a ripple current rating that exceeds the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (4):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the converter's input voltage ripple. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the relevant specifications.

The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (6):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (7)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes majority of the output voltage ripple.

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For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

In addition to improving the output voltage ripple, a larger output capacitance can improve load transient response. However, consider the maximum output capacitor limits in design application. If the output capacitance is too large, V_{OUT} will not be able to reach the design value within t_{SS}, and then the device will fail to regulate. The maximum output capacitance (C_{O_MAX}) can be calculated with Equation (10):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{SS} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{SS} is the soft-start time.

PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended to improve thermal performance. For the best results, refer to Figure 6 and follow the guidelines below:

1. Keep the power loop as small as possible.
2. Connect a large ground plane directly to PGND.
3. Add vias near PGND if the bottom layer is a ground plane.
4. Ensure the high-current paths at PGND, OUT, and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0402) input bypass capacitor, as close to the VIN and PGND pins as possible to minimize high-frequency noise.
6. Keep the paths between the input capacitor and VIN as short and wide as possible.
7. Place a VCC decoupling capacitor close to the MPM3864.
8. Connect VIN, OUT, and PGND to a large copper area to improve thermal performance and long-term reliability.
9. Ensure that any signal trace is placed far away from SW.
10. Use multiple vias to connect the power planes to internal layers.

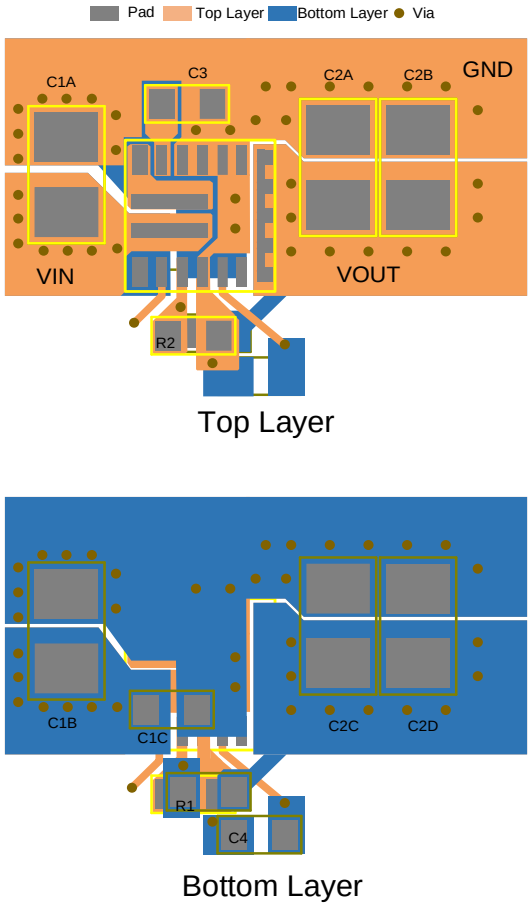

Figure 6: Recommended PCB Layout

Note:

11) The recommended layout is based on Figure 7 on page 19.

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TYPICAL APPLICATION CIRCUIT

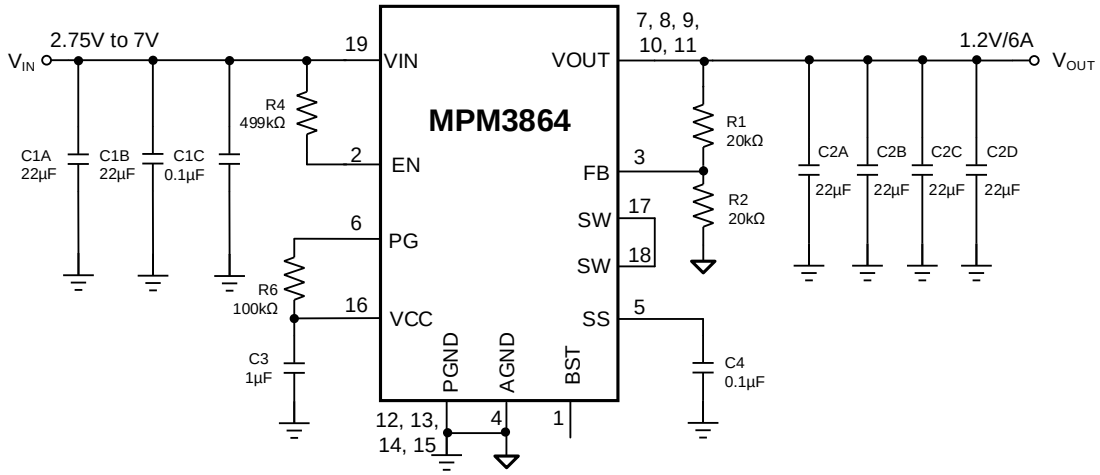

Figure 7: Typical Application Circuit with 1.2V Output

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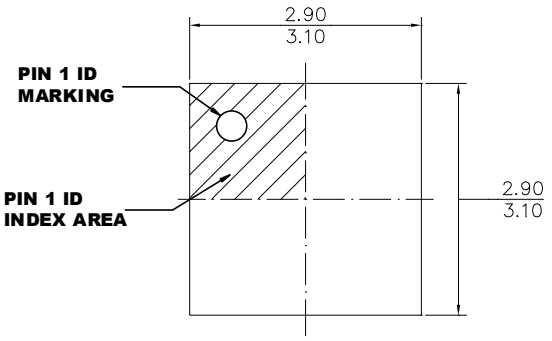
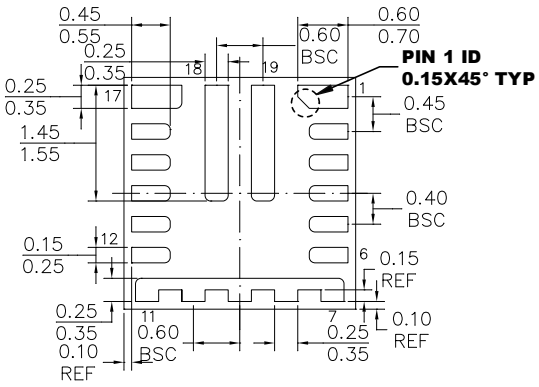
PACKAGE INFORMATION

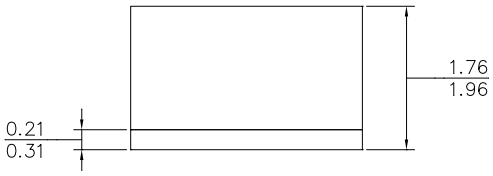
ECLGA-19 (3mmx3mm)



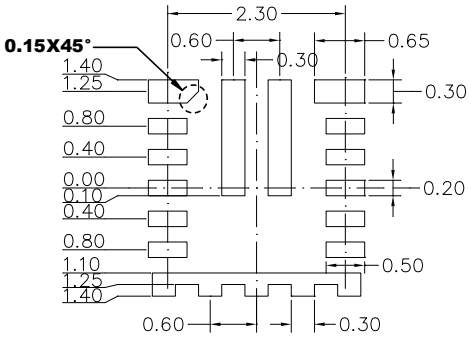
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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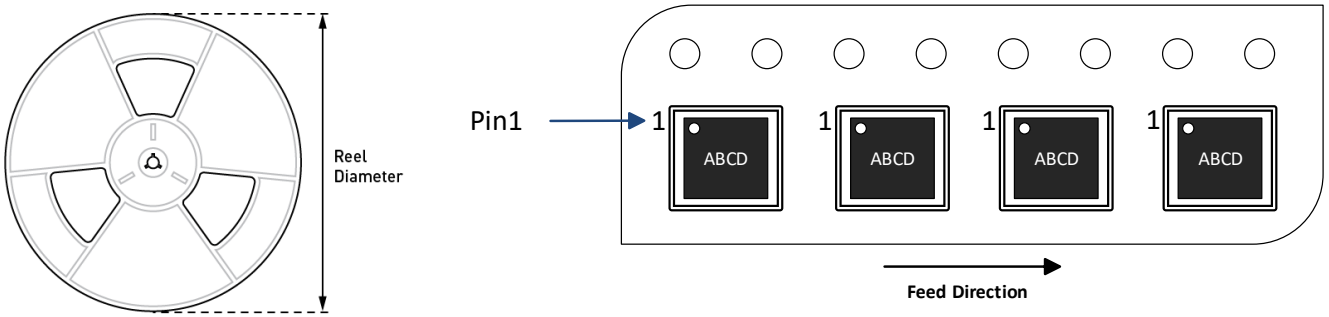
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3864GPQ-Z	ECLGA-19 (3mmx3mm)	2500	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/14/2023	Initial Release	-

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