P-Channel 20 V (D-S) MOSFET with Schottky Diode

MOSFET PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.105 at V_{GS} = - 4.5 V	- 4[a]	4.7 nC
	0.143 at V_{GS} = - 2.5 V	- 3.8	
	0.188 at V_{GS} = - 1.8 V	- 3	

SCHOTTKY PRODUCT SUMMARY		
V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A)
20	0.46 at 0.5 A	1

FEATURES

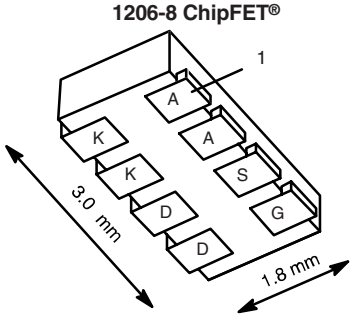
- **Halogen-free According to IEC 61249-2-21 Definition**
- LITTLE FOOT® *Plus* Schottky Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Charging Switch for Portable Devices
  - With Integrated Low V_f Trench Schottky Diode

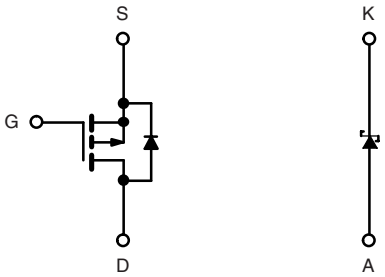
1206-8 ChipFET®



Bottom View

Marking Code

JH XX
Lot Traceability and Date Code
Part # Code



P-Channel MOSFET

Ordering Information: Si5853DDC-T1-E3 (Lead (Pb)-free)
Si5853DDC-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage (MOSFET)		V_{DS}	- 20	V
Reverse Voltage (Schottky)		V_{KA}	20	
Gate-Source Voltage (MOSFET)		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C) (MOSFET)	T_C = 25 °C	I_D	- 4[a]	A
	T_C = 70 °C		- 3.5	
	T_A = 25 °C		- 2.9[b, c]	
	T_A = 70 °C		- 2.3[b, c]	
Pulsed Drain Current (MOSFET)		I_{DM}	- 10	
Continuous Source Current (MOSFET Diode Conduction)	T_C = 25 °C	I_S	- 2.6	
	T_A = 25 °C		- 1.1[b, c]	
Average Forward Current (Schottky)		I_F	1	
Pulsed Forward Current (Schottky)		I_{FM}	3	
Maximum Power Dissipation (MOSFET)	T_C = 25 °C	P_D	3.1	W
	T_C = 70 °C		2	
	T_A = 25 °C		1.3[b, c]	
	T_A = 70 °C		0.8[b, c]	
Maximum Power Dissipation (Schottky)	T_C = 25 °C		2.5	
	T_C = 70 °C		1.6	
	T_A = 25 °C		1.2	
	T_A = 70 °C		0.76	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendation (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET)[b, c, f]	R_{thJA}	77	95	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	R_{thJF}	33	40	
Maximum Junction-to-Ambient (Schottky)[b, c, g]	R_{thJA}	85	105	
Maximum Junction-to-Foot (Drain) (Schottky)	R_{thJF}	40	50	

Notes:
a. Package limited.
b. Surface mounted on FR4 board.
c. t ≤ 5 s.
d. See Solder Profile (www.vishay.com/doc?73257). The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f .Maximum under steady state conditions for MOSFETs is 130 °C/W.
g. Maximum under steady state conditions for Schottky is 125 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS/TJ}$	I_D = - 250 µA		- 13		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)/TJ}$			2.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.4		- 1	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 85 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 2.9 A		0.085	0.105	Ω
		V_{GS} = - 2.5 V, I_D = - 2.5 A		0.117	0.143	
		V_{GS} = - 1.8 V, I_D = - 1.5 A		0.155	0.188	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 2.9 A		7		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		320		pF
Output Capacitance	C_{oss}			60		
Reverse Transfer Capacitance	C_{rss}			47		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 8 V, I_D = - 2.9 A		7.9	12	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 2.9 A		4.7	7.1	
Gate-Source Charge	Q_{gs}			0.65		
Gate-Drain Charge	Q_{gd}			1.35		
Gate Resistance	R_g	f = 1 MHz		6.5		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 4.4 Ω I_D ≅ - 2.3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		15	25	ns
Rise Time	t_r			17	30	
Turn-Off Delay Time	$t_{d(off)}$			21	30	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 4.4 Ω I_D ≅ - 2.3 A, V_{GEN} = - 8 V, R_g = 1 Ω		5	10	
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			10	15	

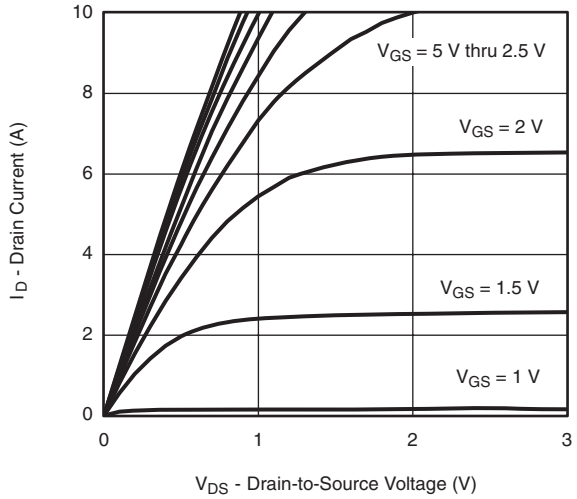
SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 2.6	A
Pulse Diode Forward Current	I_{SM}				- 10	
Body Diode Voltage	V_{SD}	I_S = - 2.3 A, V_{GS} = 0 V		- 0.85	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 2.3 A dI/dt = 100 A/µs T_J = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			9	20	nC
Reverse Recovery Fall Time	t_a			10		ns
Reverse Recovery Rise Time	t_b			5		

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

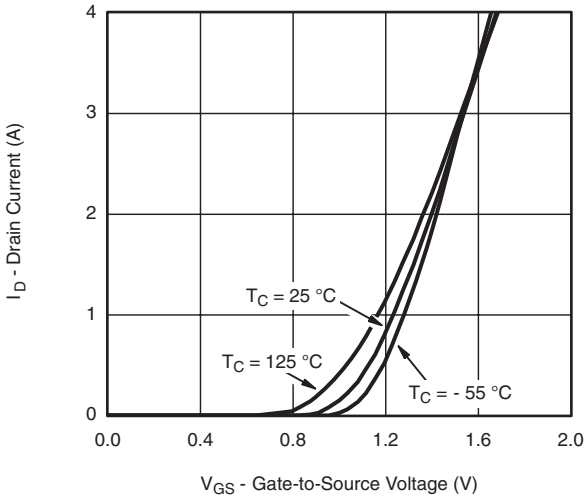
SCHOTTKY SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Forward Voltage Drop	V_F	I_F = 0.5 A		0.381	0.46	V
		I_F = 1 A		0.468	0.560	
		I_F = 1 A, T_J = 125 °C		0.44	0.53	
Maximum Reverse Leakage Current	I_{rm}	V_r = 5 V		0.0081	0.080	mA
		V_r = 5 V, T_J = 85 °C		0.4	4	
		V_r = 5 V, T_J = 125 °C		2.8	28	
		V_r = 20 V		0.0093	0.09	
		V_r = 20 V, T_J = 85 °C		0.45	4.5	
		V_r = 20 V, T_J = 125 °C		3.2	32	
Junction Capacitance	C_T	V_r = 10 V		30		pF

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

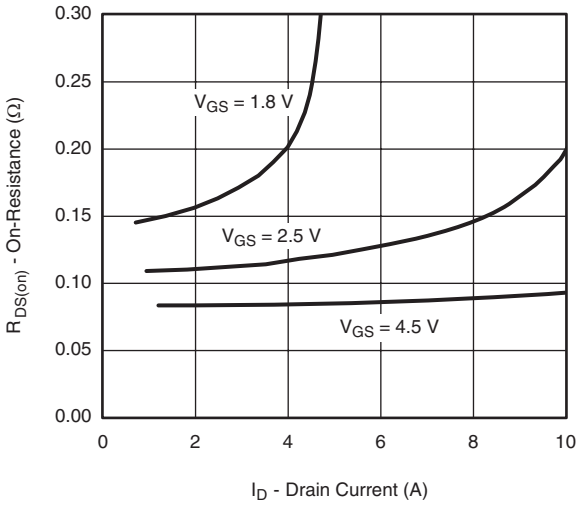
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



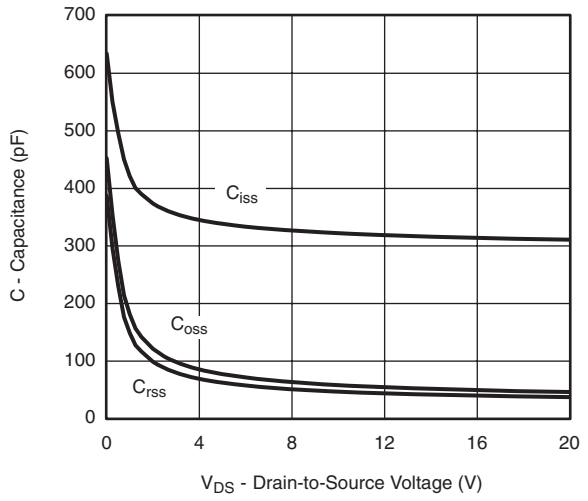
Output Characteristics



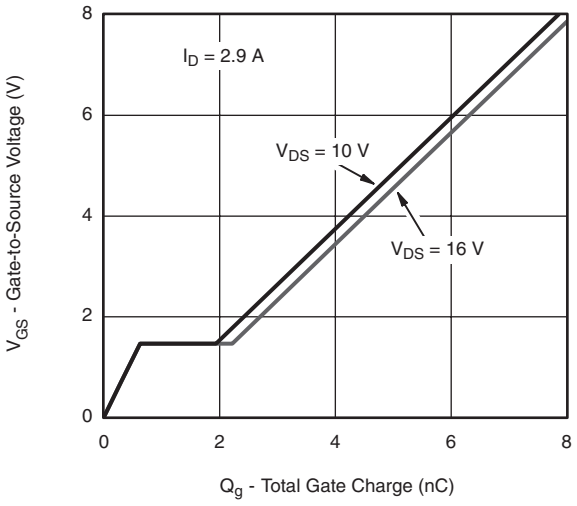
Transfer Characteristics



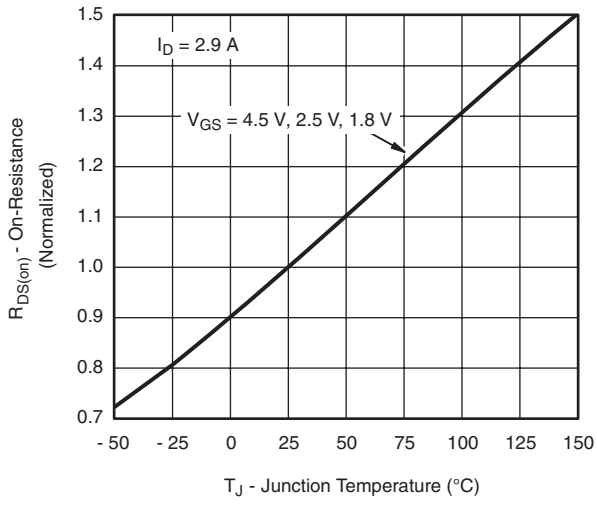
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

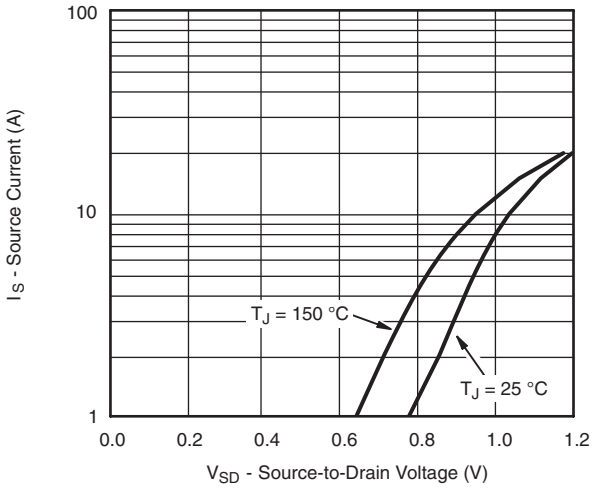


Gate Charge

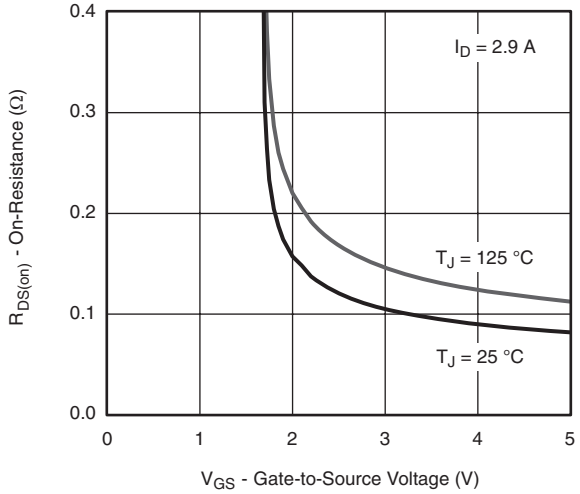


On-Resistance vs. Junction Temperature

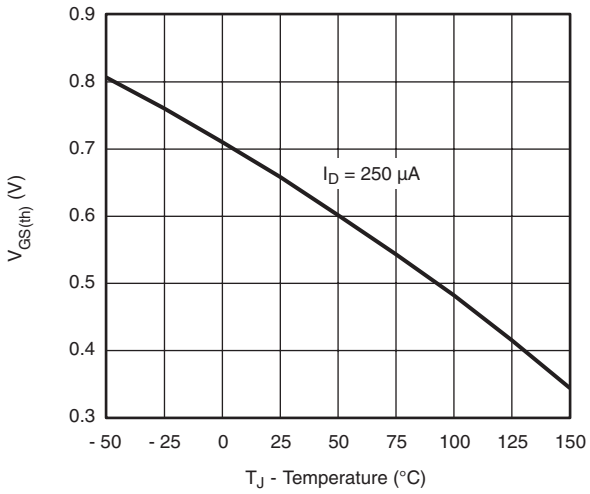
MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



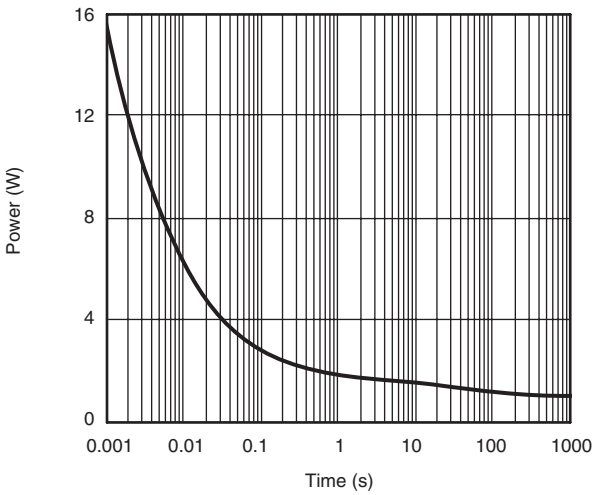
Source-Drain Diode Forward Voltage



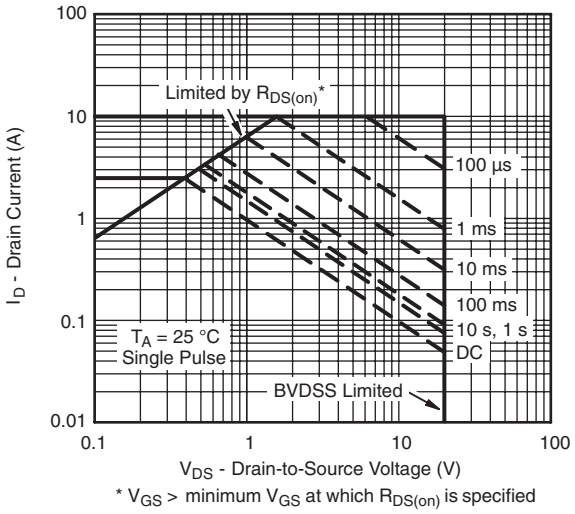
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



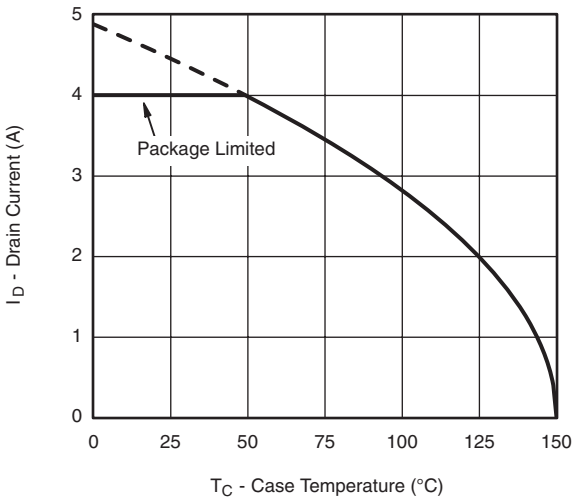
Single Pulse Power, Junction-to-Ambient



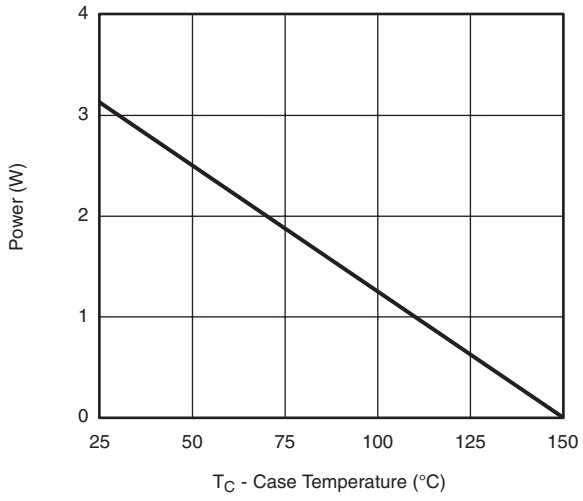
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



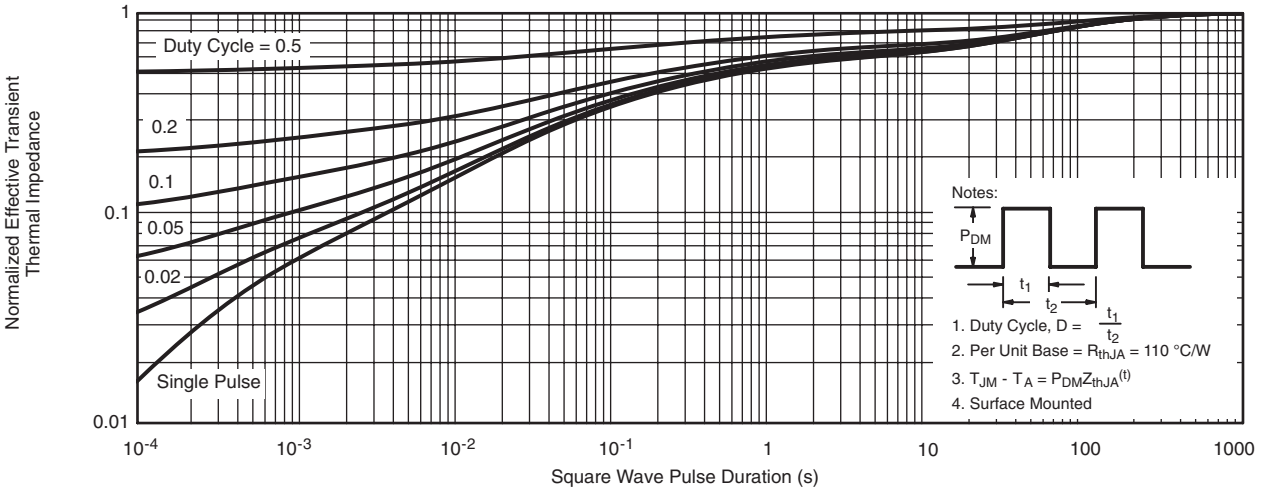
Current Derating*



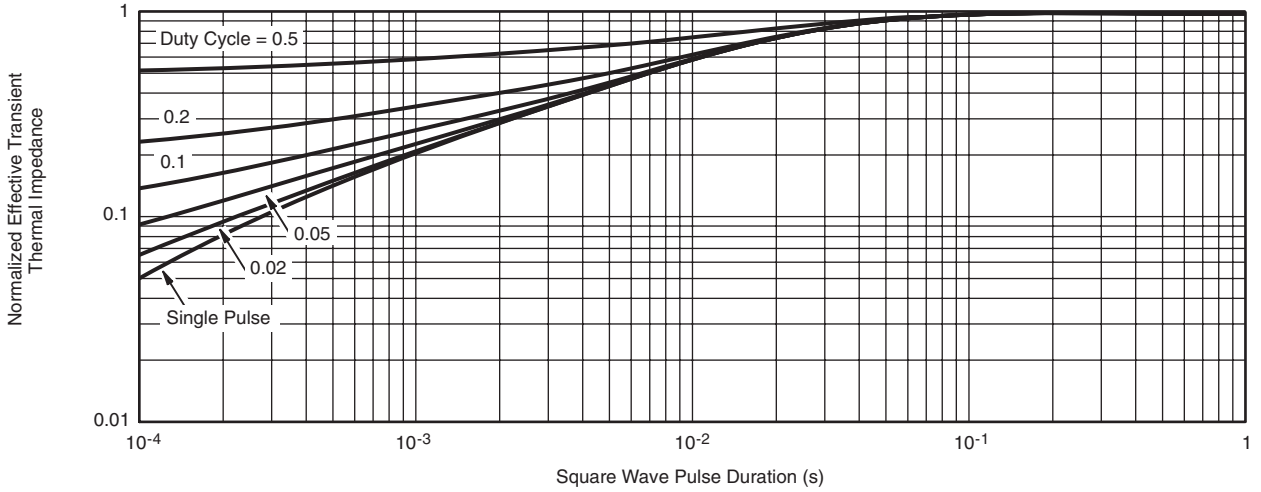
Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

MOSFET TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

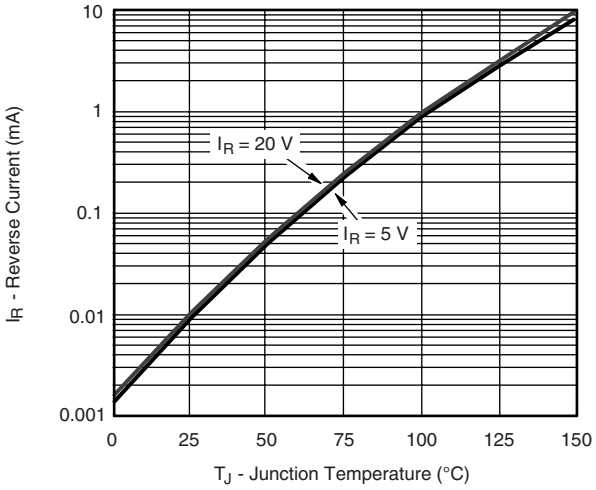


Normalized Thermal Transient Impedance, Junction-to-Ambient

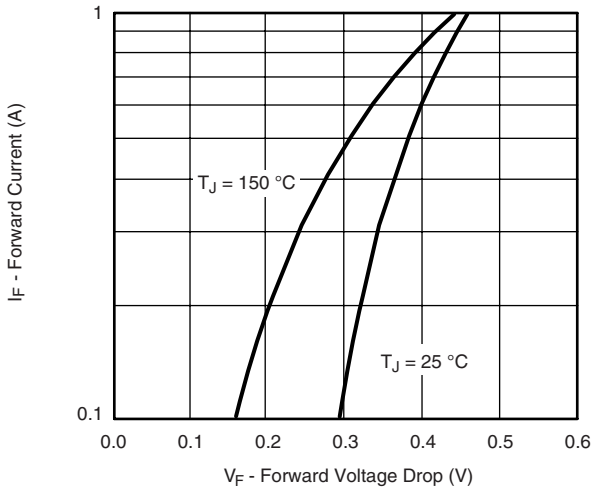


Normalized Thermal Transient Impedance, Junction-to-Foot

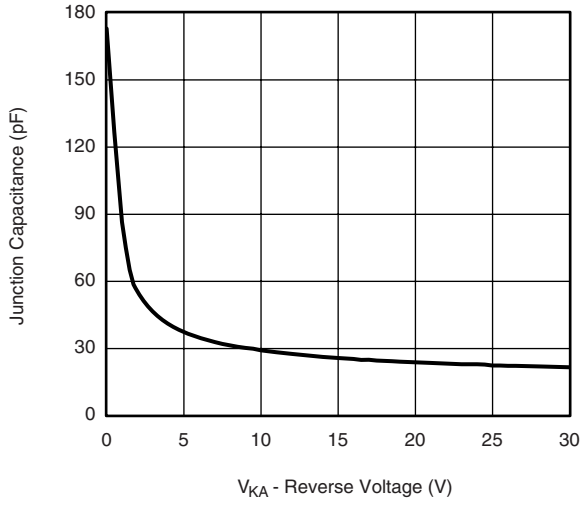
SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Reverse Current vs. Junction Temperature

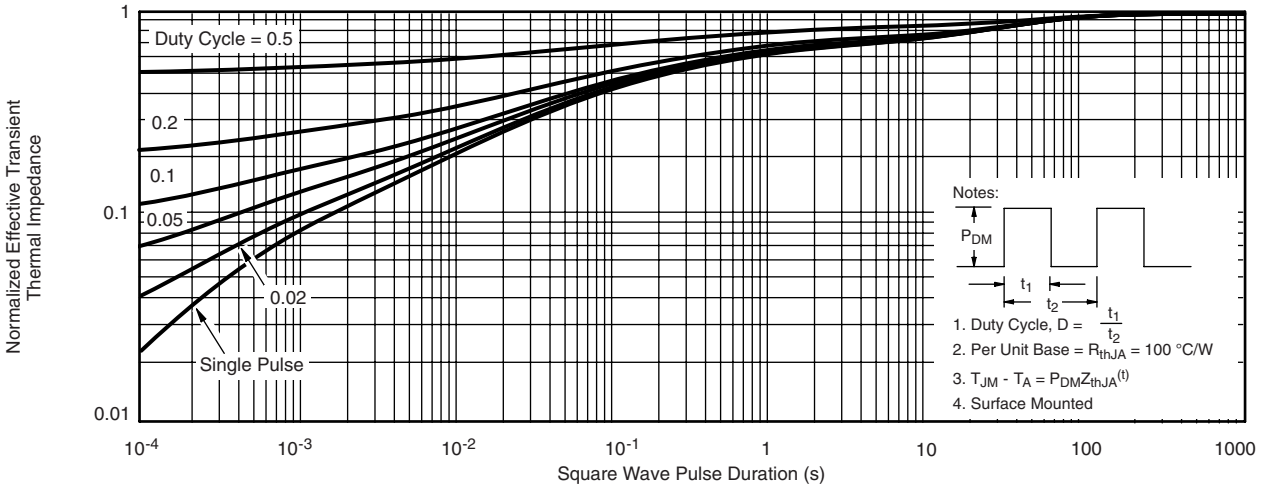


Forward Voltage Drop

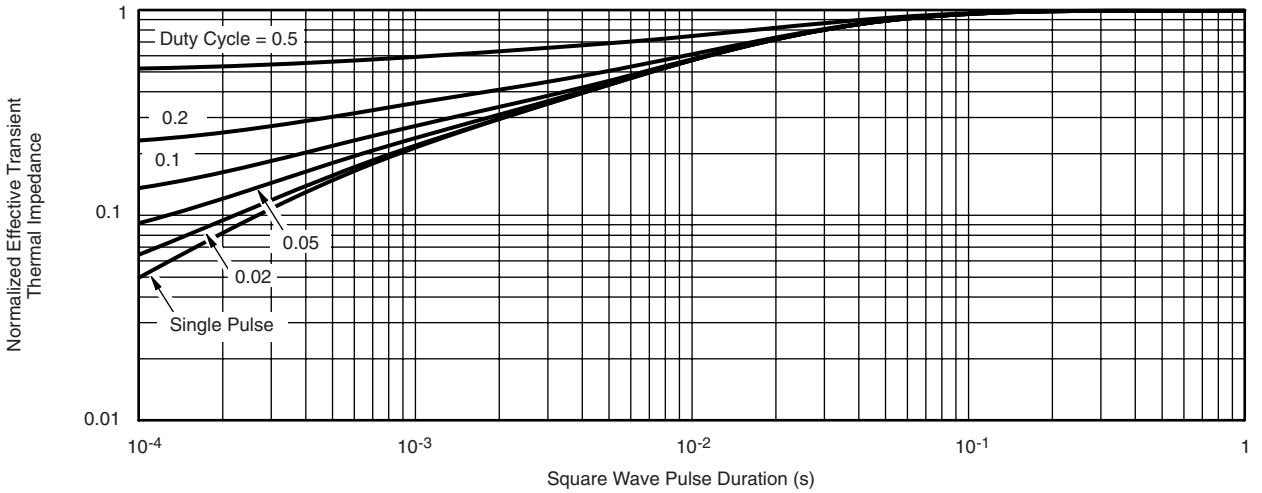


Capacitance

SCHOTTKY TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



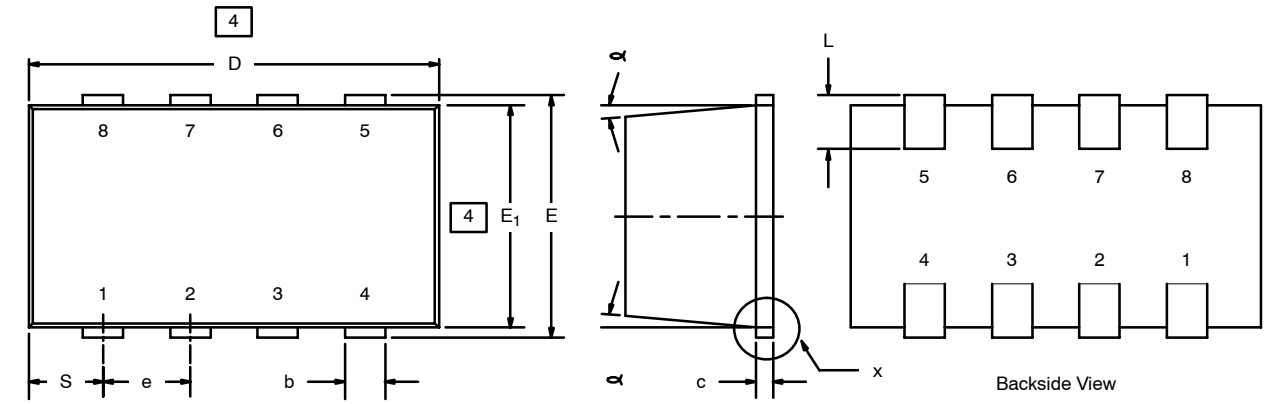
Normalized Thermal Transient Impedance, Junction-to-Ambient

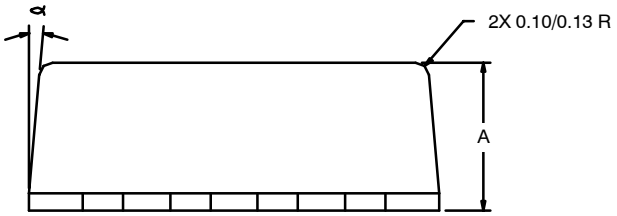


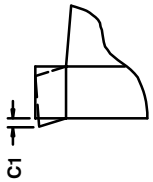
Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68979.

1206-8 ChipFET®







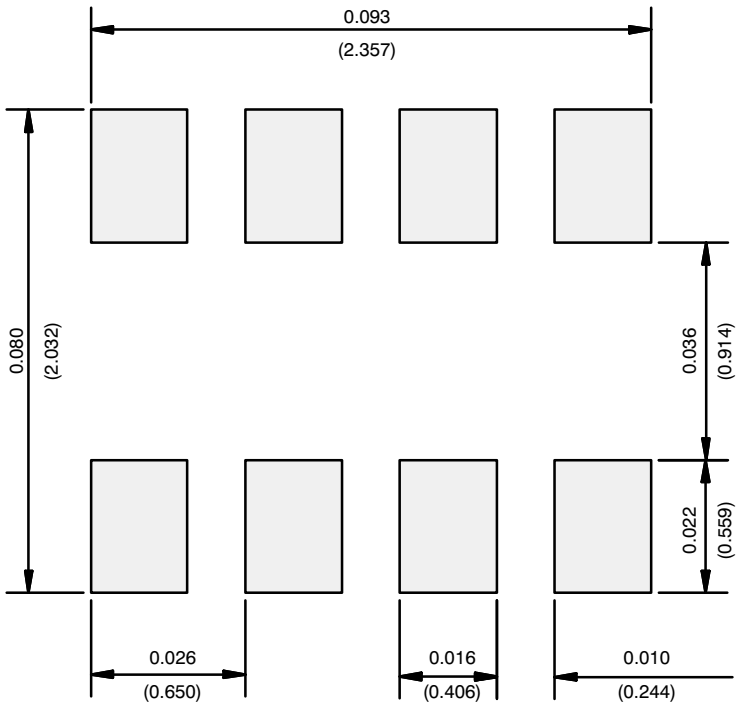
DETAIL X

NOTES:

1. All dimensions are in millimeaters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E_1	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04 DWG: 5547						

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

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