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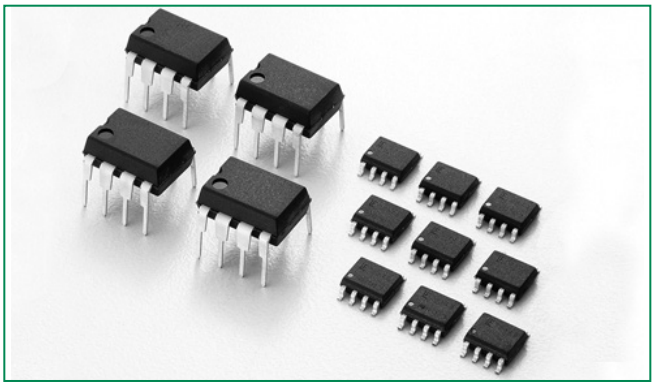
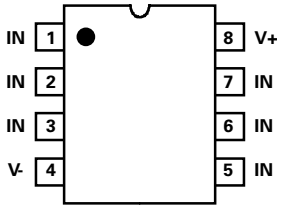
SP721 Series 3pF 4kV Diode Array

RoHS Pb GREEN

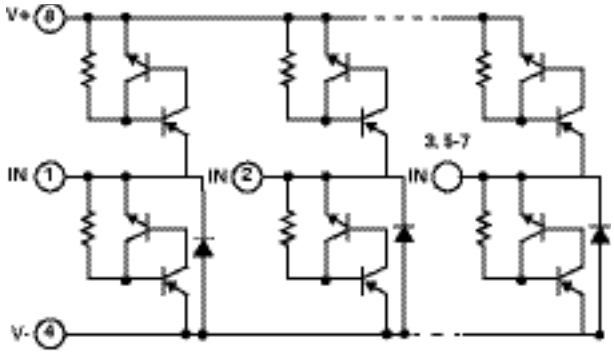


Pinout

SP721 (PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Additional Information

Datasheet | Resources | Samples

Description

The SP721 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP721 has 2 protection SCR/Diode device structures per input. There are a total of 6 available inputs that can be used to protect up to 6 external signal or bus lines. Over-voltage protection is from the IN (Pins 1 - 3 and Pins 5 - 7) to V+ or V-.

The SCR structures are designed for fast triggering at a threshold of one $+V_{BE}$ diode threshold above V+ (Pin 8) or a $-V_{BE}$ diode threshold below V- (Pin 4). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than one V_{BE} above V+. A similar clamp to V- is activated if a negative pulse, one V_{BE} less than V-, is applied to an IN input. Standard ESD Human Body Model (HBM) Capability is:

Features

- ESD Interface Capability for HBM Standards
  - MIL STD 3015.7 ..... 15kV
  - IEC 61000-4-2, Direct Discharge,
  - Single Input ..... 4kV (Level 2)
  - Two Inputs in Parallel ..... 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge ..... 15kV (Level 4)
- High Peak Current Capability
  - IEC 61000-4-5 (8/20µs) ..... ±3A
  - Single Pulse, 100µs Pulse Width ..... ±2A
  - Single Pulse, 4µs Pulse Width ..... ±5A
- Designed to Provide Over-Voltage Protection
  - Single-Ended Voltage Range to ..... +30V
  - Differential Voltage Range to ..... ±15V
- Fast Switching ..... 2ns Rise Time
- Low Input Leakages ..... 1nA at 25°C Typical
- Low Input Capacitance ..... 3pF Typical
- An Array of 6 SCR/Diode Pairs
- Operating Temperature Range ..... -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

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TVS Diode Arrays (SPA® Diodes)

General Purpose ESD Protection - SP721 Series

Absolute Maximum Ratings

Parameter	Rating	Units
Continuous Supply Voltage, (V+) - (V-)	+35	V
Forward Peak Current, I_{IN} to V_{CC}, I_{IN} to GND (Refer to Figure 5)	±2, 100µs	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note:

ESD Ratings and Capability (Figure 1, Table 1)

Load Dump and Reverse Battery (Note 2)

Thermal Information

Parameter	Rating	Units
Thermal Resistance (Typical, Note 1)	θ_{JA}	°C/W
PDIP Package	160	°C/W
SOIC Package	170	°C/W
Maximum Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature (Plastic Package)	150	°C
Maximum Lead Temperature (Soldering 20-40s)(SOIC Lead Tips Only)	260	°C

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Characteristics T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

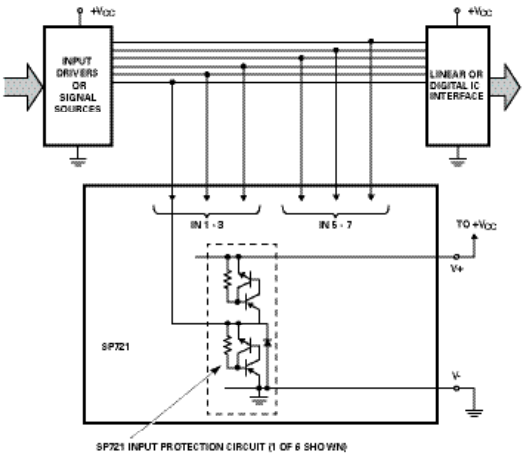
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Operating Voltage Range,	V_{SUPPLY}		-	2 to 30	-	V
V_{SUPPLY} = [(V+) - (V-)]						
Forward Voltage Drop						
IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-20	5	+20	nA
Quiescent Supply Current	$I_{QUIESCENT}$		-	50	200	nA
Equivalent SCR ON Threshold		Note 3	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD}; Note 3	-	1	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF
Input Switching Speed	t_{ON}		-	2	-	ns

Notes:

2. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to het same supply voltage source as the device or control line under protection, a current limiti ng resistor should be connected in series between the external supply and the SP721 supply pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01µF or larger romf the V+ and V- Pins to ground are recommended.
3. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for thumb-rule nformation to determine peak current and dissipation under EOS conditions.

Typical Application of the SP721

(Application as an Input Clamp for Over-voltage, Greater than 1V_{BE} Above V+ or less than -1V_{BE} below V-)



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ESD Capability

ESD capability is dependent on the application and defined test standard.The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.

For the "Modified"MIL-STD-3015.7 condition that is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground and the SP721 ESD capability is typically greater than 15kV from 100pF through 1.5kΩ.By strict definition of MIL-STD-3015.7 using "pin-to-pin"device testing, the ESD voltage capability is greater than 6kV.The MIL-STD-3015.7 results were determined from AT&T ESD Test Lab measurements.

The HBM capability to the IEC 61000-4-2 standard is greater than 15kV for air discharge (Level 4) and greater than 4kV for direct discharge (Level 2).Dual pin capability (2 adjacent pins in parallel) is well in excess of 8kV (Level 4).

For ESD testing of the SP721 to EIAJ IC121 Machine Model (MM) standard, the results are typically better than 1kV from 200pF with no series resistance.

Figure 1: Electrostatic Discharge Test

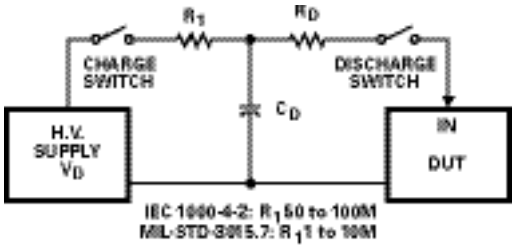


Table 1: ESD Test Conditions

Standard	Type/Mode	R_D	C_D	$\pm V_D$
MIL STD 3015.7	Modified HBM	1.5kΩ	100pF	15kV
	Standard HBM	1.5kΩ	100pF	6kV
IEC 61000-4-2	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	4kV
	HBM, Direct Discharge, Two Parallel Input Pins	330Ω	150pF	8kV
EIAJ IC121	Machine Model	0kΩ	200pF	1kV

Figure 2: Low Current SCR Forward Voltage Drop Curve

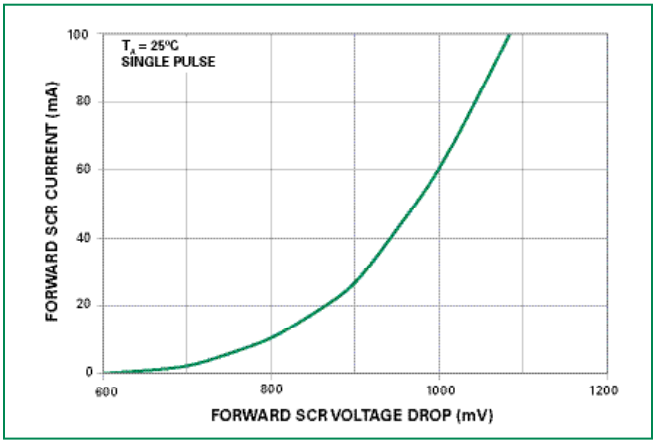
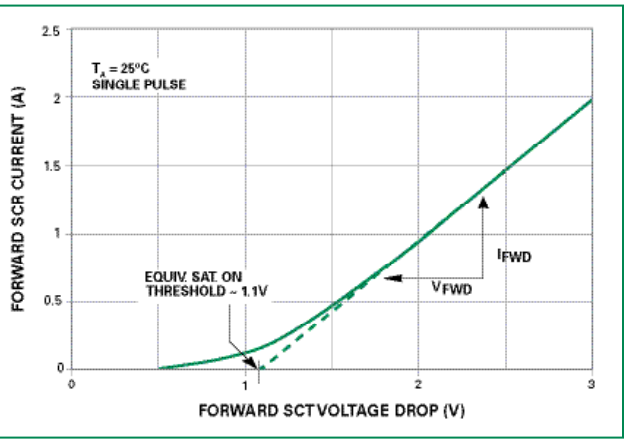


Figure 3: High Current SCR Forward Voltage Drop Curve



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Peak Transient Current Capability of the SP721

The peak transient current capability rises sharply as the width of the current pulse narrows. Destructive testing was done to fully evaluate the SP721's ability to withstand a wide range of peak current pulses vs time. The circuit used to generate current pulses is shown in Figure 4.

The test circuit of Figure 4 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP721 'IN' input pin and the (+) current pulse input goes to the SP721 V- pin. The V+ to V- supply of the SP721 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.) Figure 5 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits.

The maximum peak input current capability is dependent on the ambient temperature, improving as the temperature is reduced. Peak current curves are shown for ambient temperatures of 25ºC and 105ºC and a 15V power supply condition. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curves of Figure 5.

Note that adjacent input pins of the SP721 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.

Figure 4: Typical SP721 Peak Current Test Circuit with a Variable Pulse Width Input

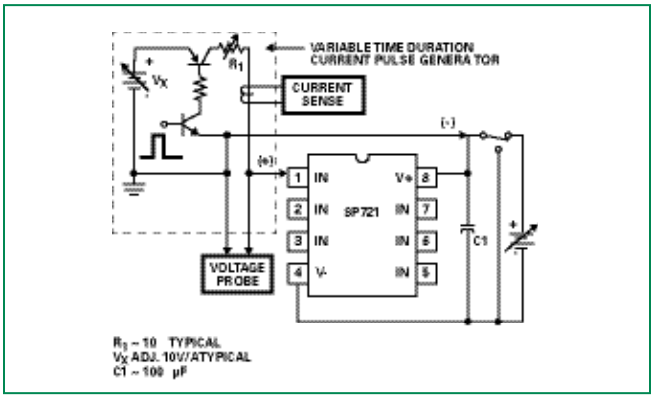
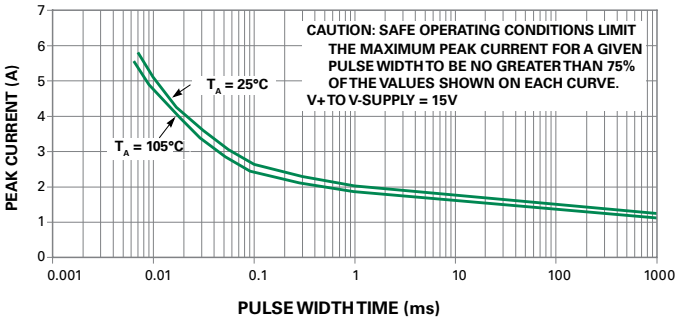


Figure 5: SP721 Typical Single Peak Current Pulse Capability

Showing the Measured Point of Overstress in Amperes vs pulse width time in milliseconds



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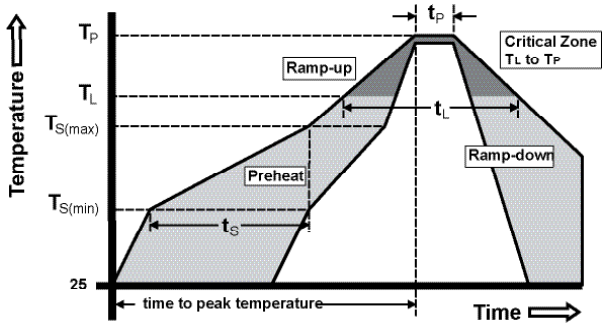
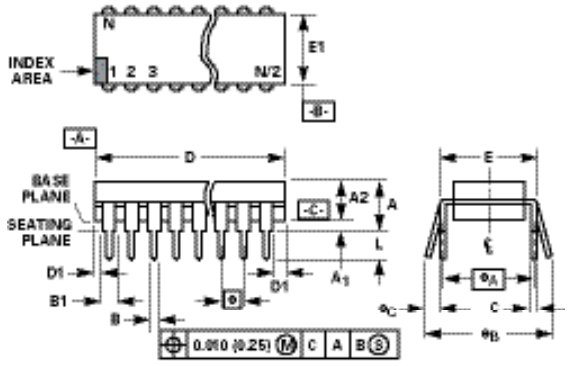
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



Package Dimensions — Dual-In-Line Plastic Packages (PDIP)



Package	PDIP				
Pins	8 Lead Dual-in-Line				
JEDEC	MS-001				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	9.01	10.16	0.355	0.400	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.10	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	8		8		9

Notes:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is t he maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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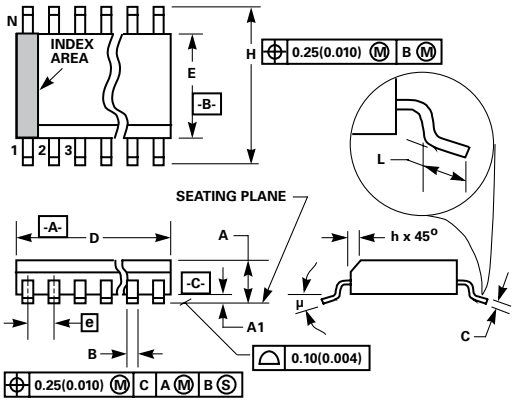
TVS Diode Arrays (SPA® Diodes)

General Purpose ESD Protection - SP721 Series

Package Dimensions — Small Outline Plastic Packages (SOIC)

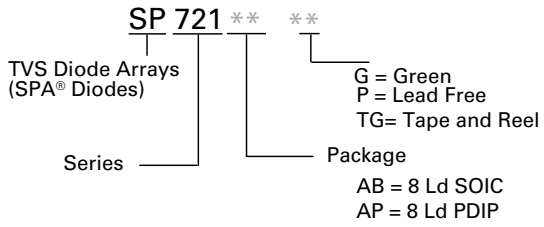


Package	SOIC				
Pins	8				
JEDEC	MS-012				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	4.80	5.00	0.1890	0.1968	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	8		8		7
μ	0°	8°	0°	8°	-

Notes:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Part Numbering System



Product Characteristics

Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

Ordering Information

Part Number	Temp. Range (°C)	Package	Environmental Informaton	Marking	Min. Order
SP721APP	-40 to 105	8 Ld PDIP	Lead-free	SP721AP(P) [1]	2000
SP721ABG	-40 to 105	8 Ld SOIC	Green	SP721A(B)G [2]	1960
SP721ABTG	-40 to 105	8 Ld SOIC Tape and Reel	Green	SP721A(B)G [2]	2500

Notes:

1. SP721AP(P) means device marking either SP721AP or SP721APP.
2. SP721A(B)G means device marking either SP721AG or SP721ABG which are good for types SP721ABG and SP721ABTG.

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