MPQ3910A

35V, Boost PWM Controller with Configurable Frequency, Soft Start, and Light-Load Operation, AEC-Q100 Qualified

DESCRIPTION

The MPQ3910A is a peak current mode, PWM boost controller that can drive an external MOSFET capable of handling more than 10A of current. The device has a typical operational current of 288µA, and can accommodate flyback, boost, and single-ended primary inductor converter (SEPIC) applications.

Current-mode control provides simple loop compensation and cycle-by-cycle current limiting. Under-voltage lockout (UVLO), soft start (SS), an internal regulated supply, and slope compensation are all provided to minimize the external component count.

The 1A gate driver minimizes the power loss of the external MOSFET while allowing the use of a wide variety of standard threshold devices. Additionally, the MPQ3910A uses pulse-skip mode to improve the efficiency under light loads or no load. Protection features include hiccup mode for overload protection (OLP), over-voltage protection (OVP), and short-circuit protection (SCP).

The MPQ3910A is available in an MSOP-10 package.

FEATURES

- Guaranteed Industrial/Automotive Temperature
- 5V to 35V Supply Voltage Range (1)
- 12V, 1A MOSFET Gate Driver
- External Soft Start (SS)
- Pulse-Skip Mode under Light Loads
- Configurable 30kHz to 400kHz Switching Frequency
- Frequency Synchronizable from 80kHz to 400kHz
- Cycle-by-Cycle Current Limit
- Over-Voltage Protection (OVP)
- Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Available in an MSOP-10 Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

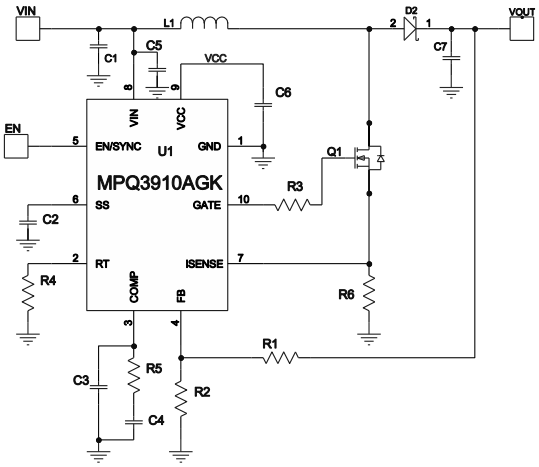
- Telecom Isolated Power Supplies
- Backup Boosts
- Start-Stop Boosts

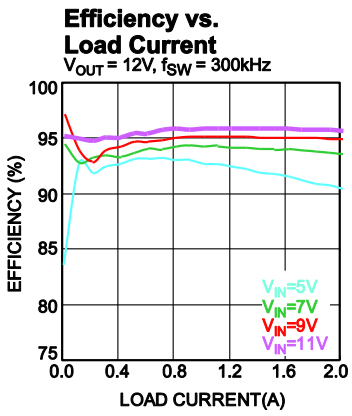
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Note:

1) See the Internal VCC Regulator section on page 12 for a <7V input voltage application.

TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3910AGK-AEC1	MSOP-10	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3910AGK-AEC1-Z).

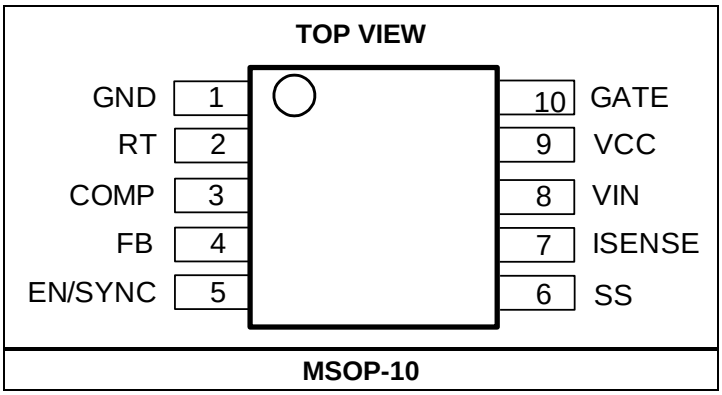
TOP MARKING

YWLLL

3910A

Y: Year code
W: Week code
3910A: First five digits of the part number
LLL: Lot number

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Power ground pin gate driver return.**
2	RT	**Switching frequency set pin.** Connect a resistor from RT to GND to set the switching frequency between 30kHz and 400kHz.
3	COMP	**Error amplifier output.**
4	FB	**Feedback and OVP monitor.** The FB pin has a respective internal reference voltage for non-isolated solutions. For isolated solutions, the FB pin monitors for over-voltage protection (OVP). If a non-isolated solution is used, connect FB to GND.
5	EN/SYNC	**On/off control Input.** EN/SYNC is internally connected to GND with a 1MΩ resistor. To synchronize the switching frequency, apply an external clock to the EN/SYNC pin. The external clock frequency must exceed the frequency set by the RT pin.
6	SS	**Soft start.** Connect a capacitor between SS and GND to control the period during which the COMP voltage rises. SS determines both the soft-start current and hiccup protection delay.
7	ISENSE	**Current sense and application mode set.** During start-up, ISENSE outputs a current signal and senses the voltage to detect the mode setting. During normal operation, ISENSE senses the voltage across the sense resistor for current-mode control, cycle-by-cycle current limiting, overload protection (OLP), and short-circuit protection (SCP).
8	VIN	**Input supply.** Connect a bypass capacitor from VIN to GND.
9	VCC	**Internal 12V regulator output.** Connect a capacitor between VCC and GND to bypass the internal regulator.
10	GATE	**External N-channel power MOSFET device driver.**

ABSOLUTE MAXIMUM RATINGS (2)

VIN to GND .....-0.3V to +40V
VCC, GATE to GND.....-0.3V to +15V
All other pins .....-0.3V to +6V
EN pin sink current 0.5mA (6)
Continuous power dissipation (T_A = 25°C) (3)
..... 0.83W
Maximum operating frequency..... 500kHz
Storage temperature ..... -55°C to +150°C
Junction temperature .....150°C
Lead temperature .....260°C

ESD Ratings

Human body model (HBM).....
JEDEC.....Class 2
AEC-Q100.....H2
Charged device model (CDM).....
JEDEC.....C3
AEC-Q100.....C3

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....7V to 35V
Supply voltage with VIN and VCC connected.....
.....5V to 13V
EN sink current ..... 0mA to 0.4mA (5)
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

MSOP-10 ..... 150 ..... 65... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.
6) See the Enable/SYNC Control (EN/SYNC) section on page 13 for more details.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 18V, T_J = -40°C to +125°C, typical values are tested at 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Management						
VCC UVLO threshold	V_{UVLO}	Rising edge	3.8	4.2	4.6	V
VCC UVLO hysteresis	V_{UVLO_HYS}			350		mV
Shutdown current	I_S	V_{EN} = 0V			1	µA
Quiescent current	I_Q	V_{FB} = 1.5V		288	523	µA
VCC regulation voltage	V_{CC}	V_{CC} load = 0mA to 10mA	10.8	11.8	12.8	V
Driving Signal						
Gate driver impedance (sourcing)		I_{GATE} = -20mA		4.1		Ω
Gate driver impedance (sinking)		I_{GATE} = 20mA		2		Ω
Error Amplifier (EA)						
Error amplifier transconductance	G_{EA}	V_{FB} is ±50mV from the FB threshold 1.26V, V_{COMP} = 1.5V		0.62		mA/V
Maximum amplifier output current		Source current		78		µA
		Sink current		70		
COMP high voltage		I_{SENSE} = 0V, V_{FB} = 1V		2.4		V
		I_{SENSE} = 1V, floating COMP				
Current Sense						
Current comparator leading edge blanking (9)	t_{LEB}			214		ns
ISENSE limit	V_{LIMIT}	T_J = 25°C	145	185	215	mV
SCP limit (7)	V_{SCP}			350		mV
Current-sense amplifier gain	G_{SENSE}	ΔV_{COMP} / ΔV_{ISENSE}		3.2		V/V
ISENSE bias current	I_{SENSE}	T_J = 25°C		0.01	0.15	µA
PWM						
V_{COMP} (skip mode) (7)		Pulse-skip mode threshold, V_{COMP}		0.95		V
Switching frequency	f_{SW}	R_T = 6.81kΩ	300	337	374	kHz
		R_T = 80.6kΩ	24	30	36	kHz
Minimum on time	t_{ON-MIN}			214	400	ns
Maximum duty cycle	D_{MAX}	R_T = 6.81kΩ	92	95		%
Soft Start (SS)						
Charge current(8)	I_{SS}			54		µA
Overload detection discharge current				17.8		µA
Discharge current during protection				1.66		µA
Charged threshold voltage				3.65		V
Overload shutdown threshold voltage				3.27		V
Protection reset threshold voltage				0.2		V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_J = -40°C to +125°C, typical values are tested at 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Feedback Management						
FB reference voltage	V_{FB}	T_J = 25°C	1.216	1.237	1.258	V
		T_J = -40°C to +125°C	1.211	1.237	1.263	V
FB bias current	I_{FB}	V_{FB} = 1.237V, T_J = 25°C		0.01	0.15	µA
OVP reference level	V_{OVP}	T_J = 25°C	1.39	1.44	1.49	V
		T_J = -40°C to +125°C	1.296		1.584	V
Enable Control						
Enable rising threshold	$V_{EN-RISING}$		1.4	1.65	1.9	V
Enable hysteresis	V_{EN-HYS}			540		mV
Enable turn-off delay	t_{TD-OFF}			20		µs
Enable input current	I_{EN}	V_{EN} = 3V		2.5	5	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			160		°C
Thermal hysteresis (7)				20		°C

Notes:

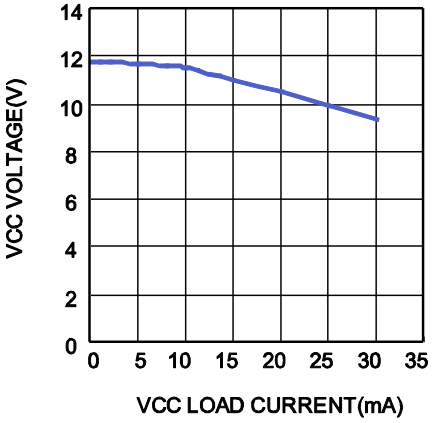
7) Guaranteed by engineering sample characterization.
8) See the Soft Start (SS) section on page 13 for a detailed function description of the discharge current and threshold voltage.
9) Same as the minimum on time.

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TYPICAL CHARACTERISTICS

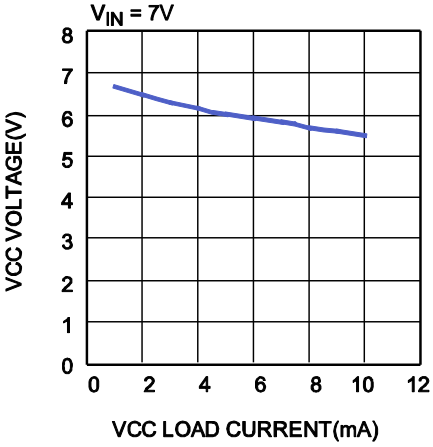
V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

VCC Voltage vs. VCC Load Current

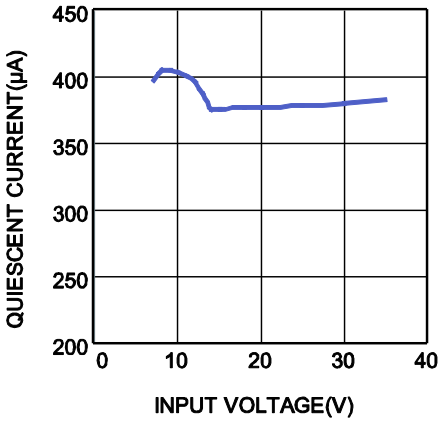


VCC Voltage vs. Load Current

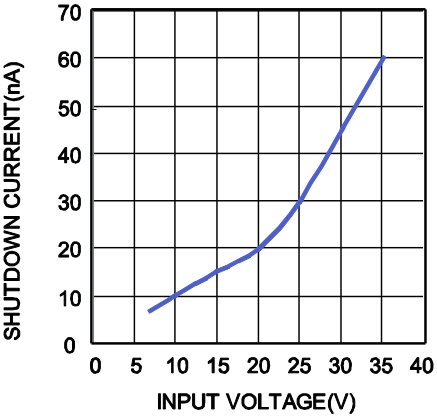
V_{IN} = 7V



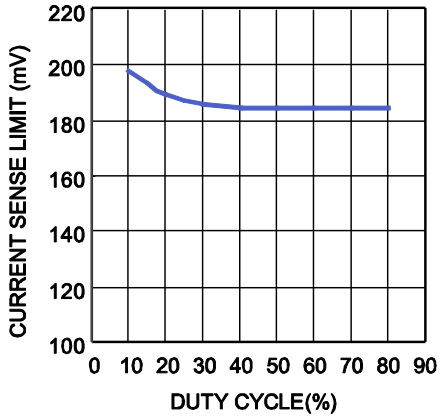
Quiescent Current vs. Input



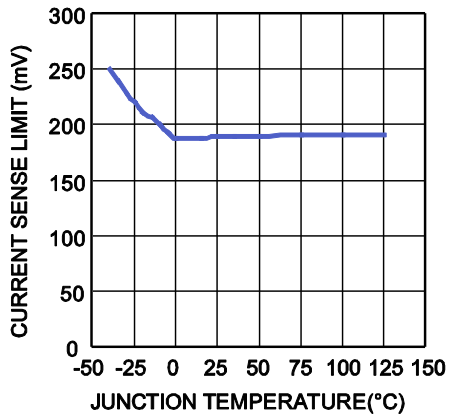
Shutdown Current vs. Input Voltage



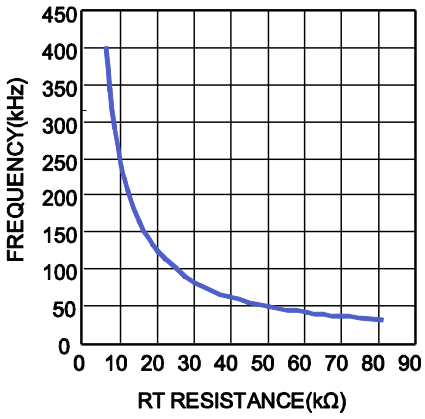
Current Sense Limit vs. Duty Cycle



Current Sense Limit vs. Temperature

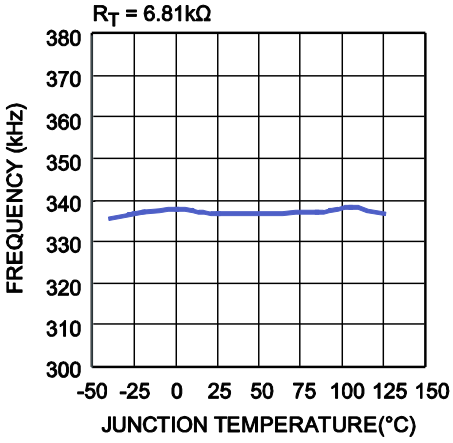


Frequency vs. RT Resistance



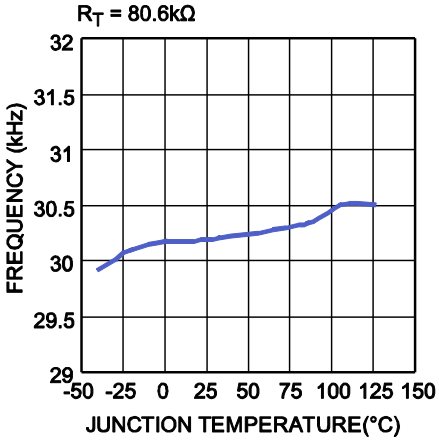
Frequency vs. Temperature

R_T = 6.81kΩ



Frequency vs. Temperature

R_T = 80.6kΩ

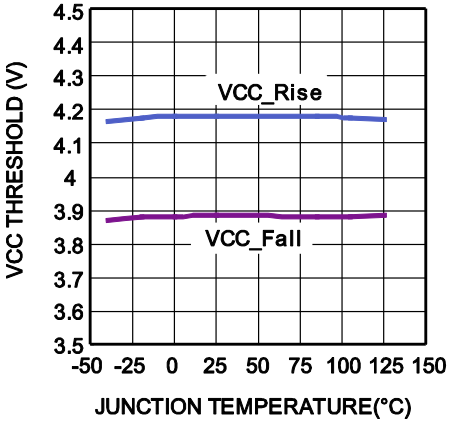


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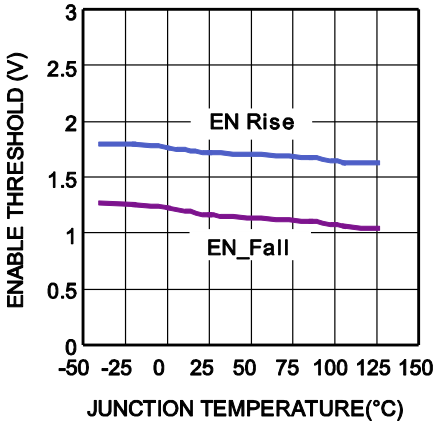
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 18V, T_A = 25°C, unless otherwise noted.

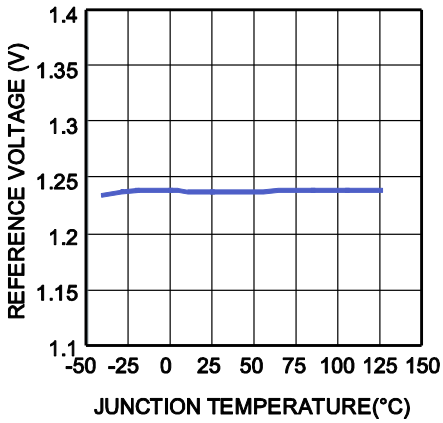
VCC Threshold vs. Temperature



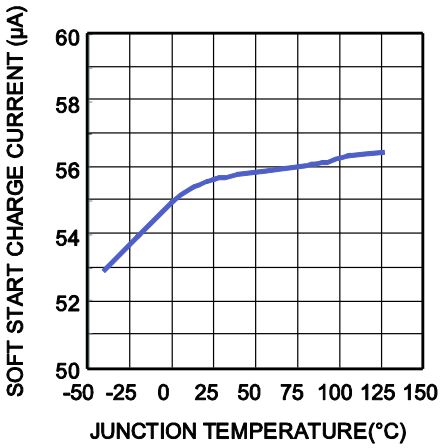
EN Threshold vs. Temperature



V_{REF} vs. Temperature

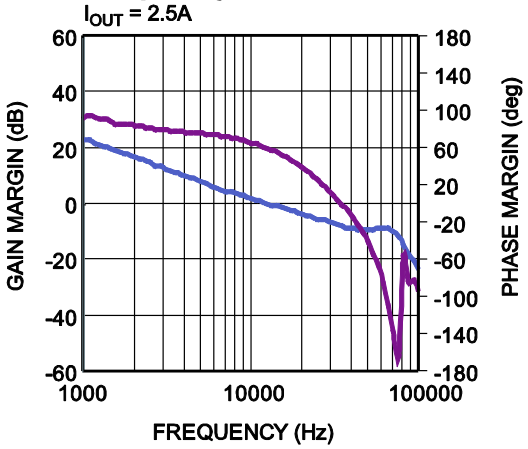


SS Charge Current vs. Temperature



Gain and Phase vs. Frequency

I_{OUT} = 2.5A

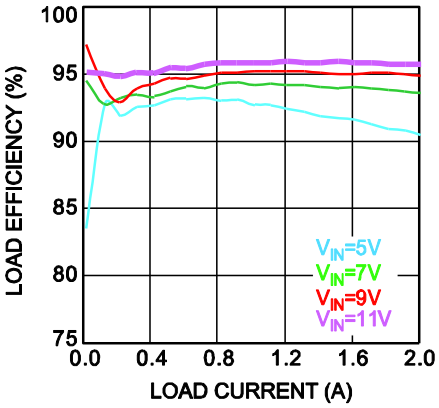


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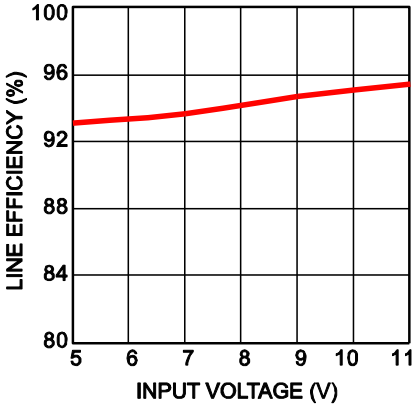
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 24V, f_{SW} = 300kHz, T_A = 25°C, unless otherwise noted.

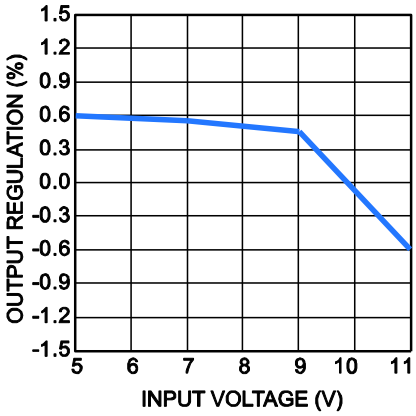
Load Efficiency
V_{OUT} = 12V



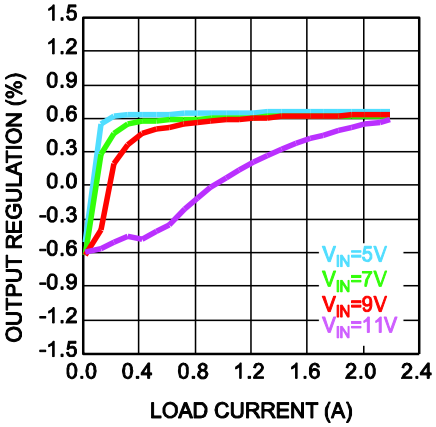
Line Efficiency
V_{OUT} = 12V



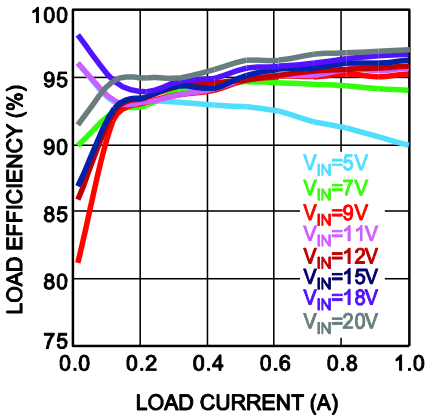
Line Regulation
V_{OUT} = 12V



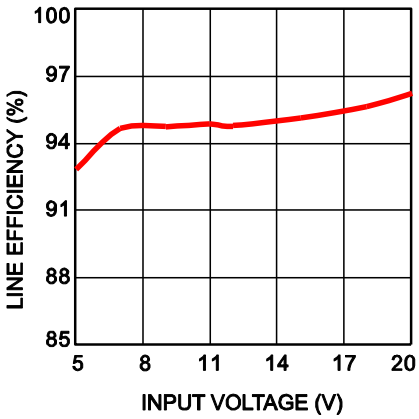
Load Regulation
V_{OUT} = 12V



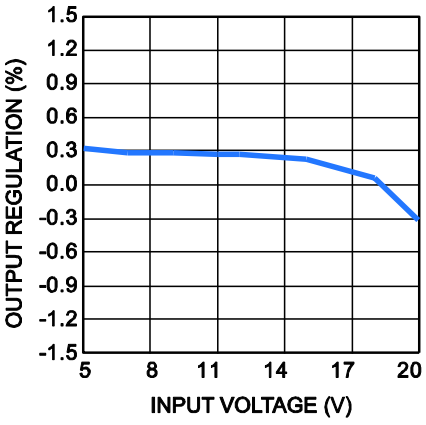
Load Efficiency
V_{OUT} = 24V



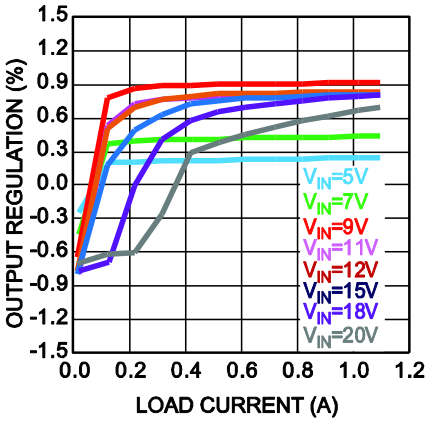
Line Efficiency
V_{OUT} = 24V



Line Regulation
V_{OUT} = 24V



Load Regulation
V_{OUT} = 24V

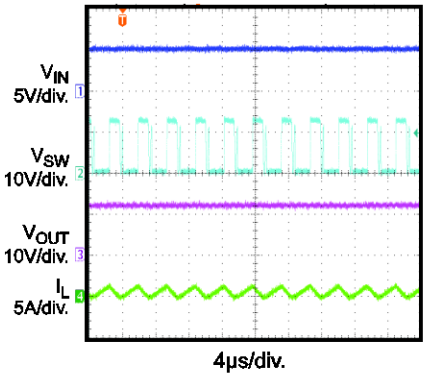


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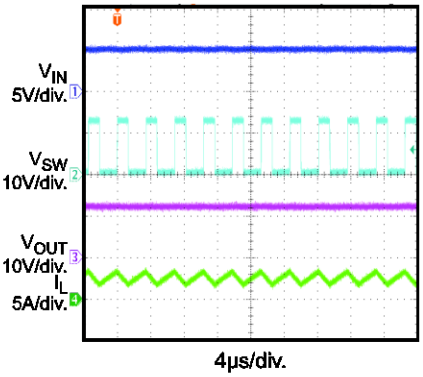
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 24V, f_{SW} = 300kHz, T_A = 25°C, unless otherwise noted.

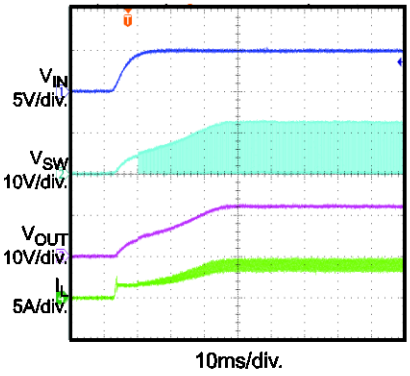
Steady State
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.2A



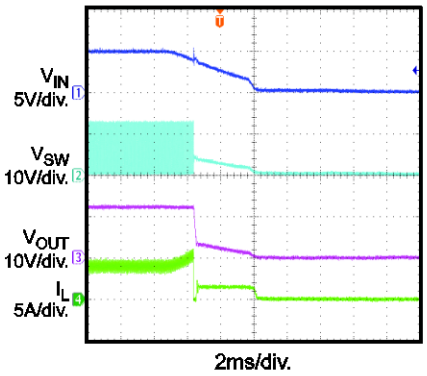
Line Efficiency
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1A



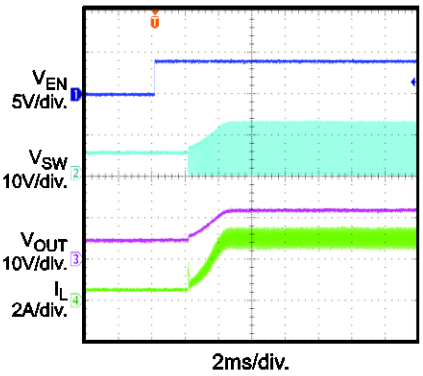
Start-Up through V_{IN}
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.5A



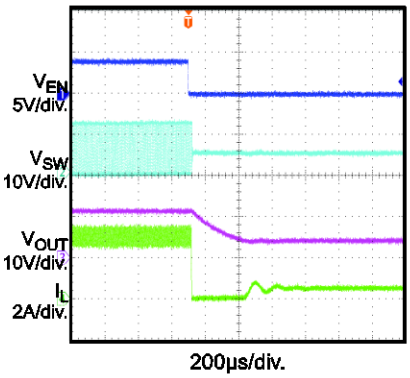
Shutdown through V_{IN}
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.5A



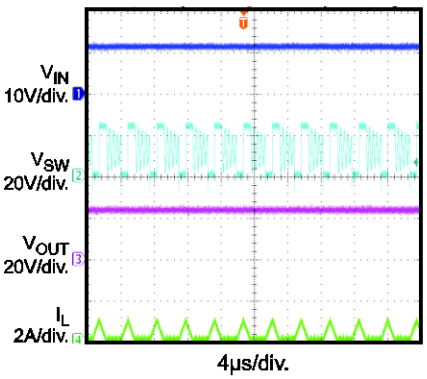
Start-Up through EN
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.2A



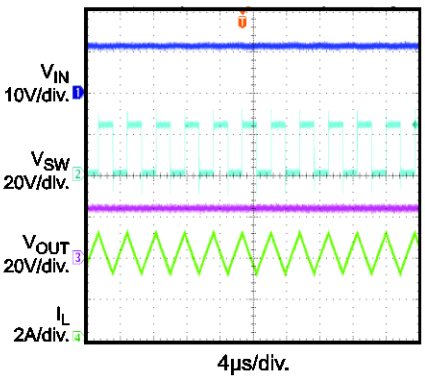
Shutdown through EN
V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 1.2A



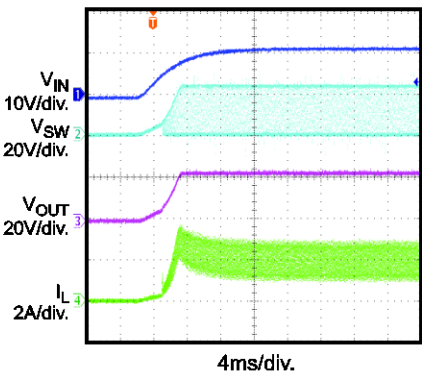
Steady State
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 0.1A



Line Efficiency
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 2A



Start-Up through V_{IN}
V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A



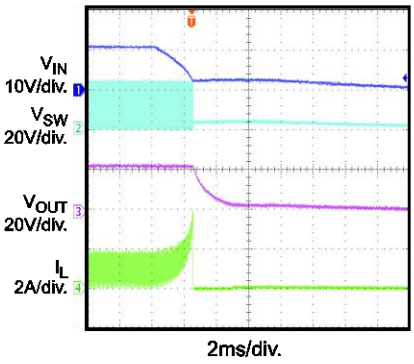
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 24V, f_{SW} = 300kHz, T_A = 25°C, unless otherwise noted.

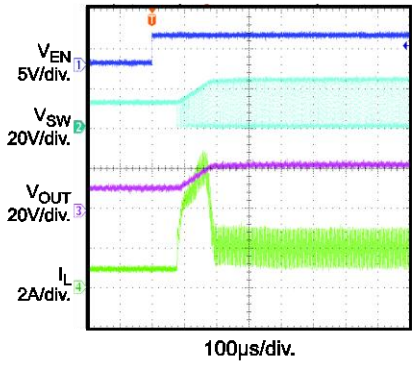
Shutdown through V_{IN}

V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A



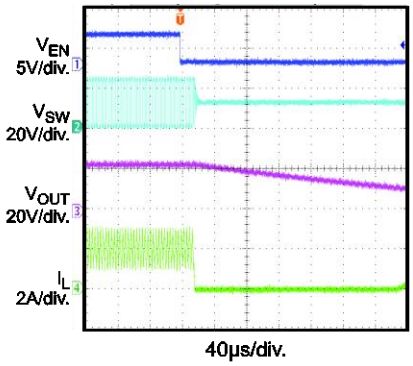
Start-Up through EN

V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A



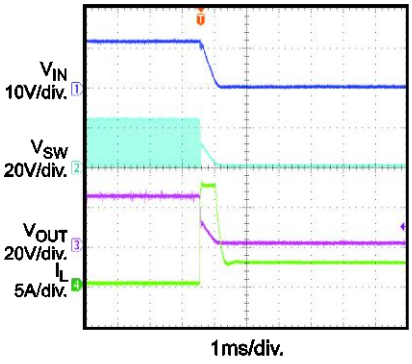
Shutdown through EN

V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 1A



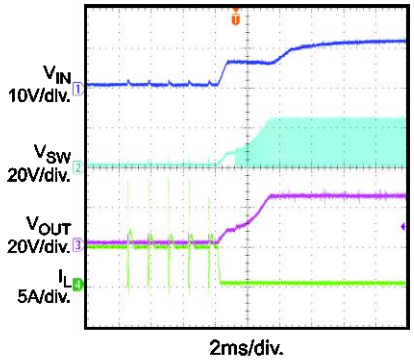
SCP

V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 0.3A



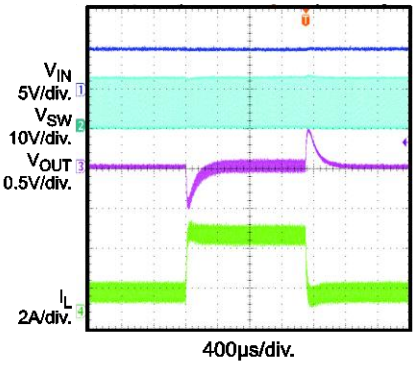
SCP Recovery

V_{IN} = 12V, V_{OUT} = 24V, I_{OUT} = 0.3A



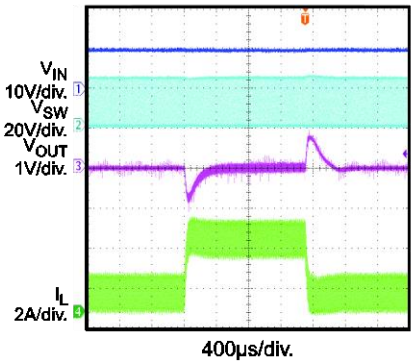
Load Transient

V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.4A to 1.5A



Load Transient

V_{IN} = 10V, V_{OUT} = 24V, I_{OUT} = 0.4A to 1.5A



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FUNTIONAL BLOCK DIAGRAM

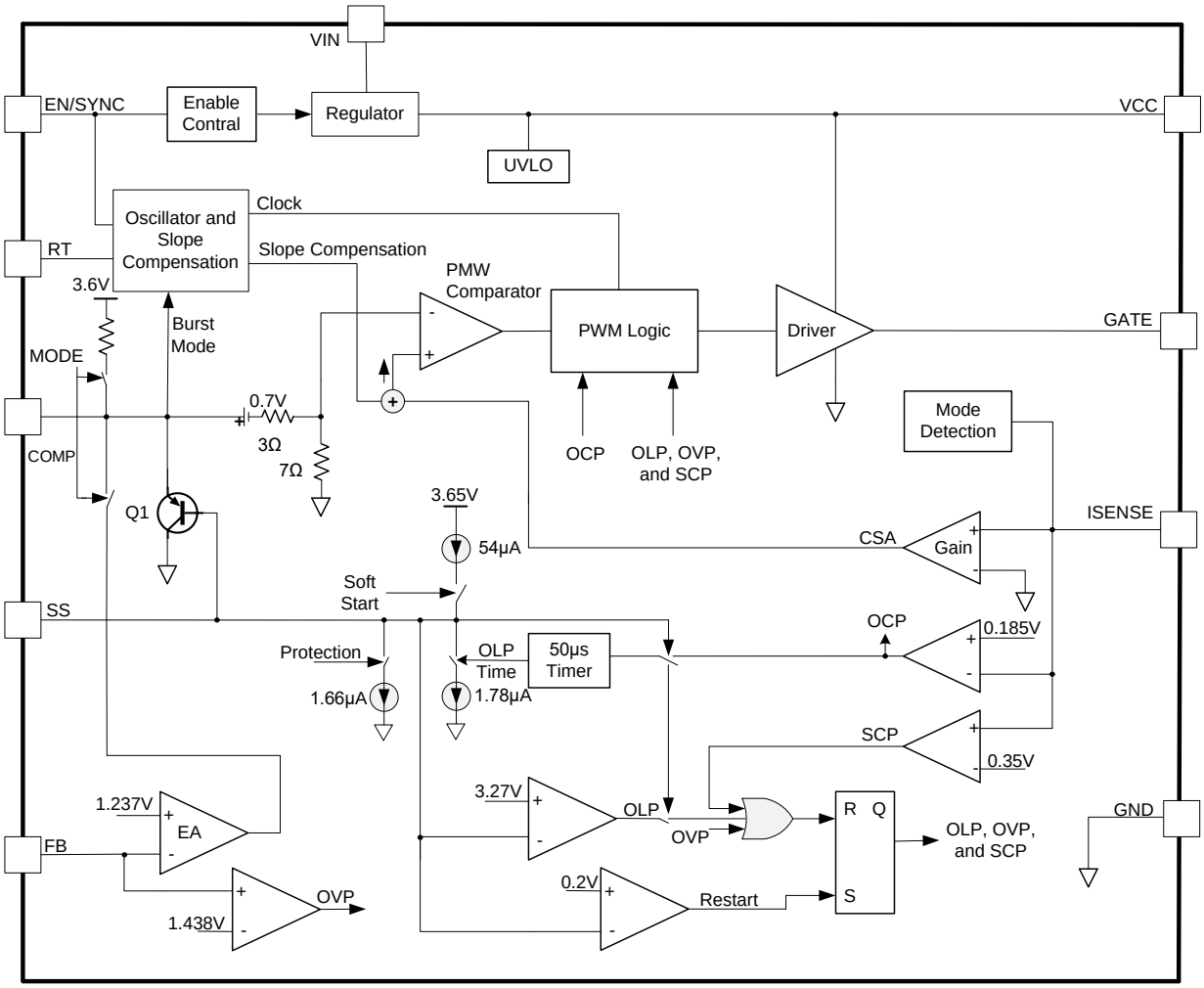


Figure 1: Functional Block Diagram

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OPERATION

The MPQ3910A uses a configurable frequency, peak current mode architecture to regulate the feedback voltage.

Pulse-Width Modulation (PWM)

At the beginning of each cycle, the external N-channel MOSFET turns on, forcing the current in the inductor to increase. The current through the MOSFET is sensed, and when the summed voltage from the amplified ISENSE signal and the slope signal rises above the voltage set by COMP (V_{COMP}), the external MOSFET turns off. The inductor current then flows to the output capacitor through a Schottky diode.

The inductor current is controlled by V_{COMP}, which is controlled by the output voltage. Therefore, the output voltage controls the inductor current to satisfy the load. This current mode architecture improves transient response and control loop stability for over-voltage protection (OVP).

Pulse-Skip Mode (PSM)

Under light-load conditions, the MPQ3910A enters pulse-skip mode (PSM) to improve light-load efficiency. PSM is based on V_{COMP}. If V_{COMP} is below the internal sleep threshold (typically 0.95V), a pause command is generated to block the turn-on clock pulse. The power MOSFET turns off immediately to save gate driving and switching losses.

The pause command also puts the entire chip into sleep mode. In sleep mode, the chip consumes very low quiescent current to further improve light-load efficiency. The gate driver output remains low until V_{COMP} exceeds the sleep threshold. Then the pause signal is reset, and the chip resumes normal PWM operation.

Internal VCC Regulator

The MPQ3910A operates from a 7V to 35V supply voltage. An internal regulator is applied to regulate the power at VCC to supply the internal circuitry of the controller, including the gate driver. The regulator has a nominal output voltage of 12V at VCC, and must be bypassed with a minimum 1µF capacitor.

When the enable pin (EN/SYNC) is high, the capacitor at VCC is charged through VIN. VCC has its own under-voltage lockout (UVLO) protection. Its UVLO rising threshold is 4.17V with a hysteresis of 350mV. When the voltage at VCC crosses the VCC UVLO threshold, the controller is enabled, and all of the internal circuitry is powered by the VCC source. If V_{IN} is sufficiently high as the capacitor charges, V_{CC} increases until it reaches the 12V regulated voltage.

When the input voltage is below 12V, V_{CC} is below V_{IN} (as well as 12V) due to an LDO drop. For normal start-up, the input voltage should exceed 7V. If VCC and VIN are connected, the MPQ3910A can start up from 5V, but the maximum input voltage should not exceed 13V. V_{CC} cannot exceed V_{IN} if both VIN and VCC are powered by an external source, since there is one diode connected from VCC to VIN.

Feedback Loop Setting

To operate in isolated and non-isolated applications, the MPQ3910A can feedback the output signal through either the FB pin or COMP pin by changing settings on the ISENSE pin. For non-isolated applications (e.g. boost mode), the MPQ3910A integrates one error amplifier that can amplify the output error signal from the FB pin. The COMP pin must have an RC network for compensation.

For isolated applications (e.g. flyback mode), the feedback signal from the optocoupler can be amplified by the secondary circuitry. Directly connecting the signal to the COMP pin simplifies loop compensation by eliminating the primary-side amplifier. The different feedback loops can be set via different ISENSE pin connections.

When the device is first enabled, the ISENSE pin outputs a current pulse (typically 50µA) for about 50µs (see Figure 2). If the reflected voltage on the ISENSE pin exceeds 185mV, the feedback signal can be directly connected to the COMP pin. In this scenario, the MPQ3910A disables the internal error amplifier between the FB and COMP pins, and pulls the COMP pin up to a 3.6V source with a 14.4kΩ resistor.

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If the detected voltage is below 185mV, the MPQ3910A enables the internal error amplifier but turns the pull-up resistor off. In this scenario, the COMP pin is just one output pin for the error amplifier, and the feedback signal should be connected to the FB pin.

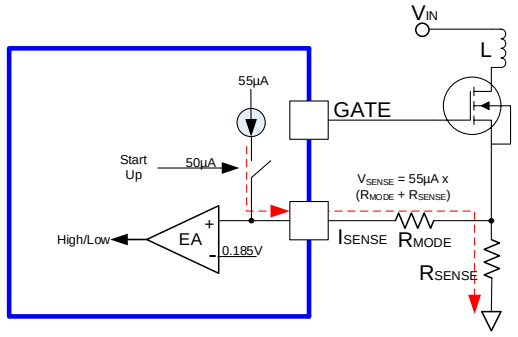


Figure 2: Feedback Mode Setting

For feedback mode through the COMP pin, connect a 5kΩ to 10kΩ resistor between the ISENSE pin and current-sense resistor. For feedback mode through the FB pin, directly connect the ISENSE pin to the current-sense resistor.

Soft Start (SS)

The MPQ3910A uses an external capacitor on the SS pin to control how quickly V_{COMP} rises during soft start (SS). When the chip starts up, the capacitor on SS is charged by a 54µA current source at a pace set by the capacitance. When the SS voltage (V_{SS}) is below the external V_{COMP}, SS overrides the COMP signal, so the PWM comparator uses V_{SS} instead of V_{COMP} as the PWM turn-off reference. When V_{SS} exceeds V_{COMP}, COMP regains control, and soft start finishes.

Soft start can reduce voltage stresses and surge currents during start-up, and prevent the converter output voltage from overshooting during start-up. Soft start occurs during the start-up time, as well as during the protection recovery time after overload protection (OLP), short-circuit protection (SCP), and over-voltage protection (OVP). Under normal conditions, the SS voltage is clamped at 3.65V.

Configurable Oscillator

The MPQ3910A's oscillating frequency is set by an external resistor (R_T) connected from RT to ground. R_T can be estimated with Equation (1):

$$R_T = \frac{2.35 \times 10^3}{f_{SW}} \quad (1)$$

Where R_T is in kΩ, and f_{SW} is in kHz.

For noise immunity, the frequency should be set between 30kHz and 400kHz.

Enable/SYNC Control (EN/SYNC)

EN/SYNC is a digital control pin that turns the MPQ3910A on and off. Drive EN/SYNC high to turn the controller on. Drive EN/SYNC low to turn the controller off. An internal 1MΩ resistor connected from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

For external clock synchronization, use a clock with a frequency that exceeds the frequency set by the RT pin, and is also between 80kHz and 400kHz. The internal clock rising edge synchronizes with the external clock rising edge. Select an external clock pulse signal with a low-level width shorter than 10µs. Otherwise, the MPQ3910A may treat this as an EN/SYNC shutdown.

EN/SYNC cannot be connected to a voltage source exceeding 6V. If the voltage source exceeds 6V, connect a pull-up resistor to the EN/SYNC pin. If a pull-up resistor is used, an internal Zener diode clamps the voltage at EN/SYNC. The maximum pull-up current for the internal Zener diode (assuming it is clamped at 6V) should be below 0.4mA. Typically, a 100kΩ pull-up resistor is recommended. The clamp voltage can be set above 6V if the pull-up current is below 0.4mA.

The re-enable time may be 5 seconds due to the soft-start capacitor discharge current (<0.1µA), which requires a longer time to discharge the soft-start voltage.

Current Sense and Over-Current Protection (OCP)

The MPQ3910A is a peak current mode controller. The current through the external MOSFET can be sensed through a sensing resistor placed in series with the source terminal of the MOSFET.

The sensed voltage on the ISENSE pin is amplified and fed to the high-speed current comparator for current-mode control.

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The current comparator takes this sensed voltage (plus the slope compensation) as one of its inputs, and compares the power switch current to the value set by V_{COMP}. When the amplified current signal exceeds the value set by V_{COMP}, the comparator output is low and turns off the power MOSFET.

If the voltage on ISENSE exceeds the current-limit threshold voltage (typically 185mV), the MPQ3910A turns off the GATE output for that cycle. The output stays off until the internal oscillator starts the next cycle and the current is sensed again. The MPQ3910A limits the MOSFET current cycle by cycle.

Overload Protection (OLP)

The peak current is limited cycle by cycle. If the load continues increasing after over-current protection (OCP) is triggered, the output voltage decreases, and the peak current triggers OCP at every cycle. The MPQ3910A sets overload detection by monitoring the ISENSE voltage.

Once the SS voltage is charged to 3.65V after start-up, overload protection (OLP) is enabled. If an OCP signal is detected, the soft-start charging current is disabled, one over-current discharge source is enabled, and the SS voltage drops at rate of 17.8μA. Simultaneously, a 50μs one-shot timer is activated after the OCP condition ends. The 17.8μA discharge source cannot be turned off until the one-shot timer becomes inactive.

If OCP is removed at least 50μs prior to the SS capacitor discharging to 3.27V, the MPQ3910A resumes normal operation, and the SS capacitor is recharged to 3.65V at a rate of 54μA.

If the SS capacitor is discharged to 3.27V, the MPQ3910A registers this as an overload condition and turns off the gate output until the next restart cycle. At the same time, the 17.8μA discharge current is disabled, and the 1.66μA overload discharge source is enabled. After the SS voltage is discharged to 0.2V, the MPQ3910A starts up again with a new soft-start cycle. This is called hiccup mode protection.

OLP detection is disabled after the SS voltage is discharged below 3.27V, and is re-enabled after the SS voltage is recharged to 3.65V. OLP occurs only after the soft start is completed.

Short-Circuit Protection (SCP)

When the output is shorted to ground, the MPQ3910A initiates over-current protection (OCP), and the current is limited cycle by cycle. Then the MPQ3910A may trigger OLP.

However, if the peak current cannot be limited by the 185mV ISENSE voltage at every cycle due to the leading-edge blanking (LEB) time, there may be current runaway, and the transformer may become saturated. If the monitored ISENSE voltage reaches 0.35V, the MPQ3910A turns off the GATE output and enters hiccup mode by discharging the SS capacitor with 1.66μA of current. The MPQ3910A can start up again if the SS voltage is discharged to 0.2V.

If the short circuit condition is removed, the output voltage recovers after the new restart cycle begins.

For boost converters, there is no way to limit the current from the input to the output if the output experiences a short-circuit condition. Use a secondary protection circuit to protect the devices from these conditions.

Over-Voltage Protection (OVP)

For isolated flyback applications, the auxiliary winding voltage's positive plateau is proportional to the output voltage. The MP3910 implements over-voltage protection (OVP) by monitoring the auxiliary winding voltage instead of directly monitoring the output voltage. The auxiliary voltage is monitored through the FB pin via a resistor divider. Once the voltage exceeds the OVP reference voltage, the MPQ3910A turns off the GATE output and discharges the SS voltage with 1.66μA of current until the SS voltage drops below 0.2V. Then the MPQ3910A initiates a new restart cycle.

To avoid a mistrigger due to the oscillation of the leakage inductance and the parasitic capacitance, OVP sampling uses a blanking time (t_{OVPS}) (typically 500ns). For certain oscillation conditions, an external filter must work with the 500ns LEB time.

Apply a DC output voltage to the FB pin to easily detect OVP conditions.

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Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold, the entire chip shuts down. When the temperature drops below its lower threshold, thermal shutdown is completed, and the chip is enabled again with a new start cycle.

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APPLICATION INFORMATION

The MPQ3910A can be used for boost topologies. For the typical external component selection for the boost converter, see Figure 3 on page 19.

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. If using 10kΩ for the low-side resistor (R_{FBL}) of the voltage divider, calculate the value for the high-side resistor (R_{FBH}) with Equation (2):

$$R_{FBH} = \frac{R_{FBL} \times (V_{OUT} - V_{REF})}{V_{REF}} \quad (2)$$

Where V_{OUT} is the output voltage. If R_{FBL} = 10kΩ, V_{OUT} = 24V, and V_{REF} = 1.237V, then R_{FBH} = 182kΩ.

Selecting the Soft-Start Capacitor

The MPQ3910A ramps the external capacitor voltage on SS to V_{COMP}, which determines the inductor peak current. The SS voltage can be calculated with Equation (3):

$$V_{SS} = \frac{54\mu A}{C_{ss}} \times t_{ss} \quad (3)$$

If overload protection (OLP), short-circuit protection (SCP), or over-voltage protection (OVP) occur, soft start acts as a timer. Once a protection occurs, the 1.66μA current discharges the SS capacitor for hiccup protection.

Selecting the Input Capacitor

An input capacitor is required to supply AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to reduce the noise. Ceramic capacitors are recommended, but tantalum or low-ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a small, high-quality, ceramic capacitor (typically 0.1μF) should be added close to the IC. The capacitance for the boost input can be calculated with Equation (4):

$$C_{IN} \approx \frac{\Delta I}{8 \times \Delta V_{IN} \times f_{SW}} \quad (4)$$

Where ΔI is the peak-to-peak inductor ripple current, and ΔV_{IN} is the input voltage ripple.

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For the best results, use low-ESR capacitors to minimize the output voltage ripple. The output capacitor's characteristics also affect system stability. For the best results, use ceramic, tantalum, or low-ESR electrolytic capacitors.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, so the output voltage ripple is mostly independent of the ESR. The output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} \approx I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} \quad (5)$$

Where ΔV_{OUT} is the output ripple voltage, V_{IN} is the DC input voltage, V_{OUT} is the DC output voltage, I_{LOAD} is the load current, f_{SW} is the switching frequency, and C_{OUT} is the value of the output capacitor.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be estimated with Equation (6):

$$\Delta V_{OUT} \approx I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times f_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (6)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors. Choose an output capacitor that satisfies the design's output ripple and load transient requirements.

Selecting the Inductor and Current-Sense Resistor

An inductor is required to transfer energy between the input source and the output capacitors. A larger-value inductor results in less ripple current and a lower peak inductor current, therefore reducing the stress on the power MOSFET. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

A good rule is to allow the peak-to-peak ripple current to be approximately 30% to 50% of the maximum input current.

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Ensure that the peak inductor current is below 80% of the IC's maximum current limit at the operating duty cycle to prevent regulation loss. Ensure that the inductor does not saturate under the worst-case load transient and start-up conditions. The required inductance value can be calculated with Equation (7), Equation (8), and Equation (9):

$$L \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I} \quad (7)$$

I_{IN} can be estimated with Equation (8):

$$I_{IN} = \frac{V_{OUT} \times I_{LOAD}}{V_{IN} \times \eta} \quad (8)$$

Where I_{LOAD} is the load current, ΔI is the peak-to-peak inductor ripple current, and η is the efficiency. ΔI can be calculated with Equation (9):

$$\Delta I = (30\% - 50\%) \times I_{IN} \quad (9)$$

For a typical design, the boost converter efficiency can reach 85% to 95%.

The switch current is typically used for peak current mode control. To avoid reaching the current limit, the voltage across the sensing resistor (R_{SENSE}) should be below 80% of the worst-case current limit voltage (about 185mV). Calculate R_{SENSE} with Equation (10):

$$R_{SENSE} = \frac{0.8 \times 0.185}{I_{L(PEAK)}} \quad (10)$$

Where $I_{L(PEAK)}$ is the peak value of the inductor current.

Selecting the Power MOSFET

The MPQ3910A can drive a wide variety of N-channel power MOSFETS. The critical parameters of selecting a MOSFET are listed below:

1. Maximum drain-to-source voltage ($V_{DS(MAX)}$)
2. Maximum current ($I_{D(MAX)}$)
3. On-resistance ($R_{DS(ON)}$)
4. Gate source charge (Q_{GS}) and gate drain charge (Q_{GD})
5. Total gate charge (Q_G)
6. Turn-on threshold (V_{TH})

Ideally, the off state voltage across the MOSFET is equal to the boost output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times the output voltage.

The maximum current through the power MOSFET occurs when the input voltage is at its minimum and the output power is at its maximum. The maximum RMS current through the MOSFET can be calculated with Equation (11):

$$I_{RMS} = I_{IN} \times \sqrt{\frac{V_{OUT} - V_{IN}}{V_{OUT}}} \quad (11)$$

The current rating of the MOSFET should be greater than 1.5 times I_{RMS}.

The MOSFET on resistance determines the conduction loss, which can be estimated with Equation (12):

$$P_{LOSS} = I_{RMS}^2 \times R_{DS(ON)} \times K \quad (12)$$

Where K is the on resistance temperature coefficient of the MOSFET. A smaller-value K is recommended.

The switching loss is related to Q_{GD} and Q_{GS1}, which determines the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate (for more details, refer to the V_{GS} vs. Q_G curve in the MOSFET's datasheet). Q_{GD} is the charge during the plateau voltage. These two parameters are used to estimate the turn-on and turn-off loss. Calculate P_{SW} with Equation (13):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW} \quad (13)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, R_G is the gate resistance, and V_{DS} is the drain-source voltage. Note that switching loss is the least accurate loss to estimate, and Equation (13) provides a simple physical expression.

A small Q_G causes a fast turn-on/off speed, which determines the spike and kick.

The turn-on threshold voltage (V_{TH}) is also important. GATE is powered by V_{CC}, so V_{TH} must be below V_{CC}. Under the worst-case conditions, V_{CC} reaches its falling under-voltage lockout (UVLO) threshold (about 3.55V), so the

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MOSFET's V_{TH} should be below this voltage to achieve sufficient driving capability.

Selecting the Diode

The boost output rectifier diode supplies current to the inductor when the MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage greater than the expected output voltage. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current.

Boost Converter Compensation Design

The output of the transconductance error amplifier (COMP) is used to compensate for the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are f_{P1} (which is set by the output capacitor (C_{OUT}) and load resistance) and f_{P2} (which starts from the origin). The zero (f_{Z1}) is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). f_{P1} can be calculated with Equation (14):

$$f_{P1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} \quad (14)$$

Where R_{LOAD} is the load resistance. f_{Z1} can be estimated with Equation (15):

$$f_{Z1} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}} \quad (15)$$

The DC mid-band loop gain can be calculated with Equation (16):

$$A_{VDC} = \frac{0.5 \times G_{EA} \times V_{IN} \times R_{LOAD} \times V_{REF} \times R_{COMP}}{V_{OUT}^2 \times R_{SENSE} \times G_{SENSE}} \quad (16)$$

Where V_{REF} is the reference voltage (about 1.237V), G_{SENSE} is the current-sense amplifier gain, and G_{EA} is the error amplifier transconductance.

The ESR zero in this example only exists at high frequencies, so it is not taken into design consideration.

There is also a right-half-plane zero (f_{RHPZ}) that exists in continuous conduction mode (the inductor current does not drop to 0A at each cycle) step-up converters. The frequency of the right half-plane zero can be calculated with Equation (17):

$$f_{RHPZ} = \frac{V_{IN}^2 \times R_{LOAD}}{2 \times \pi \times L \times V_{OUT}^2} \quad (17)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase margin and gain margin. The worst-case condition occurs when the input voltage is at its minimum and the output power is at its maximum.

To achieve system stability, f_{Z1} is placed close to f_{P1} to cancel the pole. R_{COMP} is adjusted to change the voltage gain. Ensure that the bandwidth (f_C) is about 1/10 of the lower value of the ESR zero. The right-half-plane zero can be calculated with Equation (18):

$$\frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}} \quad (18)$$

Where R_{COMP} can be estimated with Equation (19):

$$R_{COMP} = \frac{V_{OUT}^2 \times 2 \times \pi \times C_{OUT} \times f_C \times R_{SENSE} \times G_{SENSE}}{G_{EA} \times V_{REF} \times V_{IN}} \quad (19)$$

Based on these equations, R_{COMP} and C_{COMP} can be calculated.

In cases where the ESR zero is in a relatively low-frequency region and results in insufficient gain margin, an optional capacitor (C_{POLE}) should be added between COMP and GND. Then a pole formed by C_{POLE} and R_{COMP} should be placed at the ESR zero to cancel the adverse effect. Calculate C_{POLE} with Equation (20):

$$C_{POLE} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{ESRZ}} \quad (20)$$

Design Example

Table 1 shows a design example following the application guidelines for the specifications below.

Table 1: Boost Design Example

V_{IN}	10V to 20V
V_{OUT}	24V
f_{SW}	300kHz

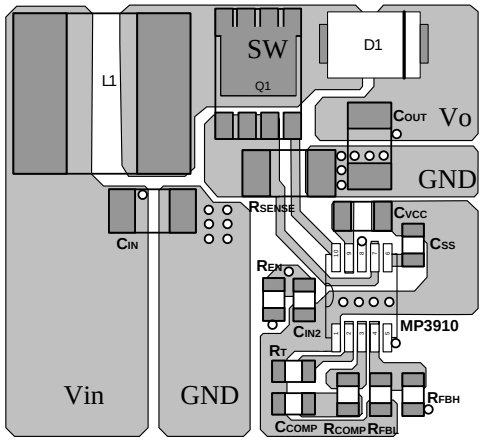
Figure 4 on page 20 shows the detailed application schematic.

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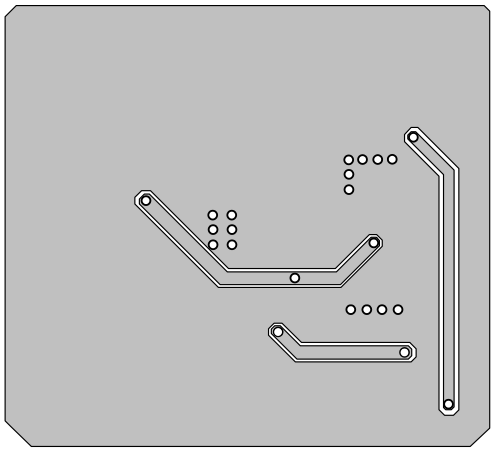
PCB Layout Guidelines

High-frequency switching regulators require very careful layout considerations for stable operation and low noise. For the best results, refer to Figure 3, and follow the guidelines below:

1. Keep the high-current path between the MOSFET drain, output diode, output capacitor, and current-sense resistor as short as possible for minimal noise and ringing.
2. Place the VCC capacitor close to VCC for the best decoupling.
3. Keep all feedback components close to FB to prevent noise injection on the FB trace.
4. Tie the ground return of the input and output capacitors to GND with a single-point connection.



Top Layer



Bottom Layer

Figure 3: Recommended Boost PCB Layout

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TYPICAL APPLICATION CIRCUITS

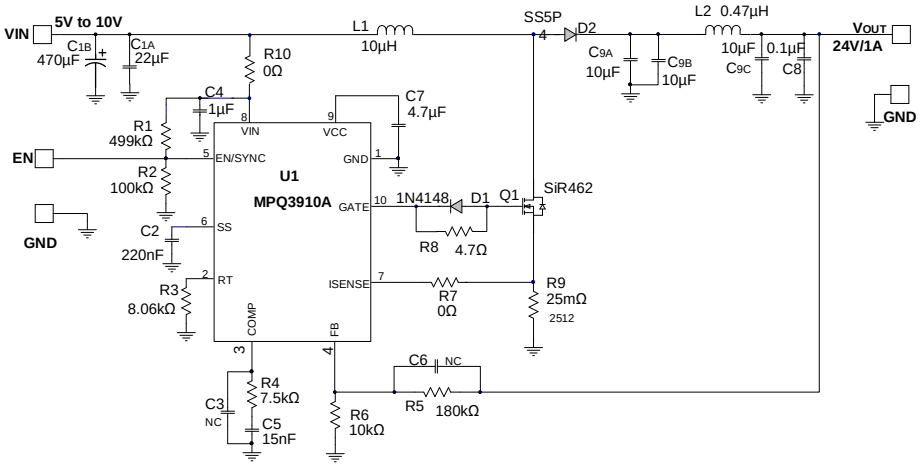


Figure 4: Typical Boost Converter Application Schematic

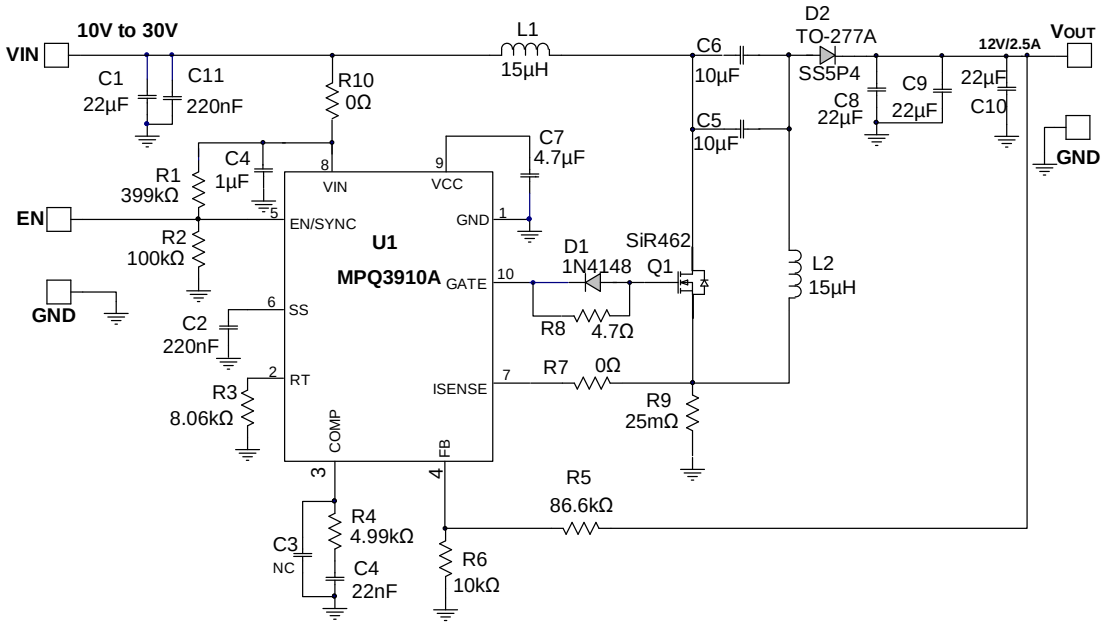


Figure 5: Typical SEPIC Converter Application Schematic

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TYPICAL APPLICATION CIRCUITS *(continued)*

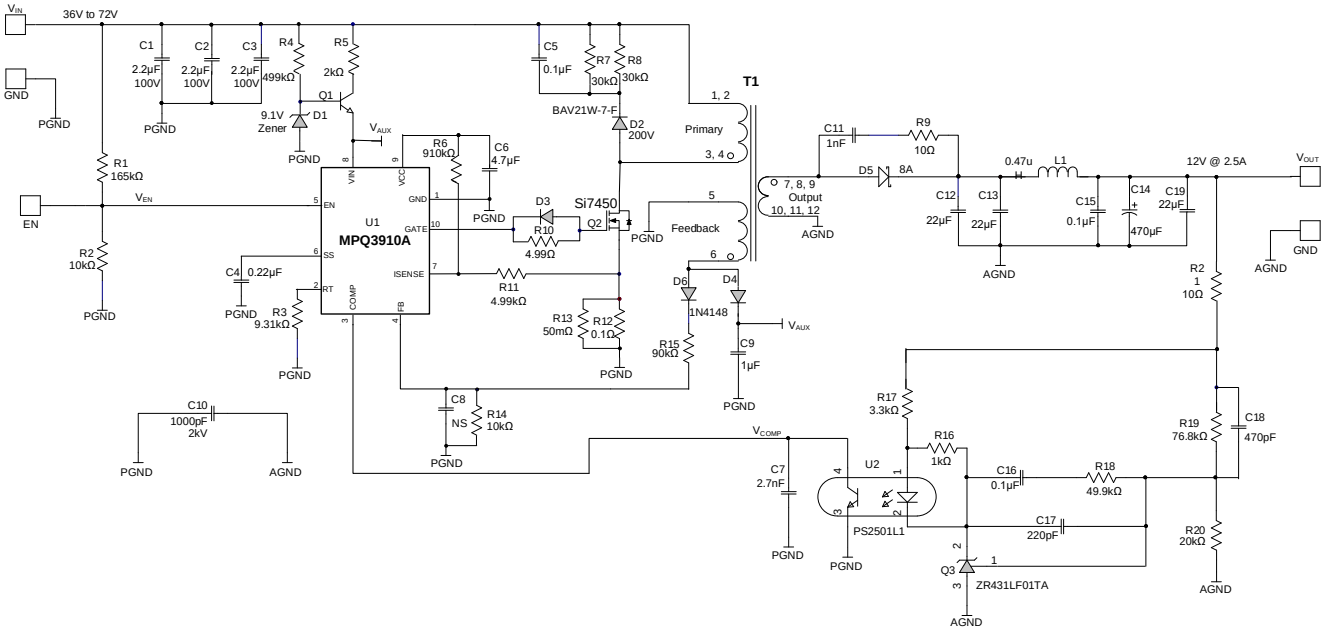


Figure 6: Typical Application Circuit for a Flyback Converter

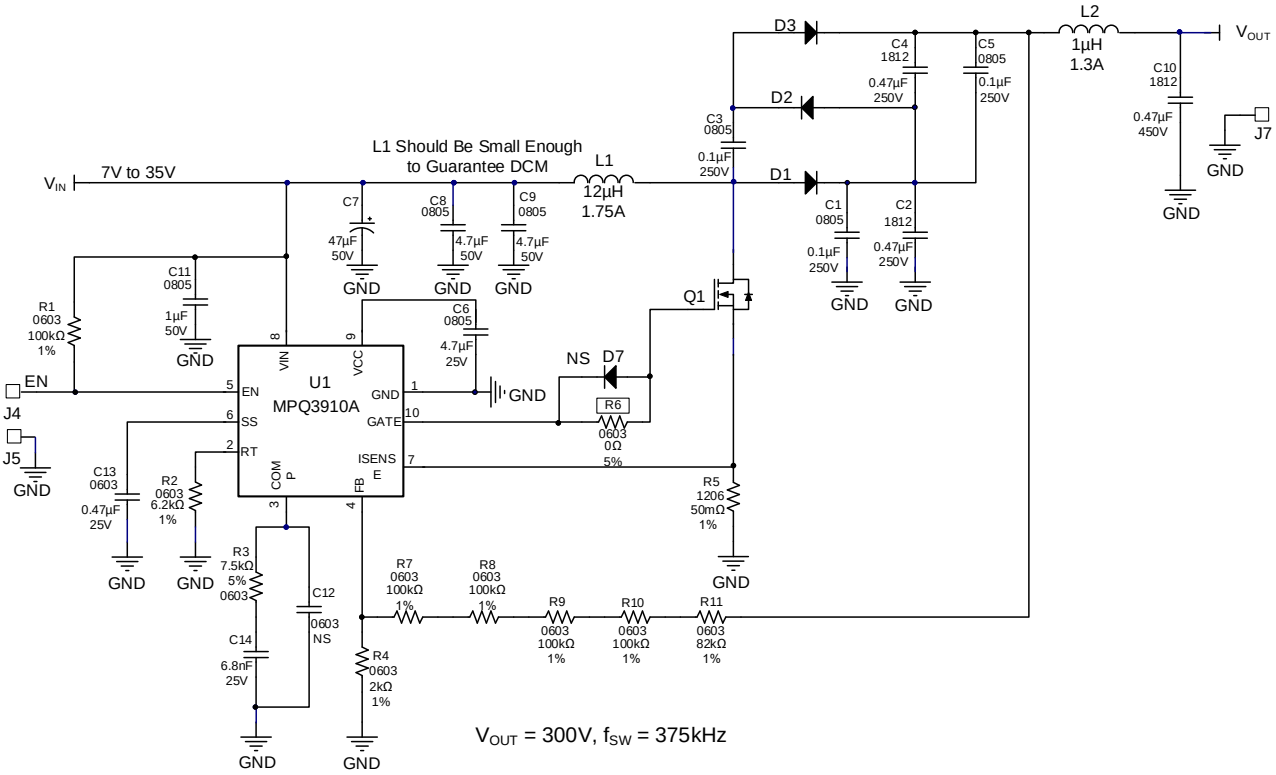


Figure 7: Typical Application Circuit for an H-V Boost Converter

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TYPICAL APPLICATION CIRCUITS *(continued)*

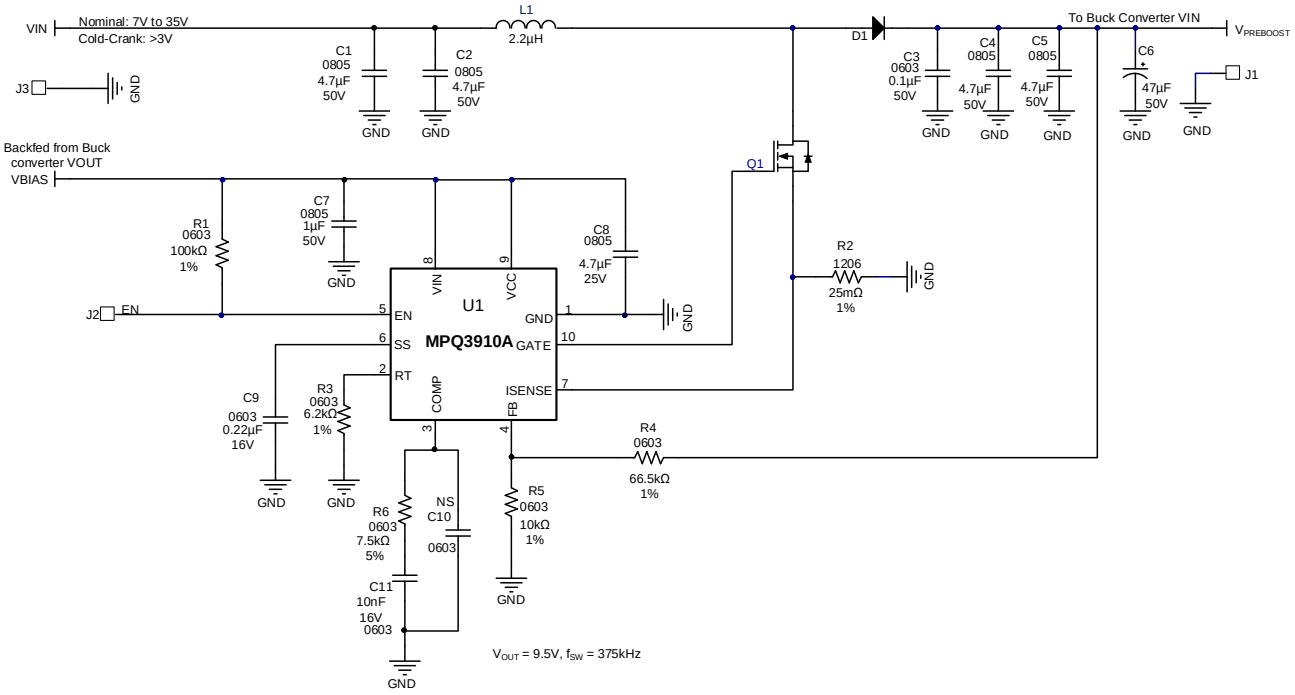
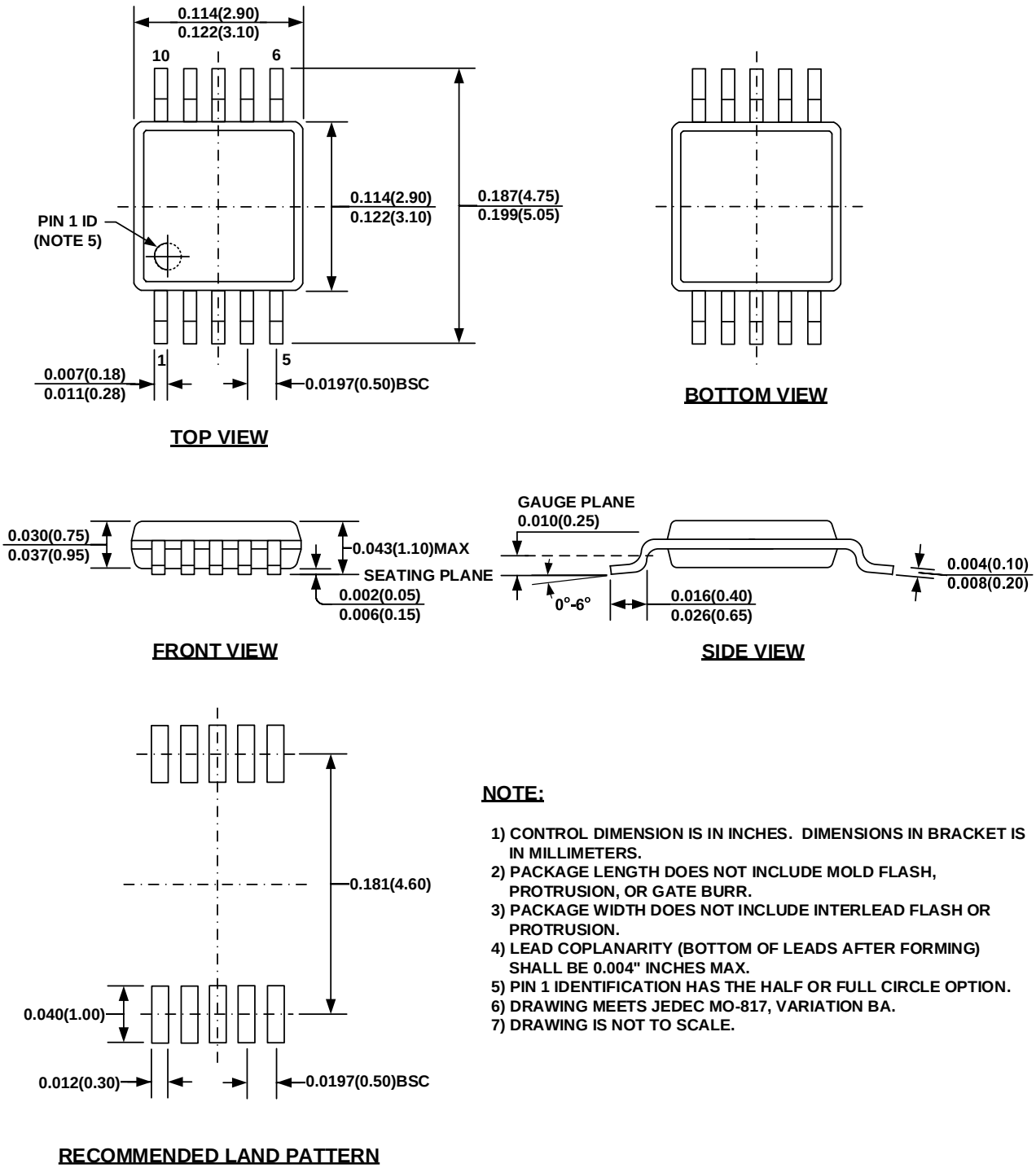


Figure 8: Typical Application Circuit for a Pre-Boost Converter

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PACKAGE INFORMATION

MSOP-10

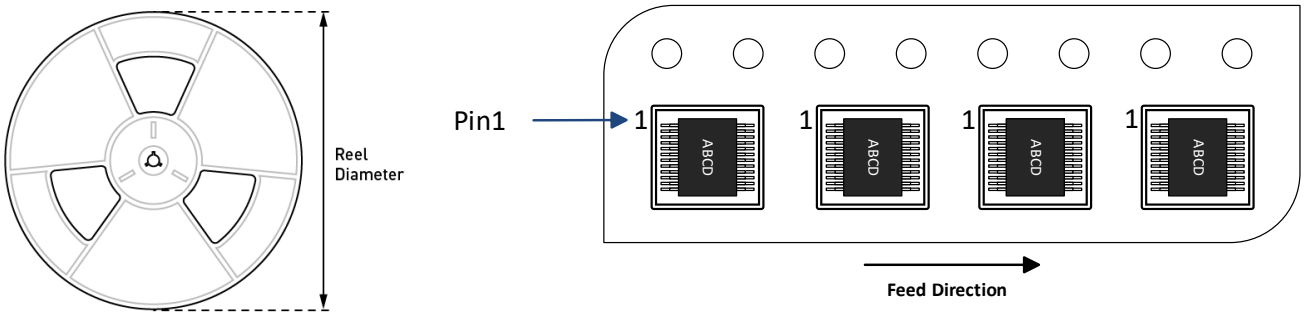


NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSIONS IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3910AGK-AEC1-Z	MSOP-10	2500	50	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	07/20/2021	Initial Release	-
1.1	2/24/2023	Updated formatting	1
		Updated Figure 1	11
		Updated the Over-Voltage Protection (OVP) section	14
		Updated Figure 6 and Figure 7	21
		Updated the Figure 8 title	22

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