NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-3.5-640480EF-MSXP

TFT Liquid Crystal Display

NHD-	Newhaven Display
3.5-	3.5" Diagonal
640480-	640 x 480 Pixels
EF-	Model
M-	MIPI Interface
S-	High Brightness, White LED Backlight
X-	TFT
P-	IPS, Wide Temperature

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REACH Compliant

RoHS Compliant

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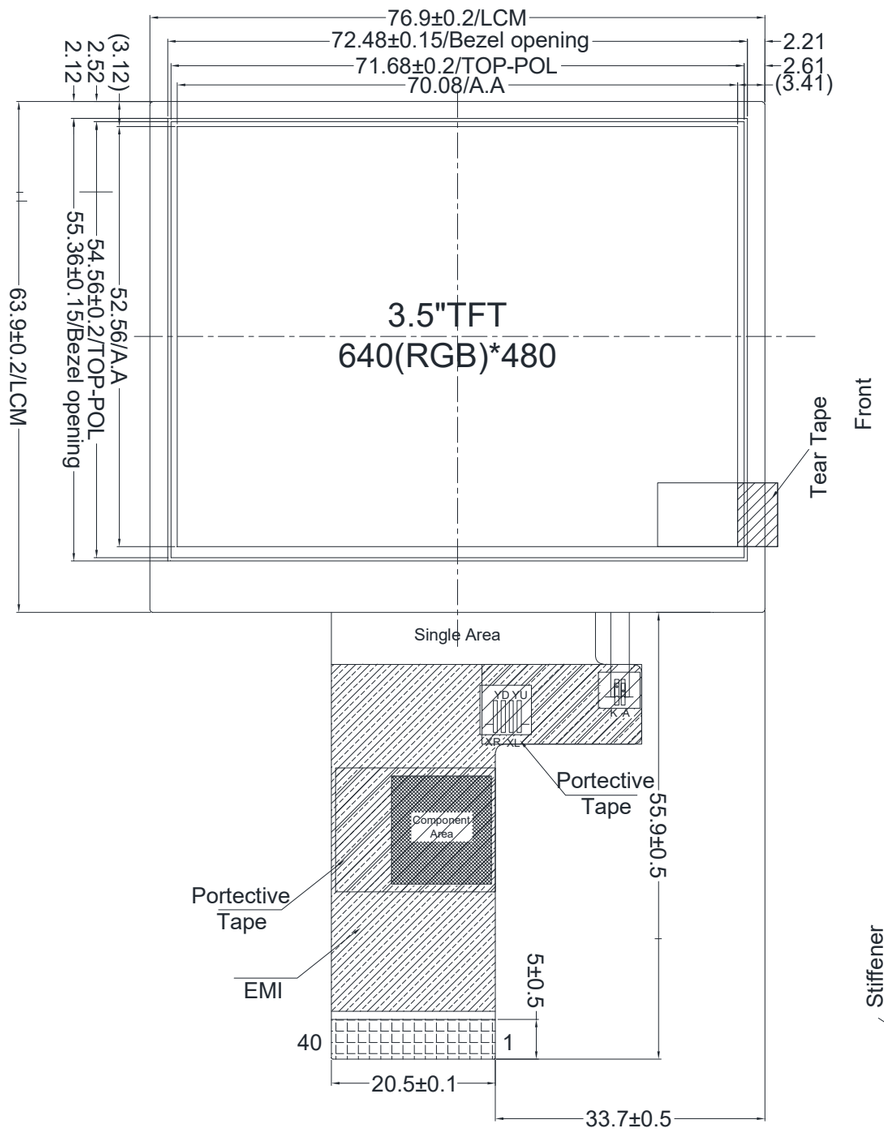
Additional Resources

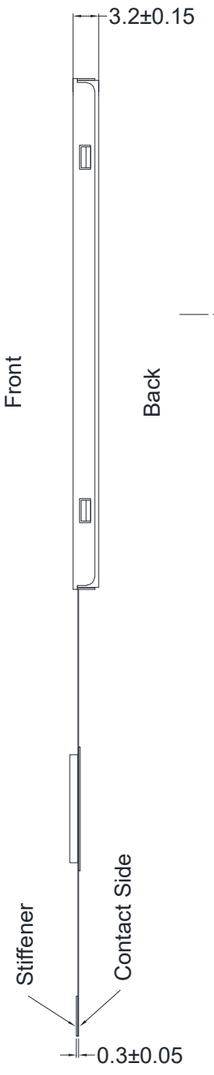
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
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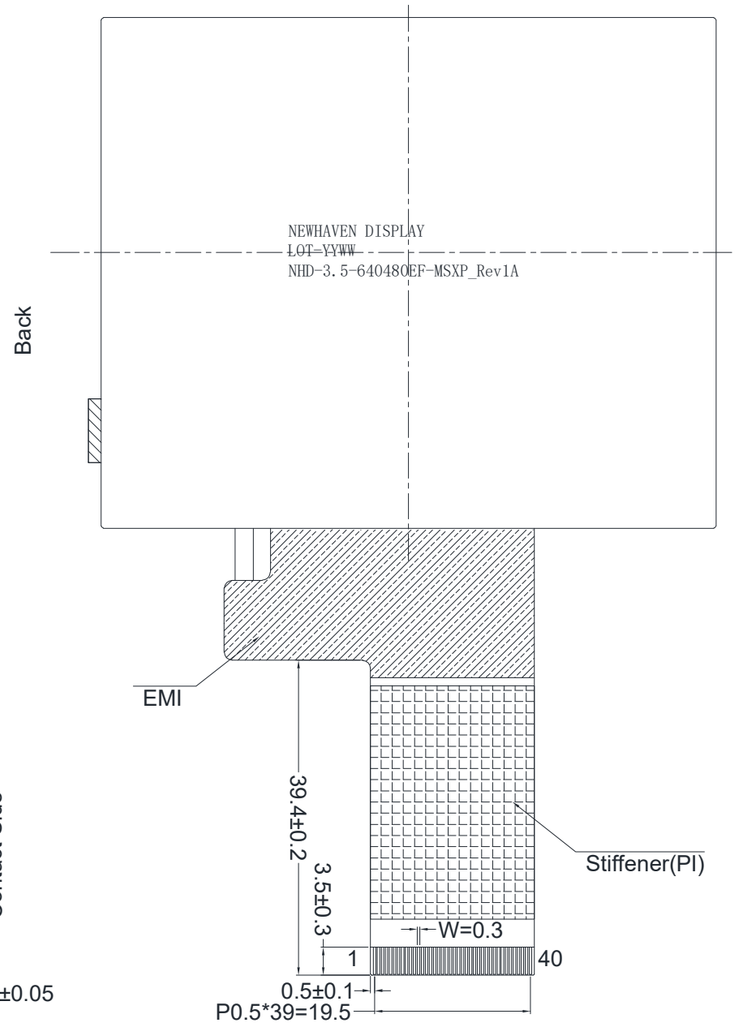
Document Revision History

Revision	Date	Description	Changed By
0	03/10/2022	Initial Release	ZP
1	05/27/2022	Electrical & Optical characteristics updated	ZP
2	06/02/2023	Date Code Format Updated on Mechanical Drawing	KL
3	9/14/2023	Pin Description and Interface Information Updated	KL

Mechanical Drawing



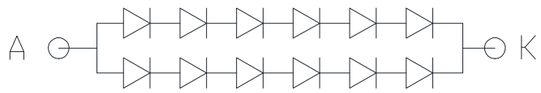




PIN	SYMBOL	PIN	SYMBOL
1	LED_K	21	VSS
2	LED_A	22	DSI_D2P
3	NC	23	DSI_D2N
4	VSS	24	VSS
5	VDD	25	DSI_D3P
6	NC	26	DSI_D3N
7	CSX	27	VSS
8	DCX	28	NC
9	SCL	29	RESX
10	SDA	30	VOUT
11	NC	31	HOUT
12	VSS	32	T_IM
13	DSI_D0P	33	IM1
14	DSI_D0N	34	IM0
15	VSS	35	LANSEL
16	DSI_D1P	36	NC
17	DSI_D1N	37	NC(XR)
18	VSS	38	NC(YD)
19	DSI_CP	39	NC(XL)
20	DSI_CN	40	NC(YU)

Product Description: 3.5” 640x480 IPS TFT

1. Driver IC: FL7703NI
2. Interface: MIPI
3. Power Requirement: 3.0V TFT, 19.2V/40mA Backlight
4. Optical Features: Normally Black, Transmissive, Anti-Glare, 950cd/m²
5. Recommended FFC Connector: 40pin 0.5mm Pitch
6. EMI Shielded FPC



Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-3.5-640480EF-MSXP
Revision: 1A

Unless otherwise specified:
• Dimensions are in Millimeters
• Third Angle Projection

Drawn By: K. Lewis
Approved By: K. Lewis
Drawn Date: 06/02/2023
Approved Date: 06/02/2023

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Pin Description

Pin No.	Symbol	External Connection	Function Description
1	LED_K	Power Supply	Backlight Cathode
2	LED_A	Power Supply	Backlight Anode
3	NC	-	No Connect
4	VSS	Power Supply	Ground
5	VDD	Power Supply	Supply Voltage for LCD and logic
6	NC	-	No Connect
7	CSX	MPU	Active LOW Chip Select signal.
8	DCX	MPU	Command/Data Select. Command: 0/LOW; Data: 1/HIGH
9	SCL	MPU	Serial Clock signal
10	SDA	MPU	Serial Data input/output signal
11	NC	-	No Connect
12	VSS	Power Supply	Ground
13	DSI_D0P	MPU	High Speed Interface Data Differential signal
14	DSI_D0N	MPU	High Speed Interface Data Differential signal
15	VSS	Power Supply	Ground
16	DSI_D1P	MPU	High Speed Interface Data Differential signal
17	DSI_D1N	MPU	High Speed Interface Data Differential signal
18	VSS	Power Supply	Ground
19	DSI_CP	MPU	High Speed Interface Clock Differential signal
20	DSI_CN	MPU	High Speed Interface Clock Differential signal
21	VSS	Power Supply	Ground
22	DSI_D2P	MPU	High Speed Interface Data Differential signal
23	DSI_D2N	MPU	High Speed Interface Data Differential signal
24	VSS	Power Supply	Ground
25	DSI_D3P	MPU	High Speed Interface Data Differential signal
26	DSI_D3N	MPU	High Speed Interface Data Differential signal
27	VSS	Power Supply	Ground
28	NC	-	No Connect
29	RESX	MPU	Active LOW Reset signal
30	VOUT	MPU	Vertical Frame Synchronization output signal
31	HOUT	MPU	Horizontal Frame Synchronization output signal
32	T_IM	MPU	Test Mode Enable signal
33	IM1	MPU	Polarity and Data Lane swap signal
34	IM0	MPU	Polarity and Data Lane swap signal
35	LANSEL	MPU	Polarity and Data Lane swap signal
36-40	NC	-	No Connect

Recommended LCD connector: 0.5mm pitch 40-Conductor FFC.

Backlight connector: on LCD connector

Interface Selection

T_IM signal can be used to select between MIPI interface (normal mode) or serial interface (test mode).

T_IM	Interface mode
0	MIPI Interface
1	DPI/DBI type-C Option 1 (9-bit SPI)

The serial interface is used to communicate between the MPU and the LCD driver chip. It uses CSX (chip select), DCX (data/command select), SCL (serial clock), SDA (serial data input/output). Serial clock (SCL) can be stopped when no communication is necessary. CSX, DCX, SCL and SDA signals should be No Connect when test mode is disabled.

IM1, I**M0** and **LANSEL** are used for the combination of polarity swap and data lane swap of MIPI DSI.

IM1	IM0	LANSEL	D0P/N	D1P/N	CP/N	D2P/N	D3P/N
0	0	0	D3P/N	D2P/N	CP/N	D1P/N	D0P/N
0	1	0	D3N/P	D2N/P	CN/P	D1N/P	D0N/P
1	**0**	**0**	**D0P/N**	**D1P/N**	**CP/N**	**D2P/N**	**D3P/N**
1	1	0	D0N/P	D1N/P	CN/P	D2N/P	D3N/P
0	0	1	D2P/N	D1P/N	CP/N	D0P/N	D3P/N
0	1	1	D2N/P	D1N/P	CN/P	D0N/P	D3N/P
1	0	1	D3P/N	D0P/N	CP/N	D1P/N	D2P/N
1	1	1	D3N/P	D0N/P	CN/P	D1N/P	D2N/P

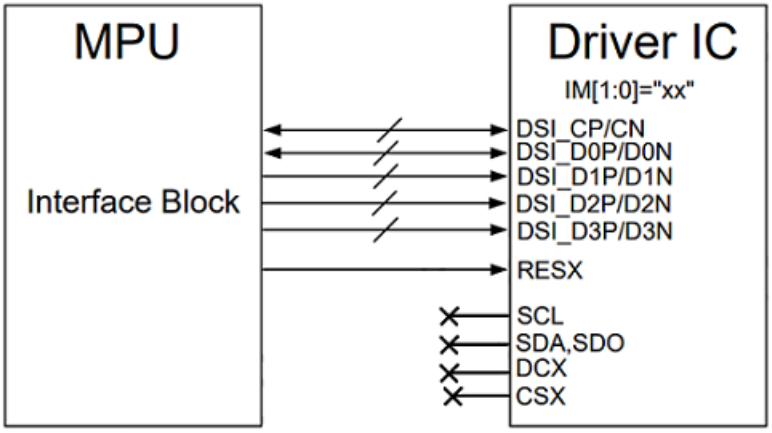
Command **SETMIPI (BAh)** is used to set MIPI related register.

BA H	SETMIPI									
	R/W	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	W	1	0	1	1	1	0	1	0	BA
Parameter 1st	R/W	HOSTTYPE	CD_DLY	x	CRC_Enable	VC_Main[1]	VC_Main[0]	Lane_Number[1]	Lane_Number[0]	33
Parameter 2nd	R/W	DSI_LDO_SEL[2]	DSI_LDO_SEL[1]	DSI_LDO_SEL[0]	LPTX_DR[2]	LPTX_DR[1]	LPTX_DR[0]	RTERM[1]	RTERM[0]	61
Parameter 3rd	R/W	x	x	x	X	IHSRX[3]	IHSRX[2]	IHSRX[1]	IHSRX[0]	06
Parameter 4th	R/W	DSI_HFP_OTP	Txs_Wait[2]	Txs_Wait[1]	Txs_Wait[0]	Tx_clk_sel[1]	Tx_clk_sel[0]	VBP_OSC_EN	VFP_OSC_EN	F9
Parameter 5th	R/W	HFP_OSC[7]	HFP_OSC[6]	HFP_OSC[5]	HFP_OSC[4]	HFP_OSC[3]	HFP_OSC[2]	HFP_OSC[1]	HFP_OSC[0]	FF
Parameter 6th	R/W	HBP_OSC[7]	HBP_OSC[6]	HBP_OSC[5]	HBP_OSC[4]	HBP_OSC[3]	HBP_OSC[2]	HBP_OSC[1]	HBP_OSC[0]	0A

Lane [1:0]: Specify the lane number selection.

Lane [1:0]	MIPI Lane
0	1 lane
1	2 lanes
2	3 lanes
3	4 lanes

Wiring Diagram



Notes:

1. Connect DSI_D3P/N to VSS in 3 data lanes application.
2. Connect DSI_D3P/N and DSI_D2P/N to VSS in 2 data lanes application.

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V_{DD}	-	2.5	3.0	3.3	V
Supply Current	I_{DD}	V_{DD} = 3V	38	50	75	mA
"H" Level input	V_{IH}	-	0.7 * V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	GND	-	0.3 * V_{DD}	V
"H" Level output	V_{OH}	-	0.8 * V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	GND	-	0.2 * V_{DD}	V
Backlight Supply Current	I_{LED}	-	30	40	50	mA
Backlight Supply Voltage	V_{LED}	I_{LED} = 40mA T_{OP} = 25°C	16.8	19.2	20.4	V
Backlight Lifetime*	-		-	30,000	-	Hrs.

*Backlight lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

Optical Characteristics:

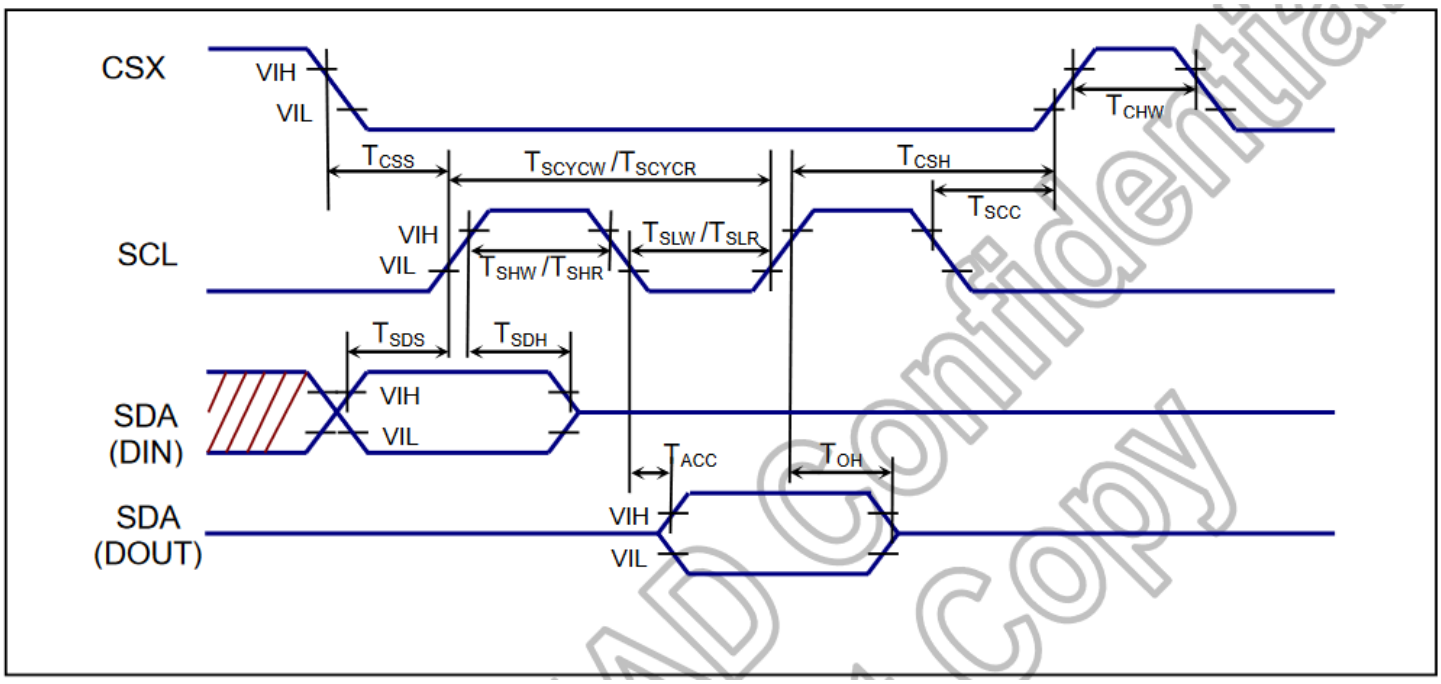
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	φY+	CR ≥ 10	-	85	-	o
	Bottom	φY-		-	85	-	o
	Left	θX-		-	85	-	o
	Right	θX+		-	85	-	o
Contrast Ratio		CR	-	600	800	-	-
Luminance		L_V	I_{LED} = 40 mA	760	950	1425	cd/m^2
Response Time (Rise + Fall)		$T_R + T_F$	T_{OP} = 25°C	-	25	50	ms
Chromaticity	Red	X_R	-	.508	.558	.608	-
		Y_R	-	.273	.323	.373	-
	Green	X_G	-	.245	.295	.345	-
		Y_G	-	.547	.597	.647	-
	Blue	X_B	-	.100	.150	.200	-
		Y_B	-	.027	.077	.127	-
	White	X_W	-	.228	.278	.328	-
		Y_W	-	.284	.334	.360	-

Driver/Controller Information

Built-in FL7703NI Driver: https://support.newhavendisplay.com/hc/en-us/articles/4688762082071-FL7703NI

Timing Characteristics

Serial Interface



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Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	15	-	ns	-
	t_{CSS}	Chip select setup time (Read)	60	-		
	t_{CSH}	Chip select hold time (Write)	15	-		
	t_{CSH}	Chip select hold time (Read)	65	-		
DCX	t_{AST}	Address setup time	0	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-		
SCL (Write)	t_{WC}	Write cycle	66	-	ns	-
	t_{WRH}	Control pulse “H” duration	15	-		
	t_{WRL}	Control pulse “L” duration	15	-		
SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse “H” duration	60	-		
	t_{RDL}	Control pulse “L” duration	60	-		
SDA (Input)	t_{DS}	Data setup time	10	-	ns	For maximum C_L=30pF For minimum C_L=8pF
	t_{DH}	Data hold time	10	-		
SDA (Output)	t_{ACC}	Read access time	-	100	ns	
	t_{OH}	Output disable time	10	-		

DSI Interface

High Speed Mode

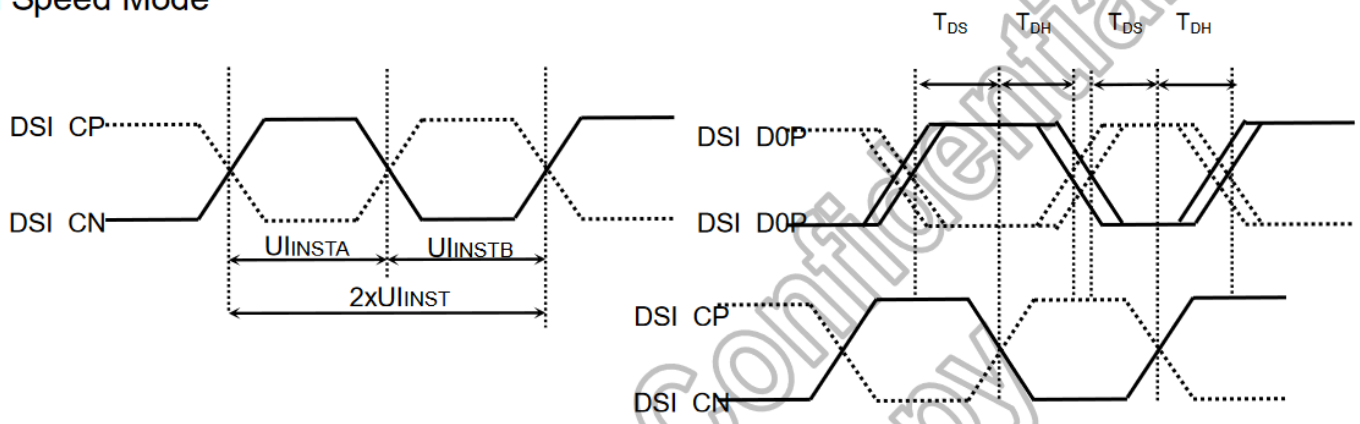


Figure 7-4: DSI clock timing Characteristics

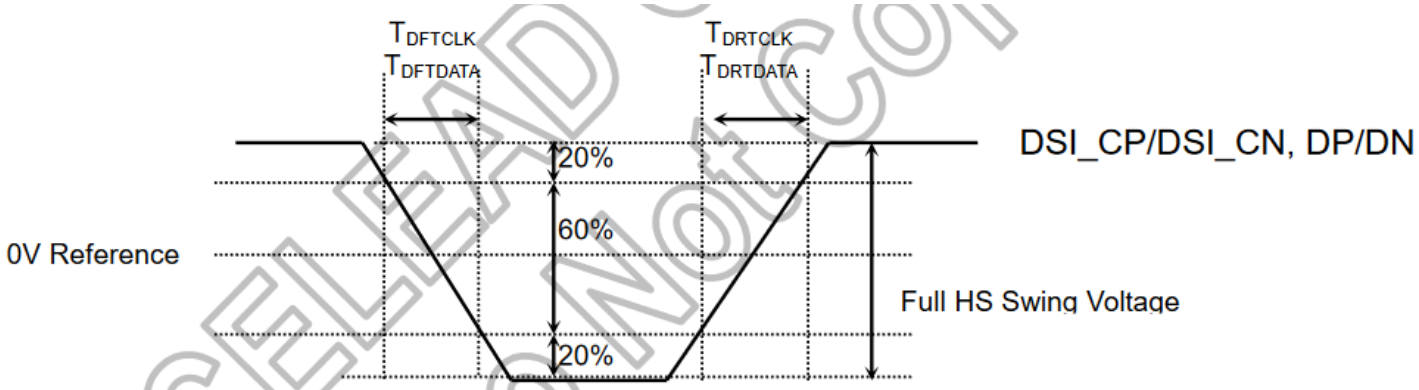


Figure 7-5: Rising and falling time on clock and data channel

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUINST	4LANE：3.30 3LANE：2.85 @ VDDD=1.8V	-	25	ns
	UI instantaneous	UINSTA UINSTB	4LANE：1.67 3LANE：1.43 @ VDDD=1.8V	-	12.5	ns
DP/DN	Data to clock setup time	TDS	0.15xUI	-	-	ps
	Data to clock hold time	TDH	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	TDRTCLK	150	-	0.3UI	ps
	Differential fall time for clock	TDFTCLK	150	-	0.3UI	ps
DP/DN	Differential rise time for data	TDRTDATA	150	-	0.3UI	ps
	Differential fall time for data	TDFTDATA	150	-	0.3UI	ps

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Low Power Mode

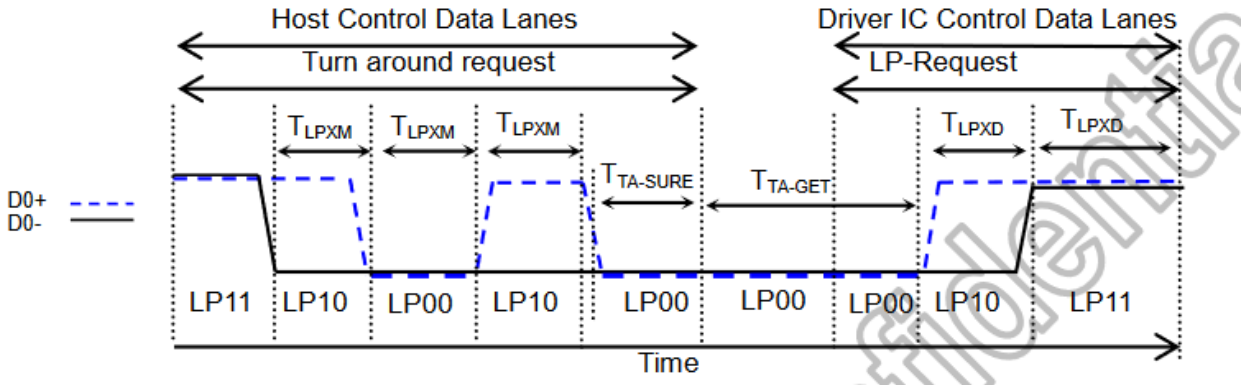


Figure 7-6: BTA from HOST to Display Module Timing

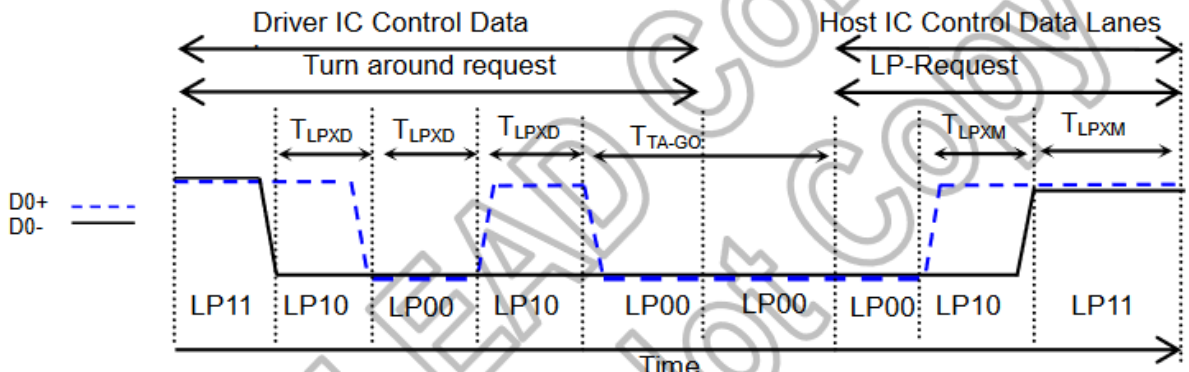
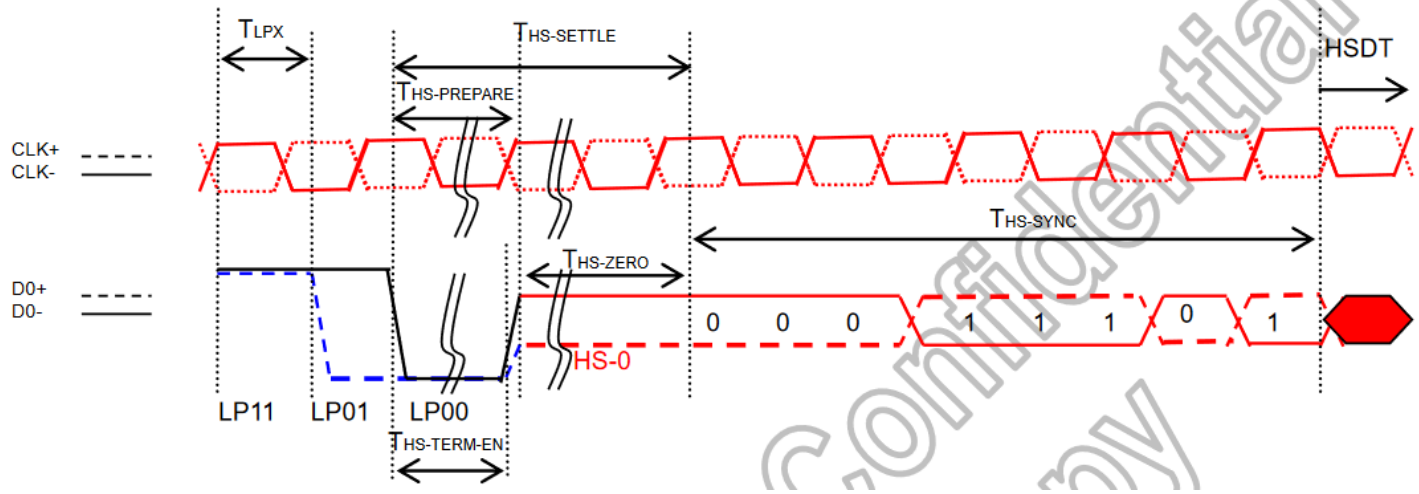


Figure 7-7: BTA from Display Module Timing to HOST

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

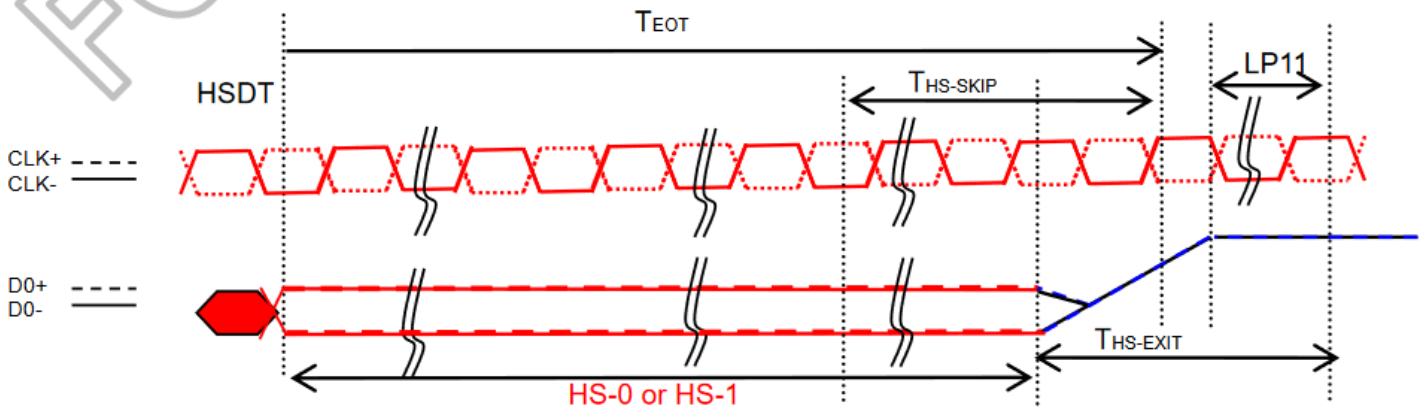
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DSI BURSTS



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

Table 7-5: DSI Low Power Mode to High Speed Mode Timing

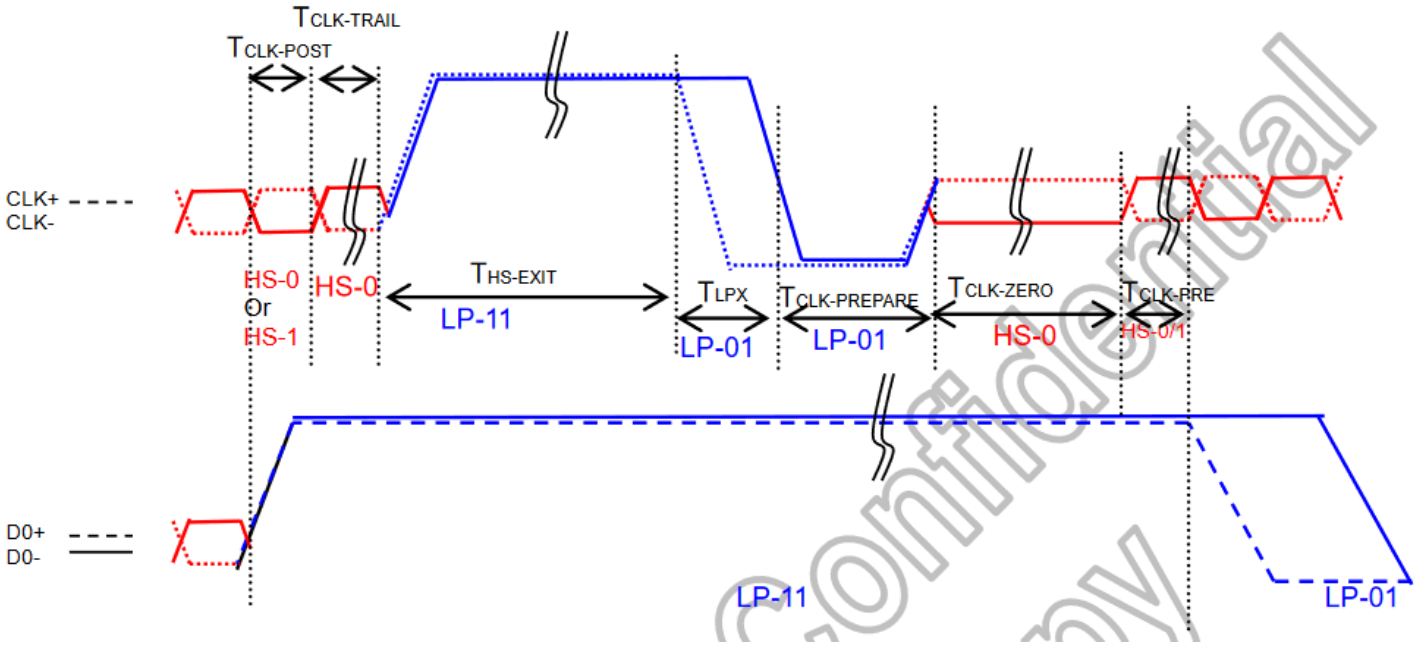


NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

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Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

Table 7-6: DSI Low Power Mode to High Speed Mode Timing

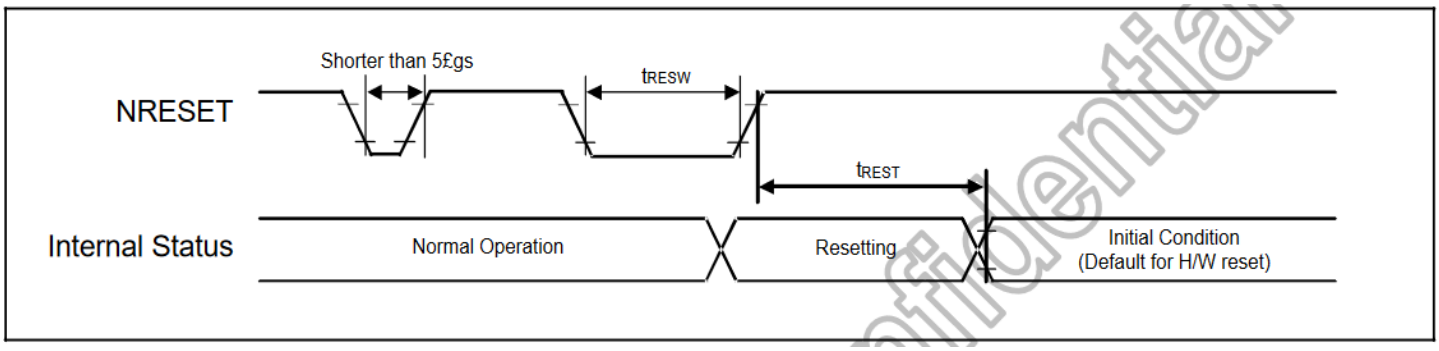


Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Table 7-7: Clock Lanes High Speed Mode to/from Low Power Mode Timing

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Reset Input Timing



Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 96hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 96hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C , 96hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 96hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+50°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C,60min -> 70°C,60min = 1 cycle 20 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-50Hz , 5G Acceleration 60 sec in each of 3 directions (X,Y,Z) For 30 minutes	3
Static electricity test	Endurance test applying electric static discharge.	Air: ±4kV 150pF/330Ω, 5 Times Contact: ±2kV 150pF/330Ω, 5 Times	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.