NCP5214

2-in-1 Notebook DDR Power Controller

The NCP5214 2−in−1 Notebook DDR Power Controller is specifically designed as a total power solution for notebook DDR memory system. This IC combines the efficiency of a PWM controller for the VDDQ supply with the simplicity of linear regulators for the VTT termination voltage and the buffered low noise reference. This IC contains a synchronous PWM buck controller for driving two external NFETs to form the DDR memory supply voltage (VDDQ). The DDR memory termination regulator output voltage (VTT) and the buffered VREF are internally set to track at the half of VDDQ. An internal power good voltage monitor tracks VDDQ output and notifies the user whether the VDDQ output is within target range. Protective features include soft−start circuitries, undervoltage monitoring of supply voltage, VDDQ overcurrent protection, VDDQ overvoltage and undervoltage protections, and thermal shutdown. The IC is packaged in DFN−22.

Features

- Incorporates VDDQ, VTT Regulator, Buffered VREF
- Adjustable VDDQ Output
- VTT and VREF Track VDDQ/2
- Operates from Single 5.0 V Supply
- Supports VDDQ Conversion Rails from 4.5 V to 24 V
- Power−saving Mode for High Efficiency at Light Load
- Integrated Power FETs with VTT Regulator Sourcing/Sinking 1.5 A DC and 2.4 A Peak Current
- Requires Only 20 μF Ceramic Output Capacitor for VTT
- Buffered Low Noise 15 mA VREF Output
- All External Power MOSFETs are N−channel
- <5.0 μA Current Consumption During Shutdown
- Fixed Switching Frequency of 400 kHz
- Soft−start Protection for VDDQ and VTT
- Undervoltage Monitor of Supply Voltage
- Overvoltage Protection and Undervoltage Protection for VDDQ
- Short−circuit Protection for VDDQ and VTT
- Thermal Shutdown
- Housed in DFN−22
- This is a Pb−Free Device

Typical Applications

- Notebook DDR/DDR2 Memory Supply and Termination Voltage
- Active Termination Busses (SSTL−18, SSTL−2, SSTL−3)

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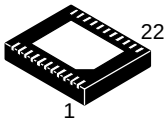
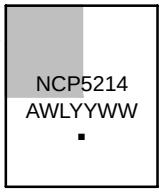
MARKING DIAGRAM

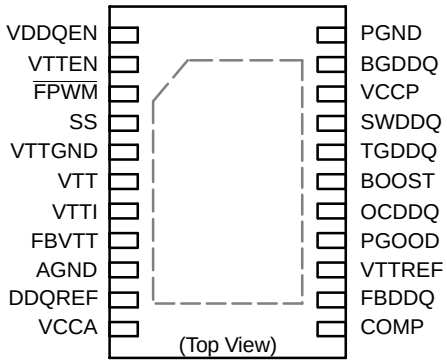


DFN−22
MN SUFFIX
CASE 506AF



NCP5214	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



NOTE: Pin 23 is the thermal pad on the bottom of the device.

ORDERING INFORMATION

Device	Package	Shipping†
NCP5214MNR2G	DFN−22 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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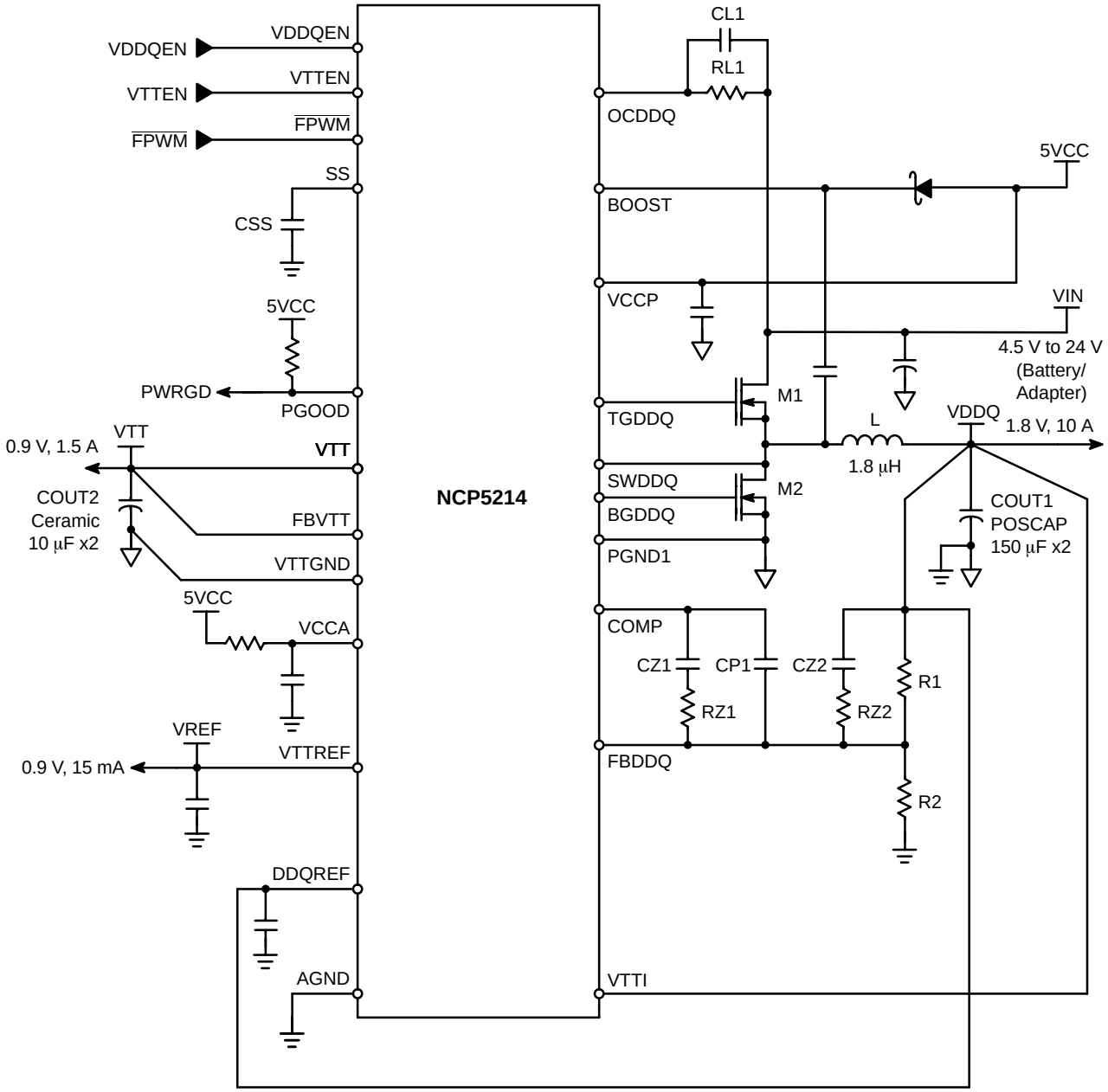


Figure 1. Typical Application Diagram

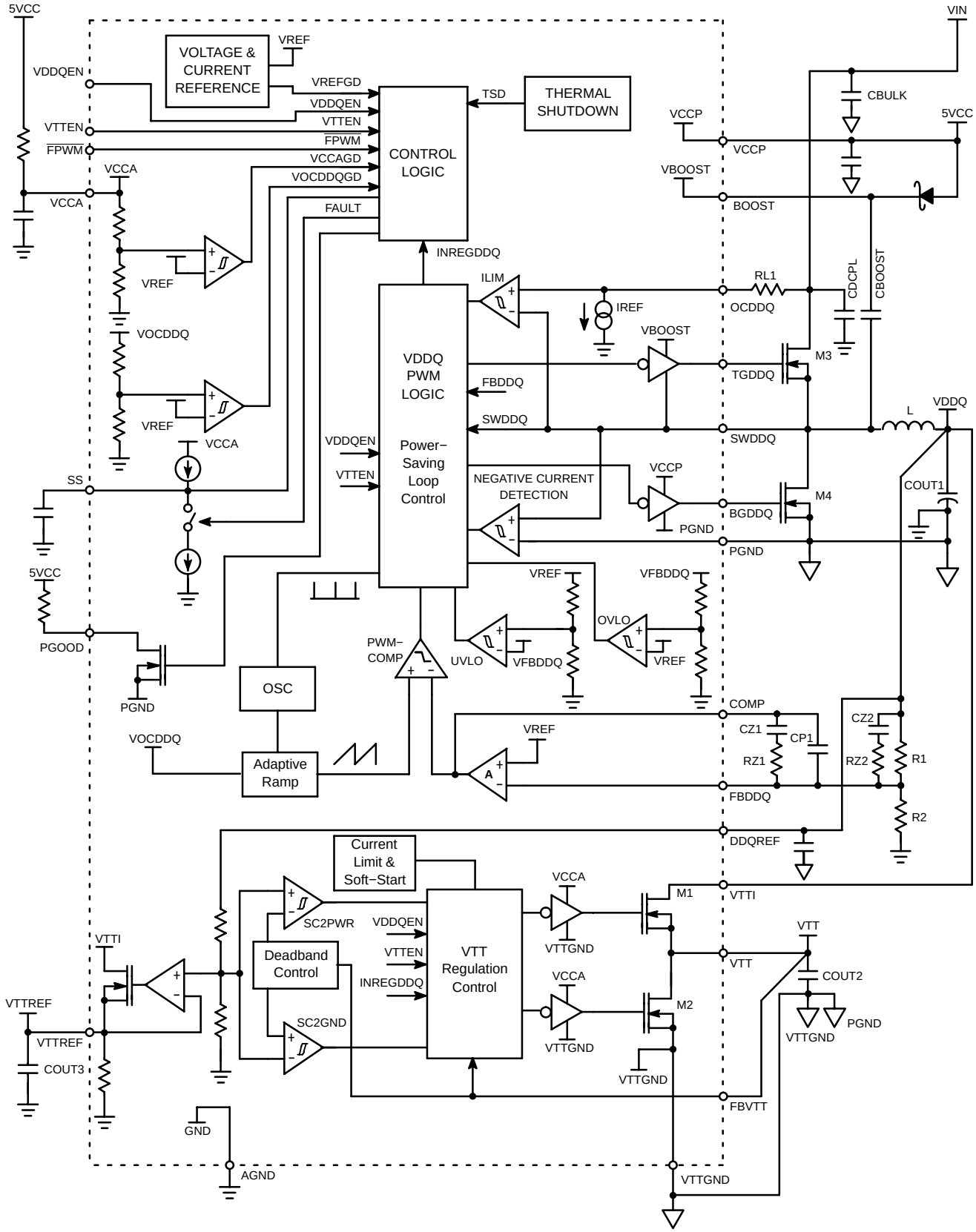


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	VDDQEN	VDDQ regulator enable input. High to enable.
2	VTTEN	VTT regulator enable input. High to enable.
3	$\overline{\text{FPWM}}$	Forced PWM enable input. Low to enable forced PWM mode and disable power−saving mode.
4	SS	VDDQ Soft−start capacitor connection to ground.
5	VTTGND	Power ground for the VTT regulator.
6	VTT	VTT regulator output.
7	VTTI	Power input for VTT regulator which is normally connected to the VDDQ output of the buck regulator.
8	FBVTT	VTT regulator feedback pin for closed loop regulation.
9	AGND	Analog ground connection and remote ground sense.
10	DDQREF	External reference input which is used to regulate VTT and VTTREF to 1/2VDDQREF.
11	VCCA	5.0 V supply input for the IC's control and logic section, which is monitored by undervoltage lock out circuitry.
12	COMP	VDDQ error amplifier compensation node.
13	FBDDQ	VDDQ regulator feedback pin for closed loop regulation.
14	VTTREF	DDR reference voltage output.
15	PGOOD	Power good signal open−drain output.
16	OCDDQ	Overcurrent sense and program input for the high−side FET of VDDQ regulator. Also the battery voltage input for the internal ramp generator to implement the voltage feedforward rejection to the input voltage variation. This pin must be connected to the VIN through a resistor to perform the current limit and voltage feedforward functions.
17	BOOST	Positive supply input for high−side gate driver of VDDQ regulator and boost capacitor connection.
18	TGDDQ	Gate driver output for VDDQ regulator high−side N−Channel power FET.
19	SWDDQ	VDDQ regulator inductor driven node, return for high−side gate driver, and current limit sense input.
20	VCCP	Power supply for the VDDQ regulator low−side gate driver and also supply voltage for the bootstrap capacitor of the VDDQ regulator high−side gate driver supply.
21	BGDDQ	Gate driver output for VDDQ regulator low−side N−Channel power FET.
22	PGND	Power ground for the VDDQ regulator.
23	THPAD	Copper pad on bottom of IC used for heatsinking. This pin should be connected to the ground plane under the IC.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11, 20) to AGND (Pin 9)	V_{CCA}, V_{CCP}	−0.3, 6.0	V
High−Side Gate Drive Supply: BOOST (Pin 17) to SWDDQ (Pin 19) High−Side FET Gate Drive Voltage: TGDDQ (Pin 18) to SWDDQ (Pin 19)	V_{BOOST}−V_{SWDDQ}, V_{TGDDQ}−V_{SWDDQ}	−0.3, 6.0	V
Input/Output Pins to AGND (Pin 9) Pins 1−4, 6−8, 10, 12−15, 21	V_{IO}	−0.3, 6.0	V
Overcurrent Sense Input (Pin 16) to AGND (Pin 9)	V_{OCDDQ}	27	V
Switch Node (Pin 19)	V_{SWDDQ}	−4.0 (<100 ns), 0.3 (dc), 32	V
PGND (Pin 22), VTTGND (Pin 5) to AGND (Pin 9)	V_{GND}	−0.3, 0.3	V
Thermal Characteristics DFN−22 Plastic Package Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	35	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Moisture Sensitivity Level	MSL	2	−

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ≤2.0 kV per JEDEC standard: JESD22–A114 except Pin 17 which is ≤500 V.
   Machine Model (MM) ≤200 V per JEDEC standard: JESD22–A115 except Pin 17 which is ≤50 V.
2. Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78.
3. Pin 16 (OCDDQ) must be pulled high to VIN through a resistor.

ELECTRICAL CHARACTERISTICS (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 5.6 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 10 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY VOLTAGE						
Input Voltage	V_{IN}	−	4.5	−	24	V
V_{CCA} Operating Voltage	V_{CCA}	−	4.5	5.0	5.5	V
V_{CCP} Operating Voltage	V_{CCP}	−	4.5	5.0	5.5	V
SUPPLY CURRENT						
V_{CCA} Quiescent Supply Current in S0	I_{VCCA_S0}	V_{DDQEN} = 5.0 V, V_{TTEN} = 5.0 V	−	3.5	10	mA
V_{CCA} Quiescent Supply Current in S3	I_{VCCA_S3}	V_{DDQEN} = 5.0 V, V_{TTEN} = 0 V	−	0.9	5.0	mA
V_{CCA} Shutdown Current	I_{VCCA_SD}	V_{DDQEN} = 0 V, V_{TTEN} = 0 V, T_A = 25°C	−	1.0	4.0	μA
V_{CCP} Quiescent Supply Current in S0	I_{VCCP_S0}	V_{DDQEN} = 5.0 V, V_{TTEN} = 5.0 V, TGDDQ and BGDDQ Open	−	−	20	mA
V_{CCP} Quiescent Supply Current in S3	I_{VCCP_S3}	V_{DDQEN} = 5.0 V, V_{TTEN} = 0 V, TGDDQ and BGDDQ Open	−	−	20	mA
V_{CCP} Shutdown Current	I_{VCCP_SD}	V_{DDQEN} = 0 V, V_{TTEN} = 0 V	−	1.0	2.0	μA
UNDERVOLTAGE MONITOR						
V_{CCA} UVLO Lower Threshold	V_{CCAUV-}	Falling Edge	−	3.7	4.1	V
V_{CCA} UVLO Hysteresis	$V_{CCAUVHYS}$	−	−	0.35	−	V
V_{OCDDQ} UVLO Upper Threshold	$V_{OCDDQUV+}$	Rising Edge	−	3.0	4.4	V
V_{OCDDQ} UVLO Hysteresis	$V_{OCDDQUVHYS}$	−	−	0.4	−	V
THERMAL SHUTDOWN						
Thermal Trip Point	T_{SD}	(Note 4)	−	150	−	°C
Hysteresis	T_{SDHYS}	(Note 4)	−	25	−	°C
V_{DDQ} SWITCHING REGULATOR						
FBDDQ Feedback Voltage, Control Loop in Regulation	V_{FBDDQ}	T_A = 25°C T_A = −40 to 85°C	0.788 0.784	0.8 0.8	0.812 0.816	V
Feedback Input Current	I_{fb}	V_{FBDDQ} = 0.8 V	−	−	1.0	μA
Oscillator Frequency	F_{SW}	−	340	400	460	kHz
Ramp Amplitude Voltage	V_{ramp}	V_{IN} = 5.0 V (Note 4)	−	1.25	−	V
Ramp Amplitude to V_{IN} Ratio	dVRAMP/dVIN	−	−	45	−	mV/V
OCDDQ Pin Current Sink	I_{OC}	V_{OCDDQ} = 4.0 V	26	31	36	μA
OCDDQ Pin Current Sink Temperature Coefficient	TC_{IOC}	T_A = −40 to 85°C	−	3200	−	ppm/°C
Minimum On Time	t_{onmin}	−	−	150	−	ns
Maximum Duty Cycle	D_{max}	V_{IN} = 5.0 V V_{IN} = 15 V V_{IN} = 24 V	− − −	90 50 32	− − −	%
Soft−Start Current	I_{ss}	V_{DDQEN} = 5.0 V, Vss = 0 V	2.8	4.0	5.2	μA
Overvoltage Trip Threshold	FBOVPth	With Respect to Error Comparator Threshold of 0.8 V	115	130	−	%
Undervoltage Trip Threshold	FBUVPth	With Respect to Error Comparator Threshold of 0.8 V	−	65	75	%

4. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 5.6 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 10 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER						
DC Gain	GAIN	(Note 5)	−	70	−	dB
Unity Gain Bandwidth	Ft	COMP_GND = 220 nF, 1.0 Ω in Series (Note 5)	−	2.0	−	MHz
Slew Rate	SR	(Note 5)	−	3.0	−	V/μS
GATE DRIVERS						
TGDDQ Gate Pull−HIGH Resistance	R_{H_TG}	V_{BOOST} − V_{SWDDQ} = 5.0 V, V_{TGDDQ} − V_{SWDDQ} = 4.0 V	−	1.8	4.0	Ω
TGDDQ Gate Pull−LOW Resistance	R_{L_TG}	V_{BOOST} − V_{SWDDQ} = 5.0 V, V_{TGDDQ} − V_{SWDDQ} = 1.0 V	−	1.8	4.0	Ω
BGDDQ Gate Pull−HIGH Resistance	R_{H_BG}	V_{CCP} = 5.0 V, V_{BGDDQ} = 4.0 V	−	1.8	4.0	Ω
BGDDQ Gate Pull−LOW Resistance	R_{L_BG}	V_{CCP} = 5.0 V, V_{BGDDQ} = 1.0 V	−	0.9	3.0	Ω
V_{TT} ACTIVE TERMINATOR						
V_{TT} with Respect to 1/2V_{DDQREF}	d_{VTT0}	1/2VDDQREF – V_{TT}, VDDQREF = 2.5 V, I_{VTT} = 0 to 2.4 A (Sink Current)	−30	−	−	mV
		I_{VTT} = 0 to –2.4 A (Source Current)	−	−	30	
		1/2VDDQREF – V_{TT}, VDDQREF = 1.8 V, I_{VTT} = 0 to 2.0 A (Sink Current)	−30	−	−	mV
		I_{VTT} = 0 to –2.0 A (Source Current)	−	−	30	
DDQREF Input Resistance	DDQREF_R	VDDQREF = 2.5 V	40	55	75	kΩ
Source Current Limit	$I_{LIMVTsrc}$	−	2.5	3.0	−	A
Sink Current Limit	$I_{LIMVTsnk}$	−	2.5	3.0	−	A
Soft−Start Source Current Limit	$I_{LIMVTSS}$	−	−	1.0	−	A
Maximum Soft−Start Time	$t_{ssvttmax}$	−	−	0.32	−	ms
V_{TTREF} OUTPUT						
V_{TTREF} Source Current	I_{VTTR}	VDDQREF = 1.8 V or 2.5 V	15	−	−	mA
V_{TTREF} Accuracy Referred to 1/2V_{DDQREF}	d_{VTTR}	1/2VDDQREF – V_{TTR}, VDDQREF = 2.5 V, I_{VTTR} = 0 mA to 15 mA	−25	−	25	mV
		1/2VDDQREF – V_{TTR}, VDDQREF = 1.8 V, I_{VTTR} = 0 mA to 15 mA	−18	−	18	mV

5. Guaranteed by design, not tested in production.

ELECTRICAL CHARACTERISTICS (continued) (V_{IN} = 12 V, T_A = −40 to 85°C, V_{CCA} = V_{CCP} = V_{BOOST} − V_{SWDDQ} = 5.0 V, L = 1.8 μH, C_{OUT1} = 150 μF x 2, C_{OUT2} = 22 μF x 2, RL1 = 5.6 kΩ, R1 = 4.3 kΩ, R2 = 3.3 kΩ, RZ1 = 10 kΩ, RZ2 = 130 Ω, CP1 = 100 pF, CZ1 = 2.2 nF, CZ2 = 4.7 nF, for min/max values unless otherwise noted. Typical values are at T_A = 25°C.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
CONTROL SECTION						
VDDQEN Pin Threshold High	V_{DDQEN_H}	−	1.4	−	−	V
VDDQEN Pin Threshold Low	V_{DDQEN_L}	−	−	−	0.5	V
VDDQEN Pin Input Current	I_{IN_VDDQEN}	V_{DDQEN} = 5.0 V	−	−	1.0	μA
VTTEN Pin Threshold High	V_{TTEN_H}	−	1.4	−	−	V
VTTEN Pin Threshold Low	V_{TTEN_L}	−	−	−	0.5	V
VTTEN Pin Input Current	I_{IN_VTTEN}	V_{DDQEN} = V_{TTEN} = 5.0 V	−	−	1.0	μA
$\overline{FPWM}$ Pin Threshold High	$\overline{FPWM}_H$	−	1.4	−	−	V
$\overline{FPWM}$ Pin Threshold Low	$\overline{FPWM}_L$	−	−	−	0.5	V
$\overline{FPWM}$ Pin Input Current	$I_{IN_\overline{FPWM}}$	V_{DDQEN} = V_{TTEN} = $\overline{FPWM}$ = 5.0 V	−	−	1.0	μA
PGOOD Pin ON Resistance	PGOOD_R	$I_{_PGOOD}$ = 5.0 mA	−	70	−	Ω
PGOOD Pin OFF Current	PGOOD_LK	−	−	−	1.0	μA
PGOOD LOW−to−HIGH Hold Time, for S5 to S0	t_{hold}	(Note 6)	−	−	200	μs

6. Guaranteed by design, not tested in production.

TYPICAL OPERATING CHARACTERISTICS

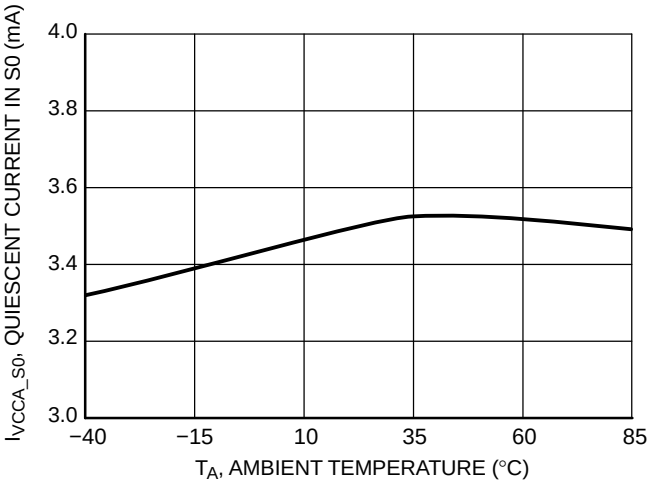


Figure 3. VCCA Quiescent Current in S0 vs. Ambient Temperature

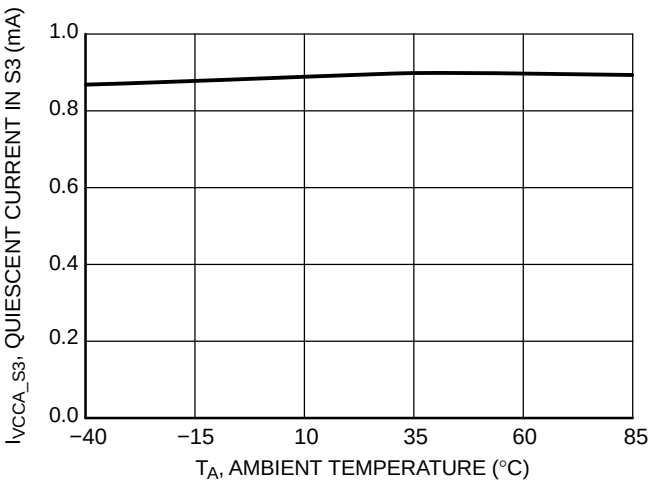


Figure 4. VCCA Quiescent Current in S3 vs. Ambient Temperature

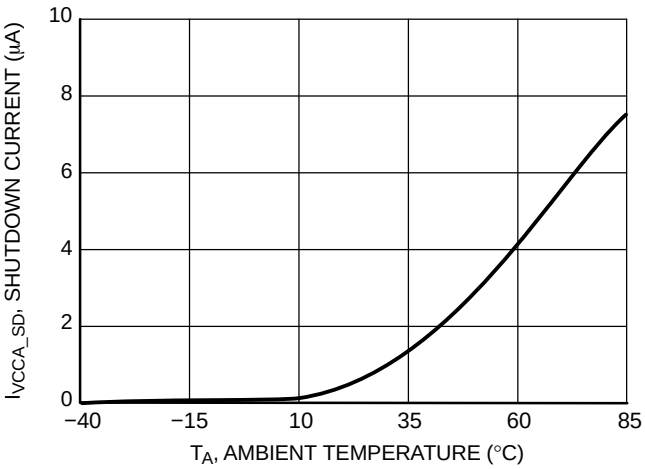


Figure 5. VCCA Shutdown Current vs. Ambient Temperature

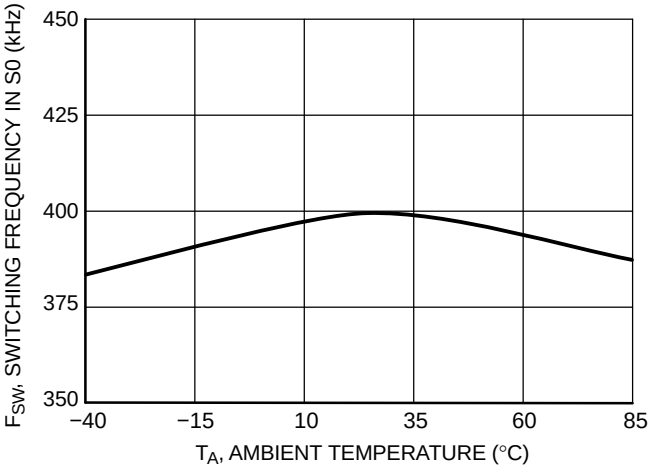


Figure 6. Switching Frequency in S0 vs. Ambient Temperature

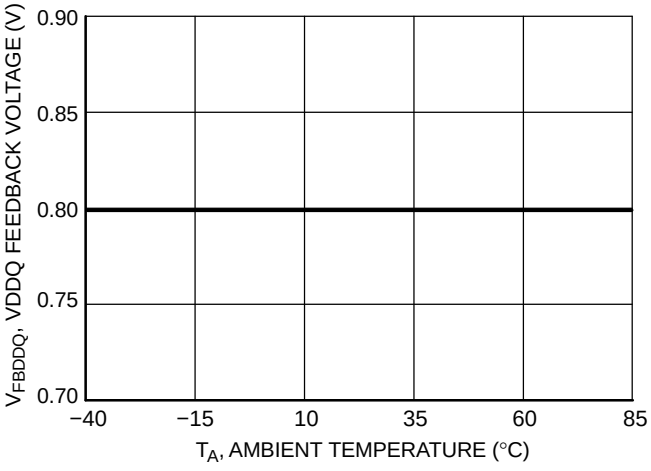


Figure 7. VDDQ Feedback Voltage vs. Ambient Temperature

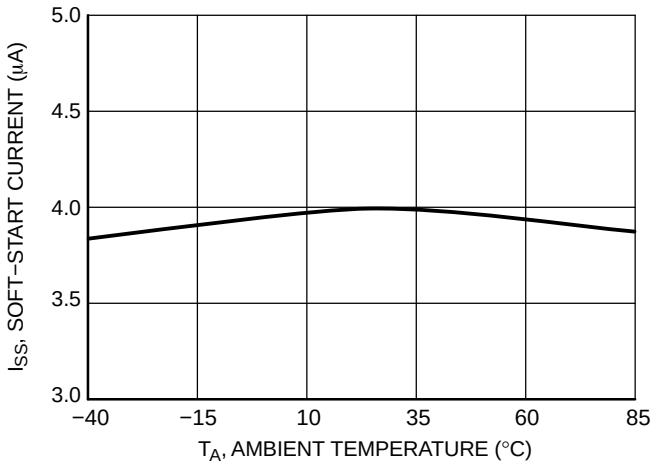


Figure 8. Soft−Start Current vs. Ambient Temperature

TYPICAL OPERATING CHARACTERISTICS

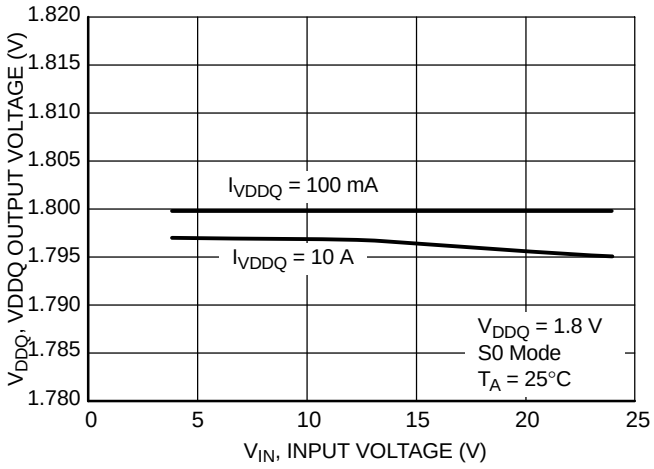


Figure 9. VDDQ Output Voltage vs. Input Voltage

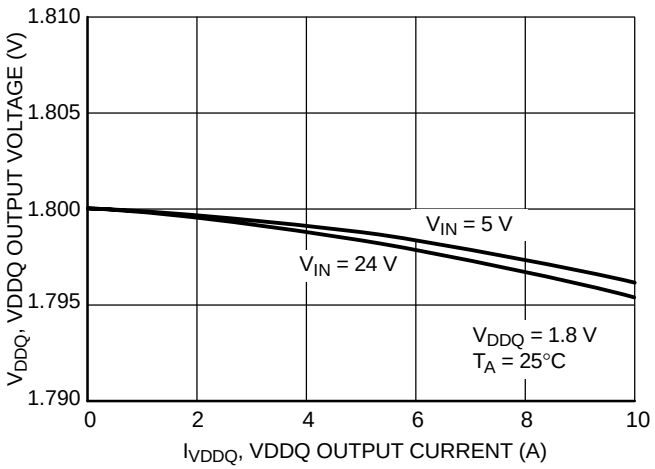


Figure 10. VDDQ Output Voltage vs. VDDQ Output Current

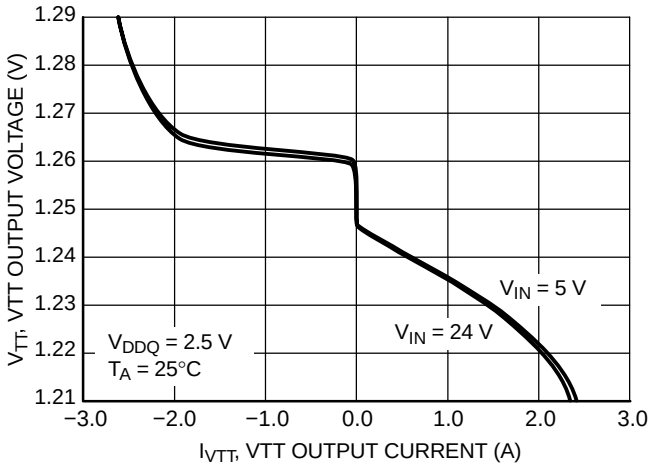


Figure 11. VTT Output Voltage (DDR) vs. VTT Output Current

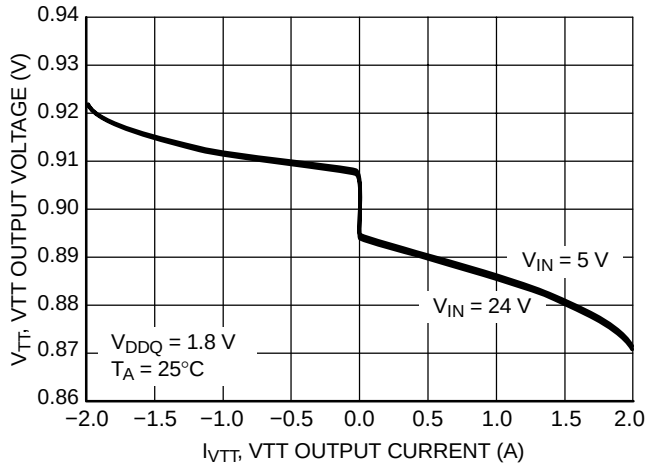


Figure 12. VTT Output Voltage (DDR2) vs. VTT Output Current

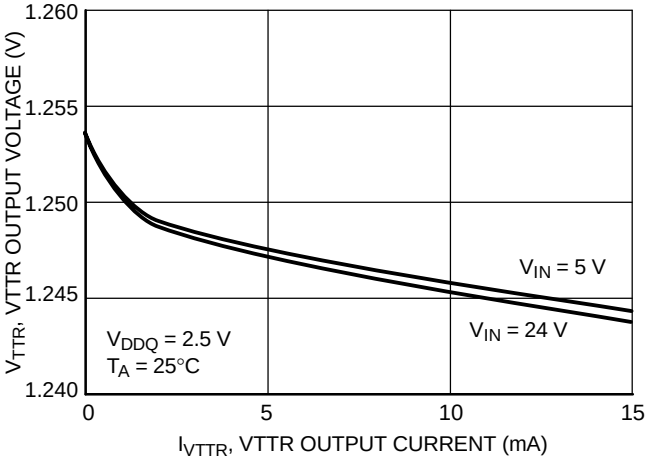


Figure 13. VTTR Output Voltage (DDR) vs. VTTR Output Current

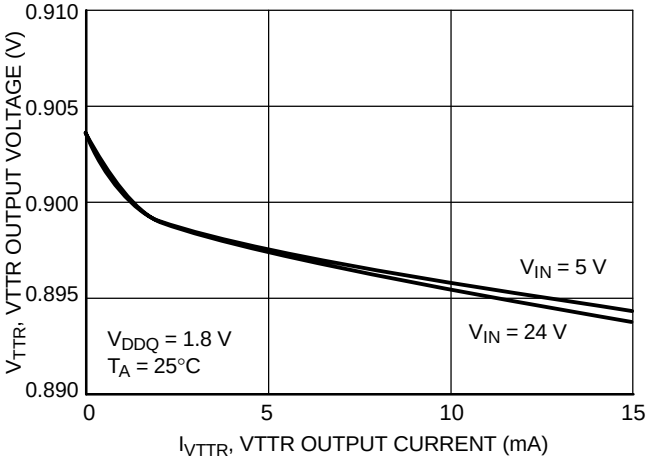


Figure 14. VTTR Output Voltage (DDR2) vs. VTTR Output Current

TYPICAL OPERATING CHARACTERISTICS

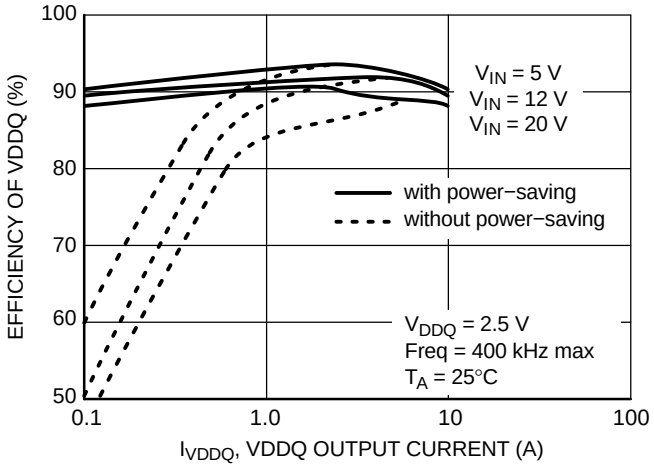


Figure 15. VDDQ Efficiency (DDR) vs. VDDQ Output Current

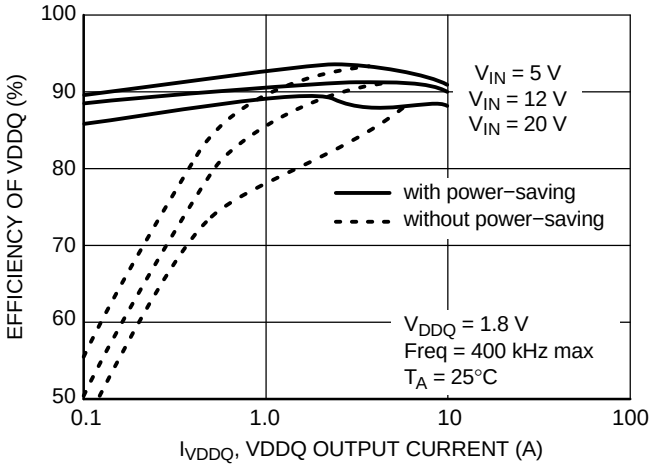


Figure 16. VDDQ Efficiency (DDR2) vs. VDDQ Output Current

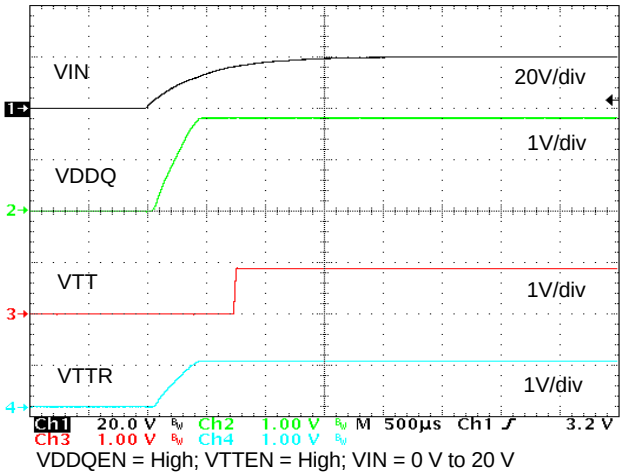


Figure 17. Power−Up Waveforms

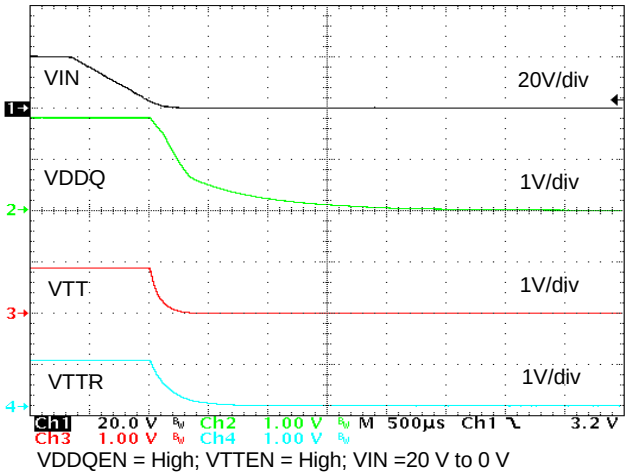


Figure 18. Power−Down Waveforms

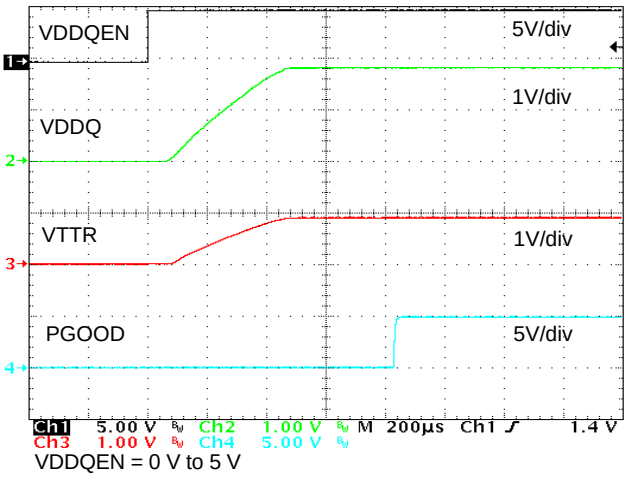


Figure 19. VDDQ, VTTR Start−Up Waveforms

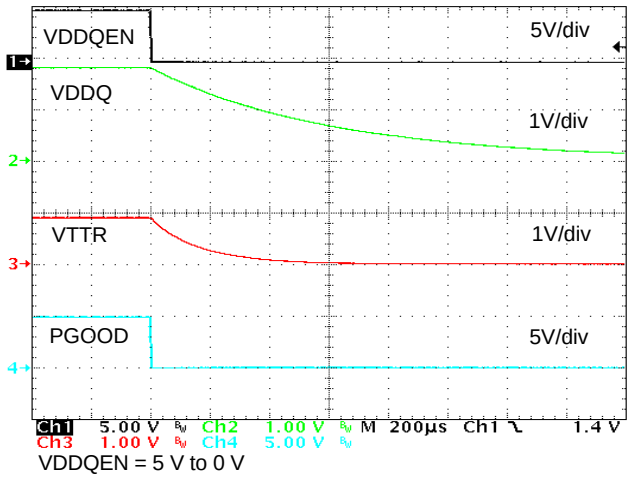
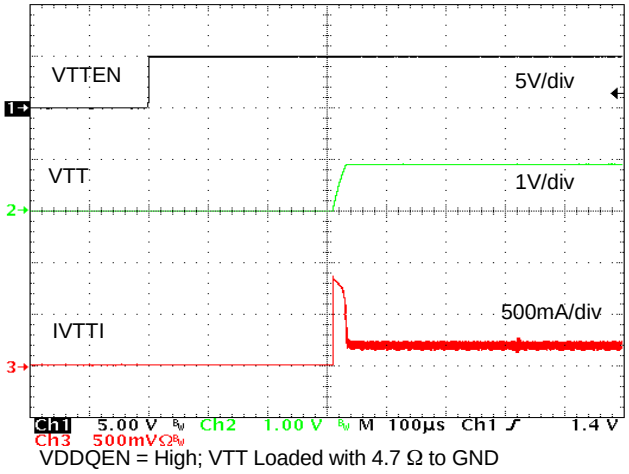


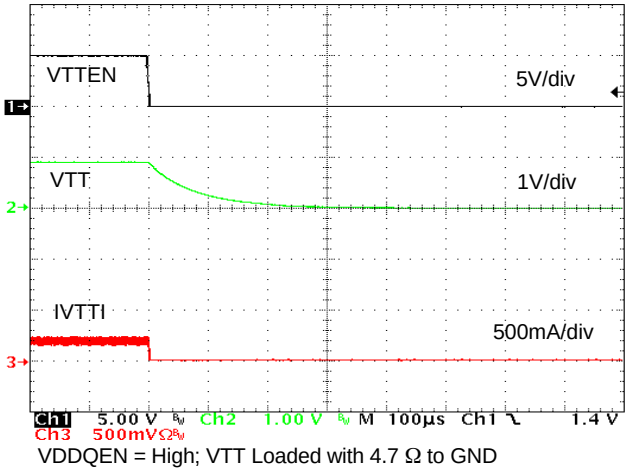
Figure 20. VDDQ, VTTR Shutdown Waveforms

TYPICAL OPERATING CHARACTERISTICS



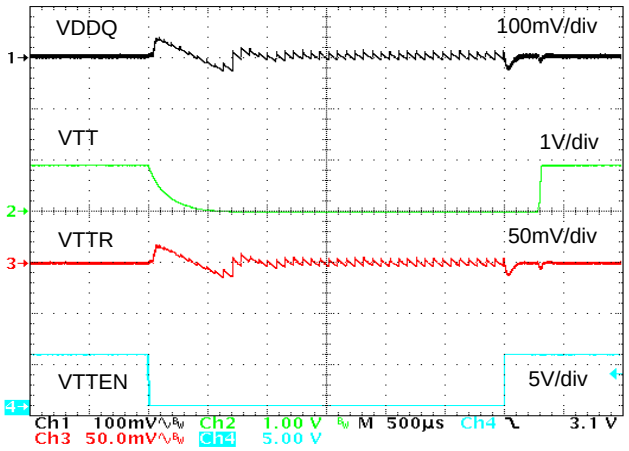
VDDQEN = High; VTT Loaded with 4.7 Ω to GND

Figure 21. VTT Start−Up Waveforms



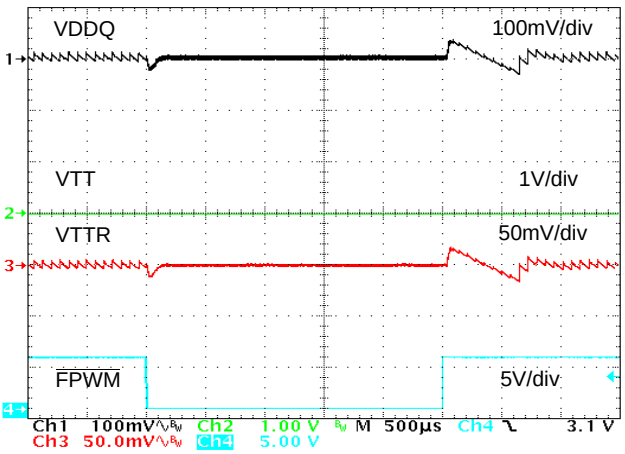
VDDQEN = High; VTT Loaded with 4.7 Ω to GND

Figure 22. VTT Shutdown Waveforms



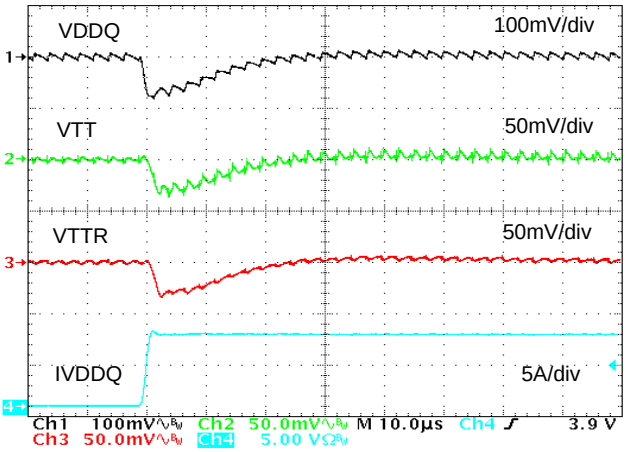
IVDDQ = 50 mA, IVTT = 100 mA, IVTTR = 5 mA

Figure 23. S0−S3−S0 Transition Waveforms



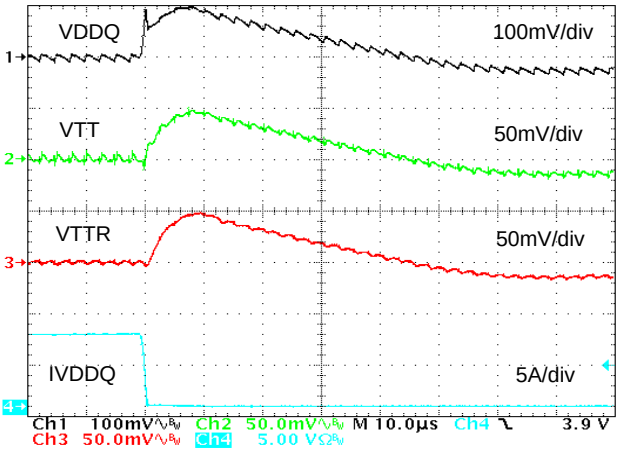
IVDDQ = 50mA, IVTT = 100mA, IVTTR = 5mA, VTTEN = 0V

Figure 24. PS−FPWM−PS Transition Waveforms



IVDDQ = 0 A−7 A, IVTT = 1.5 A, IVTTR = 15 mA

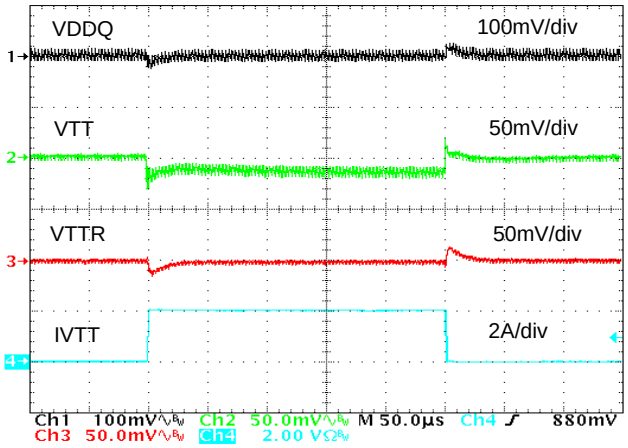
Figure 25. VDDQ Load Transient



IVDDQ = 7 A−0 A, IVTT = 1.5 A, IVTTR = 15 mA

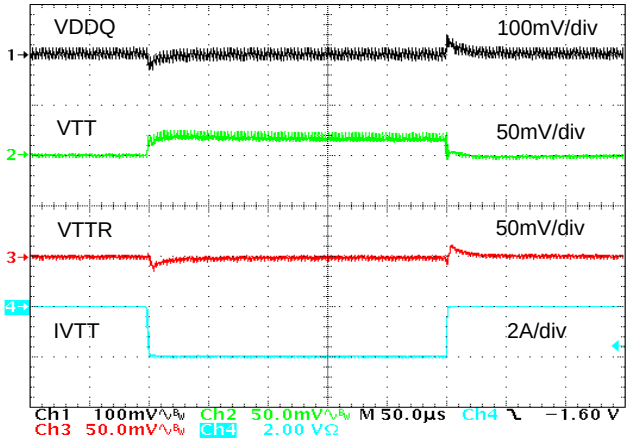
Figure 26. VDDQ Load Transient

TYPICAL OPERATING CHARACTERISTICS



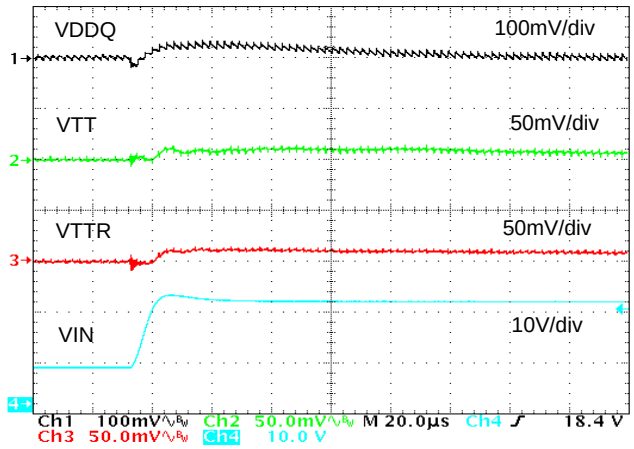
IVDDQ = 8 A, IVTT = 0 A to 2 A to 0 A, IVTTR = 15 mA

Figure 27. VTT Source Current Transient



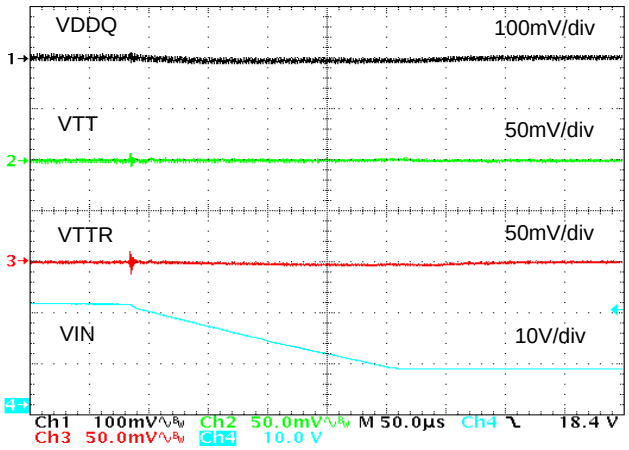
IVDDQ = 8 A, IVTT = 0 A to −2 A to 0 A, IVTTR = 15 mA

Figure 28. VTT Sink Current Transient



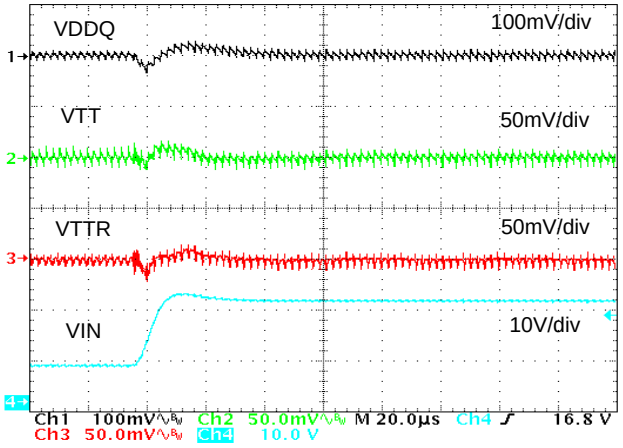
IVDDQ = 0 A, IVTT = 0 A, IVTTR = 0 mA, VIN = 7 V to 20 V

Figure 29. Line Transient 7V to 20V at No Load



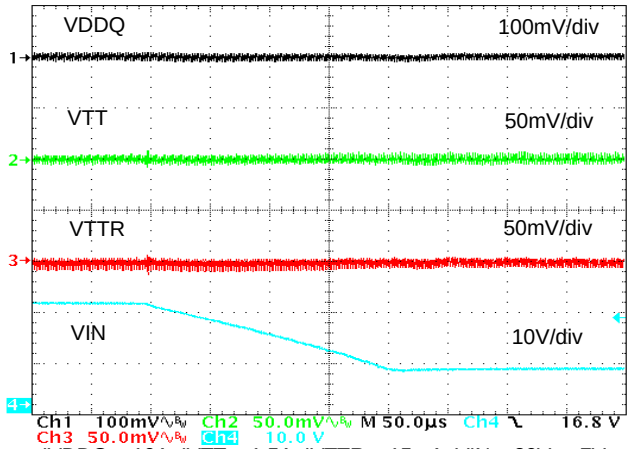
IVDDQ = 0 A, IVTT = 0 A, IVTTR = 0 mA, VIN = 20 V to 7 V

Figure 30. Line Transient 20V to 7V at No Load



IVDDQ = 10A, IVTT = 1.5A, IVTTR = 15mA, VIN = 7V to 20V

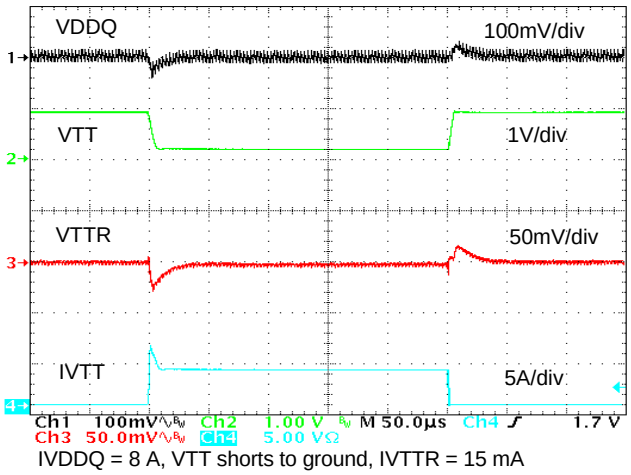
Figure 31. Line Transient 7V to 20V at Full Load



IVDDQ = 10A, IVTT = 1.5A, IVTTR = 15mA, VIN = 20V to 7V

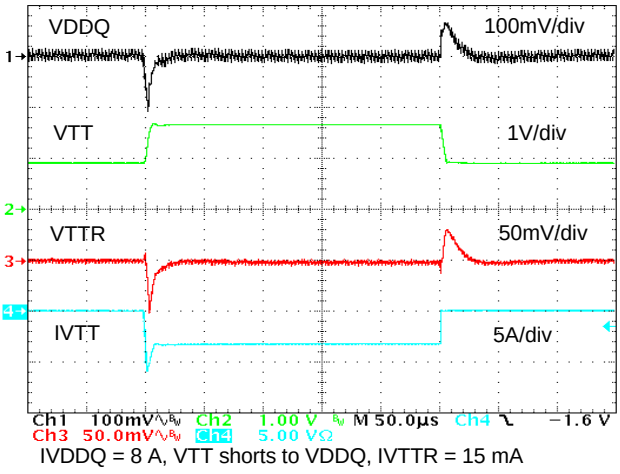
Figure 32. Line Transient 20V to 7V at Full Load

TYPICAL OPERATING CHARACTERISTICS



IVDDQ = 8 A, VTT shorts to ground, IVTTR = 15 mA

Figure 33. VTT Short Circuit to Ground and Recovery



IVDDQ = 8 A, VTT shorts to VDDQ, IVTTR = 15 mA

Figure 34. VTT Short Circuit to VDDQ and Recovery

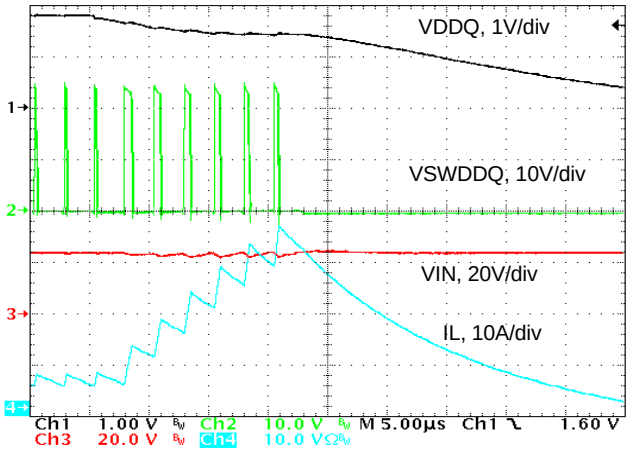


Figure 35. VDDQ OCP by Short Circuit to Ground

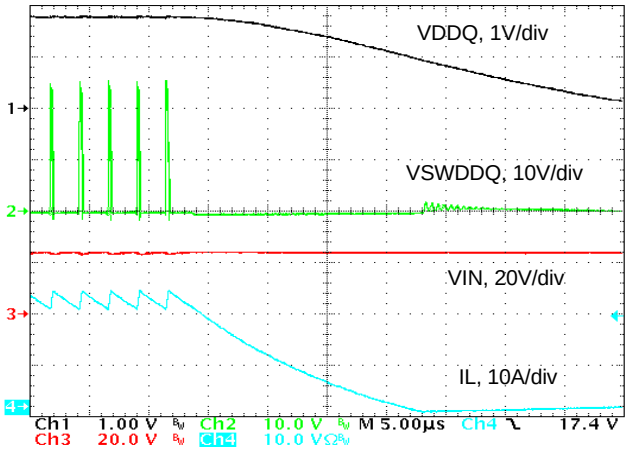


Figure 36. VDDQ OCP by Steady IVDDQ Increase

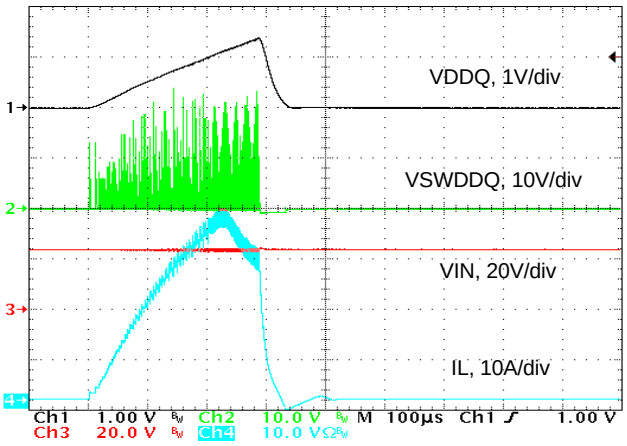


Figure 37. VDDQ OCP by Start into a Short Circuit

DETAILED OPERATING DESCRIPTION

General

The NCP5214 2−in−1 Notebook DDR Power Controller combines the efficiency of a PWM controller for the VDDQ supply, with the simplicity of using a linear regulator for the VTT termination voltage power supply. The VDDQ output can be adjusted through the external potential divider, while the VTT is internally set to track half VDDQ.

The inclusion of VDDQ power good voltage monitor, soft−start, VDDQ overcurrent protection, VDDQ overvoltage and undervoltage protections, supply undervoltage monitor, and thermal shutdown makes this device a total power solution for high current DDR memory system. The IC is packaged in DFN−22.

Control Logic

The internal control logic is powered by VCCA. The IC is enabled whenever VDDQEN is high (exceed 1.4 V). An internal bandgap voltage, VREF, is then generated. Once VREF reaches its regulation voltage, an internal signal VREFGD will be asserted. This transition wakes up the supply undervoltage monitor blocks, which will assert VCCAGD if VCCA voltage is within certain preset levels.

The control logic accepts external signals at VCCA, OCDDQ, VDDQEN, VTTEN, and $\overline{\text{FPWM}}$ pins to control the operating state of the VDDQ and VTT regulators in accordance with Table 1. A timing diagram is shown in Figure 38.

VDDQ Switching Regulator in Normal Mode (S0)

The VDDQ regulator is a switching synchronous rectification buck controller directly driving two external N−Channel power FETs. An external resistor divider sets the nominal output voltage. The control architecture is voltage mode fixed frequency PWM with external compensation and with switching frequency fixed at 400 kHz ± 15%. As can be observed from Figure 1, the VDDQ output voltage is divided down and fed back to the inverting input of an internal error amplifier through FBDDQ pin to close the loop at VDDQ = VFBDDQ × (1 + R1/R2). This amplifier compares the feedback voltage with an internal VREF (= 0.800 V) to generate an error signal for the PWM comparator. This error signal is further compared with a fixed frequency RAMP waveform derived from the internal oscillator to generate a pulse−width−modulated signal. This PWM signal drives the external N−Channel Power FETs via the TGDDQ and BGDDQ pins. External inductor L and capacitor COUT1 filter the output waveform. The VDDQ output voltage ramps up at a pre−defined soft−start rate when the IC enters state S0 from S5. When in normal mode, and regulation of VDDQ is detected, signal INREGDDQ will go HIGH to notify the control logic block.

Input voltage feedforward is implemented to the RAMP signal generation to reject the effect of wide input voltage variation. With input voltage feedforward, the amplitude of the RAMP is proportional to the input voltage.

For enhanced efficiency, an active synchronous switch is used to eliminate the conduction loss contributed by the forward voltage of a diode or Schottky diode rectifier. Adaptive non−overlap timing control of the complementary gate drive output signals is provided to reduce large shoot−through current that degrades efficiency.

Tolerance of VDDQ

The tolerance of VFBDDQ and the ratio of external resistor divider R1/R2 both impact the precision of VDDQ. With the control loop in regulation, VDDQ = VFBDDQ × (1 + R1/R2). With a worst case (for all valid operating conditions) VFBDDQ tolerance of ±1.5%, a worst case range of ±2.5% for VDDQ = 1.8 V will be assured if the ratio R1/R2 is specified as 1.2500 ±1%.

Table 1. State, Operation, Input and Output Condition Table

	Input Conditions					Operating Conditions			Output Conditions		
Mode	VCCA	VOCDDQ	VDDQEN	VTTEN	$\overline{\text{FPWM}}$	VDDQ	VTTREF	VTT	TGDDQ	BGDDQ	PGOOD
S5	Low	X	X	X	X	H−Z	H−Z	H−Z	Low	Low	Low
S5	X	Low	X	X	X	H−Z	H−Z	H−Z	Low	Low	Low
S0	High	High	High	High	X	Normal	Normal	Normal	Normal	Normal	H−Z
S3	High	High	High	Low	High	Standby	Normal	H−Z	Standby (Power−saving)	Standby (Power−saving)	H−Z
S3	High	High	High	Low	Low	Normal	Normal	H−Z	Normal	Normal	H−Z
S5	X	X	Low	X	X	H−Z	H−Z	H−Z	Low	Low	Low

VDDQ Regulator in Standby Mode (S3)

During state S3, a power−saving mode is activated when the $\overline{\text{FPWM}}$ pin is pulled to VCCA. In power−saving mode, the switching frequency is reduced with the VDDQ output current and the low−side FET is turned off after the detection of negative inductor current, so as to enhance the efficiency of the VDDQ regulator at light loads. The switching frequency can be reduced smoothly until it reaches the minimum frequency at about 15 kHz. Therefore, perceptible audible noise can be avoided at light load condition.

In power−saving mode, the low−side MOSFET is turned off after the detection of negative inductor current and the converter cannot sink current. The power−saving mode can be disabled by pulling the $\overline{\text{FPWM}}$ pin to ground. Then, the converter operates in forced−PWM mode with fixed switching frequency and ability to sink current.

Fault Protection of VDDQ Regulator

During state S0 and S3, external resistor (RL1) between OCDDQ and VIN sets the current limit for the high−side switch. An internal 31 μA current sink (IOC) at OCDDQ pin establishes a voltage drop across this resistor and develops a voltage at the non−inverting input of the current limit comparator. The voltage at the non−inverting input is compared to the voltage at SWDDQ pin when the high−side gate drive is high after a fixed period of blanking time (150 ns) to avoid false current limit triggering. When the voltage at SWDDQ is lower than that at the non−inverting input for 4 consecutive internal clock cycles, an overcurrent condition occurs, during which, all outputs will be latched off to protect against a short−to−ground condition on SWDDQ or VDDQ. The IC will be reset once VCCA or VDDQEN is cycled.

Feedback Compensation of VDDQ Regulator

The compensation network is shown in Figures 2 and 39.

VTT Active Terminator in Normal Mode (S0)

The VTT active terminator is a two−quadrant linear regulator with two internal N−channel power FETs. It is capable of sinking and sourcing at least 1.5 A continuous current and up to 2.4 A transient peak current. It is activated in normal mode in state S0 when the VTTEN pin is HIGH and VDDQ is in regulation. Its input power path is from VDDQ with the internal FETs gate drive power derived from VCCA. The VTT internal reference voltage is derived from the DDQREF pin. The VTT output is set to VDDQ/2 when VTT output is connecting to the FBVTT pin directly. This regulator is stable with only a minimum 20 μF output capacitor. The VTT regulator will have an internal soft−start when it is transited from disable to enable. During the VTT soft−start, a current limit is used as a current source to charge up the VTT output capacitor. The current limit is initially 1.0 A during VTT soft−start. It is then increased to 2.5 A after 128 internal clock cycles which is typically 0.32 ms.

VTT Active Terminator in Standby Mode (S3)

VTT output is high−impedance in S3 mode.

Fault Protection of VTT Active Terminator

To provide protection for the internal FETs, bidirectional current limit is implemented, preset at the minimum of 2.5 A magnitude.

Thermal Consideration of VTT Active Terminator

The VTT terminator is designed to handle large transient output currents. If large currents are required for very long duration, then care should be taken to ensure the maximum junction temperature is not exceeded. The 5x6 DFN−22 has a thermal resistance of 35°C/W (dependent on air flow, grade of copper, and number of vias). *In order to take full advantage from this thermal capability of this package, the thermal pad underneath must be soldered directly onto a PCB metal substrate to allow good thermal contact. It is recommended that PCB with 2 oz. copper foil is used and there should have 6 to 8 vias with 0.6 mm hole size underneath the package's thermal pad connecting the top layer metal to the bottom layer metal and the internal layer metal substrates of the PCB.*

VTTREF Output

The VTTREF output tracks VDDQREF/2 at ±2% accuracy. It has source current capability of up to 15 mA. VTTREF should be bypassed to analog ground of the device by 1.0 μF ceramic capacitor for stable operation. The VTTREF is turned on as long as VDDQEN is pulled high. In S0 mode, VTTREF soft−starts with VDDQ and tracks VDDQREF/2. In S3 mode, VTTREF is kept on with VDDQ. VTTREF is turned off only in S4/S5 like VDDQ output.

Output Voltages Sensing

The VDDQ output voltage is sensed across the FBDDQ and AGND pins. FBDDQ should be connected through a feedback resistor divider to the VDDQ point of regulation which is usually the local VDDQ bypass capacitor for load. The AGND should be connected directly through a sense trace to the remote ground sense point which is usually the ground of local VDDQ bypass capacitor for load.

The VTT output voltage is sensed between the FBVTT and VTTGND pins. The FBVTT should be connected to the VTT regulation point, which is usually the VTT local bypass capacitor, via a direct sense trace. The VTTGND should be connected via a direct sense trace to the ground of the VTT local bypass capacitor for load.

Supply Voltage Undervoltage Monitor

The IC continuously monitors VCCA and VIN through VCCA pin and OCDDQ pin respectively. VCCAGD is set HIGH if VCCA is higher than its preset threshold (derived from VREF with hysteresis). The IC will enter S5 state if VCCA fails while in S0 and both VDDQEN and VTTEN remain HIGH.

Thermal Shutdown

When the chip junction temperature exceeds 150°C, the entire IC is shutdown. The IC resumes normal operation only after the junction temperature dropping below 125°C.

Power Good

The PGOOD is an open−drain output of a window comparator which continuously monitors the VDDQ output voltage. The PGOOD is pulled low when the VDDQ rises 12% above or drops 12% below the nominal regulation point. The PGOOD becomes high impedance when the VDDQ is within ±12% of the preset nominal regulation voltage. A 100 kΩ resistor is recommended to connect between PGOOD and VCCA as pull−up resistor for logic level output.

Overvoltage Protection

When the VDDQ output is above 106% but below 130% of the nominal regulation output voltage, the controller turns off the high−side MOSFET and turns on the low−side MOSFET to discharge the excessive output voltage. When the VDDQ output voltage goes back down to the nominal regulation voltage, normal switching cycles are resumed. When the VDDQ output exceeds 130% (typ) of the nominal regulation voltage for 4 consecutive internal clock cycles, the controller sets overvoltage fault, the device is latched off by turning off both the high−side and low−side MOSFETs. The overvoltage fault latch can be reset and the controller can be restarted by toggling VDDQEN, VCCA, or VIN.

Undervoltage Protection

In S3 power−saving mode with reduced switching at lighter loads, when the VDDQ falls below 94% of the nominal regulation voltage, the reduced switching frequency is raised up back to the maximum switching frequency. When VDDQ voltage is back to nominal regulation voltage, the normal S3 power−saving operation is resumed. In both S0 and S3 modes, when the VDDQ falls below 65% (typ) of the nominal regulation voltage for 4 consecutive internal clock cycles, the undervoltage fault is set, the device is latched off by turning off both the high−side and low−side MOSFETs. The output is discharged by the load current. The load current and output capacitance determine the discharge rate. Cycling VDDQEN, VCCA, or VIN can reset the undervoltage fault latch and restart the controller.

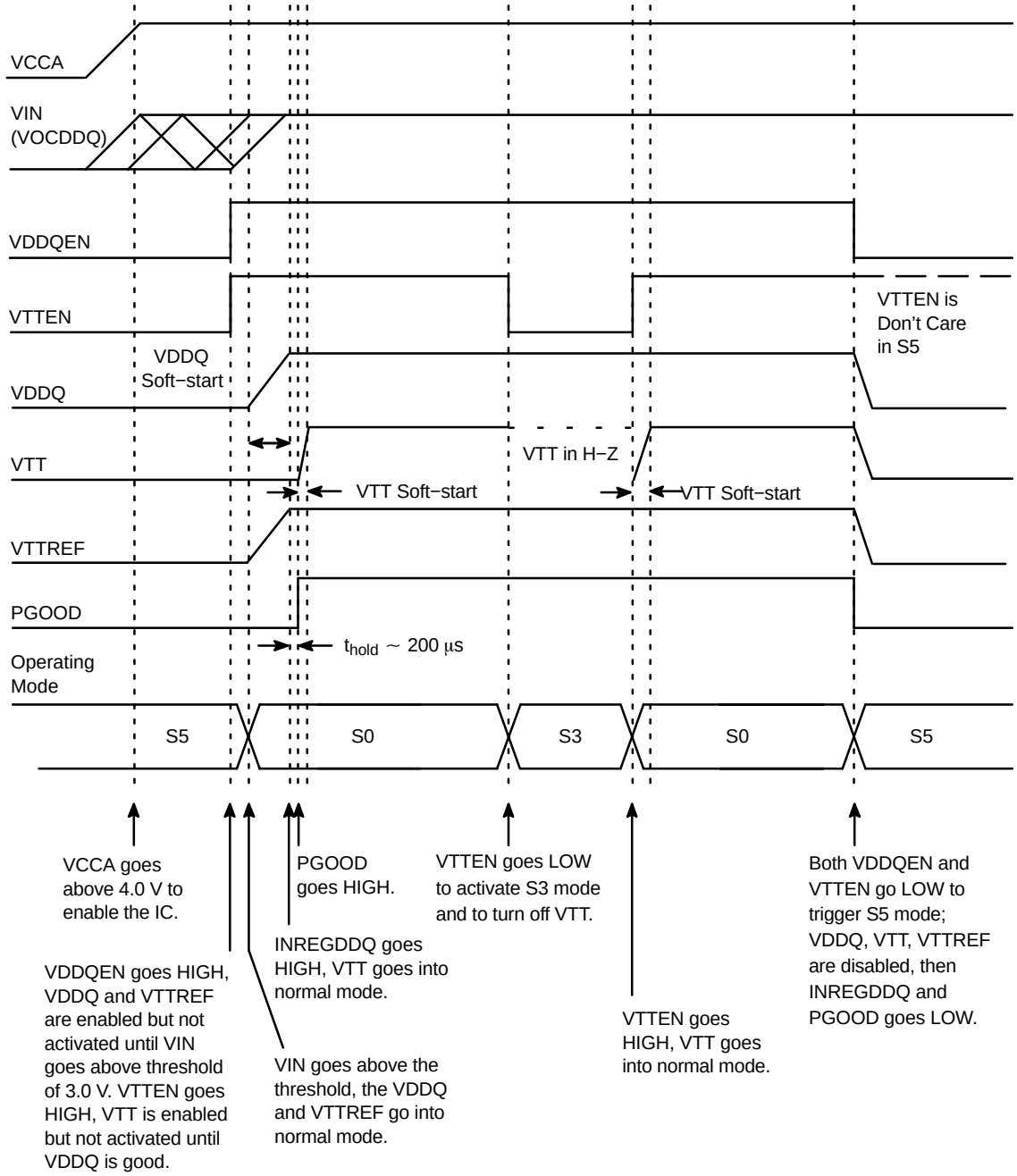


Figure 38. Powerup and Powerdown Timing Diagram

APPLICATION INFORMATION

Input Capacitor Selection for VDDQ Buck Regulator

The input capacitor is important for proper regulation operation of the buck regulator. It minimizes the input voltage ripple and current ripple from the power source by providing a local loop for switching current. The input capacitor should be placed close to the drain of the high−side MOSFET and source of the low−side MOSFET with short, wide traces for connection. The input capacitor must have large enough rms ripple current rating to withstand the large current pulses present at the input of the bulk regulator due to the switching current. The required input capacitor rms ripple current rating can be estimated by the following with minimum V_{IN}:

$$I_{CIN(RMS)} \geq I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}} - \left(\frac{V_{OUT}}{V_{IN}}\right)^2} \quad \text{(eq. 1)}$$

Besides, the voltage rating of the input capacitor should be at least 1.25 times of the maximum input voltage. Capacitance of around 20 μF to 50 μF should be sufficient for most DDR applications. Ceramic capacitors are the most suitable choice of input capacitor for notebook applications due to their low ESR, high ripple current, and high voltage rating. POSCAP or OS−CON capacitors can also be used since they have good ESR and ripple current rating, but they are larger in size and more expensive. Aluminum electrolytic capacitors are also a choice for their high voltage rating and low cost, but several aluminum capacitors in parallel should be used for the required ripple current. If ceramic capacitors are used, X5R and X7R types are preferred rather than the Y5V type since the X5R and X7R types are ceramic capacitors and have smaller tolerance and temperature coefficient.

Output Capacitor Selection for VDDQ Buck Regulator

The output filter capacitor plays an important role in steady state output ripple voltage, load transient requirement, and loop compensation stability. The ESR and the capacitance of the output capacitor are the most important parameters needed to be considered. In general, the output capacitor must have small enough ESR for output ripple voltage and load transient requirement. Besides, the capacitance of the output capacitor should be large enough to meet the overshoot and undershoot during load transient. Since steady state output ripple voltage, transient load undershoot and overshoot are the largest at maximum V_{IN}, the ESR and capacitance of output capacitor should be estimated at the maximum V_{IN} condition.

For steady output ripple voltage, both ESR and capacitance of the output capacitor are the contributing factors, however, the capacitor ESR is the dominant factor. The output ripple voltage is calculated as follows:

$$V_{ripple} = I_{L(ripple)} \times ESR + \frac{I_{L(ripple)} \times t_{on}}{C_{OUT}} \quad \text{(eq. 2)}$$

$$V_{ripple} = I_{L(ripple)} \times ESR, \text{ for small } t_{on} \text{ and large } C_{OUT} \quad \text{(eq. 3)}$$

where $I_{L(ripple)}$ is the inductor ripple current, t_{on} is on−time, and C_{OUT} is the output capacitance.

The inductor ripple current can be calculated by the equation:

$$I_{L(ripple)} = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}} \quad \text{(eq. 4)}$$

where L is the inductance and f_{SW} is the switching frequency. The output ripple voltage can be reduced by either using the inductor with larger inductance or the output capacitor with smaller ESR. Thus, the ESR needed to meet the ripple voltage requirement can be obtained by:

$$ESR \leq \frac{V_{ripple} \times L \times f_{SW} \times V_{IN}}{(V_{IN}-V_{OUT}) \times V_{OUT}} \quad \text{(eq. 5)}$$

The inductor ripple current is typically 30% of the maximum load current and the ripple voltage is typically 2% of the output voltage. Thus, the above inequality can be simplified to:

$$ESR \leq \frac{0.02 \times V_{OUT}}{0.3 \times I_{LOAD(max)}} \quad \text{(eq. 6)}$$

For the load transient, the output capacitor contributes to both the load−rise and the load−release responses. The voltage undershoot during step−up load can be calculated by the equation:

$$V_{undershoot} = \Delta I_{LOAD} \times ESR + \frac{\Delta I_{LOAD}}{C_{OUT}} \times \left(\frac{1-\frac{V_{OUT}}{V_{IN}}}{f_{SW}}\right) \quad \text{(eq. 7)}$$

where ΔI_{LOAD} is the change in output current. If the second term is ignored, then it becomes the following inequality:

$$ESR \leq \frac{V_{undershoot}}{\Delta I_{LOAD}} \quad \text{(eq. 8)}$$

The maximum ESR requires to meet voltage undershoot requirement at step−up load transient can be estimated from the above inequality.

Then, the required output capacitor capacitance can be obtained by the following:

$$C_{OUT} \geq \frac{\Delta I_{LOAD}}{V_{undershoot}-\Delta I_{LOAD} \times ESR} \times \left(\frac{1-\frac{V_{OUT}}{V_{IN}}}{f_{SW}}\right) \quad \text{(eq. 9)}$$

The output voltage overshoot during load−release is because the excessive stored energy in the inductor is absorbed by the output capacitor. The overshoot voltage can be calculated by the following equation:

$$V_{overshoot} = \sqrt{\frac{LI^2_{STEP(peak)} + C_{OUT}V^2_{OUT}}{C_{OUT}}} - V_{OUT} \quad \text{(eq. 10)}$$

Then the required output capacitor capacitance can be estimated by:

$$C_{OUT} \geq \frac{L \times I^2_{STEP(peak)}}{(V_{overshoot} + V_{OUT})^2 - V^2_{OUT}} \quad \text{(eq. 11)}$$

$$I_{STEP(peak)} = \Delta I_{LOAD} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2L \times f_{SW} \times V_{IN}} \quad \text{(eq. 12)}$$

where $I_{STEP(peak)}$ is the load current step plus half of the ripple current at the load release and ΔI_{LOAD} is the change in the output load current.

Besides, the ESR and the capacitance of the output filter capacitor also contribute to double pole and ESR zero frequencies of the output filter, and the poles and zeros frequencies of the compensation network for close loop stability. The compensation network will be discussed in more detail in the Loop Compensation section.

Other parameters about output filter capacitor that needed to be considered are the voltage rating and ripple current rating. The voltage rating should be at least 1.25 times the output voltage and the rms ripple current rating should be greater than the inductor ripple current. Thus, the voltage rating and ripple current rating can be obtained by:

$$V_{rating} \geq 1.25 \times V_{OUT} \quad \text{(eq. 13)}$$

$$I_{COUT(RMS)} \geq I_{L(ripple)} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f_{SW} \times V_{IN}} \quad \text{(eq. 14)}$$

SP−Cap, POSCAP and OS−CON capacitors are suitable for the output capacitor since their ESR is low enough to meet the ripple voltage and load transient requirements. Usually, two or more capacitors of the same type, capacitance and ESR can be used in parallel to achieve the required ESR and capacitance without change the ESR zero position for maintaining the same loop stability. Other than the performance point of view, the physical size and cost are also the concerned factors for output capacitor selection.

Inductor Selection

The inductor should be chosen according to the inductor ripple current, inductance, maximum current rating, transient load release, and DCR.

In general, the inductor ripple current is 20% to 40% of the maximum load current. A ripple current of 30% of the maximum load current can be used as a typical value. The required inductance can be estimated by:

$$L \geq \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{0.3 \times I_{LOAD(max)} \times V_{IN} \times f_{SW}} \quad \text{(eq. 15)}$$

where $I_{LOAD(max)}$ is the maximum load current.

The DC current rating of the inductor should be about 1.2 times of the peak inductor current at maximum output load current. Therefore, the maximum DC current rating of the inductor can be obtained by:

$$I_{L(rating)} = 1.2 \times I_{L(peak)} \quad \text{(eq. 16)}$$

where $I_{L(peak)}$ is the peak inductor current at maximum load current which is determined by:

$$I_{L(peak)} = I_{LOAD(max)} + \frac{I_{L(ripple)}}{2} = I_{LOAD(max)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad \text{(eq. 17)}$$

Since the excessive energy stored in the inductor contributed to the output voltage overshoot during load release, the following inequality can be used to ensure that the selected inductance value can meet the voltage overshoot requirement at load release:

$$L \leq \frac{C_{OUT} \times \left((V_{overshoot} + V_{OUT})^2 - V^2_{OUT}\right)}{I^2_{STEP(peak)}} \quad \text{(eq. 18)}$$

In addition, the inductor also needs to have low enough DCR to obtain good conversion efficiency. In general, inductors with about 2.0 mΩ to 3.0 mΩ per μH of inductance can be used. Besides, larger inductance value can be selected to achieve higher efficiency as long as it still meets the targeted voltage overshoot at load release and inductor DC current rating.

MOSFET Selection

External N−channel MOSFETs are used as the switching elements of the buck controller. Both high−side and low−side MOSFETs must be logic−level MOSFETs which can be fully turned on at 5.0 V gate−drive voltage. On−resistance ($R_{DS(on)}$), maximum drain−to−source voltage (V_{DSS}), maximum drain current rating, and gate charges (Q_G, Q_{GD}, Q_{GS}) are the key parameters to be considered when choosing the MOSFETs.

For on−resistance, it should be the lower; the better is the performance in terms of efficiency and power dissipation. Check the MOSFET's rated $R_{DS(on)}$ at V_{GS} = 4.5 Vwhen selecting the MOSFETs. The low−side MOSFET should have lower $R_{DS(on)}$ than the high−side MOSFET since the turn−on time of the low−side MOSFET is much longer than the high−side MOSFET in high V_{IN} and low V_{OUT} buck converter. Generally, high−side MOSFET with $R_{DS(on)}$ about 7.0 mΩ and low−side MOSFET with $R_{DS(on)}$ about 5.0 mΩ can achieve good efficiency.

The maximum drain current rating of the high−side MOSFET and low−side MOSFET must be higher than the peak inductor current at maximum load current. The low−side MOSFET should have larger maximum drain current rating than the high−side MOSFET since the low−side MOSFET have longer turn−on time.

The maximum drain−to−source voltage rating of the MOSFETs used in buck converter should be at least 1.2 times of the maximum input voltage. Generally, V_{DSS} of 30 V should be sufficient for both high−side MOSFET and low−side MOSFET of the buck converter for notebook application.

As a general rule of thumb, the gate charges are the smaller; the better is the MOSFET while $R_{DS(on)}$ is still low enough. MOSFETs are susceptible to false turn−on under high dV/dt and high VDS conditions. Under high dV/dt and high V_{DS} condition, current will flow through the C_{GD} of the capacitor divider formed by C_{GD} and C_{GS}, cause the C_{GS} to charge up and the V_{GS} to rise. If the V_{GS} rises above the threshold voltage, the MOSFET will turn on. Therefore, it should be checked that the low−side MOSFET have low Q_{GD} to Q_{GS} ratio. This indicates that the low−side MOSFET have better immunity to short moment false turn−on due to high dV/dt during the turn−on of the high−side MOSFET. Such short moment false turn−on will cause minor shoot−through current which will degrade efficiency, especially at high input voltage condition.

Overcurrent Protection of VDDQ Buck Regulator

The OCP circuit is configured to set the current limit for the current flowing through the high−side FET and inductor during S0 and S3. The overcurrent tripping level is programmed by an external resistor RL1 connected between the OCDDQ pin and drain of the high−side FET. An internal 31 μA current sink (IOC) at pin OCDDQ establishes a voltage drop across the resistor RL1 at a magnitude of RL1xIOC and develops a voltage at the non−inverting input of the current limit comparator. Another voltage drop is established across the high−side MOSFET $R_{DS(on)}$ at a magnitude of $I_L x R_{DS(on)}$ and a voltage is developed at SWDDQ when the high−side MOSFET is turned on and the inductor current flows through the $R_{DS(on)}$ of the MOSFET. The voltage at the non−inverting input of the current limit comparator is then compared to the voltage at SWDDQ pin when the high−side gate drive is high after a fixed period of blanking time (150 ns) to avoid false current limit triggering. When the voltage at SWDDQ is lower than the voltage at the non−inverting input of the current limit comparator for four consecutive internal clock cycles, an overcurrent condition occurs, during which, all outputs will be latched off to protect against a short−to−ground condition on SWDDQ or VDDQ. i.e., the voltage drop across the $R_{DS(on)}$ of high−side FET developed by the drain current is larger than the voltage drop across RL1, the OCP is triggered and the device will be latched off.

The overcurrent protection will trip when a peak inductor current hit the I_{LIMIT} determined by the equation:

$$I_{LIMIT} = \frac{RL1 \times IOC}{R_{DS(on)}} \quad \text{(eq. 19)}$$

It should be noted that the OCDDQ pin must be pulled high to VIN through a resistor RL1 and this pin cannot be left floating for normal operation. The voltage drop across RL1 must be less than 1.0 V to allow enough headroom for the voltage detection at the OCDDQ pin under low VIN condition. In addition, since the MOSFET $R_{DS(on)}$ varies with temperature as current flows through the MOSFET increases, the OCP trip point also varies with the MOSFET $R_{DS(on)}$ temperature variation.

Since the IOC and $R_{DS(on)}$ have device variations and MOSFET $R_{DS(on)}$ increase with temperature, to avoid false triggering the overcurrent protection in normal operating output load range, calculate the RL1 value from the previous equation with the following conditions such that minimum value of inductor current limit is set:

1. The minimum IOC value from the specification table.
2. The maximum $R_{DS(on)}$ of the MOSFET used at the highest junction temperature.
3. Determine I_{LIMIT} for $I_{LIMIT} > I_{LOAD(max)} + I_{L(ripple)}/2$, where $I_{LOAD(max)} = I_{VDDQ(max)} + I_{VTT(max)}$ if VTT is powered by VDDQ.

Besides, a decoupling capacitor C_{DCPL} should be added closed to the lead of the current limit setting resistor RL1 which connected to the drain of the high−side MOSFET.

Loop Compensation

Once the output LC filter components have been determined, the compensation network components can be selected. Since NCP5214 is a voltage mode PWM converter with output LC filter, Type III compensation network is required to obtain the desired close loop bandwidth and phase boost with unconditional stability. The NCP5214 PWM modulator, output LC filter and Type III compensation network are shown in Figure 39. The output LC filter has a double pole and a single zero. The double pole is due to the inductance of the inductor and capacitance of the output capacitor, while the single zero is due to the ESR and capacitance of the output capacitor. The Type III compensation has two RC pole−zero pairs. The two zeros are used to compensate the LC double pole and provide 180° phase boost. The two poles are used to compensate the ESR zero and provide controlled gain roll−off. For an ideally compensated system, the Bode plot should have the close−loop gain roll−off with a slope of −20 dB/decade crossing the 0 dB with the required bandwidth and the phase margin larger than 45° for all frequencies below the 0 dB frequency. The closed loop gain is obtained by adding the modulator and filter gain (in dB) to the compensation gain (in dB).The bandwidth is the frequency at which the gain is 0 dB and the phase margin is the difference between the close loop phase and 180°. The goal of compensation is to achieve a stable close loop system with the highest possible bandwidth, the gain having −20 dB/decade slope at 0 dB gain crossing, and sufficient phase margin for stability. The bandwidth of close loop gain should be less than 50% of the switching frequency and the compensation gain should be bounded by the error amplifier open loop gain.

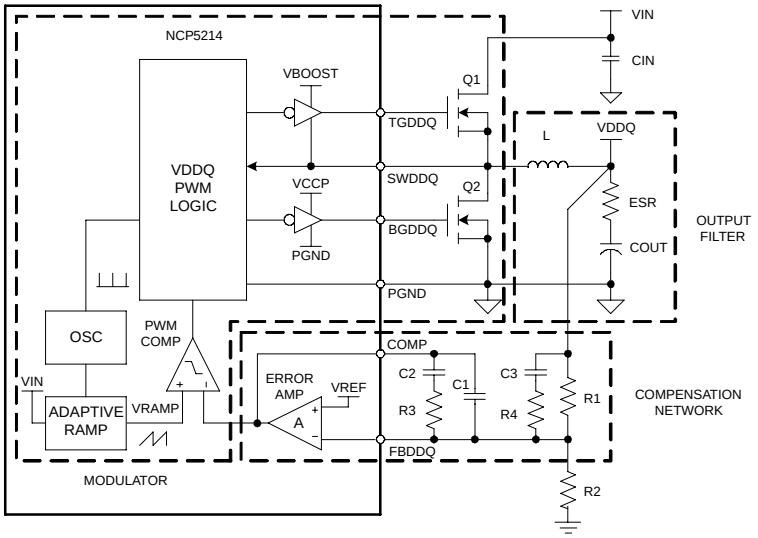


Figure 39. Voltage Mode Buck Converter with Modulator, LC filter and Type III Compensation

Modulator DC Gain can be calculated by:

$$G_{MOD(DC)} = 20 \log \frac{V_{IN}}{V_{RAMP}} \quad \text{(eq. 20)}$$

LC filter double pole and ESR zero break frequencies are defined by:

$$f_{PLC} = \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \quad \text{(eq. 21)}$$

$$f_{ZESR} = \frac{1}{2\pi \times ESR \times C_{OUT}} \quad \text{(eq. 22)}$$

Compensation network DC Gain can be calculated by the equation:

$$G_{COMP(DC)} = 20 \log \frac{R_3}{R_1} \quad \text{(eq. 23)}$$

Type III compensation poles and zeros break frequencies are defined by the below equations:

$$f_{Z1} = \frac{1}{2\pi \times R_3 \times C_2} \quad \text{(eq. 24)}$$

$$f_{P1} = \frac{1}{2\pi \times R_3 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)} \quad \text{(eq. 25)}$$

$$f_{Z2} = \frac{1}{2\pi \times (R_1 + R_4) \times C_3} \quad \text{(eq. 26)}$$

$$f_{P2} = \frac{1}{2\pi \times R_4 \times C_3} \quad \text{(eq. 27)}$$

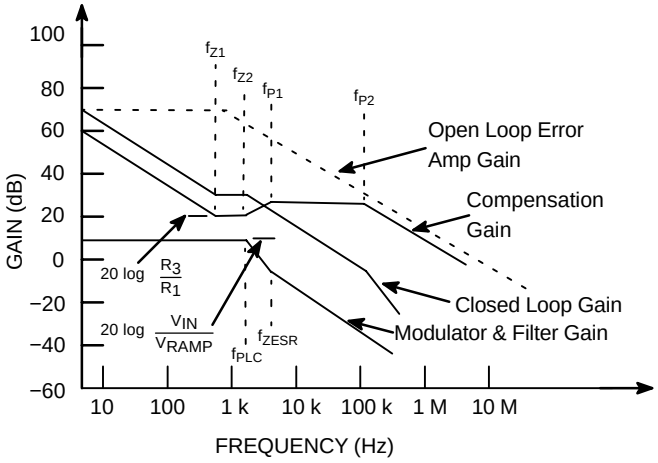


Figure 40. Asymptotic Bode Plot of the Converter Gain

Close loop system bandwidth can be calculated by:

$$BW = \frac{R3}{R1} \times \frac{V_{IN}}{V_{RAMP}} \times \frac{1}{2\pi \times \sqrt{L \times C_{OUT}}} \quad \text{(eq. 28)}$$

Since the ramp amplitude of the PWM modulator has a voltage feedforward function, the ramp amplitude is a function of V_{IN} which can be determined by:

$$V_{RAMP} = 1.25\ V + 0.045 \times (V_{IN} - 5.0\ V) \quad \text{(eq. 29)}$$

Below are some guidelines for setting the compensation components:

1. Set a value for R_1 between 2.0 kΩ and 5.0 kΩ.
2. Set a target for the close loop bandwidth which should be less than 50% of the switching frequency.
3. Pick compensation DC gain (R_3/R_1) for desired close loop bandwidth.
4. Place 1st zero at half filter double pole.
5. Place 1st pole at ESR zero.
6. Place 2nd zero at filter double pole.
7. Place 2nd pole at half the switching frequency.

By using the above equations and guidelines, the compensation components values can be determined by the equations below:

$$R_3 = \frac{2\pi \times BW \times V_{RAMP} \times R_1 \times \sqrt{L \times C_{OUT}}}{V_{IN}} \quad \text{(eq. 30)}$$

$$C_2 = \frac{2 \times \sqrt{L \times C_{OUT}}}{R_3} \quad \text{(eq. 31)}$$

$$C_1 = \frac{C_2}{\left(\frac{R_3 \times C_2}{ESR \times C_{OUT}}\right) - 1} \quad \text{(eq. 32)}$$

$$R_4 = \frac{R_1}{\pi \times f_{SW} \times \sqrt{L \times C_{OUT}} - 1} \quad \text{(eq. 33)}$$

$$C_3 = \frac{1}{\pi \times R_4 \times f_{SW}} \quad \text{(eq. 34)}$$

The modulator and filter gain, compensation gain, and close loop gain asymptotic Bode plot can be drawn by the calculated results to check the compensation gain and close loop gain obtained. An example of asymptotic Bode plot is shown in Figure 40.

The phase of the output filter can be calculated by:

$$Phase_{(Filter)} = -\tan^{-1}(2\pi f \times ESR \times C_{OUT}) - \tan^{-1}\left(\frac{2\pi f \times ESR + DCR \times C_{OUT}}{2\pi f^2 \times L \times C_{OUT} - 1}\right) \quad \text{(eq. 35)}$$

where the DCR of the inductor can be neglected if the DCR is small.

The phase of the Type III compensation network can be calculated by:

$$Phase_{(TypeIII)} = -90^\circ + \tan^{-1}(2\pi f \times R_3 \times C_2) - \tan^{-1}\left(2\pi f \times R_3 \times \frac{C_1 \times C_2}{C_1 + C_2}\right) + \tan^{-1}(2\pi f \times (R_1 + R_4) \times C_3) - \tan^{-1}(2\pi f \times R_4 \times C_3) \quad \text{(eq. 36)}$$

The close loop phase can be calculated by summing the filter phase and compensation phase:

$$Phase_{(CloseLoop)} = Phase_{(Filter)} + Phase_{(TypeIII)} \quad \text{(eq. 37)}$$

Then the close loop phase margin can be estimated by:

$$Phase_{(Margin)} = Phase_{(CloseLoop)} - (-180^\circ) \quad \text{(eq. 38)}$$

It should be checked that closed loop gain has a 0 dB gain crossing with −20 dB/decade slope and a phase margin of 45° or greater. The compensation components values may require some adjustment to meet these requirements. Besides, the compensation gain should be checked with the error amplifier open loop gain to make sure that it is bounded by the error amplifier open loop gain.

The poles and zeros locations and hence the compensation network components values may need to be further fine tuned after actual system testing and analysis.

Feedback Resistor Divider

The output voltage of the buck regulator can be adjusted by the feedback resistor divider formed by R_1 and R_2. Once the value of R_1 is selected when determining the compensation components, the value of R_2 can be obtained by:

$$R_2 = \frac{0.8 \times R_1}{V_{OUT} - 0.8} \quad \text{(eq. 39)}$$

It is recommended to adjust the value of R_2 to fine−tune the output voltage when it is necessary. The value of R_1 should not be changed since the compensation DC gain and the 2nd zero break frequency of the compensation gain are contributed by R_1. If the value of R_1 is changed, the compensation, the close loop bandwidth and phase margin, and the system stability will be affected. Besides, it is recommended to use resistors with at least 1% tolerance for R_1 and R_2.

Soft−Start of Buck Regulator

A VDDQ soft−start feature is incorporated in the device to prevent surge current from power supply and output voltage overshoot during power up. When VDDQEN, VCCA, and VOCDDQ rise above their respective upper threshold voltages, the external soft−start capacitor C_{SS} will be charged up by a constant current source, I_{ss}. When the soft−start voltage (Vcss) rises above the SS_EN voltage (∼50 mV), the BGDDQ and TGDDQ will start switching and VDDQ output will ramp up with VFBDDQ following the soft−start voltage. When the soft−start voltage reaches the SS_OK voltage (∼Vref + 50 mV), the soft−start of

VDDQ is finished. The C_{ss} will continue to charge up until it reaches about 2.5 V to 3.0 V.

The soft−start time t_{ss} can be programmed by the soft−start capacitor according to the following equation:

$$t_{SS} \approx \frac{0.8 \times C_{SS}}{I_{SS}} \quad \text{(eq. 40)}$$

Ceramic capacitors with low tolerance and low temperature coefficient, such as B, X5R, X7R ceramic capacitors are recommended to be used as the C_{SS}. Ceramic capacitors with Y5V temperature characteristic are not recommended.

Soft−Start of VTT Active Terminator

The VTT source current limit is used as a constant current source to charge up the VTT output capacitor during VTT soft−start. Besides, the VTT source current limit is reduced to about 1.0 A for 128 internal clock cycles to minimize the inrush current during VTT soft−start. Therefore, the VTT soft−start time t_{SSVTT} can be estimated by the equation:

$$t_{SSVTT} \approx \frac{C_{OUTVTT} \times VTT}{I_{LIMVTSS}} \quad \text{(eq. 41)}$$

where C_{OUTVTT} is the capacitance of VTT output capacitor and $I_{LIMVTSS}$ is the VTT soft−start source current limit.

Boost Supply Diode and Capacitor

An external diode and capacitor are used to generate the boost voltage for the supply of the high−side gate driver of the bulk regulator. Schottky diode with low forward voltage should be used to ensure higher floating gate drive voltage can be applied across the gate and the source of the high−side MOSFET. A Schottky diode with 30 V reverse voltage and 0.5 A DC current ratings can be used as the boost supply diode for most applications. A 0.1 μF to 0.22 μF ceramic capacitor should be sufficient as the boost capacitor.

VTTI Input Power Supply for VTT and VTTR

Both VTT and VTTR are supplied by VTTI for sourcing current. VTTI is normally connected to the VDDQ output for optimum performance. If VTTI is connected to VDDQ, no bypass capacitor is required to add to VTTI since the bulk capacitor at VDDQ output is sufficiently large. Besides, the maximum load current of VDDQ is the sum of $I_{VDDQ(max)}$ and $I_{VTT(max)}$ when making electrical design and components selection of the VDDQ buck regulator. VTTI can also be connected to an external voltage source. However, extra power dissipation will be generated from the internal VTT high−side MOSFET and more heatsinking is required if the external voltage is higher than VDDQ. Whereas, the headroom will be limit by the $R_{DS(on)}$ of the VTT linear regulator high−side MOSFET, and the maximum VTT output current with VTT within regulation window will also be reduced if the external voltage is lower than VDDQ. Besides, the VTTI pin input must be bypassed to VTTGND with at least a 10 μF capacitor if external voltage source is used.

Design Example

A design example of a VDDQ bulk converter with the following design parameters is shown below:

DDR2 VDDQ bulk converter design parameters:

1. Input voltage range: 7.0 V to 20 V.
2. Nominal V_{OUT}: 1.8 V.
3. Static tolerance: 2% ($\pm$36 mV).
4. Transient tolerance: $\pm$100 mV.
5. Maximum output current: 10 A ($I_{VDDQ(max)}$ = 8.0 A, $I_{VTT(max)}$ = 2.0 A).
6. Load transient step: 1.0 A to 8.0 A.
7. Switching frequency: 400 kHz.
8. Bandwidth: 100 kHz.
9. Soft−start time: 400 μs.

a. Calculate input capacitor rms ripple current rating and voltage rating:

$$I_{CIN(RMS)} \geq 10\ A \times \sqrt{\frac{1.836\ V}{8.0\ V} - \left(\frac{1.836\ V}{8.0\ V}\right)^2} = 4.2\ A \quad \text{(eq. 42)}$$

$$V_{CIN(rating)} \geq 20 \times 1.25\ V = 25\ V \quad \text{(eq. 43)}$$

Therefore, two 10 μF 25 V ceramic capacitors with 1210 size in parallel are used.

b. Calculate inductance, rated current and DCR of inductor:

First, suppose ripple current is 0.3 times the maximum output current, such that:

$$L \geq \frac{(20\ V - 1.836\ V) \times 1.836\ V}{0.3 \times 10\ A \times 20\ V \times 400\ kHz} = 1.39\ \mu H \quad \text{(eq. 44)}$$

Second, the overshoot requirement at load release is then considered and supposes two 220 μF capacitors in parallel are used as an initially guess, such that:

$$L \leq \frac{440\ \mu F \times ((100\ mV + 1.836\ V)^2 - (1.836\ V)^2)}{\left(7\ A + \frac{0.3 \times 7\ A}{2}\right)^2} = 2.56\ \mu H \quad \text{(eq. 45)}$$

Thus, inductors with standard inductance values of 1.5 μH, 1.8 μH and 2.2 μH can be used. As a trade−off between smaller overshoot and better efficiency, the average value of 1.8 μH inductor is selected.

Then, the maximum rated DC current is calculated by:

$$I_{L(rated)} = 1.2 \times \left(10\ A + \frac{(20\ V - 1.836\ V) \times 1.836\ V}{2 \times 1.8\ \mu H \times 400\ kHz \times 20}\right) = 13.39\ A \quad \text{(eq. 46)}$$

Therefore, inductor with maximum rated DC current of 14 A or larger can be used.

Finally, the DCR of inductor is 2.0 mΩ per μH of inductance as a rule of thumb, then:

$$DCR = \frac{2\ m\Omega}{1\ \mu H} \times 1.8\ \mu H = 3.6\ m\Omega \quad \text{(eq. 47)}$$

Thus, inductor with 1.8 μH inductance, 14 A maximum rated DC current and 3.5 mΩ DCR is chosen.

c. Calculate ESR and capacitance of output filter capacitor:

First, the ESR required to achieve the desired output ripple voltage is considered. Suppose the output ripple voltage is 2% of the nominal output voltage.

$$ESR \le \frac{(0.02 \times 1.8\ V) \times 1.8\ \mu H \times 400\ kHz \times 20\ V}{(20\ V - 1.8\ V) \times 1.8\ V} = 15.8\ m\Omega \quad \text{(eq. 48)}$$

Second, the ESR required to meet the transient load undershoot requirement is considered, such that:

$$ESR \le \frac{100\ mV}{7\ A} = 14.3\ m\Omega \quad \text{(eq. 49)}$$

Therefore, the suitable ESR is 12 mΩ or smaller, and the value of 7.5 mΩ is selected for more design margin and better performance. Then, two same SP−Caps or POSCAPs each with 15 mΩ ESR in parallel having a resultant ESR of 7.5 mΩ should be good enough to meet the requirements.

Then, check that whether the previously supposed capacitance meets the undershoot and overshoot requirements.

To ensure that undershoot requirement of less than 100 mV is achieved, the capacitance must be:

$$C_{OUT} \ge \frac{7\ A}{100\ mV - 7\ A \times 7.5\ m\Omega} \times \left(\frac{\left(1 - \frac{1.8\ V - 36\ mV}{20\ V}\right)}{400\ kHz} \right) = 335.9\ \mu F \quad \text{(eq. 50)}$$

To make sure that overshoot requirement of less than 100 mV is fulfilled, capacitance must be:

$$C_{OUT} \ge \frac{1.8\ \mu H \times \left(7\ A + \frac{(20\ V - 1.836\ V) \times 1.836\ V}{2 \times 1.8\ \mu H \times 400\ kHz \times 20\ V}\right)^2}{(100\ mV + 1.836\ V)^2 - (1.836\ V)^2} = 317.6\ \mu F \quad \text{(eq. 51)}$$

Therefore, output capacitor with capacitance of 440 μF should meet both undershoot and overshoot requirements. Sometimes, it may take several times of iterations between the process of selecting inductance of the inductor and ESR and capacitance of the output capacitor.

Then, the voltage rating of the output capacitor is estimated by:

$$V_{rated} \ge 1.25 \times 1.836\ V = 2.3\ V \quad \text{(eq. 52)}$$

Thus, output capacitor with 2.5 V or larger rated voltage is used.

Finally, the rated rms ripple current of the output capacitor is considered:

$$I_{COUT(rms)} \ge \frac{(20\ V - 1.836\ V) \times 1.836\ V}{1.8\ \mu H \times 400\ kHz \times 20\ V} = 2.3\ A \quad \text{(eq. 53)}$$

Thus, capacitor with rated rms ripple current of 3.0 A or larger should be selected. Two capacitors each with 1.5 A rated ripple current can be connected in parallel to provide a total of 3.0 A rated rms ripple current.

Therefore, two same capacitors in parallel each with capacitance of 220 μF, ESR of 15 mΩ, rated voltage of 2.5 V, and rated rms ripple current of 1.5 A are used.

d. Calculate the resistance value of OCP current limit setting resistor:

First, the OCP current limit is estimated at maximum load condition, such that:

$$I_{LIMIT} > 8\ A + 2\ A + \frac{(20\ V - 1.836\ V) \times 1.836\ V}{2 \times 1.8\ \mu H \times 400\ kHz \times 20\ V} = 11.16\ A \quad \text{(eq. 54)}$$

Thus, I_{LIMIT} is set to 11.5 A. Suppose from the high−side MOSFET data sheet, the maximum $R_{DS(on)}$ is 10 mΩ.

Then, the value of RL1 is calculated by:

$$RL1 = \frac{11.5\ A \times 10\ m\Omega}{26\ \mu A} = 4.4\ k\Omega \quad \text{(eq. 55)}$$

Therefore, the resistor with standard value of 4.7 kΩ is selected for RL1.

e. Calculate the RC values of the compensation network:

First, 4.3 kΩ is chosen as the value of R_1 which is in the range between 2.0 kΩ and 5.0 kΩ.

Since the worst case of stability is at the maximum V_{IN}, the close loop compensation should be considered at maximum V_{IN}. Then the ramp amplitude can be calculated as below:

$$V_{RAMP} = 1.25\ V + 0.045 \times (20\ V - 5\ V) = 1.925\ V \quad \text{(eq. 56)}$$

Since the L = 1.8 μH, C_{OUT} = 440 μF, and the target close loop bandwidth is 100 kHz, the value of R_3 can be calculated as:

$$R_3 = \frac{2\pi \times 100\ kHz \times 1.925\ V \times 4.3\ k\Omega \times \sqrt{1.8\ \mu H \times 440\ \mu F}}{20\ V} = 7.3\ k\Omega \quad \text{(eq. 57)}$$

Thus, standard value of 7.5 kΩ is selected for R_3.

If the first zero break frequency is placed at half the LC filter's double pole, the value of C_2 can be calculated by:

$$C_2 = \frac{2 \times \sqrt{1.8\ \mu H \times 440\ \mu F}}{7.5\ k\Omega} = 7.5\ nF \quad \text{(eq. 58)}$$

Thus, standard value of 8.2 nF is chosen for C2.

If the 1st pole break frequency is placed at the LC filter's ESR zero, the value of C_1 can be calculated by:

$$C_1 = \frac{8.2\ nF}{\frac{7.5\ k\Omega \times 8.2\ nF}{7.5\ m\Omega \times 440\ \mu F} - 1} = 464.9\ pF \quad \text{(eq. 59)}$$

Thus, standard value of 470 pF can be chosen for C_1. However, 180 pF is selected for more phase boost at the 0 dB gain crossing.

Then, if the second zero break frequency is placed at the LC filter's double pole and the second pole is placed at half the switching frequency, the value of R_4 can be calculated by:

$$R_4 = \frac{4.3\ k\Omega}{\pi \times 400\ kHz \times \sqrt{1.8\ \mu H \times 440\ \mu F} - 1} = 125\ \Omega \quad \text{(eq. 60)}$$

Thus, standard value of 130 Ω is selected for R_4.

Then, C_3 can be calculated by:

$$C_3 = \frac{1}{\pi \times 130\ \Omega \times 400\ kHz} = 6.12\ nF \quad \text{(eq. 61)}$$

Therefore, standard value of 5.6 nF is selected for C_3.

Then, the close loop phase margin can be estimated by the following:

$$\begin{aligned} Phase_{(Filter)} &= -\tan^{-1}(2\pi \times 100\ kHz \times 7.5\ m\Omega \times 440\ \mu F) \\ &\quad -\tan^{-1}\left(\frac{2\pi \times 100\ kHz \times 7.5\ m\Omega}{2\pi \times (100\ kHz)^2 \times 1.8\ \mu H \times 440\ \mu F - 1}\right) \\ &= -153.66^\circ \end{aligned}$$

$$\begin{aligned} Phase_{(TypeIII)} &= -90 + \tan^{-1}(2\pi \times 100\ kHz \times 7.5\ k\Omega \times 8.2\ nF) \\ &\quad -\tan^{-1}\left(2\pi \times 100\ kHz \times 7.5\ k\Omega \times \frac{180\ pF \times 8.2\ nF}{180\ pF + 8.2\ nF}\right) \\ &\quad + \tan^{-1}(2\pi \times 100\ kHz \times (4.3\ k\Omega + 130\ \Omega) \times 5.6\ nF) \\ &\quad -\tan^{-1}(2\pi \times 100\ kHz \times 130\ \Omega \times 5.6\ nF) \\ &= 20.57^\circ \end{aligned} \quad \text{(eq. 62)}$$

$$Phase_{(closeloop)} = -153.66^\circ + 20.57^\circ = -133.09^\circ$$

$$Phase_{(margin)} = Phase_{(closeloop)} - (-180^\circ) = -133.09^\circ - (-180^\circ) = 46.91^\circ$$

Therefore, the phase margin is large enough for stability.

f. Calculate the resistance value of feedback resistor divider:

Since a 4.3 kΩ resistor is chosen as the high−side resistor R_1, the resistance value of low−side resistor R_2 can be calculated by:

$$R_2 = \frac{0.8 \times 4.3\ k\Omega}{1.8\ V - 0.8\ V} = 3.44\ k\Omega \quad \text{(eq. 63)}$$

Therefore, a 3.44 kΩ resistor is selected for the low−side feedback resistor R_2.

g. Calculate soft−start capacitor value for the desired 400 μs VDDQ soft−start time:

$$C_{SS} = \frac{4.0\ \mu A \times 400\ \mu s}{0.8\ V} = 2.0\ nF \quad \text{(eq. 64)}$$

Therefore, 2.0 nF X5R ceramic capacitor is selected for the soft−start capacitor.

PCB Layout Guidelines

Cautious PCB layout design is very critical to ensure high performance and stable operation of the DDR power controller. The following items must be considered when preparing PCB layout:

1. All high−current traces must be kept as short and wide as possible to reduce power loss. High−current traces are the trace from the input voltage terminal to the drain of the high−side MOSFET, the trace from the source of the high−side MOSFET to the inductor, the trace from inductor to the VDDQ output terminal, the trace from the input ground terminal to the VDDQ output ground terminal, the trace from VDDQ output to VTTI pin, the trace from VTT pin to VTT output terminal, and the trace from VTT output ground terminal to the VTTGND pin. Power handling and heaksinking of high−current traces can be improved by also routing the same high−current traces in the other layers and joined together with multiple vias.
2. Power components which include the input capacitor, high−side MOSFET, low−side MOSFET and VDDQ output capacitor of the buck converter section must be positioned close together to minimize the current loop. The input capacitor must be placed close to the drain of the high−side MOSFET and the source of the low−side MOSFET.
3. To ensure the proper function of the device, separated ground connections should be used for different parts of the application circuit according to their functions. The input capacitor ground, the low−side MOSFET source, the VDDQ output capacitor ground, the VCCP decoupling capacitor ground should be connected to the PGND. The trace path connecting the source of the low−side MOSFET and PGND pin should be minimized. The VTT output capacitor ground should be connected to the VTTGND first with a short trace, it is then connected to the ground plane of PGND. The VCCA decoupling capacitor ground, the ground of the VDDQ feedback resistor, the soft−start capacitor ground, the VTTREF output capacitor ground should be connected to the AGND. The AGND pin is then connected directly through a sense trace to the remote ground sense point of the PGND, which is usually the ground of the local bypass capacitor for the load. Never connect the AGND, PGND and VTTGND together just under the thermal pad.
4. The thermal pad of the DFN−22 package should be connected to the ground planes in the internal layer and bottom layer from the copper pad at top layer underneath the package through six to eight vias with 0.6 mm hole−diameter to help heat dissipation and ensure good thermal capability. It is recommended to use PCB with 1 oz or 2 oz copper foil. The thermal pad can be connected to either PGND ground plane or AGND ground plane but not both.
5. The input capacitor ground terminal, the VDDQ output capacitor ground terminal and the source of the low−side MOSFET must be connected to the PGND ground plane through multiple vias.
6. Sensitive traces like trace from FBDDQ, trace from COMP, trace from OCDDQ, trace from FBVTT and trace from VTTREF should be avoided from the high−voltage switching nodes like SWDDQ, BOOST, TGDDQ and BGDDQ.
7. Separate sense trace should be used to connect the VDDQ point of regulation, which is usually the local bypass capacitor for load, to the feedback resistor divider to ensure accurate voltage sensing. The feedback resistor divider should be place close to the FBDDQ pin.
8. Separate sense trace should be used to connect the VTT point of regulation, which is usually the local bypass capacitor for load, to the FBVTT pin.
9. Separate sense trace should be used to connect the VDDQ point of regulation to the DDQREF pin to ensure that the reference voltage to VTT is accurately half of the VDDQ voltage.
10. The traces length between the gate driver outputs and gates of the MOSFETs must be minimized to avoid parasitic impedance.
11. To ensure normal function of the device, an RC filter should be placed close to the VCCA pin and a decoupling capacitor should be placed close to the VCCP pin.
12. The copper trace area of the switching node which includes the source of the high−side MOSFET, drain of the low−side MOSFET and high voltage side of the inductor should be minimized by using short wide trace to reduce EMI.
13. A snubber circuit consists of a 3.3 Ω resistor and 1.0 nF capacitor may need to be connected across the switching node and PGND to reduce the high−frequency ringing occurring at the rising edge of the switching waveform to obtain more accurate inductor current limit sensing of the VDDQ buck converter. However, adding this snubber circuit will slightly reduce the conversion efficiency.
14. VTTI should be connected to VDDQ output with wide and short trace if VDDQ is used as the sourcing supply for VTT. An input capacitor of at least 10 μF should be added close to the VTTI pin and bypassed to VTTGND if external voltage supply is used as the VTT sourcing supply.

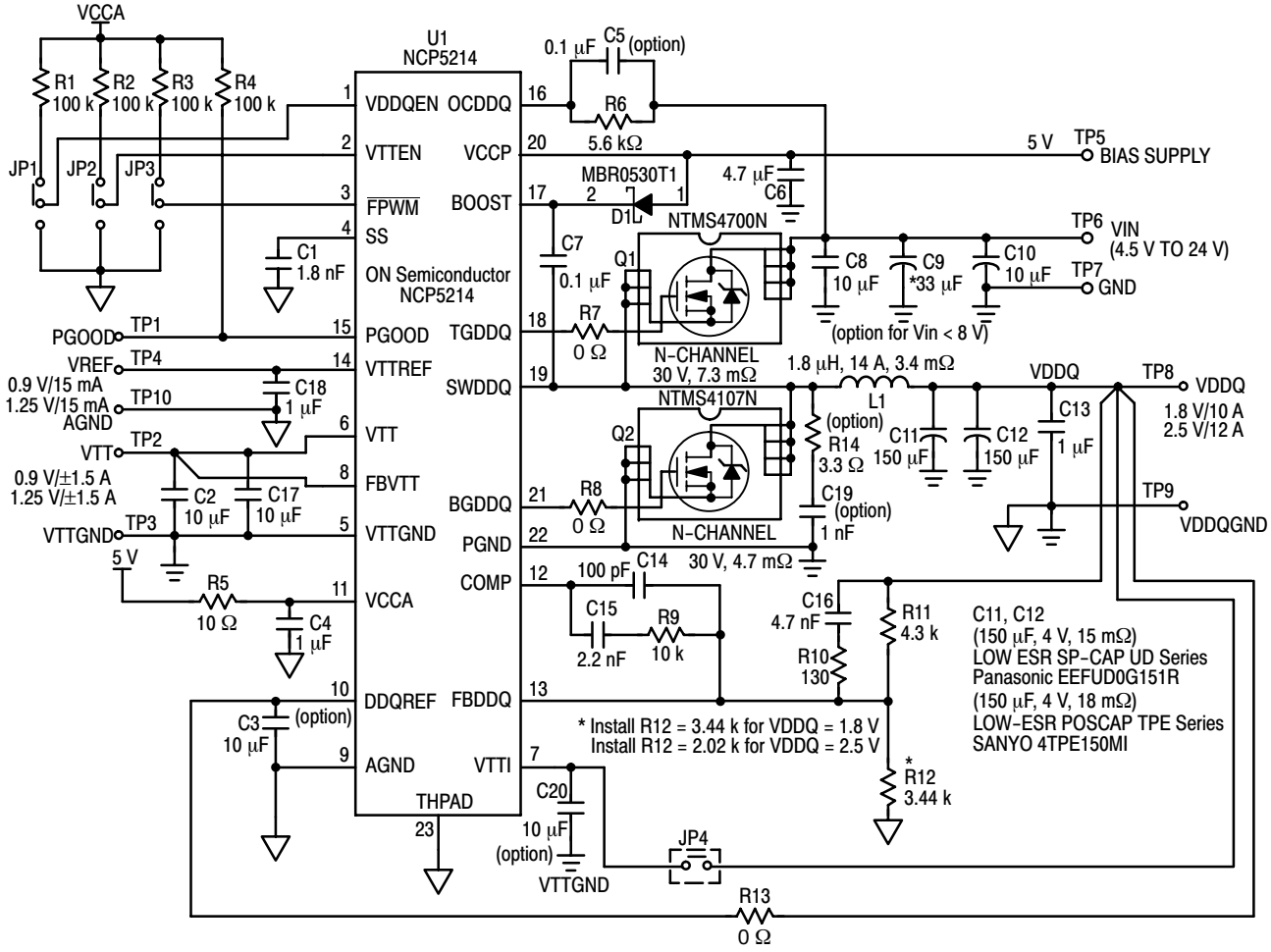


Figure 41. Schematic Diagram of Evaluation Board

PCB Layout of Evaluation Board

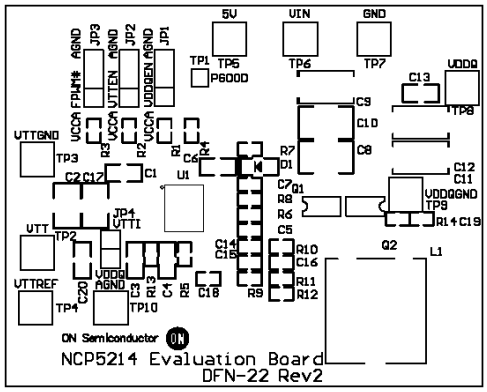


Figure 42. Silkscreen of Evaluation Board PCB

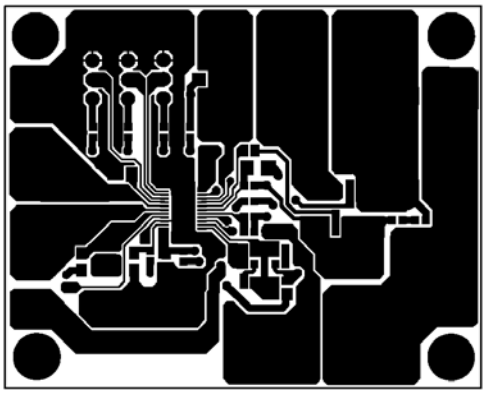


Figure 43. Top Layer of Evaluation Board PCB Layout

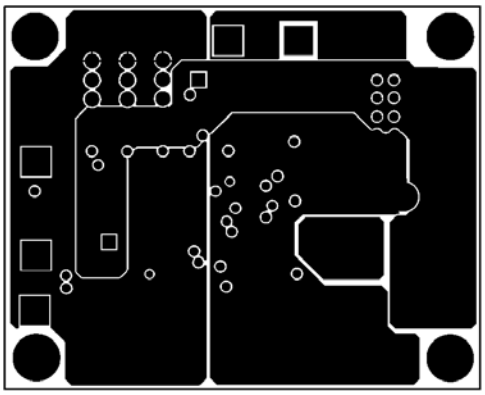


Figure 44. Middle Layer1 of Evaluation Board PCB Layout

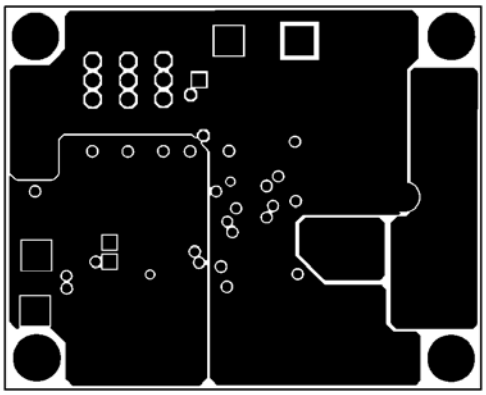


Figure 45. Middle Layer2 of Evaluation Board PCB Layout

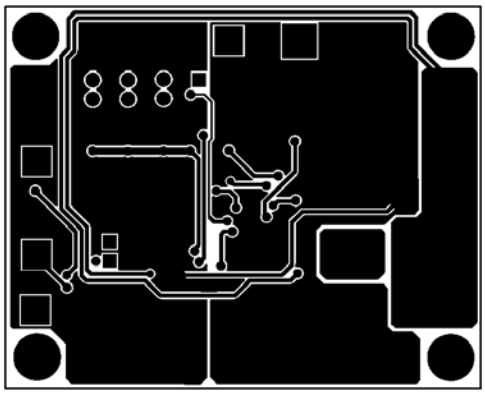


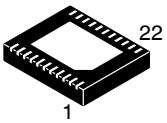
Figure 46. Bottom Layer of Evaluation Board PCB Layout

Table 2. Bill of Materials of the Evaluation Board

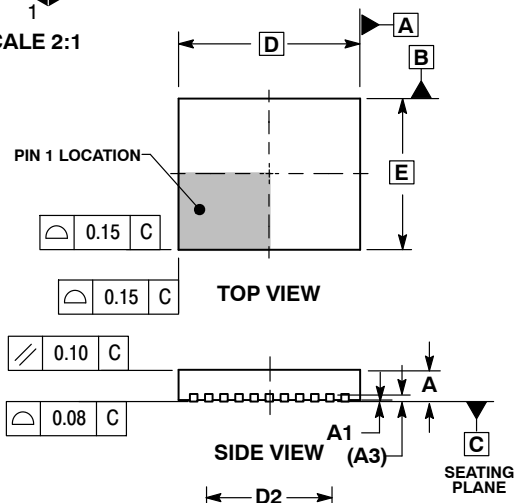
Item	Qty	Designators	Part Description	Mfg. & P/N	Remark
1	1	C1	Capacitor, Ceramic, 1.8 nF/50 V 0603	Panasonic ECJ1VB1H182K	
2	2	C2, C17	Capacitor, Ceramic, 10 μF/6.3 V 0805	Panasonic ECJ2FB0J106M	
3	2	C3, C20	Capacitor, Ceramic, 10 μF/6.3 V 0805	Panasonic ECJ2FB0J106M	C3 & C20 are optional
4	3	C4, C13, C18	Capacitor, Ceramic, 1 μF/10 V 0805	Panasonic ECJ1VB1A105M	
5	2	C5, C7	Capacitor, Ceramic, 0.1 μF/25 V 0603	Panasonic ECJ1VB1E104K	C5 is optional
6	1	C6	Capacitor, Ceramic, 4.7 μF/10 V 0603	Panasonic ECJ2FB1C475M	
7	2	C8, C10	Capacitor, Ceramic, 10 μF/25 V 1210	Panasonic ECJ4YB1E106M	
8	1	C9	Capacitor, Electrolytic, 33 μF/35 V Size D	Panasonic EEVFK1V330P	C9 is optional
9	2	C11, C12	Capacitor, SP−CAP, 150 μF/4 V Size D / Capacitor, POSCAP, 150 μF/4 V Size D	Panasonic EEFUD0G151R / Sanyo 4TPE150MI	
10	1	C14	Capacitor, Ceramic, 100 pF/50 V 0603	Panasonic ECJ1VC1H101K	
11	1	C15	Capacitor, Ceramic, 2.2 nF/50 V 0603	Panasonic ECJ1VB1H222K	
12	1	C16	Capacitor, Ceramic, 4.7 nF/50 V 0603	Panasonic ECJ1VB1H472K	
13	1	C19	Capacitor, Ceramic, 1 nF/50 V 0603	Panasonic ECJ1VB1H102K	C19 is optional
14	1	D1	Diode, 0.5 A 30 V schottky SOD−123	ON Semiconductor MBR0530T1	
15	3	JP1, JP2, JP3	Header, 3−pin, 100 mil spacing	Any	
16	1	JP4	Header, 2−pin, 100 mil spacing	Any	
17	1	L1	Inductor, SMD, 1.8 μH/14 A / Inductor, SMD, 1.5 μH/17 A	Panasonic ETQP2H1R8BFA / TOKO FDA1055−1R5M=P3	
18	1	Q1	MOSFET, N−Channel SO−8, 30 V/14.5 A	ON Semiconductor NTMS4700N	
19	1	Q2	MOSFET, N−Channel SO−8, 30 V/19 A	ON Semiconductor NTMS4107N	
20	4	R1, R2, R3, R4	Resistor, 100 kΩ 5% 0603	Panasonic ERJ3GEYJ104V	
21	1	R5	Resistor, 10 Ω 5% 0603	Panasonic ERJ3GEYJ100V	
22	1	R6	Resistor, 5.6 kΩ 1% 0603	Panasonic ERJ3EKF5602V	
23	1	R7	Resistor, 0 Ω 5% 0603	Panasonic ERJ3GEYJ0R0V	
24	2	R8, R13	Resistor, 0 Ω 5% 0603	Panasonic ERJ3GEYJ0R0V	
25	1	R9	Resistor, 10 kΩ 1% 0603	Panasonic ERJ3EKF1002V	
26	1	R10	Resistor, 130 Ω 1% 0603	Panasonic ERJ3EKF1300V	
27	1	R11	Resistor, 4.3 kΩ 1% 0603	Panasonic ERJ3EKF4301V	
28	1	R12	Resistor, 3.44 kΩ 1% 0603	Panasonic ERJ3EKF3441V	
29	1	R14	Resistor, 3.3 Ω 5% 0603	Panasonic ERJ3GEYJ3R3V	R14 is optional
30	8	TP1 − TP8	Header, single pin	Any	
31	1	U1	2−in−1 Notebook DDR Power Controller	ON Semiconductor NCP5214	
32	4		Shunt, 100 mil jumper	Any	
33	1		Test Pin, 0.7 mm Diameter, 12 mm Height	Any	Place at the GND between C11 and C8
34	4		Bumpon, 4.44 x 0.20 transparent	3M	
35	1		4−layered PCB 2500 mil x 2000 mil	Any	

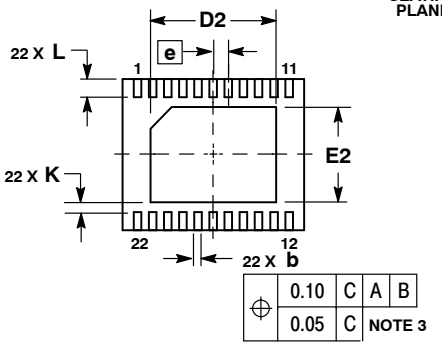
DFN22 6x5x0.9 MM, 0.5 P
CASE 506AF
ISSUE A

DATE 15 AUG 2005



SCALE 2:1



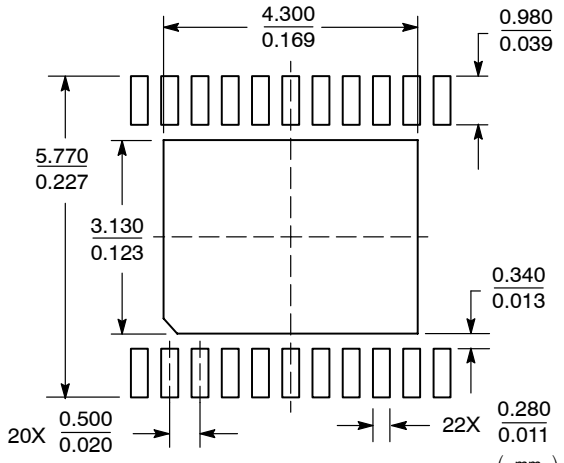


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

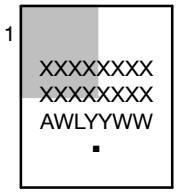
	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	3.98	4.28
E	5.00 BSC	
E2	2.98	3.28
e	0.50 BSC	
K	0.20	---
L	0.50	0.60

SOLDERING FOOTPRINT



SCALE 8:1 (mm / inches)

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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