User's Manual
SYG-70CP-BA &
SYG-70CR-BA



Future Designs, Inc.
Your Development Partner
996 A Cleaner Way, Huntsville, AL 35805

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1 SYG-70CP-BA and SYG-70CR-BA Overview

1.1 Introduction

The Future Designs, Inc. ΣyG™ (pronounced "sig") Family provides a complete and qualified Graphical User Interface (GUI) / Human Machine Interface (HMI) platform for the rapid release of customer products. The core of ΣyG is Renesas Synergy™ – a comprehensive and integrated software-based microcontroller platform. FDI adds the Synergy platform to its GUI hardware, systems, and production expertise. The result is a sum of high-quality products that provide a robust and proven source for GUI and HMI solutions:

ΣyG = Renesas Synergy+ GUI

1.2 ESD Warning

The SYG-70CP-BA and SYG-70CR-BA are shipped in a protective anti-static package. Do not subject the module to high electrostatic potentials. Exposure to high electrostatic potentials may cause damage to the boards that will not be covered under warranty. General practice for working with static sensitive devices should be followed when working with the kit.



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1.3 Calibrating the Touch Screen

Upon first booting the Out of Box (OOB) Demo, Sensor to Cloud, the board will prompt for touch screen calibration. Once calibration is complete, the calibration data is saved into the non-volatile data storage where it is accessed by other programs later. This data persists through power loss so that calibrating will not be necessary on subsequent boots. Reference section 10.3.1 for organization and location of this data.

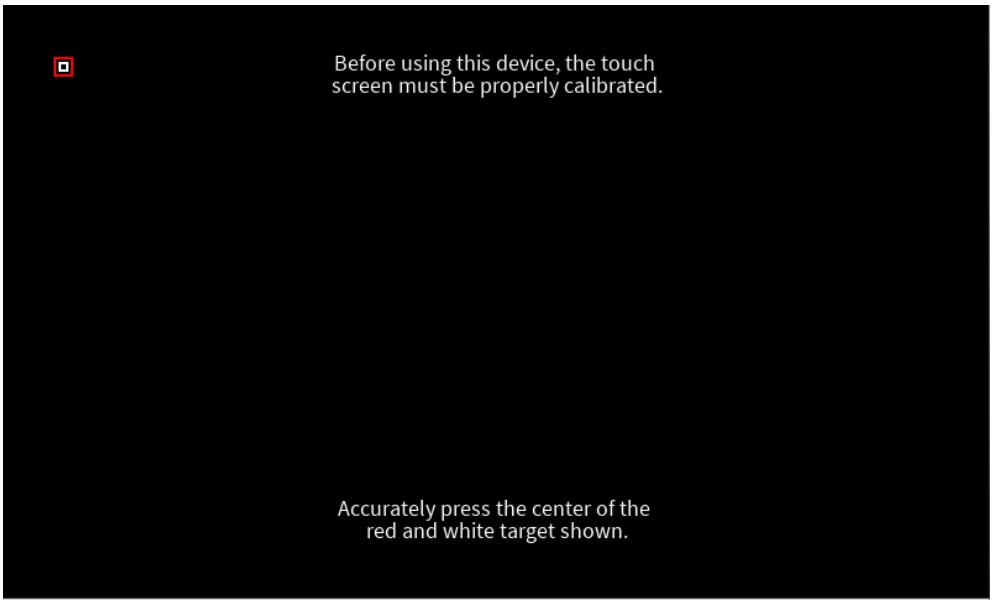


Figure 1 – Calibration Screen

The screen can be calibrated again at any time by pressing the "Calibration" button on the Status screen.

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Figure 2 – Status Screen

1.4 SYG-70CP-BA Block Diagram

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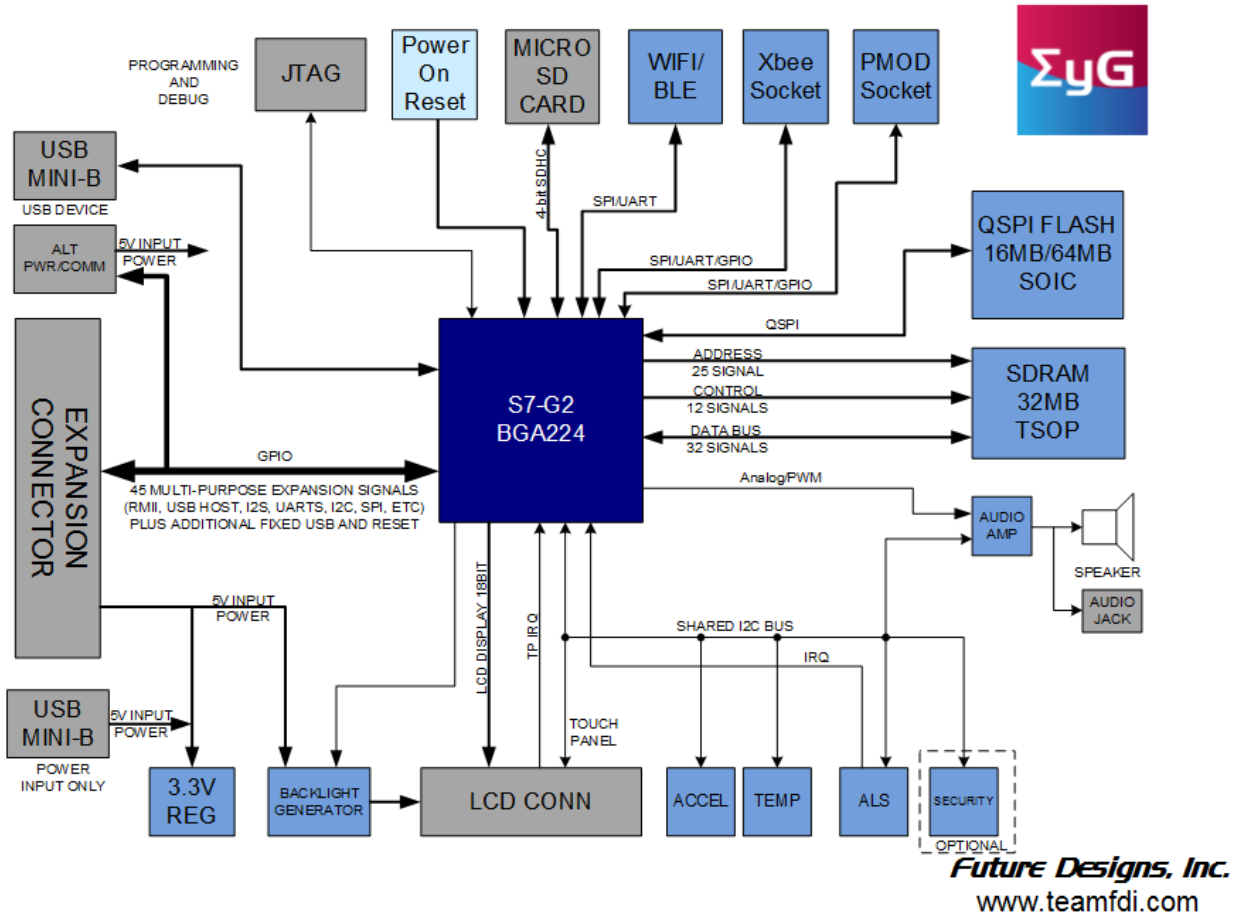


Figure 3 - SYG-70CP-BA Block Diagram

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1.5 SYG-70CR-BA Block Diagram

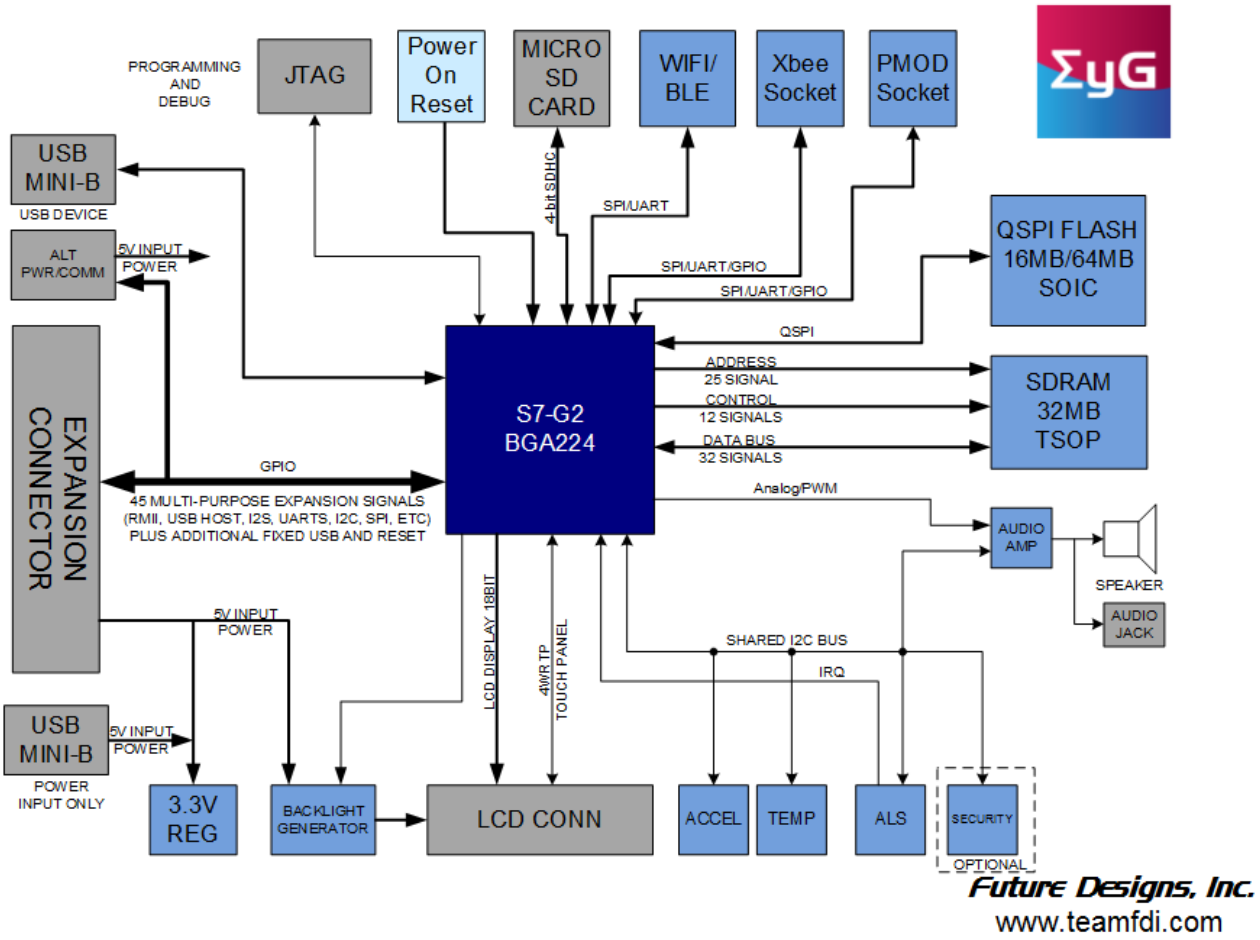


Figure 4 - SYG-70CR-BA Block Diagram

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Board Layout

1.6 Component Layout

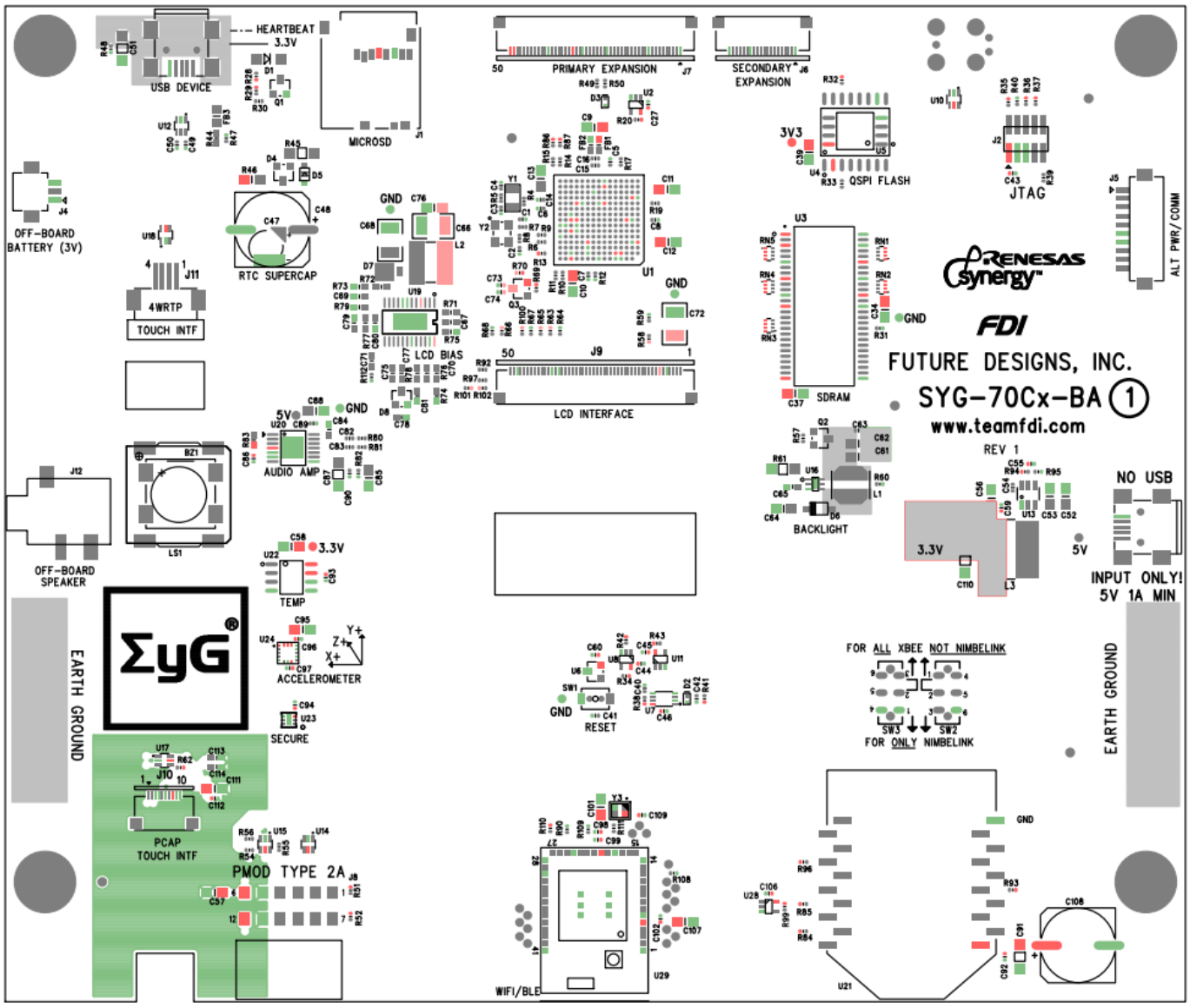


Figure 5 - Component Layer (Top)

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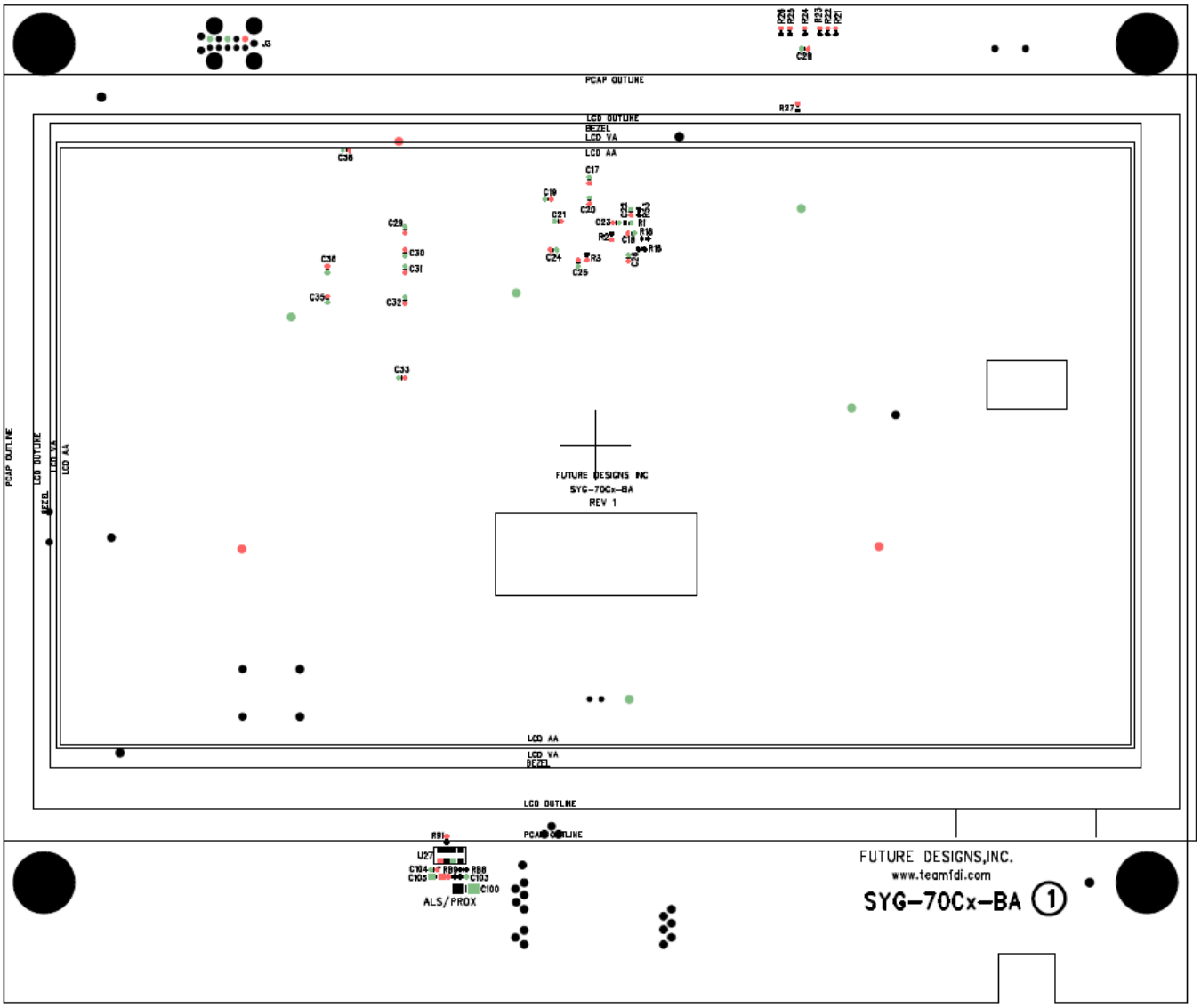


Figure 6 – Component Layer (Bottom)

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1.7 Specifications

1.7.1 Display Specifications

Screen Size (inches)		7
Touch Screen Type	**SYG-70CP-BA**	PCAP
	SYG-70CR-BA	4-Wire Resistive
Display Technology		a-si TFT
Brightness (nits typ)	**SYG-70CP-BA**	300
	SYG-70CR-BA	280
Resolution		800x480 (WVGA)
Contrast Ratio (typ)		500:1
Aspect Ratio		15:9
Colors		262k (18 bit)
Pixel Pitch (W x H mm)		0.179 x 0.1926
Viewing Angles (U/D L/R)	**SYG-70CP-BA**	60/70° 70/70°
	SYG-70CR-BA	50/70° 70/70°
Surface Finish		Anti-glare
Touch Panel Hardness	**SYG-70CP-BA**	5H
	SYG-70CR-BA	3H
Active Area (W x H mm)	**SYG-70CP-BA**	154.08 x 85.95
	SYG-70CR-BA	154.08 x 85.92
Response Time (ms typ)		25 Tr / 25 Tf
Backlight LEDs		24 (3S x 8P)
Backlight Life (hrs)		20k
Backlight Power Consumption (mW typ)		1536

1.7.2 Microcontroller and Memory Specifications

MCU (Microcontroller)	Renesas S7G2
Microcontroller Family	S7
Microcontroller Clock (MHz)	240
Microcontroller SRAM (KB)	640
Microcontroller Flash (KB)	4092
External Flash (MB)	16
External Flash Type	QSPI
Optional External Flash (MB)	64
External SDRAM (MB)	32
Optional External SDRAM (MB)	64
Non-volatile data storage (KB)	64

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1.7.3 Board Specifications

SD Card Interface	4-bit SD Card Interface
USB	Device
Accelerometer	Yes
Temp Sensor	Yes
Super Cap RTC Backup	Yes
Ambient Light Sensor	Yes
On-board Speaker	Yes
Headphone Jack	Yes
Additional Features	Wi-Fi, Wireless, Cellular, XBEE
Power Input	USB Device Mini-B or Hirose DF13 or Flex Cable
Input VDC	5
Power Consumption (mA typ/max)	800/955
Operating Temperature	-20° to 70° C
Storage Temperature	-30° to 80° C
JTAG	J-Link Lite CortexM-9 Debug Connector
Tag Connect	Yes
Expansion Connector	UART, I2C, SPI, USB Host/Device, RMII for Ethernet 10/100
Other Expansion Ports	UART, SPI, I2C, RTC Ext. Battery
Pmod Interface	Type 2A
Reverse Scan	None
Video Playback from microSD Interface	Yes
Mounting	#6 screws in 4 corners

1.7.4 Overall Specifications

Size (W x H x D mm)	170.18 x 143.64 x 14.70
Weight (grams)	275
RoHS Compliant	Yes

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1.8 Board Dimensions

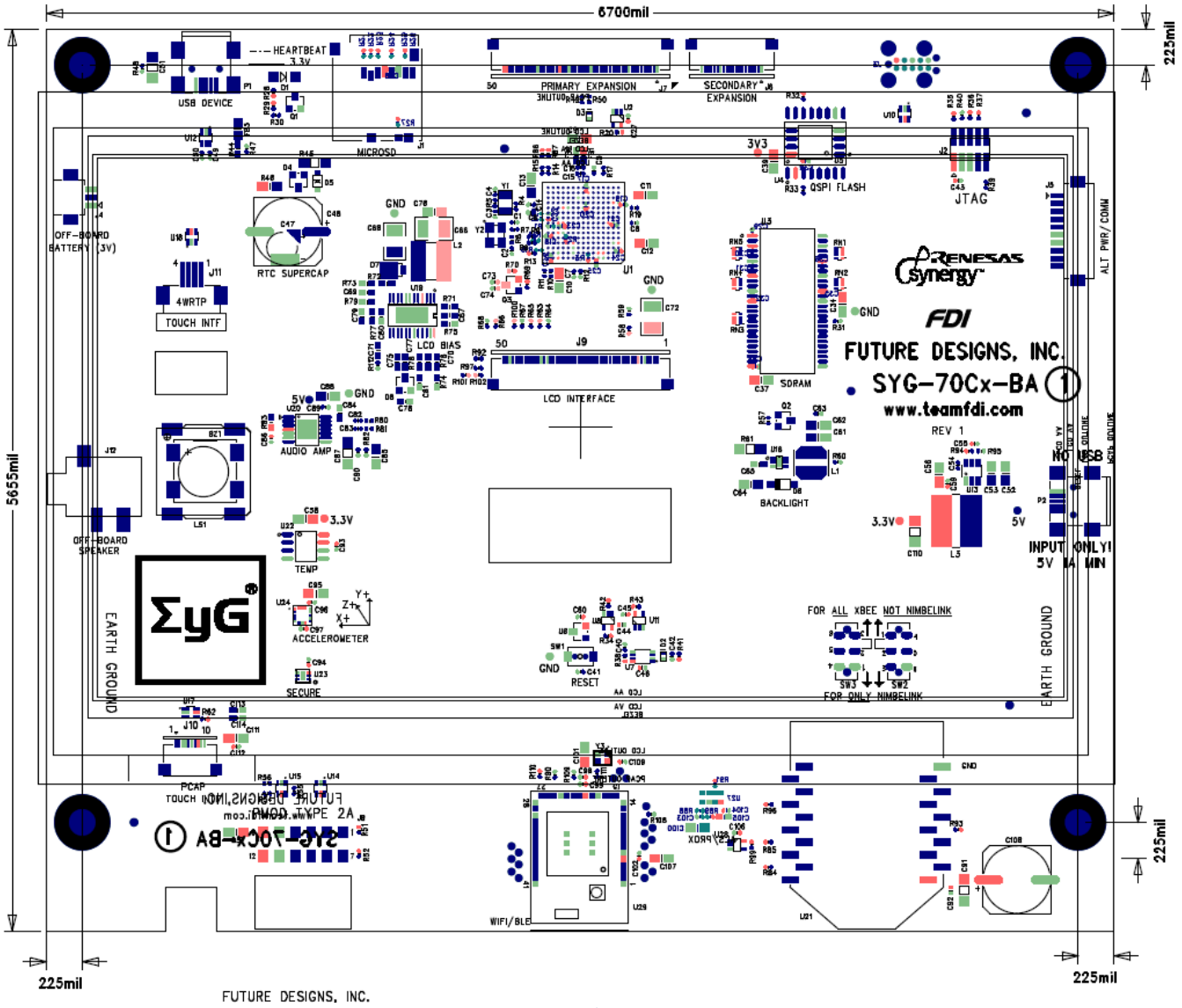


Figure 7- Board Dimensions

Note: Mounting holes are .167" in diameter and are not threaded, but do provide Earth Ground

Not Pictured: Total Height – 822 mil, Height off PCB – 319 mil

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2 Input Power Sources

The SYG-70CP-BA and SYG-70CR-BA can both be powered multiple ways depending on your requirements. The various power input methods are described below.

Input power requirements are 5V ±5%, 1 A minimum.

2.1 5V input via USB Mini-B (P2)

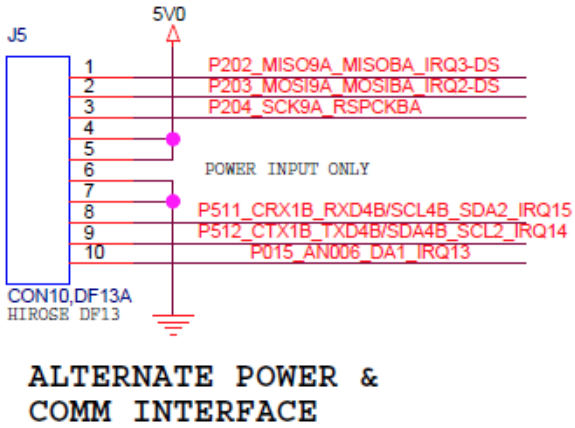
The most convenient power source available is the USB Mini-B connector. This connector is labeled "NO USB" "INPUT ONLY! 5V 1A MIN" so that it cannot be confused with the USB Mini-B Device port. No data is sent over this cable, it is strictly for powering the SYG-70CP.



2.2 Alternate Power Connection (J5)

The alternate power connector comes in the form of the DF13A-10P-1.25H connector. This connector accepts the DF13-10S-1.25C socket connector. Pins 4 and 5 accept 5V and pins 6 and 7 accept Ground. The remaining lines are for use with COMMs and will be described in the peripheral section of this manual.





ALTERNATE POWER & COMM INTERFACE

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2.3 Power Requirements

2.3.1 USB Power (P2)

Rating: +5VDC ±5%, 1A Minimum Input

+5VDC ±5% is the input power range specification. The +5VDC output level to either the Expansion Board connector or the 5V devices may be affected if the +5VDC input power is not within specifications.

- USB High Power Specifications are 500mA maximum, and 4.75V to 5.25V standard.
- USB Low Power Specifications are 100mA maximum, and 4.4V to 5.25V standard.

2.3.2 70-pin Expansion Connectors (J6 & J7)

Rating: **+5VDC ±5%, 300mA Maximum Output (1A Minimum if Input)**

The SYG-70CP-BA/SYG-70CR-BA can provide a maximum of 300mA of 3.3V power for "external use" over the expansion connectors J7 (50 pin) and J6 (20 pin).
If more than 300mA of 3.3V is needed for an expansion board:

- Then the primary power input (i.e. 5V) should be located on the expansion board rather than on the SYG-70CP
- The expansion board should include its own 3.3V voltage regulator
- Ensure the 3.3V voltage rails of the SYG-70CP-BA/SYG70CR-BA & Expansion Board are not connected.
- The SYG-70CP-BA/SYG-70CR-BA should be powered using 5V from the expansion board over the 70-pin breakout, instead of powering the expansion board from the SYG-70CP-BA/SYG-70CR-BA USB connector.

More information on this connector can be found in the Expansion Connectors section of this document.

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2.3.3 Alternate Power & Communication Interface Connector (J5)

Rating: +5VDC ±5%, 1A Minimum Input, 2A Maximum Input

Alternate Power/Communication Interface Connector, J7, is a great alternative to bringing external power onto the SYG-70CP-BA/SYG-70CR-BA in cases where the onboard power regulator isn't sufficient.

More information on this connector can be found in the 10 Pin Alternate Power & Comm Interface section of this document.

Note: This is a Power Input only connector. Do not use this connector to power an external device.

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3 Renesas Synergy S7G2 Microcontroller

The microcontroller unit (MCU) on the SYG-70CP-BA/SYG-70CR-BA is a 32-bit, 240 MHz, Cortex® M4 processor with 4 MB of internal flash and 640 KB of SRAM. MCUs from the Synergy family include qualified commercial-grade software to enable rapid development of applications which require a real-time operating system. The Synergy Software Package (SSP) integrates the full suite of Express Logic® software including the ThreadX RTOS and suite of X-Ware stacks. For more information on Renesas Synergy MCUs visit: https://www.renesas.com/en-us/products/synergy/features.html

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4 Development Tools

To develop applications for the SYG-70CP-BA/SYG-70CR-BA, it is highly recommended to use one of the two development environments provided with the purchase of SYG-70CP-BA and SYG-70CR-BA. All of the below software is available on the Renesas Synergy Gallery website and includes:

4.1 e2 studio

- The Renesas Synergy™ Platform's Eclipse-based e2 studio Integrated Solution Development Environment (ISDE) is your workbench, providing you all the tools you need to create differentiated applications for Synergy MCU devices.
- An open tool platform, the Eclipse CDT (C/C++ Development Tooling) standard allows plug-ins for many innovative tool functions. Renesas engineers created solution-based plug-ins for Synergy that guide the design process in three intuitive phases covering Synergy MCUs and software – the Preparation Phase, the Build Phase, and the Debug Phase.

4.2 IAR Embedded Workbench® for Synergy

- IAR Embedded Workbench, the worlds most widely used embedded development environment, is now completely integrated with the Renesas Synergy™ Platform. The new product IAR EW for Synergy provides add-on functionality to simplify and accelerate software development, and provide the best performance and smallest code size. Renesas created the Synergy Standalone Configurator (SSC) which is available to IAR EW for Synergy users as a separate download. The SSC includes the Synergy Project Generator as well as the Synergy Project Editor, including configurators like the Clock Configurator, Pin Configurator, RTOS Configurator, and SSP Module Selector/Configurator.

4.3 Synergy Software Package (SSP)

- Part of the Renesas Synergy™ Platform, the Synergy Software Package (SSP) features software that has been integrated, optimized, tested, and qualified by Renesas for Synergy users – and is also maintained and warranted by Renesas on an ongoing basis.
- The SSP includes the ThreadX® real-time operating system (RTOS), the X-Ware™ suite of stacks and middleware (NetX™, NetX Duo™, USBX™, GUIX™, FileX®) plus other quality stacks, libraries, and drivers all connected by a rich Application Framework for ease of use. A common robust API resides over these components enabling you to focus on your own product application code without delays

4.4 TraceX®

- TraceX® is Express Logic's host-based analysis tool that provides developers with a graphical view of real-time system events and enables them to visualize and better understand the behavior of their real-time systems. With TraceX, developers can see clearly the occurrence of system events like interrupts and context switches that occur out of view of standard debugging tools. The ability to identify and study these events, and to pinpoint the timing of their occurrence in the context of the overall system's operation enables developers to resolve programming problems by finding unexpected behavior and letting them investigate specific areas further.

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4.5 GUIX Studio™

- GUIX Studio™ provides a complete WYSIWYG screen design environment which allows the user to drag-and-drop graphical elements used to build the UI screens. GUIX Studio automatically generates C code compatible with the GUIX™ library, ready to be compiled and run on the target. Developers can produce pre-rendered fonts for use within an application using the integrated GUIX Studio font generation tool. Fonts can be generated in monochrome or anti-aliased formats, and are optimized to save space on the target. Fonts can include any set of characters, including Unicode characters for multi-lingual applications.

4.6 Renesas Verified Software Add-Ons

- A selection of specialty software components developed, licensed, and serviced by Renesas VSA partner companies
- Tested and verified by Renesas to be compatible with the SSP per Renesas SSP interoperability requirements
- Continuously tested for SSP interoperability with each new SSP maintenance release
- Free evaluation version available, full licensing required from the VSA partner company for end-product production

4.7 Renesas Qualified Software Add-Ons

- A selection of specialty software components, licensed and serviced directly by Renesas
- Developed under the same quality standards and guidelines as the SSP
- Tightly integrated and optimized for use with SSP and API structure
- Free evaluation version available, full licensing required from Renesas for end-product production

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5 Board Support Package (BSP)

To allow users to begin application development quickly, Board Support Packages have been developed to pre-configure the S7G2 MCU's pins to support the various peripherals on board the SYG-70CP-BA/SYG-70CR-BA. This allows you to focus on application development instead of spending hours tracing signals through schematics. To install the BSP, download the relevant ".pack" files from the TeamFDI website using the links below. The files come packages as a zip and contain both the file for the board and the files for the touch screen. These files can also be found by navigating to the relevant product page under the software tab:

https://www.teamfdi.com/product-details/syg-70cp-ba/#software
https://www.teamfdi.com/product-details/syg-70cr-ba/#software

Once you have the files, ensure e2studio or IAR is closed and copy the file into the **Packs** directory of your e2studio or SSC directory.
If you installed e2studio into its default directory, this folder will be located at:
C:\Renesas\e2_studio\internal\projectgen\arm\Packs

If you use IAR Embedded Workbench with SSC, and installed it into its default directory, it will be located at:
C:\Renesas\Synergy\SSC\internal\projectgen\arm\Packs

Note: If you use both IAR and e2studio, you must install the pack in BOTH locations.

Once the *.pack files have been placed into the directory, open e2studio or IAR and either development environment's **New Synergy C Project** wizard will be updated to include the "SYG_70CP" or "SYG_70CR" as a new board option to select.

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6 Memory

6.1 32 MB External SDRAM

The 32MB 16Mbx16 SDRAM is a high-speed CMOS, dynamic random-access memory in an industry standard 54 ball VFBGA package. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks are organized as 8192 rows by 512 columns by 16 bits. The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a highspeed, fully random access. The 256Mb SDRAM is designed to operate in 3.3V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide pre-charge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Micron is a longtime leader in the SDRAM space, offering solutions from 64Mb to 256Mb, as well as a full suite of simulation models and technical support. The MT48LC16M16A2P-6AIT:G is supported on a cost effective 50nm process technology, with assured lifecycle support for years to come.

For more technical information visit http://www.micron.com/

This memory is accessed through the S7G2 microcontroller (MCU) External Memory Interface peripheral which is pre-configured on projects created using the provided Board Support Package (BSP).

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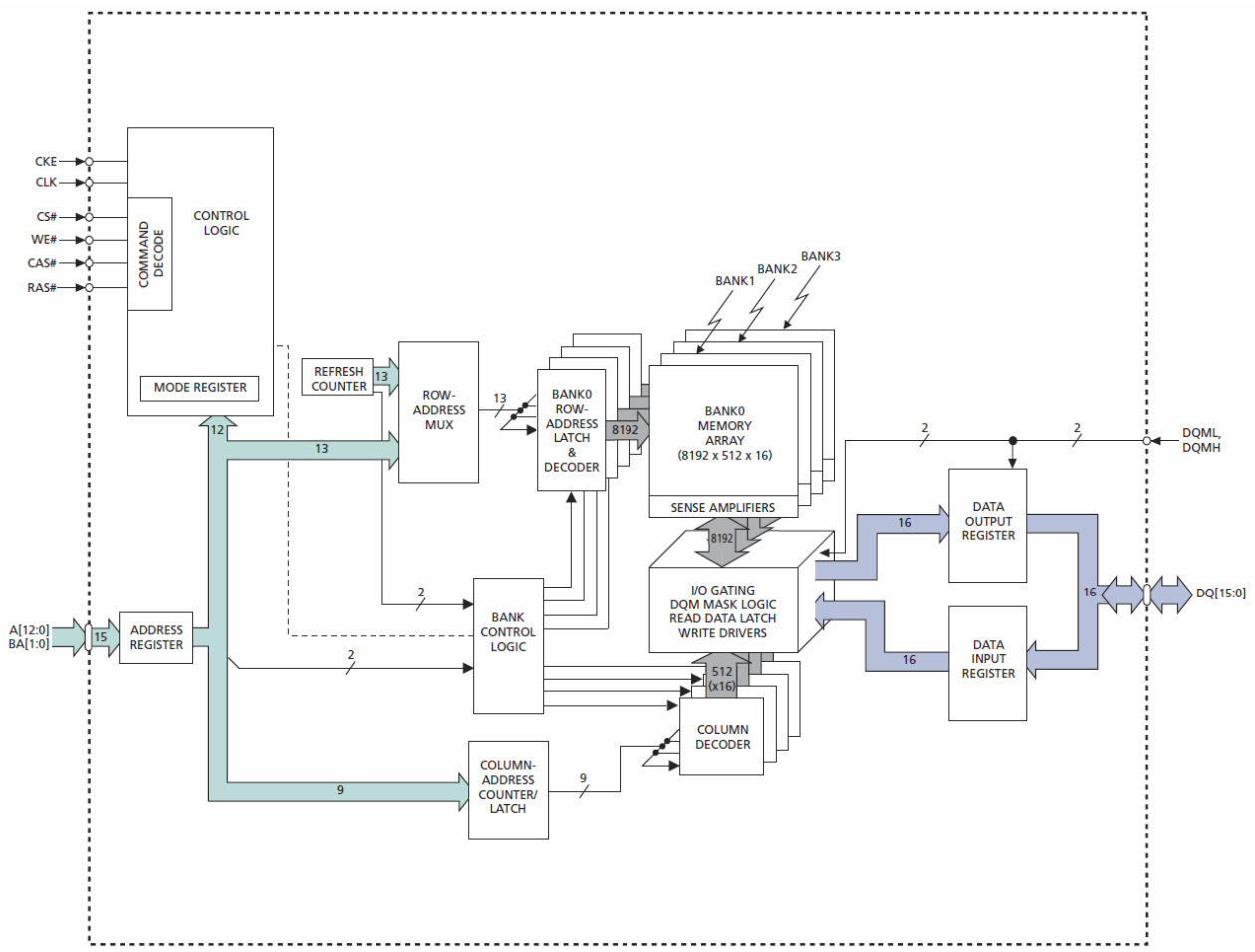


Figure 8 - SDRAM Block Diagram

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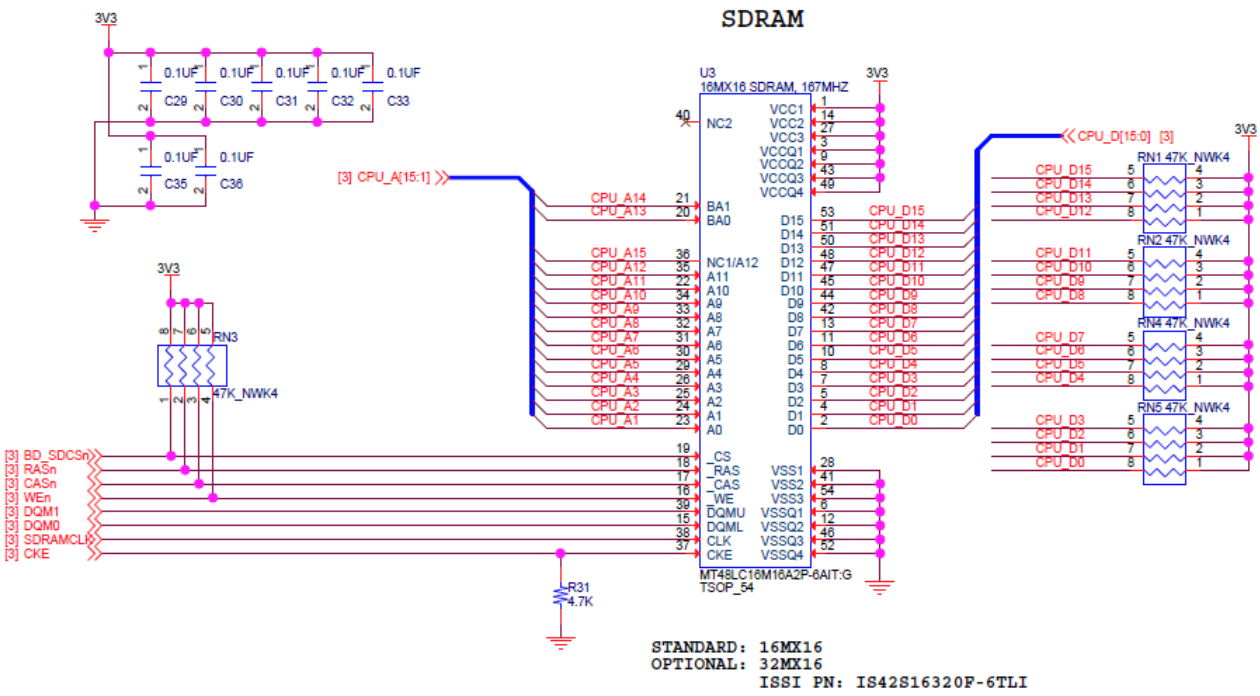


Figure 9 - SDRAM Schematic

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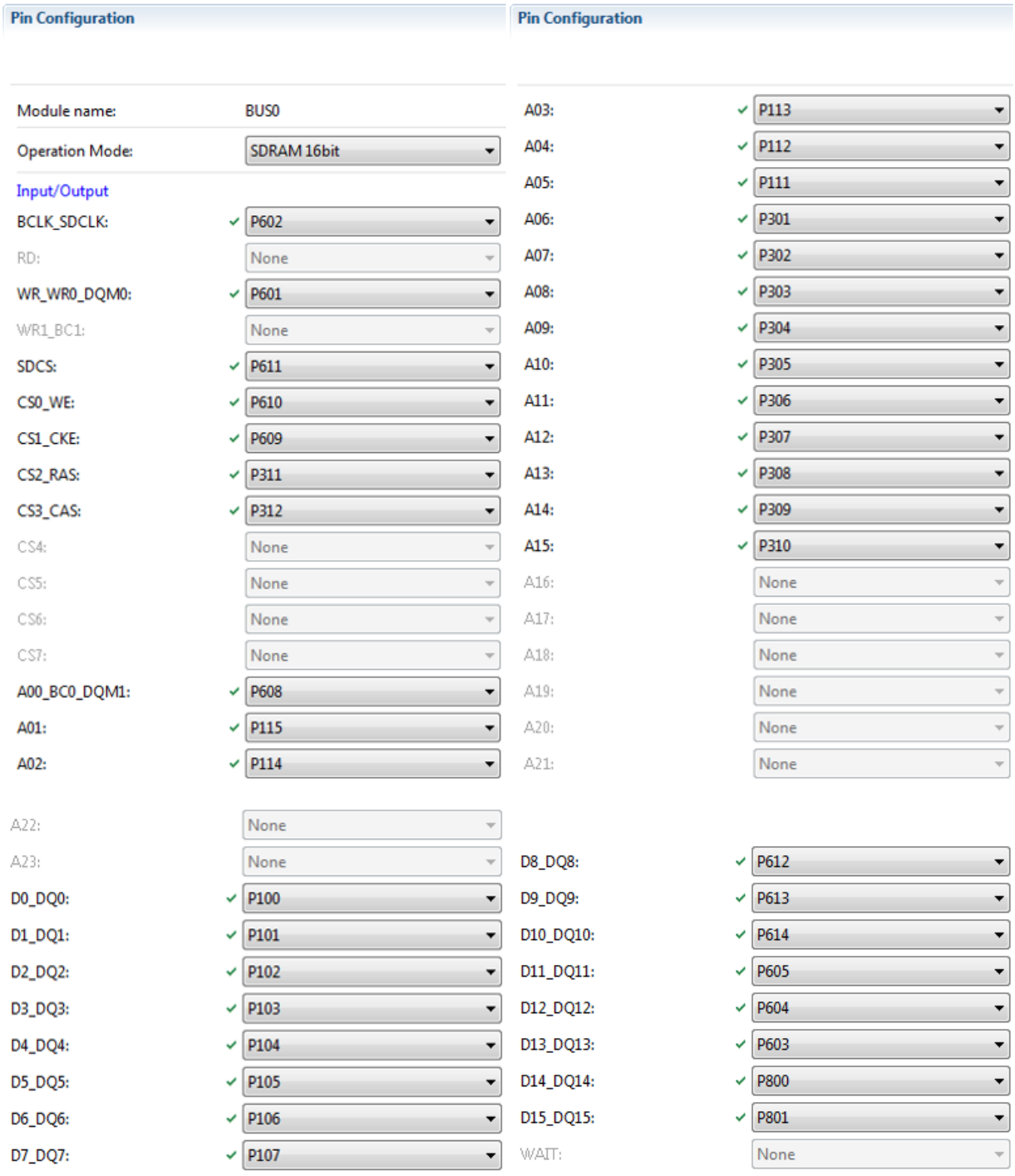


Figure 10 - Synergy SDRAM Pin Configuration

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6.2 16MB QSPI Flash, MX25L12835FMI-10G

Macronix Serial Multi I/O (MXSMIO™) Flash provides not only Single I/O, but also Multi-I/O interfaces. MX66xxx35 or MX25xxx33/35/39/73/75 series offering Dual I/O or Quad I/O operations which double or quadruple the read performance of systems for high-end consumer applications.

The QSPI Flash provides additional Code Space if needed, but also provides storage for fonts and images (which can be large on WVGA displays such as this one).

This memory is accessed through the S7G2 MCU's dedicated QSPI0 peripheral port.

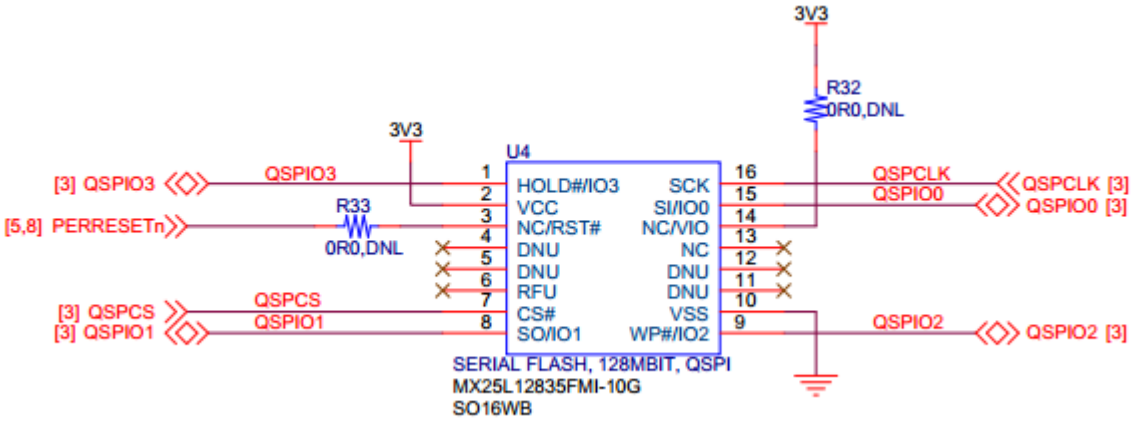


Figure 11 – QSPI Flash Pin Connections

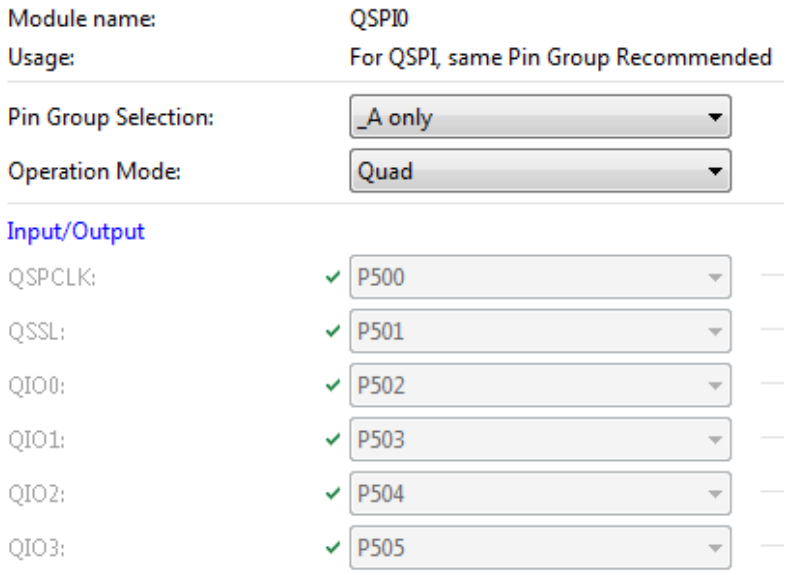


Figure 12 - Synergy QSPI Flash Pin Configuration

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7 Peripherals

The SYG-70CP-BA/SYG-70CR-BA has a large variety of peripherals available to use in a wide array of projects. A Board Support Package (BSP) is provided with the purchase of the SYG-70CP-BA/SYG-70CR-BA and is used to greatly simplify the configuration of the specific I/O needed for a given project. After installing the BSP, creating a New Synergy C Project dialog inside of e2 Studio or IAR Embedded Workbench will allow for the selection of the SYG-70CP-BA/SYG-70CR-BA. Creating a new project with this board choice will create a default pin configuration that will be used to configure the S7G2 MCU through the Synergy Configurator in e2 Studio or the Synergy Standalone Configurator (SSC) in IAR Embedded Workbench. There are certain options that are not configured by default, but are optional depending on your project requirements. Refer to the following sections to determine configuration requirements specific to your project and I/O needs.

7.1 LCD Panel

7.1.1 7.0" TFT WVGA 800x480 PCAP Touch Screen Display (-70CP models only)

The SYG-70CP-BA is equipped with a Tianma TM070RVHG01-01 7.0" TFT WVGA Projected Capacitance Touch screen display. This 800 x 480 touch screen has a 15:9 aspect ratio and 300 nits of brightness and a contrast ratio of 500:1.

The PCAP Display uses the SSD25XX Touch IC. The correct driver is shown below:

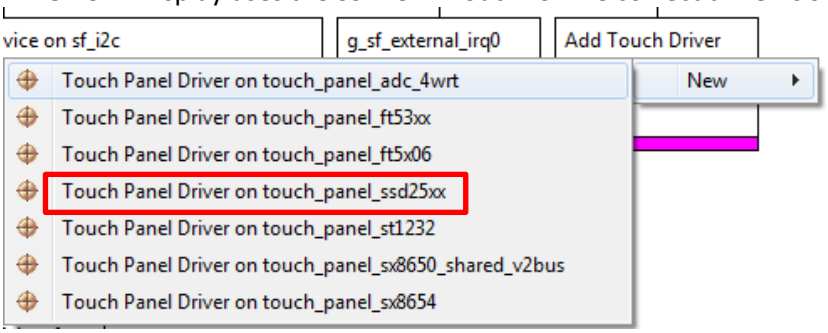


Figure 13 - Synergy Capacitive Touch Panel Driver

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7.1.2 7.0" TFT WVGA 800x480 4WR Touch Screen Display (-70CR models only)

The SYG-70CR-BA is equipped with a Tianma TM070RBHG04 7.0" TFT WVGA Projected Capacitance Touch screen display. This 800 x 480 touch screen has a 15:9 aspect ratio and 280 nits of brightness and a contrast ratio of 500:1.

The 4WR Display uses the on-board ADC. The correct driver is shown below:

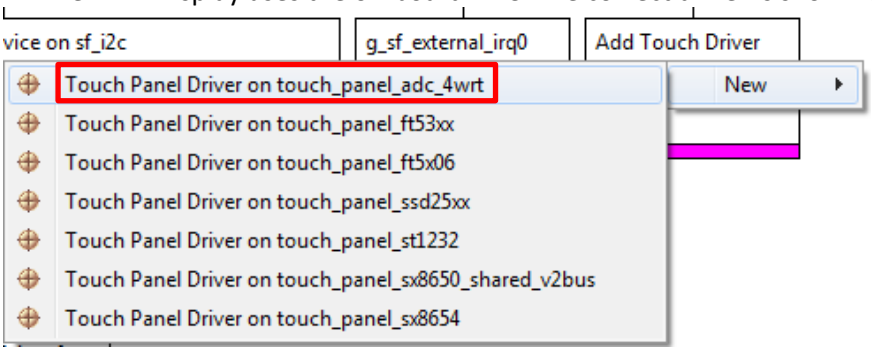


Figure 14 – Synergy Resistive Touch Panel Driver

7.1.3 Backlight Generator

Backlight brightness can be controlled using a PWM signal to control the backlight generator circuit. The pin for the PWM signal is configured in the BSP provided with the SYG-70CP-BA/SYG-70CR-BA, and the backlight circuit accepts 5KHz to 100KHz frequencies.

Note: For Full brightness, drive P713 high (P713 = 1).

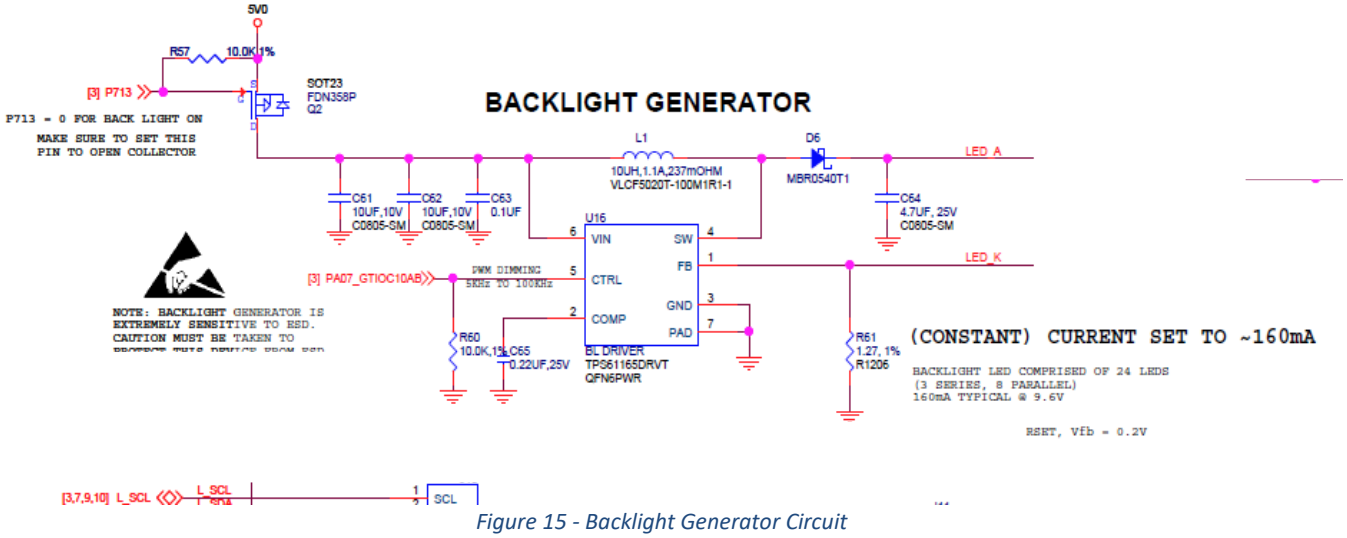


Figure 15 - Backlight Generator Circuit

It is also possible to turn off the backlight by setting P713 "low" (Low = 0). See the note on the schematic for more details.

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7.1.4 LCD Interface

The LCD interfaces with the SYG-70CP-BA/SYG-70CR-BA through connector J9. This 0.5mm pitch flat ribbon cable connector is robust and allows for sturdy connection of the LCD cable to the SYG-70CP-BA/SYG-70CR-BA. Several resistor options are available to support a wide variety of optional LCD displays, if required. The LCD Interface connector schematic is shown below:

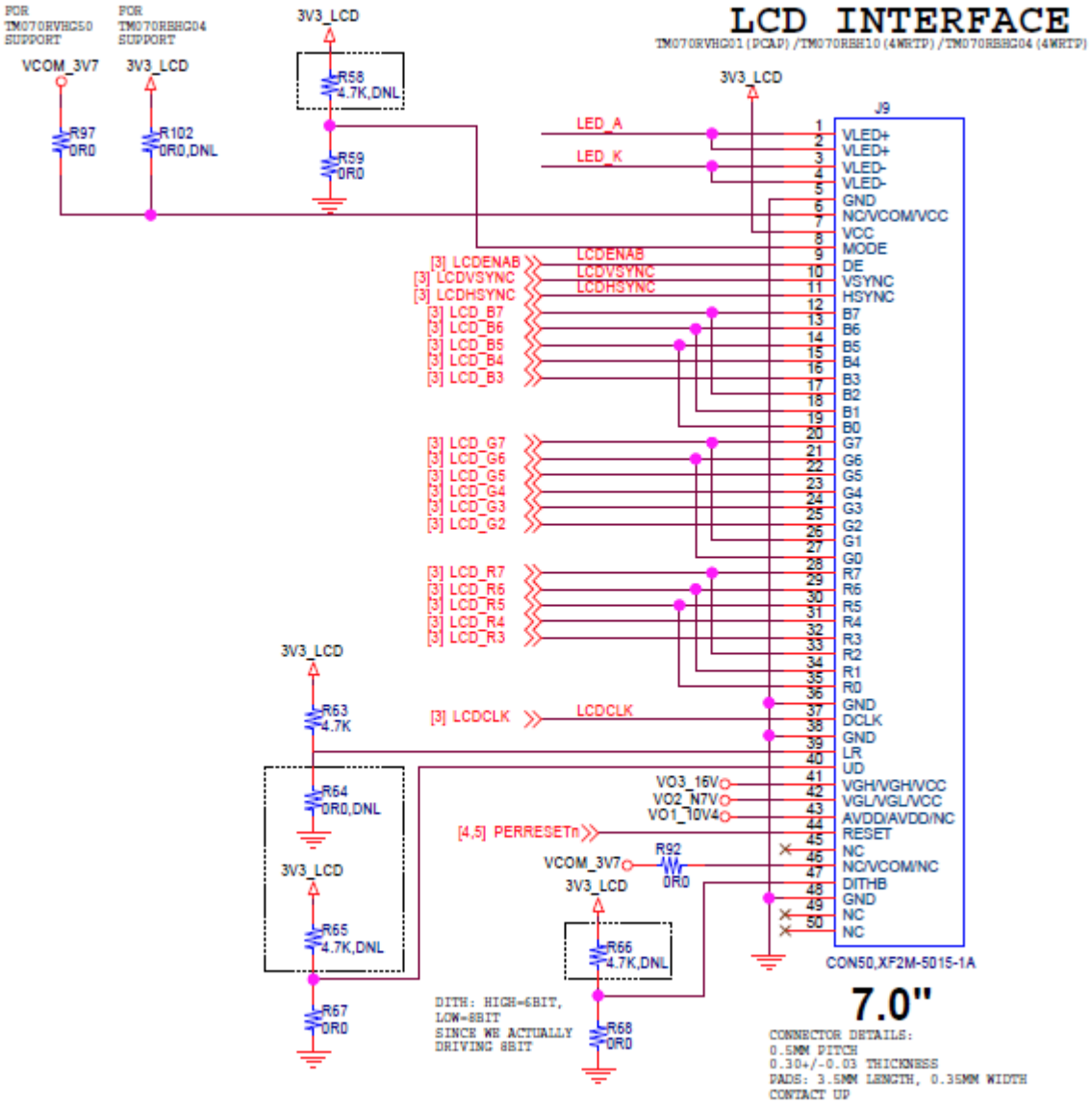


Figure 16 - LCD Interface Schematic

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7.1.5 LCD Power Switch

The SYG-70CP-BA/SYG-70CR-BA has an LCD Power Switch circuit that allows for turning off the LCD if desired. This is separate from the backlight control, although the operation of this is similar.

To enable the LCD (which is disabled by default), set P415 (P415_LCDPWR on the schematic) to "low (Low = 0). See the note on the schematic below for more details.

When Powered Off (P415_LCDPWR = 1), do not drive any of the LCD control pins on the LCD interface (J9), or damage to the LCD may occur!

Make sure to set P415_LCDPWR to n-ch open drain for proper operation of the LCD Power Switch circuit.

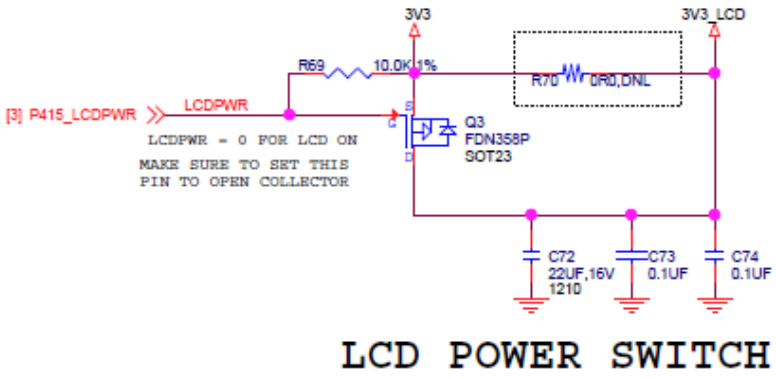


Figure 17 - LCD Power Switch Schematic

7.1.6 LCD Bias Voltage Generator

The SYG-70CP-BA/SYG-70CR-BA features a Bias Voltage Generator that is factory configured to work with either the Tianma TM070RVHG50-00 7.0" TFT WVGA Projected Capacitance Touch screen panel or the Tianma TM070RBHG04 TFT WVGA 4-Wire Resistive Touch screen panel. This bias voltage generation circuit provides accurately calibrated voltages through a highly reliable Texas Instruments TPS65100PWPR LCD Voltage Regulator.

For additional display compatibility, contact FDI at https://www.teamfdi.com/support

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7.1.7 PCAP Touch Interface (SYG-70CP-BA)

The 10 pin PCAP Touch Interface connector J10, is a 0.5mm flexible printed circuit cable connection that allows for reliable and robust connections to the touch controller on the LCD. This interface includes an I2C (L_SCL & L_SDA) connection, PCAP_IRQ, and PCAP_RST to allow for full control over the touch controller on the LCD. It also includes ESD protection to prevent possible damage to the SYG-70CP-BA due to Electrostatic Discharge.

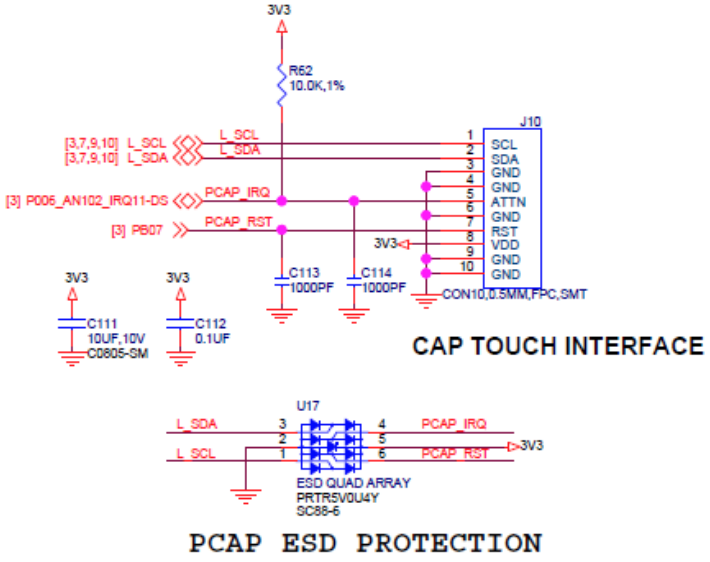


Figure 18 - PCAP Touch Interface and ESD Protection

7.1.8 Resistive Touch Interface (SYG-70CR-BA)

The 4 pin Resistive Touch Interface connector J11, is a 1mm flexible printed circuit cable connection that allows for connections to 4 wires from the Resistive Touch Panel. These 4 wires are connected to the S7G2 utilizing the Analog to Digital converter to interpret touch coordinates. It also includes ESD protection to prevent possible damage to the SYG-70CR-BA due to Electrostatic Discharge.

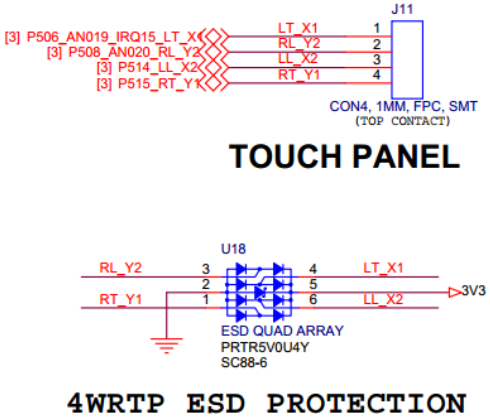


Figure 19 - 4WR Touch Interface and ESD Protection

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7.2 Wireless

The SYG-70CP-BA/SYG-70CR-BA comes equipped with a module for wireless connectivity. On hardware revs older than 2.0, it is a LSR 450-0152R module. On hardware revs 2.0 and later, it is a ESP-WROOM-32 Wireless Module.

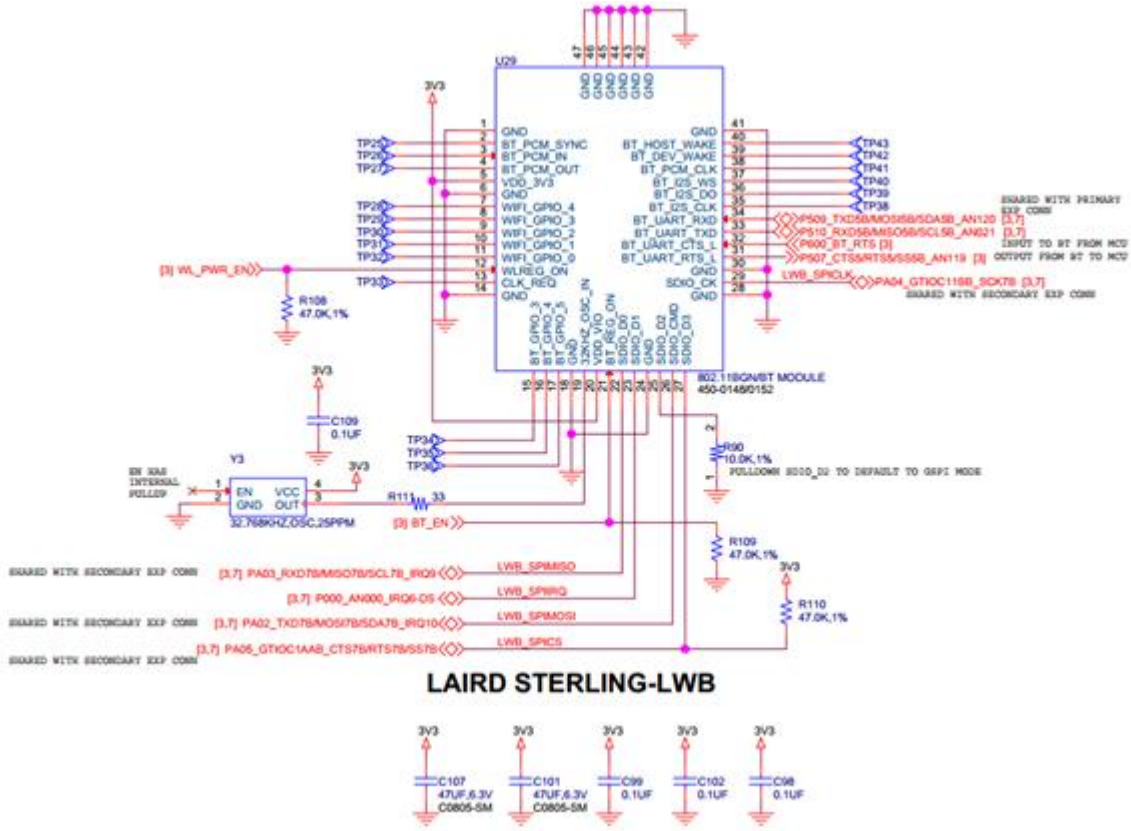


Figure 20.a - LSR 450-0152R module Schematic

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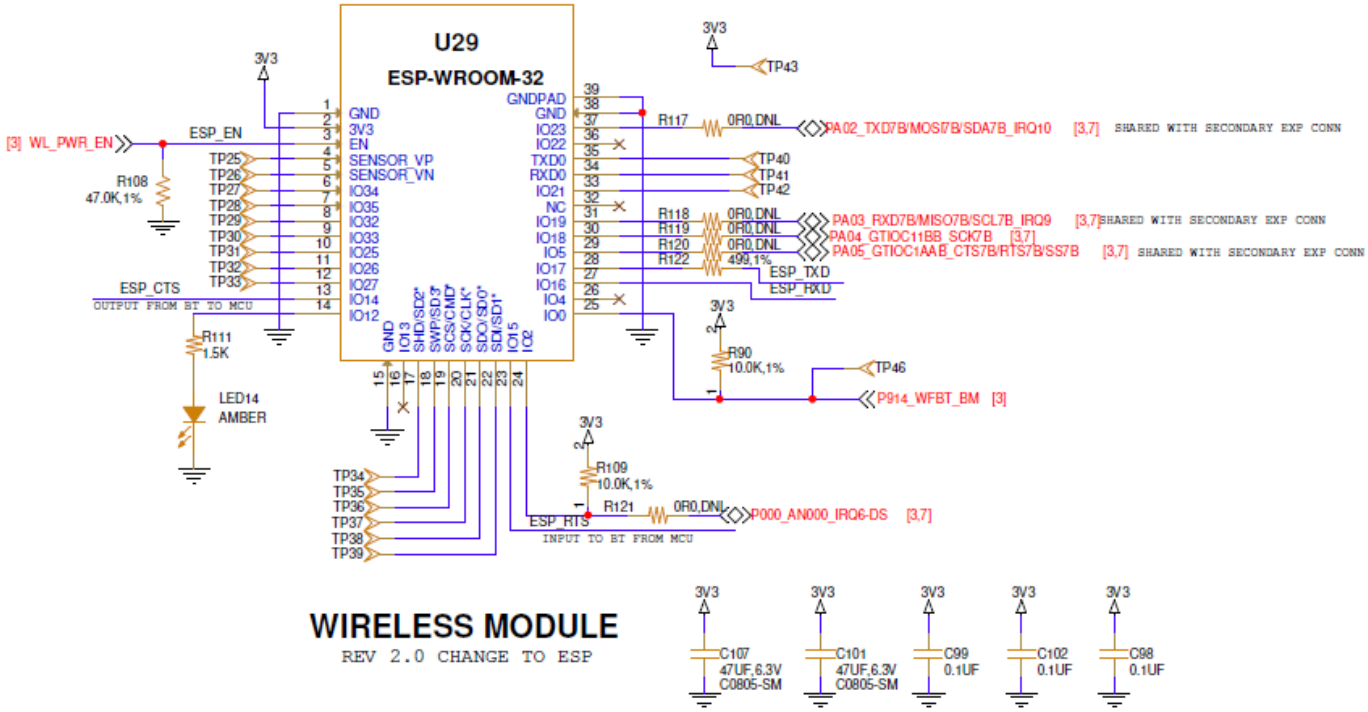


Figure 21.b - ESP-WROOM-32 Wireless Module Schematic

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Wireless capabilities are connected though one of the S7G2 MCU's SPI buses (7B). These pins are shared with the secondary expansion connector, detailed later in this document. When connecting to the Secondary Expansion connector and using the wireless module, be sure that you do not have any conflicting signals.

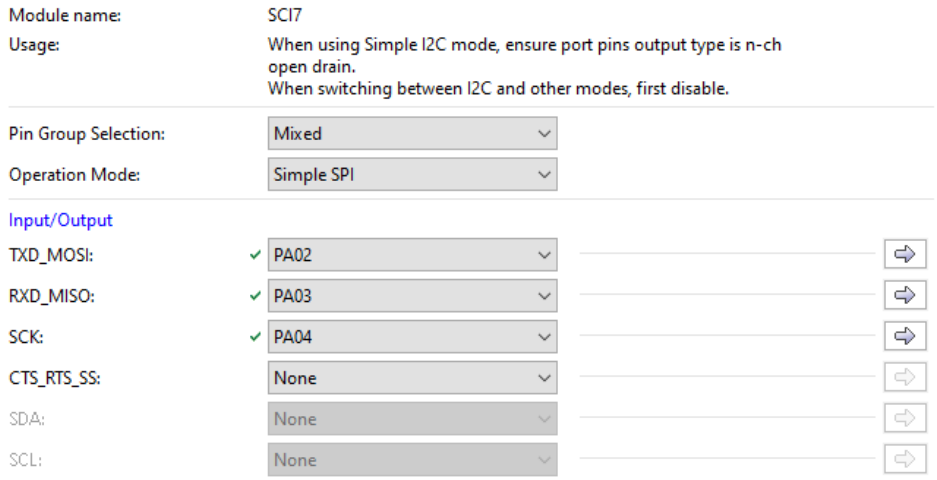


Figure 21 - Wireless SPI Configuration

7.3 SD card interface

The SD card interface is connected to the micro SD socket (J1). These signals are dedicated to the microSD Card and are not shared with any other functions on the SYG-70CP. This interface is capable of 4-bit SD mode up to 50 MHz.

MicroSD cards are common, cost effective, and provide a large amount of user-changeable memory.

1	**DAT2/RSV**
2	**CD_DAT3/CS#**
3	**CMD/SDI**
4	**VDD**
5	**CLK/SCLK**
6	**VSS**
7	**DAT0/SDO**
8	**DAT1/RSV**
9	**CD**

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The microSD card must be removed using the spring loaded "push-pull" mechanism on the microSD socket. Forceful removal of a microSD card will result in permanent damage to the socket that is not covered under warranty. To insert the card, push it into the socket until a "click" sound is heard. Similarly, to remove the card, push the card into the socket. The push-pull mechanism will "click" again and eject the card from the socket. The card is now available for safe removal.

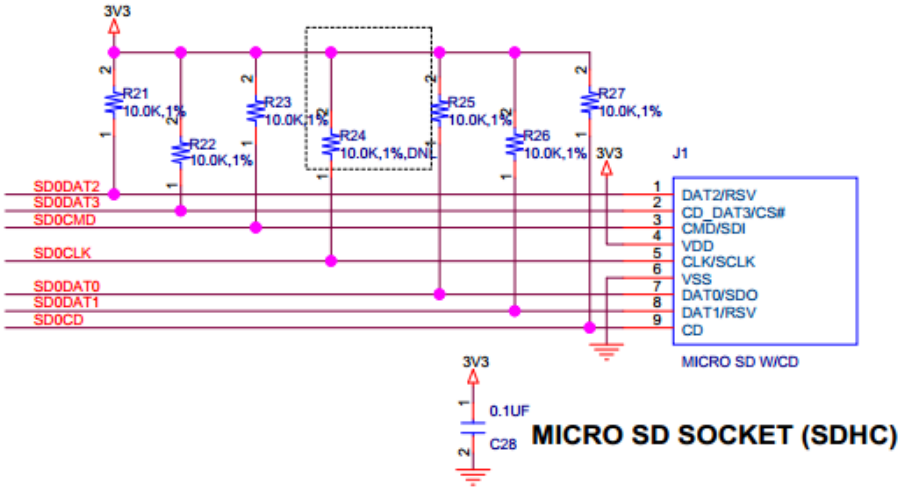


Figure 22 - microSD Card Socket

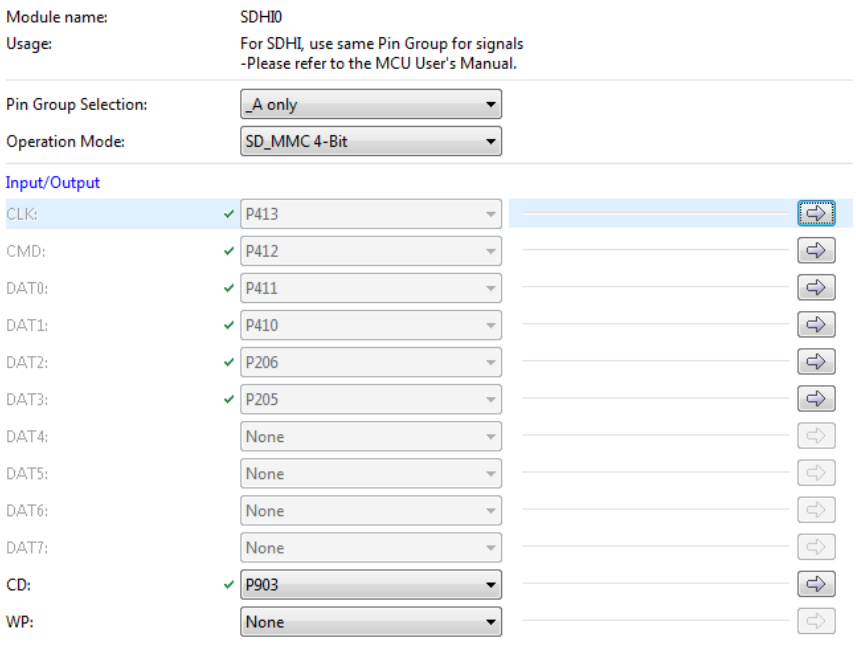
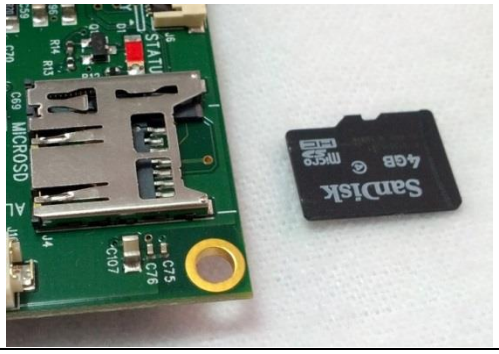


Figure 233 - microSD Card Configuration

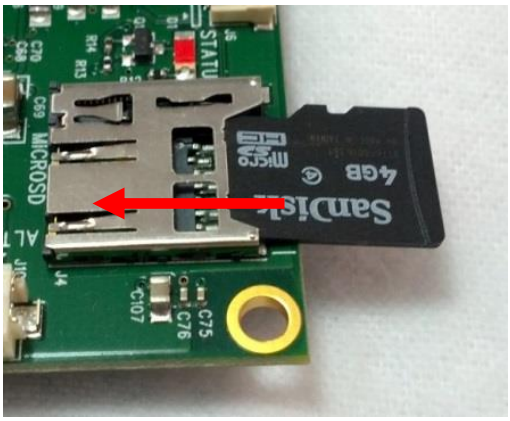
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7.3.1 microSD Card Insertion Instructions

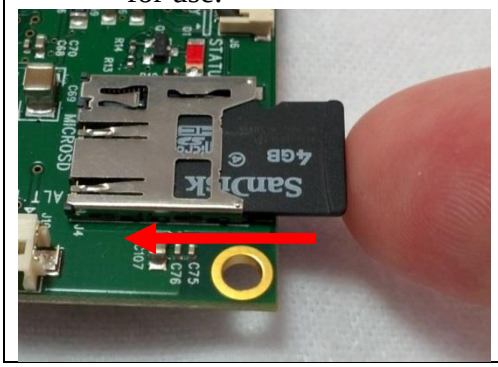
1) First, prepare to insert the microSD card into the socket by positioning it with its text facing up. Position the ridge, or "lip", of the card furthest from the socket.



2) Next, partially insert the card into the socket.



3) Then, use your finger to gently push the card into the socket. When the card "clicks" into place it is in its final, locked position. The card is now ready for use.

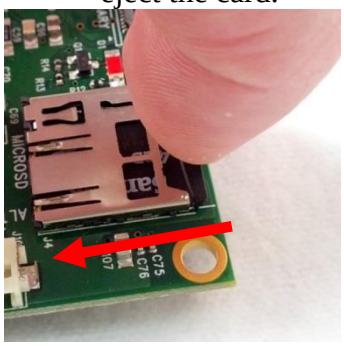
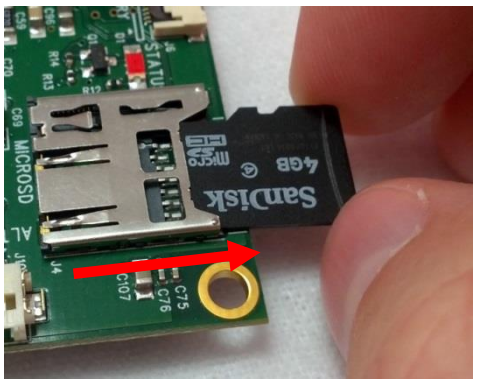


4) Note: Once the microSD card is fully inserted it should not fall out, even if the unit is shaken vigorously.



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7.3.2 microSD Card Removal Instructions

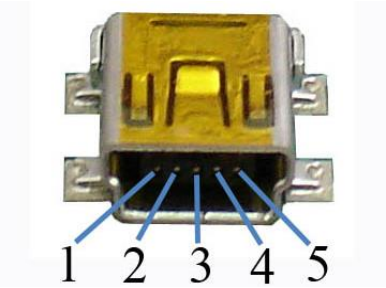
1) Begin to remove the microSD card by gently pushing the card into the socket. The socket will "click" and eject the card. 	2) Once the microSD card is ejected, it will partially extend out from the socket. 
3) Carefully grab the ridged edge or sides of the microSD card to gently pull it out. 	4) The microSD card is now fully removed from the socket. 

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7.4 USB Device

The SYG-70CP-BA/SYG-70CR-BA features a USB Device port (P1). This Mini-B connector allows for connecting the SYG-70CP-BA/SYG-70CR-BA to a USB Host device (such as a PC). This port is not meant to power the SYG-70CP-BA/SYG-70CR-BA and it is not recommended to connect this port to a power source (such as a mini-USB wall adapter).

The operational mode of the port is dependent on the software utilized (i.e. Mass Storage or Human-Interface).



Pin Number	Description
1	USB 5V
2	D-
3	D+
4	NC
5	Signal Ground

Note: Do not try to power the SYG-70CP-BA/SYG-70CR-BA through this USB Device port (P1). To power the SYG-70CP-BA/SYG-70CR-BA, use either P2 (mini-B USB) or one of the expansion connectors (J5, J6, J7).

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7.5 Real-Time Clock

The SYG-70CP-BA/SYG-70CR-BA features a Real-Time Clock (RTC) with an onboard supercapacitor and a 32.768 KHz crystal to accurately track time for a variety of application uses. The onboard supercapacitor 0.08F (C47) allows the RTC to continue to operate even if power is disconnected from the SYG-70CP-BA/SYG-70CR-BA for a short time. An optional 0.47F supercapacitor (C48) is available for a longer backup hold time.

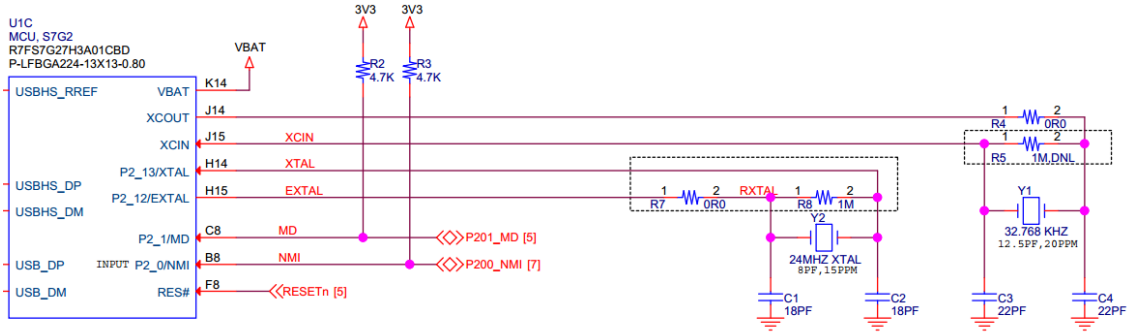


Figure 244 - RTC Schematic

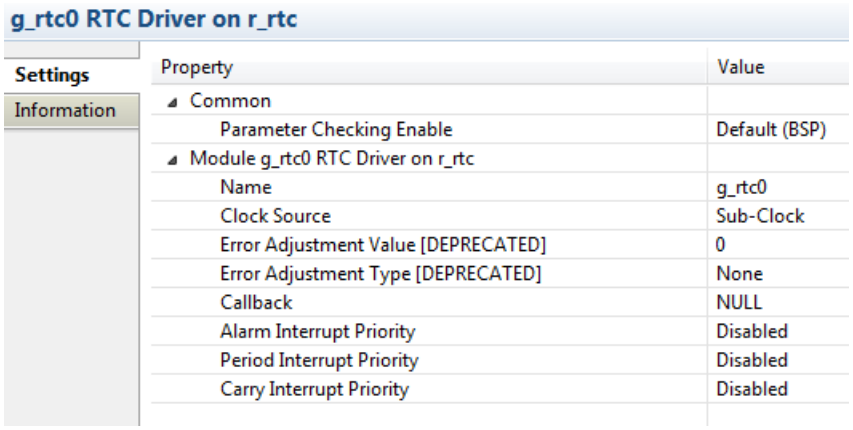


Figure 25 - RTC Synergy Configuration

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7.5.1 Supercapacitor Backup

The RTC supercapacitor (C47) allows for the RTC to continue to when main power is disconnected. The RTC supercapacitor is rated for 3.5V at 70C.

The RTC supercapacitor voltage is connected to the VBAT supply pin to the S7G2 MCU, and allows the MCU to continue to run the RTC even when the main power is disconnected.

The default RTC supercapacitor is 0.08F, but there is an optional 0.47F RTC supercapacitor footprint that allows for longer RTC operating times while the unit is disconnected from power.

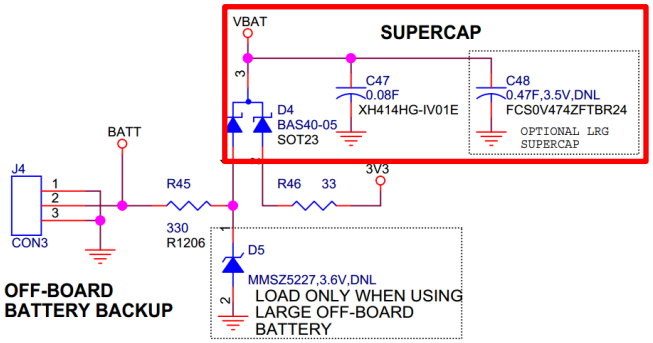


Figure 25- RTC Supercapacitor and Off-board Battery Backup Schematic

The RTC supercapacitor discharge graph shown below indicates the expected discharge curve when the unit has been plugged in for 24 hours before power was removed. The test unit was set to low power mode with all peripherals set to high impedance.

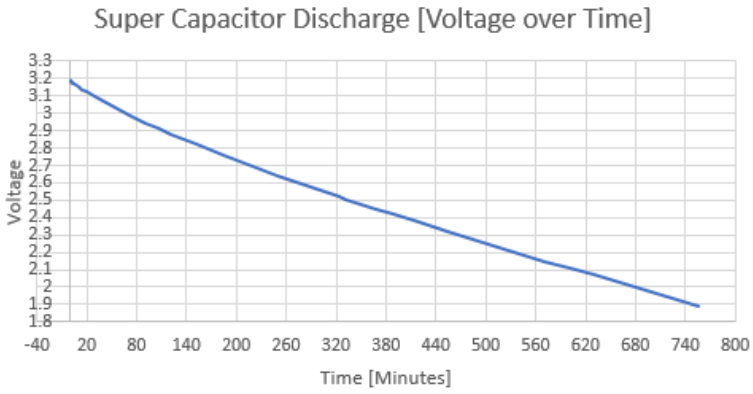


Figure 26 - Supercapacitor Voltage vs. Time

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7.5.2 Off-Board Battery

The SYG-70CP-BA/SYG-70CR-BA features a three-pin connector that allows for the use of an off-board battery backup. This battery should ideally be no larger than 3.6 Volts (3.3 Volts recommended). When using an off-board battery backup, D5 should also be loaded as a precautionary measure (to prevent high-voltage spikes from reaching the MCU and the RTC supercapacitor).

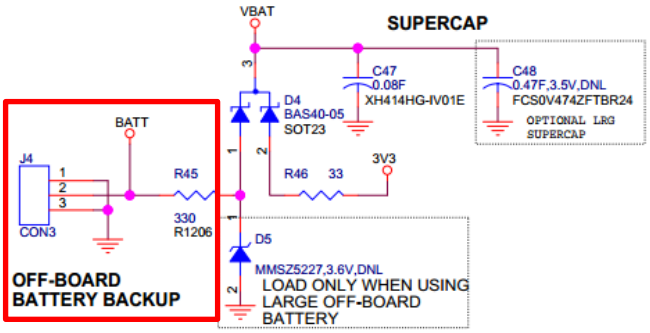


Figure 278 - Off-board Battery Backup Schematic

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7.6 Audio Amplifier

The SYG-70CP-BA/SYG-70CR-BA features an onboard LM48100Q-Q1 audio amplifier rated at 1.3 Watts. This audio amplifier allows applications to output a wide range of audio types through either a speaker, buzzer, or off-board speaker.

The audio amplifier features volume and mode control via I2C, and has dial audio inputs (for the SYG-70CP-BA/SYG-70CR-BA, these are DAC and PWM audio inputs) that can be mixed/multiplexed to the device output. Each input path has its own independent, 32-step volume control.

The audio amplifier I2C bus, PWM, and DAC pins are configured in the BSP included with the SYG-70CP-BA/SYG-70CR-BA.

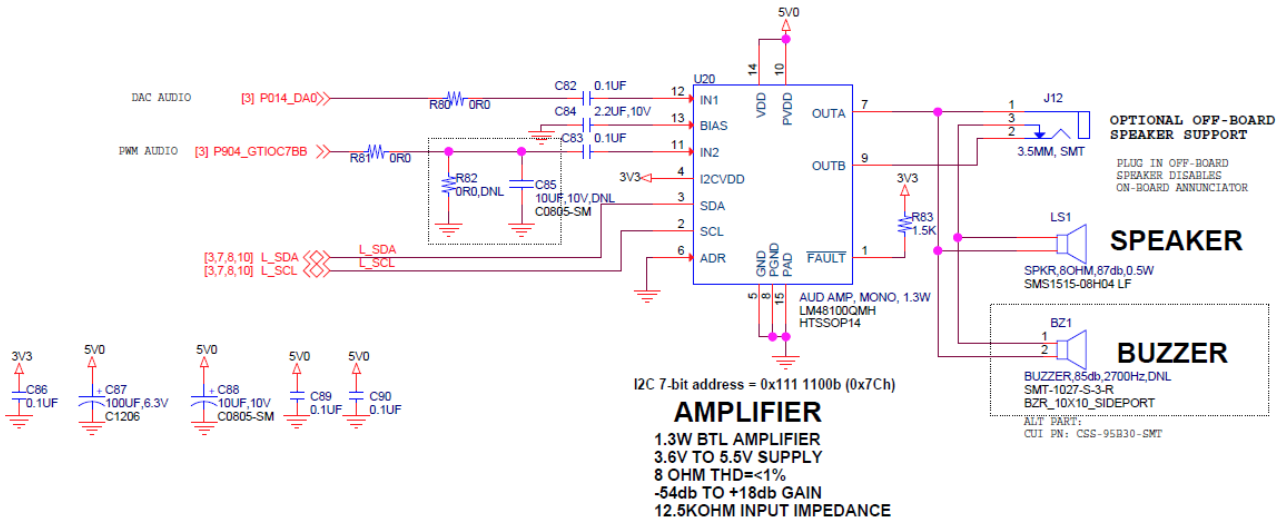


Figure 29 - Audio Amplifier Schematic

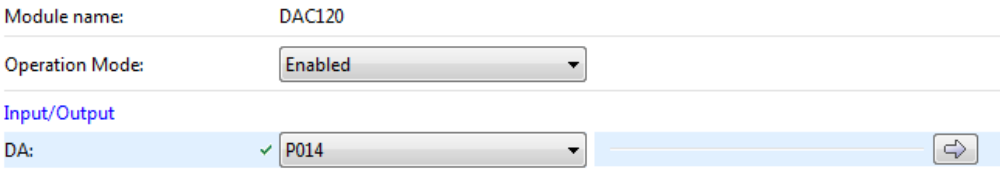


Figure 28 – Audio Amp DAC Configuration

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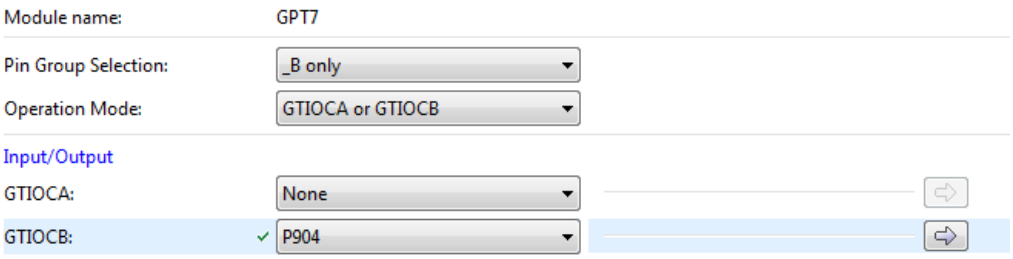


Figure 291 - Audio Amp PWM Configuration

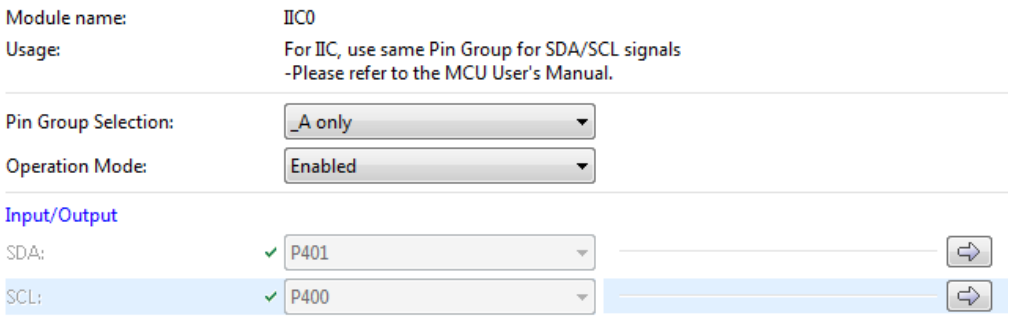


Figure 32 - Audio Amp I2C Configuration

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7.6.1 On-Board Speaker

The on-board speaker on the SYG-70CP-BA/SYG-70CR-BA is a 0.5 Watt 8 Ohm surface mount speaker manufactured by BeStar. This speaker is rated for 87 dBA.

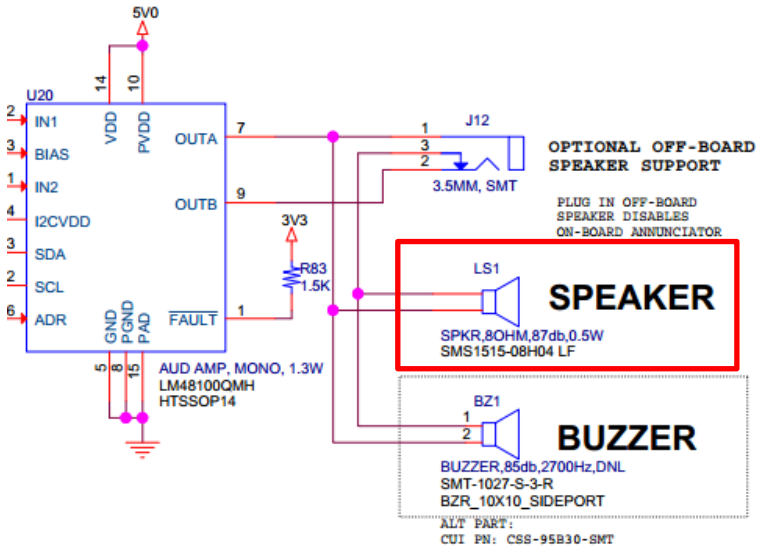


Figure 303 - Speaker, Buzzer, and Optional Off-board Speaker Schematic

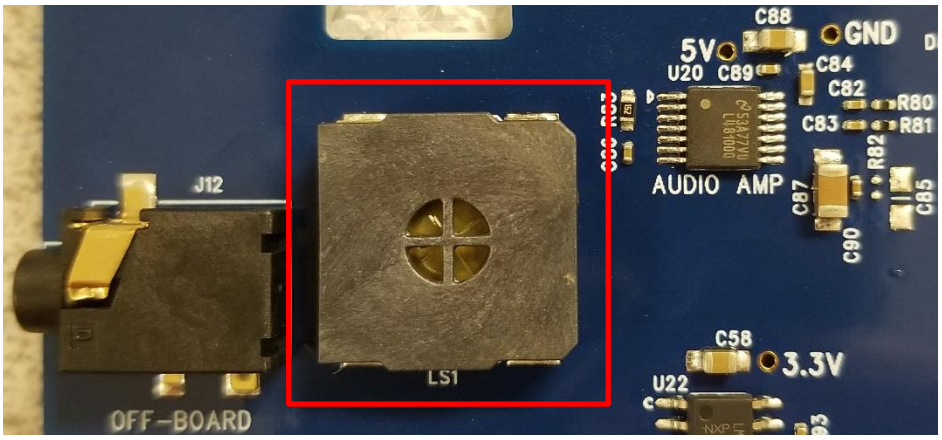


Figure 314 - Onboard Speaker

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7.6.2 Optional On-Board Buzzer

The SYG-70CP-BA/SYG-70CR-BA features an optional on-board buzzer manufactured by PUI Audio, Inc. This surface mount buzzer is rated at 85dB and produces a 2.7 KHz tone.

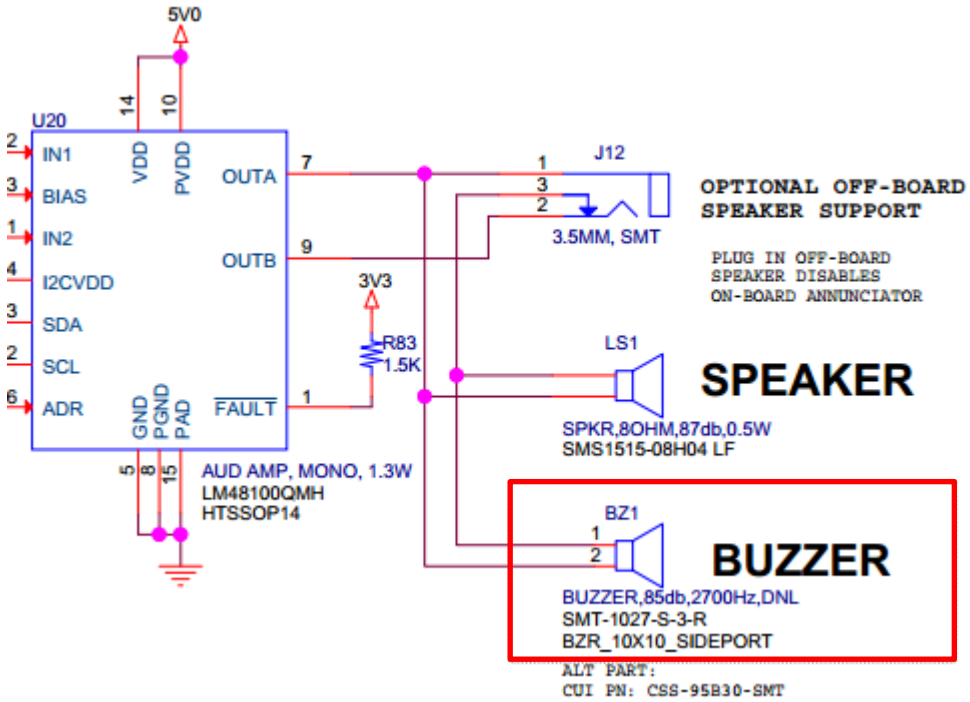


Figure 35- Speaker, Buzzer, and Optional Off-board Speaker Schematic

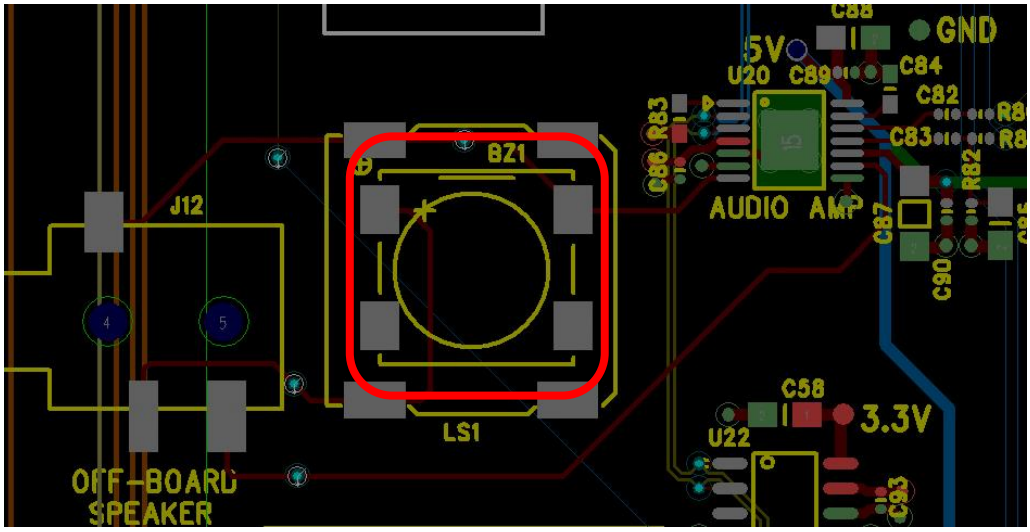


Figure 3632 - Optional Footprint for Buzzer on PCB

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7.6.3 Optional Off-Board Speaker Support

Also available on the SYG-70CP-BA/SYG-70CR-BA is an optional off-board speaker connector (J12). This connector allows for connecting 3.5mm speaker devices to the audio amplifier output. This is useful if your design includes external speakers or has a need to bring the audio output off-board.

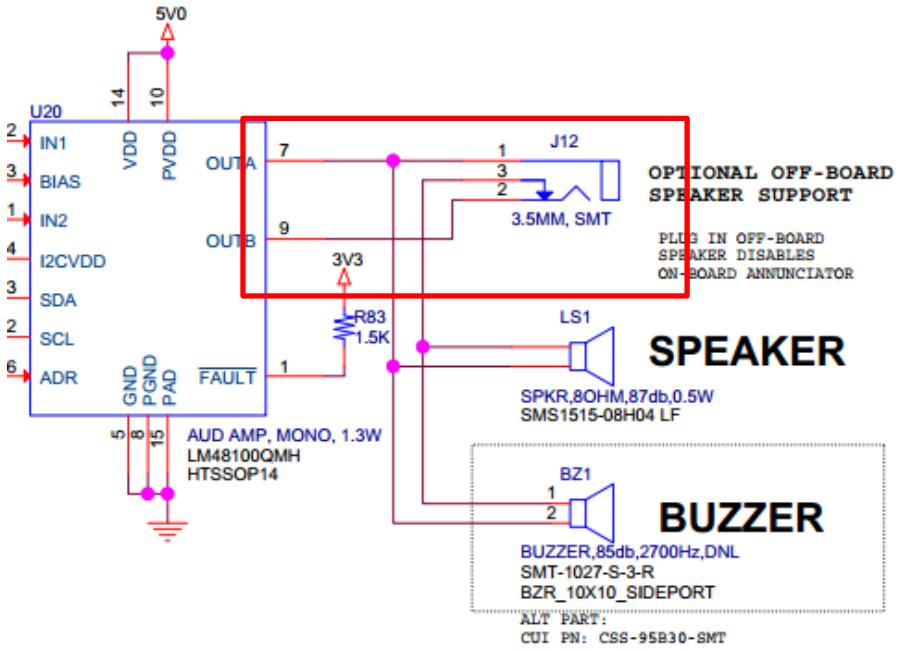


Figure 37 - Speaker, Buzzer, and Off-board Speaker Schematic



Figure 33 - Off-board Speaker Connector

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7.7 3-Axis Accelerometer

The SYG-70CP-BA/SYG-70CR-BA features the LIS3DH 3-Axis accelerometer, an ultra-low-power high-performance linear accelerometer with an I2C output. The accelerometer has dynamically user-selectable full scales of ±2/±4/±8/±16 g and is capable of measuring accelerations with output data rates from 1 Hz to 5.3 kHz. It also features a 32-level first-in, first-out (FIFO) buffer allowing the user to store data to limit intervention by the S7G2 MCU.

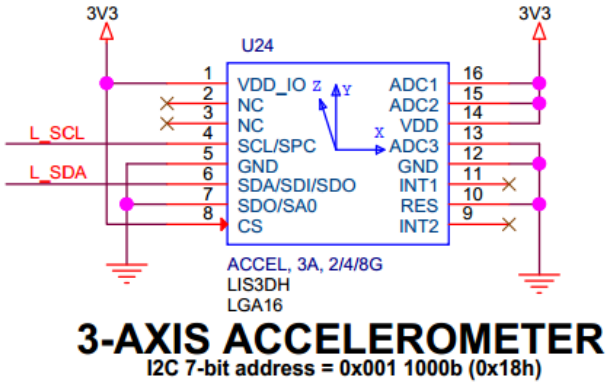


Figure 38 - 3 Axis Accelerometer Schematic

Property	Value
◢ Common	
Parameter Checking	Default (BSP)
◢ Module g_i2c3 I2C Master Driver on r_riic	
Name	g_i2c3
Channel	0
Rate	Standard
Slave Address	0x18
Address Mode	7-Bit
Callback	NULL
Receive Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit End Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Error Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)

Figure 39 - Accelerometer I2C Driver Configuration Example

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7.8 Temperature Sensor

The SYG-70CP-BA/SYG-70CR-BA features a LM75DB Temperature Sensor. This I2C-based temperature sensor has a range of -55 Celsius to 125 Celsius, with an accuracy of ±2C from -25C to 100 C, and ±3C from -55 C to 125 C.

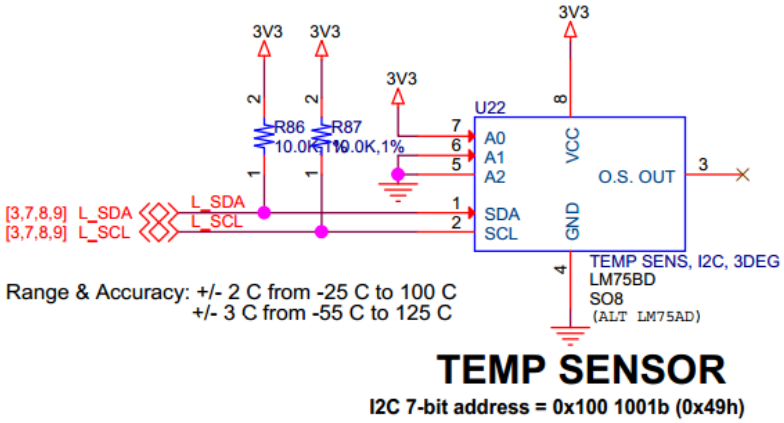


Figure 35 - Temperature Sensor Schematic

Property	Value
◢ Common	
Parameter Checking	Default (BSP)
◢ Module g_i2c2 I2C Master Driver on r_riic	
Name	g_i2c2
Channel	0
Rate	Standard
Slave Address	0x49
Address Mode	7-Bit
Callback	NULL
Receive Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit End Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Error Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)

Figure 36 - Temperature Sensor I2C Configuration Example

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7.9 Ambient Light / Proximity Sensor

The SYG-70CP-BA/SYG-70CR-BA features a SFH7776 Ambient Light & Proximity Sensor that allows for easy control of the LCD Backlight by sensing the amount of ambient light around the LCD display. The Ambient Light Sensor also features a proximity detection sensor.

The Proximity sensor delivers output values within the range of 0 up to 4095 (12 bit, linear).

The Ambient Light Sensor delivers output values in the range from 0 to 65545 (16 bit). The range of the ambient light sensor sensitivity can be set by the user and covers more than 4 ½ decades in each setting. Two threshold levels for the ambient light sensor can be set via the I2C bus, an upper and lower threshold.

The ALS/Prox sensor is connected to the MCU via I2C as well as an interrupt signal, allowing for MCU interrupts to occur when thresholds are reached.

Note: The ALS/Proximity sensor was designed to be used as a supplement for LCD backlight control and placement of the sensor on the SYG-70CP-BA/SYG-70CR-BA may not be indicative of a final design placement. Special consideration should be used when considering the ALS/Proximity sensor in your design, especially if a housing or enclosure is used.

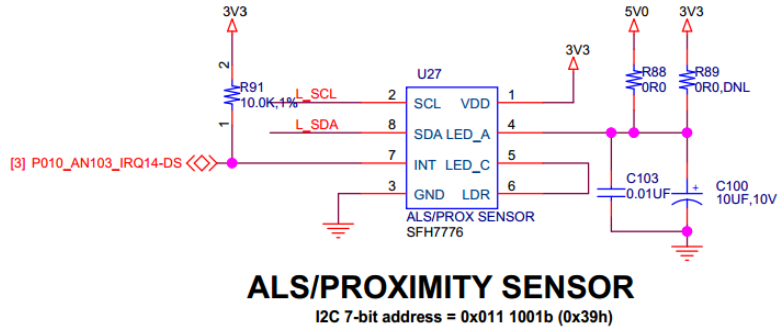


Figure 4237 - ALS/Proximity Sensor Schematic

Property	Value
◢ Common	
Parameter Checking	Default (BSP)
◢ Module g_i2c1 I2C Master Driver on r_riic	
Name	g_i2c1
Channel	0
Rate	Standard
Slave Address	0x39
Address Mode	7-Bit
Callback	NULL
Receive Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Transmit End Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)
Error Interrupt Priority	Priority 3 (CM4: valid, CM0+: lowest - not valid if using ThreadX)

Figure 3 - ALS/Proximity Sensor Synergy Configuration

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7.10 PMOD Type 2A Connector with SPI and optional I2C

A Pmod Type 2A Connector is available on the SYG-70CP-BA/SYG-70CR-BA. This 12 pin connector features SPI signals connected to the MCU, and has a load option available to connect I2C devices via Pmod. This connector also features a Reset Out signal allowing for peripheral reset control and an IRQ signal to allow for MCU interrupts from the Pmod peripheral.

Pmod expansion connectors can be used with the large array of sensors and add-on modules available from many different suppliers. Some modules communicate via the I2C protocol, while others use SPI or UART. For details about the different Pmod specifications, see the Pmod specification manual (https://www.digilentinc.com/Pmods/Digilent-Pmod_%20Interface_Specification.pdf) . More information about the Pmod Standard can also be found here (https://reference.digilentinc.com/reference/pmod/specification).

The Pmod connector includes ESD Protection as well to ensure the SYG-70CP-BA/SYG-70CR-BA remains safe from any potential ESD.

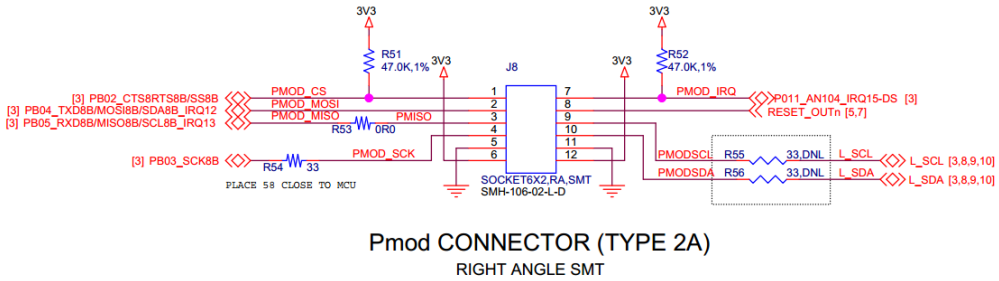


Figure 38 - Pmod Type 2A Connector Schematic

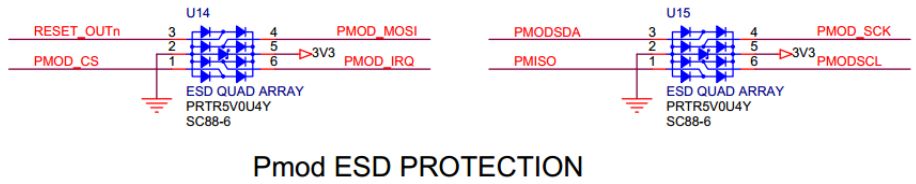


Figure 39 - Pmod Connector ESD Protection Schematic

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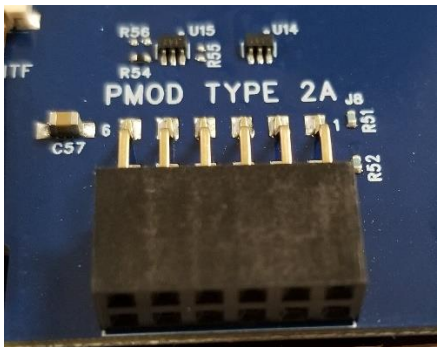


Figure 46 - Pmod Type 2A Connector

7.11 Cortex-M 9-pin JTAG Debug Connector

The Cortex-M 9-pin JTAG Debug Connector (J2) included on the SYG-70CP-BA/SYG-70CR-BA allows for JTAG and Single Wire Debugging (SWD) through the IDE of your choice. This connector includes a Reset signal (active LOW) for MCU resets, and can be configured to allow for SCI Boot mode for the S7G2 MCU.

This smaller connector provides 100% of the functionality of the standard 20-pin JTAG connector, but utilizes 70% less board space.

Pin Number	Description	Pin Number	Description
1	VCC	6	TDO
2	TMS	7	X
3	GND	8	TDI
4	TCK	9	GND
5	GND	10	RST#

Pin 7 on the JTAG Debug Connector is keyed to ensure correct connector orientation.

Kits come with the SEGGER J-Link Lite Cortex-M shown below. With the J-Link Lite no adapter is required.



Figure 47 - Segger J-Link Lite Cortex M 10-pin Adapter

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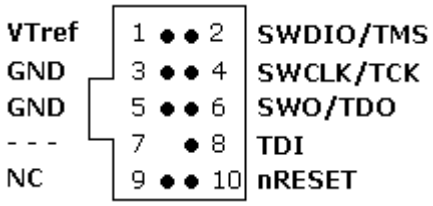


Figure 48- J-Link Lite 10 pin Schematic

SEGGER and OLIMEX both provide adapters to convert the standard 20-pin JTAG to the new ARM 9-pin JTAG. The SEGGER adapter also allows for connecting TRST using a solder bridge if needed. These adapters have female pins, and are only compatible with 20-pin JTAG units that have male pins. Each of these adapters comes with the required cable.

SEGGER 9-pin adapter - http://www.SEGGER.com/jlink-adapters.html#CM_9pin
OLIMEX 9-pin adapter - https://www.olimex.com/Products/ARM/JTAG/ARM-JTAG-20-10/

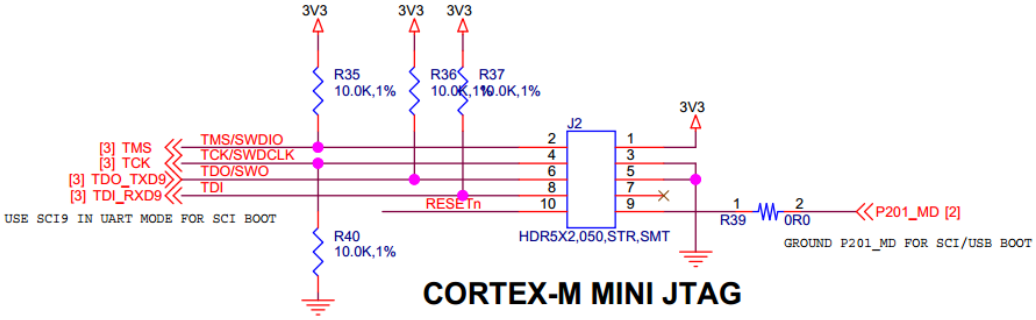


Figure 49 - J-Link Lite Cortex-M Schematic

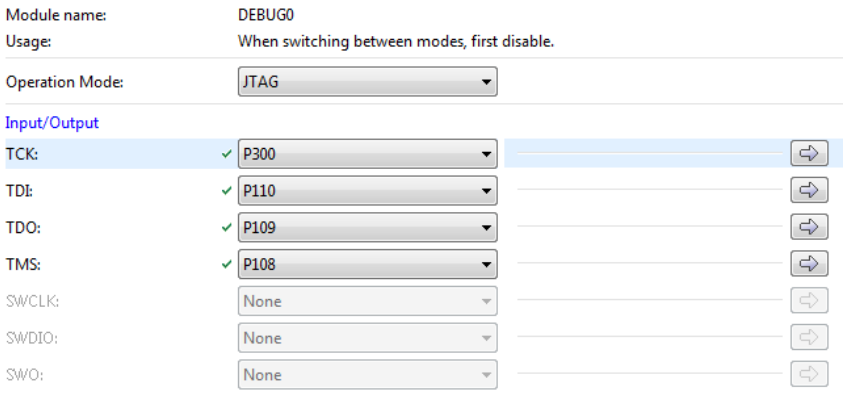


Figure 40 - J-Link Debug Synergy Configuration

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7.11.1 10 Pin Tag-Connect

Also available is the 10 Pin Tag-Connect Header (J3). This footprint allows for connecting a 10-pin Tag-Connect debug header directly into the PCB, with no mating connector or header required. This allows for a low-profile, low-cost option for debugging, and is designed so that it is impossible to plug in the connector incorrectly.

- Adapter: http://www.tag-connect.com/TC2050-ARM2010
- Cable with legs: http://www.tag-connect.com/TC2050-IDC
- Cable with no legs: http://www.tag-connect.com/TC2050-IDC-NL
- Holding clip for no-legs cable version: http://www.tag-connect.com/TC2050-CLIP

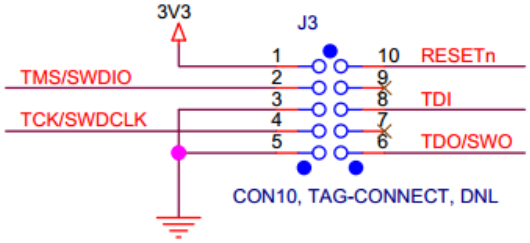


Figure 41 - Tag Connect Header & Connector



Figure 42 - Tag Connect Header inserted into PCB

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TAG CONNECT JTAG

Figure 43 - Tag Connect Schematic

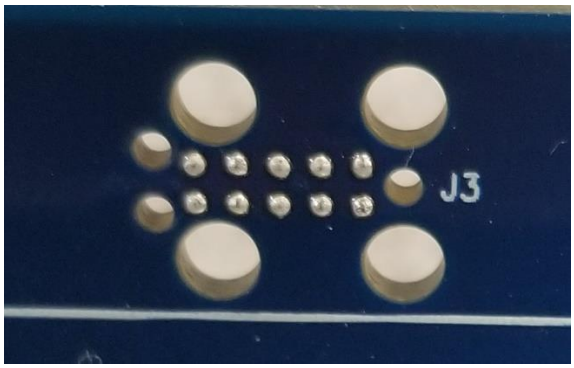


Figure 44 - Tag Connect PCB Footprint

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7.12 XBee Expansion Socket

The XBee socket on the SYG-70CP-BA/SYG-70CR-BA allows for adding modules that conform to the Digi XBee Ecosystem. These modules are a family of form factor compatible communication modules that allow you to customize your wireless radio solution on the SYG-70CP-BA/SYG-70CR-BA. In addition to the standard pin compatibility with the Digi XBee ecosystem, the SYG-70CP-BA/SYG-70CR-BA also has compatibility with the NimbeLink Skywire™ 4G LTE CAT 1 Verizon Embedded Modem. This is a Digi XBee footprint standard device capable of 10Mb/s download and 5Mb/s upload speeds.

Due to minor pin requirement changes from standard XBee devices and the NimbeLink Skywire 4G LTE CAT 1 module, the SYG-70CP-BA/SYG-70CR-BA have been designed with a switch to easily modify your setup to accommodate the module of your choice.

By switching SW3 & SW4, you can configure your SYG-70CP-BA/SYG-70CR-BA for the correct pin configuration for your chosen XBee module. Below you can see the schematic for SW2 and SW3, noting what changes are made when the switches are configured.

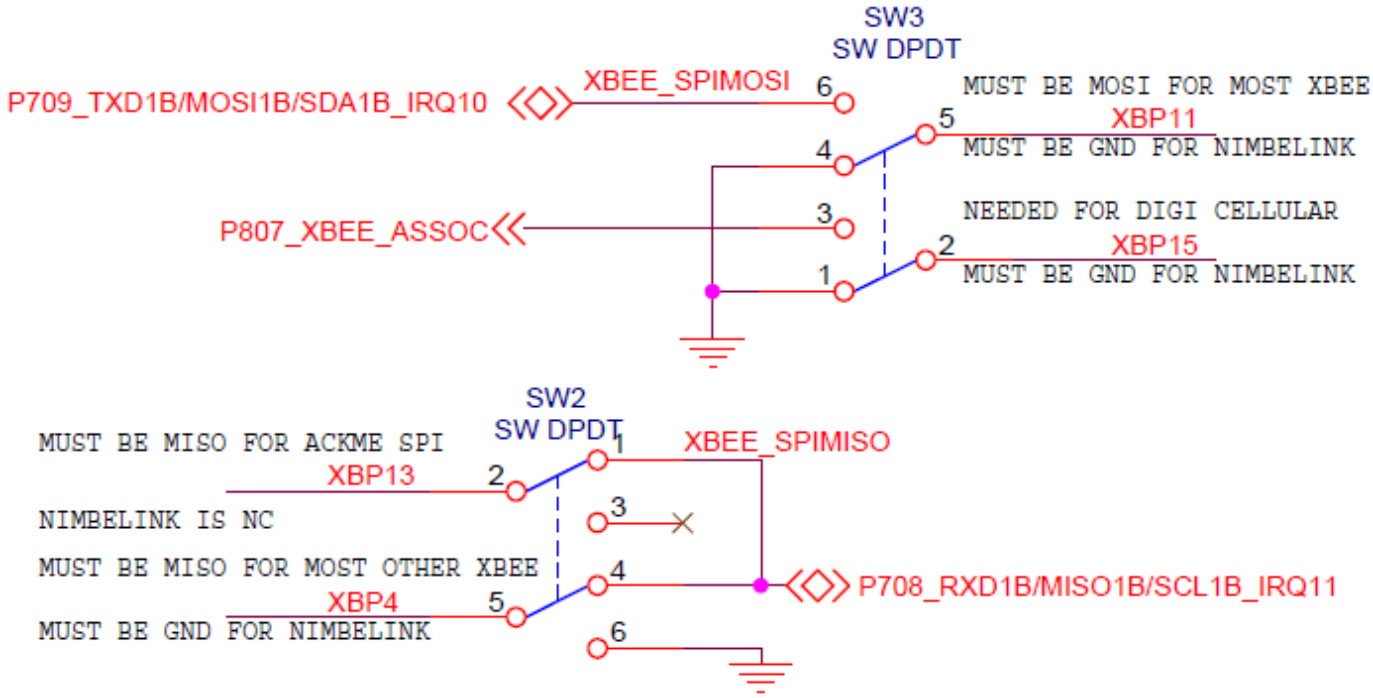


Figure 45 - XBee Configuration Switches Schematic

The switches are clearly labeled for ease of use on the PCB silkscreen of the SYG-70CP-BA/SYG-70CR-BA. Simply move both switches (SW2 and SW3) simultaneously in one direction for all standard Digi XBee modules, and in the other direction for NimbeLink Skywire modules.

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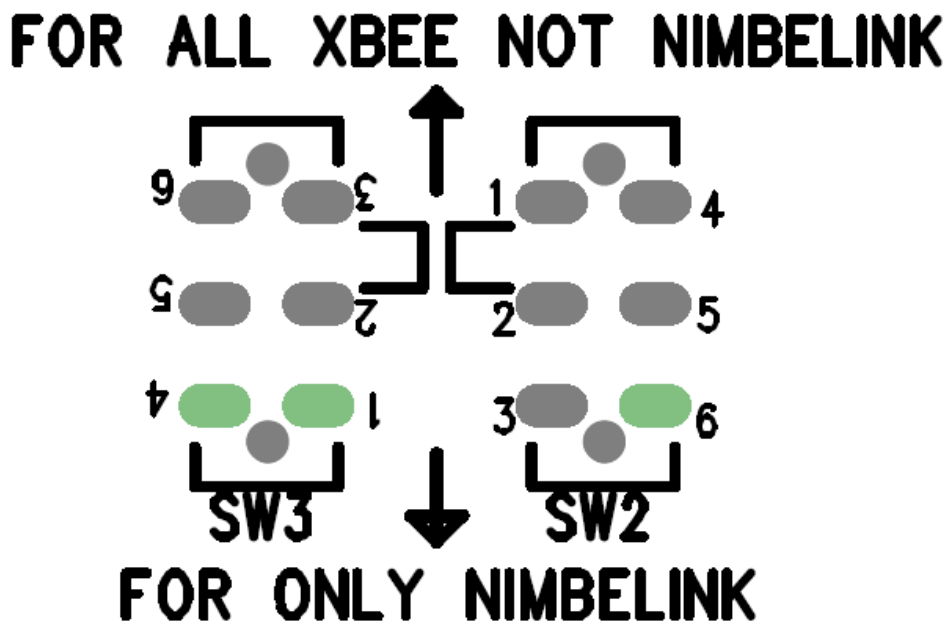


Figure 56 - XBee Configuration PCB Silkscreen

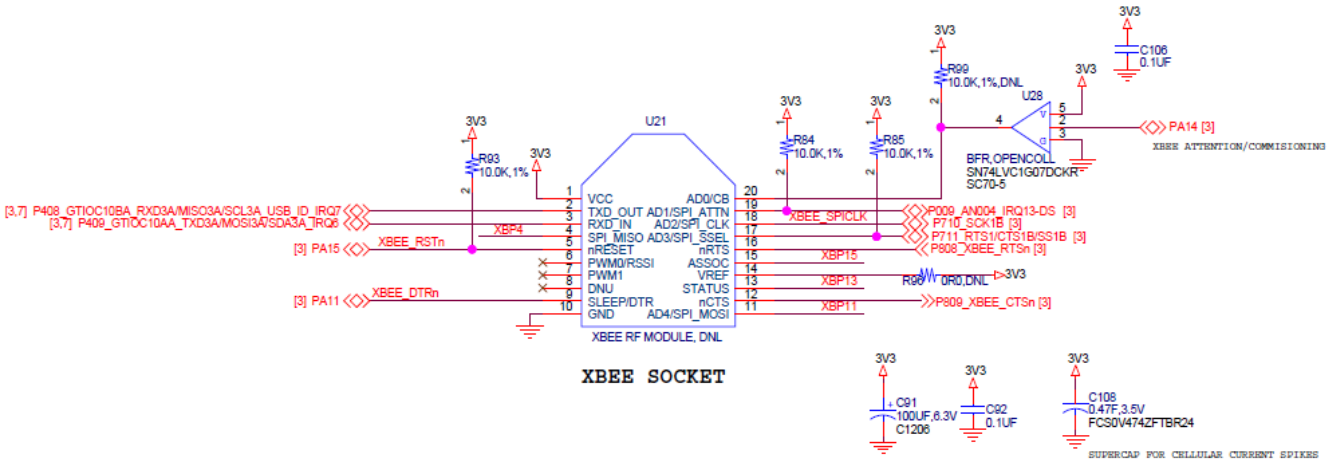


Figure 57 - XBee Socket Schematic

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7.12.1 XBee supercapacitor

The SYG-70CP-BA/SYG-70CR-BA comes pre-installed with a 0.08F supercapacitor (C47) to provide backup power to the RTC. We also provide provisions to install an optional 0.47F supercapacitor (C108 in the schematic). This supercapacitor is intended for use in high-current applications, such as cellular modems, that can experience power spikes. If the supercapacitor is not loaded and your design requires it, ensure that the supercapacitor you choose matches our footprint and your design requirements. The reference part is shown below, including the manufacturer's part number.

Note: If the C108 0.47 F supercapacitor is loaded on your SYG-70CP-BA/SYG-70CR-BA, you may experience that the unit may remain powered for up to 45 seconds. The S7G2 MCU will enter an immediate reset mode, and the D1 LED Indicator will stay solid on (not blinking), indicating that the MCU is not running but that power is applied. The brightness of the LED will dim over a 45 second period as the supercapacitor is discharged. If power is reapplied during this process, the onboard reset generation circuit will bring the MCU up in a normal Power-On Reset. Take caution when handling the SYG-70CP-BA/SYG-70CR-BA while it is still powered by the 0.47 F supercapacitor to prevent damage to the device.

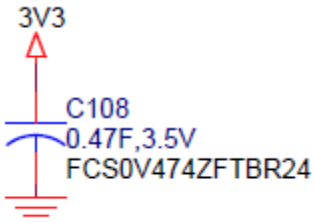


Figure 58 - XBee Supercapacitor Schematic

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7.13 Expansion Connectors

The SYG-70CP-BA/SYG-70CR-BA features multiple expansion connectors, allowing a total of 80 pins to interface with optional expansion boards. These expansion boards provide a wide range of uses to adapt to the needs of your design, and allow for enhanced flexibility of the SYG-70CP-BA/SYG-70CR-BA.

The SYG-70CP-DK/SYG-70CR-DK Development Kit includes an Expansion Board (EXP-BRKOUT) with 70-pin breakout and optional RS232, as well as a 20-pin flex cable and 50-pin flex cable. This board will allow for quicker and easier development with access to a variety of MCU signals, as well as power and ground. RS232, in conjunction with Renesas Synergy software, allows for accessing the debug console via a PC using a terminal emulator program (eg. TeraTerm, PuTTY, etc). This functionality is included in the SYG-70CP-BA/SYG-70CR-BA BSP.

Note: The 4-bit microSD Card Slot on the breakout expansion board (EXP-BRKOUT) conflicts with the on-board microSD card slot on the SYG-70CP-BA/SYG-70CR-BA, so the microSD Slot on the Expansion board should not be used.

Note: When using I/O signals on the SYG-70CP-BA/SYG-70CR-BA Expansion Connectors (J6 & J7) to connect via the customers Expansion Board to external connectors or signals, it is the customer's responsibility to provide adequate ESD protection and filtering to prevent damage to any pins that are not directly protected on the SYG-70CP-BA/SYG-70CR-BA. Any damage caused by improper connectivity is not covered under warranty.

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7.13.1 50 Pin Expansion Connector Pin Details

EXP Pin	SYG-70Cx Function	S7G2 Pin Capabilities	Notes
J7-1	GND	GND	
J7-2	P510_RXD5B/MISO5B/SCL5B_AN021	GPIO	Pin shared with Sterling-LWB
		SCI5: RXD_MISO	
		SCI5: SCL	
		ADC0: AN21	
J7-3	P509_TXD5B/MOSI5B/SDA5B_AN120	GPIO	Pin shared with Sterling-LWB
		SCI5: TXD_MOSI	
		SCI5: SDA	
		ADC1: AN20	
J7-4	P708_RXD1B/MISO1B/SCL1B_IRQ11	GPIO	Pin is MISO for most XBEE.
		SCI1: RXD_MISO	Pin is available when Nimbelink XBEE is used and SW2 is set to Nimbelink
		SCI1: SCL	
		IRQ0: IRQ11	
J7-5	P709_TXD1B/MOSI1B/SDA1B_IRQ10	GPIO	Pin is MISO for most XBEE.
		SCI1: TXD_MOSI	Pin is available when Nimbelink XBEE is used and SW2 is set to Nimbelink
		SCI1: SDA	
		IRQ0: IRQ10	
J7-6	PA13	GPIO	
		TRACE0: TDATA0	
J7-7	PA12	GPIO	
		TRACE0: TCLK	
J7-8	P408_GTIOC10BA_RXD3A/MISO3A/SCL3A_USB_ID_IRQ7	GPIO	Pin shared with XBEE socket (RXD)
		GPT10: GTIOCB	
		SCI3: RXD_MISO	
		SCI3: SCL	
		IRQ0: IRQ07	
J7-9	P409_GTIOC10AA_TXD3A/MOSI3A/SDA3A_IRQ6	GPIO	Pin shared with XBEE socket (TXD)
		GPT10: GTIOCA	
		SCI3: TXD_MOSI	
		SCI3: SDA	
		IRQ0: IRQ06	

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J7-10	GND	GND	
J7-11	USBHS_DM	USB HS D-	Dedicated USB signal
J7-12	USBHS_DP	USB HS D+	Dedicated USB signal
J7-13	PB01_CTS3B/RTS3B/SS3B_USBHS_VBUS	GPIO	
		SCI3: CTS/RTS	CTS/RTS are on same pin. Function defined in software. If CTS is chosen, External RTS (GPIO) must be used for RTS function.
		SCI3: SS	
J7-14	P706_RXD3B/MISO3B/SCL3B_USBHS_OVRCURB_IRQ7	GPIO	
		SCI3: RXD_MISO	
		SCI3: SCL	
		USBHS: OVERCURRENT	
		IRQ0: IRQ7	
J7-15	PB00_SCK3_USBHS_VBUS	GPIO	Output only due to U2 XNOR gate. Gate gives compatibility with low-true and high-true USB VBUS switches.
		SCI3: SCK	For High-true vbus switches: leave pin as input mode
		USBHS: VBUS ENABLE	For low-true vbus switches: set PB06 low to invert VBUS_EN
J7-16	P203_MOSI9A_MOSIBA_IRQ2-DS	GPIO	
		SCI9: TXD_MOSI	
		SCI2: CTS/RTS/SS	
		SPI/QSPI: MOSIB_A	
		MII: ET0_COL	
		IRQ2 - DS	
J7-17	P202_MISO9A_MISOBA_IRQ3-DS	GPIO	
		SCI9: RXD_MISO	
		SCI2: SCK	
		SPI/QSPI: MISOB_A	
		MII: ET0_ERXD2	
		IRQ3 - DS	
J7-18	P204_SCK9A_RSPCKBA	GPIO	
		SCI9: SCK	
		SCI4: SCK	
		I2C0: SCL	

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		MII: ET0_RX_DV	
		GTIOC_5A_A	
J7-19	P207_SSLB2A_TS02	GPIO	
		SPI/QSPI: SSLB2	
J7-20	P811_CTX0C	GPIO	
		CAN0: CTX	
J7-21	P812_CRX0C	GPIO	
		CAN0: CRX	
J7-22	GND	GND	
J7-23	RESET_INn	RESET_INn	From Expansion to MCU
J7-24	RESET_OUTn	RESET_OUTn	From MCU to Expansion.
J7-25	P015_AN006_DA1_IRQ13	GPIO	
		AN006/AN106	Primary DAC/ADC for Expansion
		DA1/IVCMP1	
		IRQ13	
J7-26	P008_AN003_IRQ12-DS	GPIO	
		AN003	
		IRQ12 - DS	
J7-27	P404_GTIOC3BB_ET1MDIO_PIXD6	GPIO	
		GTIOC_3B_B	
		RTCIC2	
		MII: ET1_MDIO	
		RMII: ET1_MDIO	
		PIXD6	
J7-28	P403_GTIOC3AB_ET1MDC_PIXD7	GPIO	
		GTIOC_3A_B	
		RTCIC1	
		SCI7: CTS_RTS_SS	
		SSI: SCK0	
		MII: ET1_MDC	
		RMII: ET1_MDC	
		PIXD7	
J7-29	GND	GND	
J7-30	P701_GTIOC5B_REF50CK1_PIXD2	GPIO	
		GTIOC_5B_B	
		MII: ET1_ETXD0	

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		RMII: REF50CK1	
		PIXD2	
J7-31	P704_ET1RMIIRXER_HSYNC	GPIO	
		MII: ET1_RX_CLK	
		RMII: RMII1_RX_ER	
		HSYNC	
J7-32	3.3V	3.3V	
J7-33	P703_GTIOC6B_ET1RMIIRXD1_PIXD0	GPIO	
		GTIOC_6B_B	
		MII: ET1_ERXD0	
		RMII: RMII1_RXD1	
		PIXD0	
J7-34	P702_GTIOC6A_ET1RMIIRXD0_PIXD1	GPIO	
		GTIOC_6A_B	
		MII: ET1_ERXD1	
		RMII: RMII1_RXD0	
		PIXD1	
J7-35	P705_ET1RMII_CRSDV_PIXCLK	GPIO	
		MII: ET1_CRS	
		RMII: RMII1_CRS_DV	
		PIXCLK	
J7-36	P405_GTIOC1A_ET1RMIITXDEN_PIXD5	GPIO	
		GTIOC_1A_B	
		SSI: TXD0_A	
		MII: ET1_TX_EN	
		RMII: RMII1_TXD_EN	
		PIXD5	
J7-37	P406_GTIOC1B_ET1RMIITXD1_PIXD4	GPIO	
		GTIOC_1B_B	
		SSI: RXD0_A	
		MII: ET1_RX_ER	
		RMII: RMII1_TXD1	
		PIXD4	
J7-38	P700_GTIOC5A_ET1RMIITXD0_PIXD3	GPIO	
		GTIOC_5A_B	
		MII: ET1_ETXD1	
		RMII: RMII1_TXD0	

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		PIXD3	
J7-39	GND	GND	
J7-40	P200_NMI	NMI	
J7-41	P511_GTIOC0BB_CRX1B_RXD4B/SCL4B_SDA2_IRQ15_PCKO	GPIO	
		GTIOC_0B_B	
		CAN: CRX1_B	
		SCI4: RXD_MISO	
		SCI4: SCL	
		IIC: SDA2	
		MII: ET1_TX_ER	
		IRQ15	
		PCKO	
J7-42	P512_GTIOC0AB_CTX1B_TXD4B/SDA4B_SCL2_IRQ14_VSYNC	GPIO	
		GTIOC_0A_B	
		CAN: CTX1_B	
		SCI4: TXD_MOSI	
		IIC: SCL2	
		MII: ET1_ETXD2	
		IRQ14	
		VSYNC	
J7-43	USBD_DP	USBD_DP	
J7-44	USBD_DM	USBD_DM	
J7-45	USBD_VBUS	USBD_VBUS	
J7-46	5V	5V	
J7-47	5V	5V	
J7-48	5V	5V	
J7-49	3.3V	3.3V	
J7-50	3.3V	3.3V	

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7.13.2 20 Pin Expansion Connector Pin Details:

J6-1	GND	GND	
J6-2	P707_TXD3B/MOSI3B/SDA3B_USHBS_OVRCURA_IRQ8	GPIO	
		SCI3: TXD_MOSI	
		SCI3: SDA	
		USBHS_OVRCURA	
		IRQ8	
J6-3	P806	GPIO	
J6-4	P805	GPIO	
J6-5	P813_GTIOC9BB	GPIO	
		TDATA3	
		GTIOC_9B_B	
J6-6	P912_GTIOC8AB	GPIO	
		GTIOC_8A_B	
J6-7	P911_GTIOC8BB	GPIO	
		GTIOC_8B_B	
J6-8	PA06_GTIOC10BB	GPIO	
		GTIOC_10B_B	
J6-9	PA05_GTIOC1AAB_CTS7B/RTS7B/SS7B	GPIO	
		GTIOC_11A_B	
		SCI7: CTS_RTS_SS	LAIRD STERLING-LWB SPI_CS signal
J6-10	PA04_GTIOC11B_SCK7B	GPIO	
		GTIOC_11B_B	
		SCI7: SCK7	LAIRD STERLING-LWB SPI_CLK signal
J6-11	PA03_RXD7B/MISO7B/SCL7B_IRQ9	GPIO	
		SCI7: RXD_MISO	LAIRD STERLING-LWB SPI_MISO signal
		SCI7: SCL	
		IRQ9	
J6-12	PA02_TXD7B/MOSI7B/SDA7B_IRQ10	GPIO	
		SCI7: TXD_MOSI	LAIRD STERLING-LWB SPI_MOSI signal
		SCI7: SDA	
J6-13	5V	5V	
J6-14	GND	GND	
J6-15	P005_AN101_IRQ10-DS	GPIO	INPUT ONLY
		AN101	

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		IRQ10-DS	
J6-16	P004_AN100_IRQ9-DS	GPIO	INPUT ONLY
		AN100	
		IRQ9-DS	
J6-17	P002_AN002_IRQ8-DS	GPIO	INPUT ONLY
		AN002	
		IRQ8-DS	
J6-18	P001_AN001_IRQ7-DS	GPIO	INPUT ONLY
		AN001	
		IRQ7-DS	
J6-19	P000_AN000_IRQ6-DS	GPIO	INPUT ONLY
		AN000	
		IRQ6-DS	
J6-20	GND	GND	

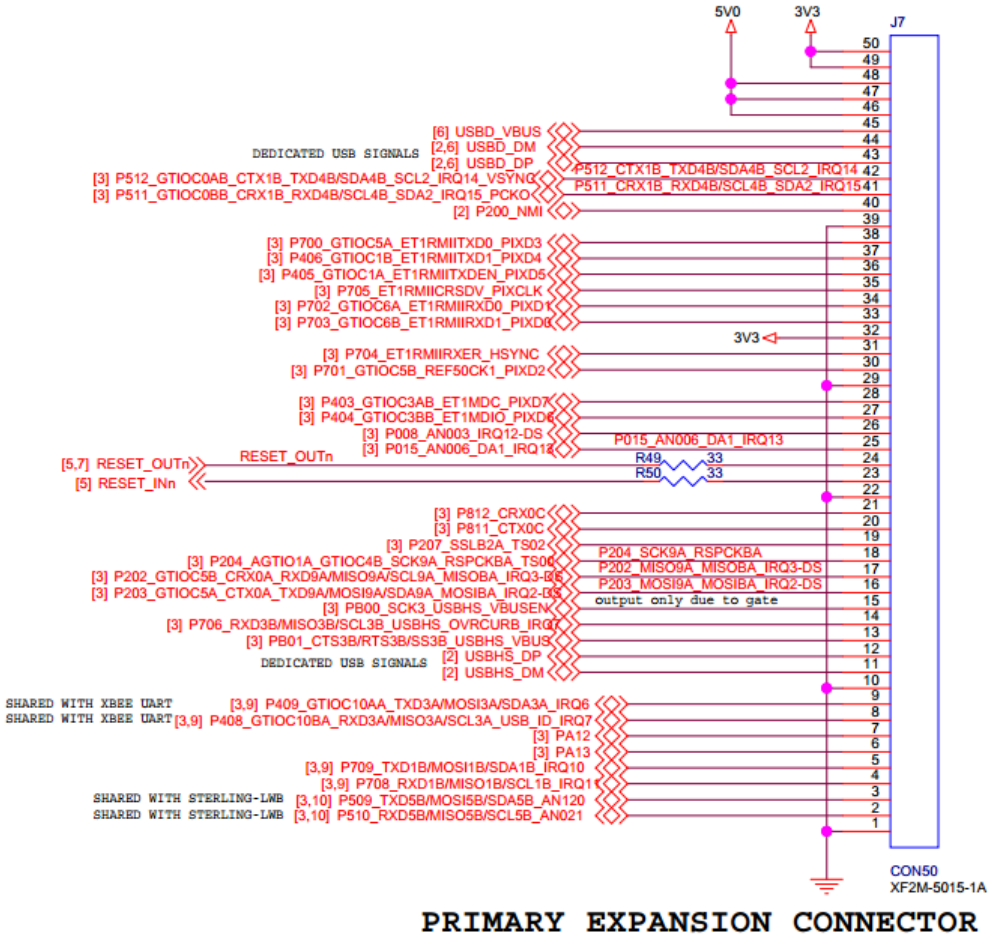
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7.13.3 50 Pin Primary Expansion Connector (J7)

The Primary Expansion Connector (J7) is a 50 pin flat cable connector that provides both dedicated and shared signals to external add-on expansion boards. The connector (Omron PN: XF2M-5015-1A) provides a small footprint and allows for 50 signals to connect to an expansion board.

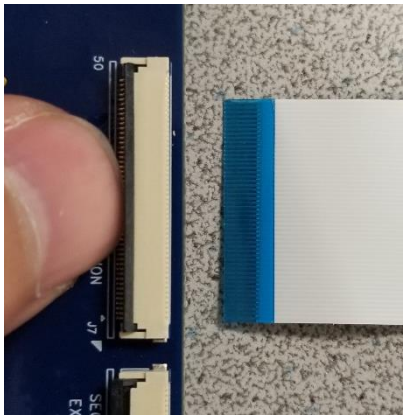
Recommended 50 Pin Cable: Molex 21020-7650
Important signals to note on the Primary Expansion Connector are:

- Dedicated USB Device and Host
- Ethernet RMII
- Multiple SCI Ports
- Multiple IRQ signals
- Multiple Analog Inputs
- Reset In (active LOW) & Reset Out (active LOW)
- 5V & 3.3V Power
- Ground

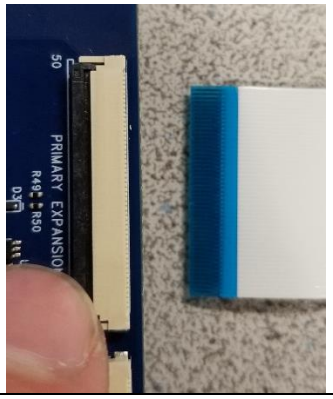


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Figure 59 - Primary Expansion Connector Schematic

1) Prepare to insert the 50-pin cable by orienting the cable to where the pins are face down. 	2) Flip up the black locking tab to prepare the socket to accept the cable. 
3) Insert the cable into the port as far as it will easily go. 	4) Press down on the black locking tab until it locks the cable firmly in place. 

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1) The cable black locking tab should be down initially. 	2) Flip up the black locking tab to prepare to remove the cable. 
3) Remove the cable from the socket. 	4) Press down on the black locking tab so the tab will not get damaged. 

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7.13.4 20 Pin Secondary Expansion Connector (J6)

The 20-pin secondary expansion connector provides additional GPIO and Analog Inputs to the SYG-70CP-BA/SYG-70CR-BA, as well as an additional 5V power pin and three ground pins. The connector (Omron PN: XF2M-2015-1A) provides a small footprint and allows for 20 additional signals for an expansion board.

Recommended 20 pin cable: Molex 21020-0209

Important signals to note on the Secondary Expansion Connector are:
SCI Port
GPIO
GTIOC
Multiple Analog Inputs
Multiple IRQ Signals
5V Power
Ground

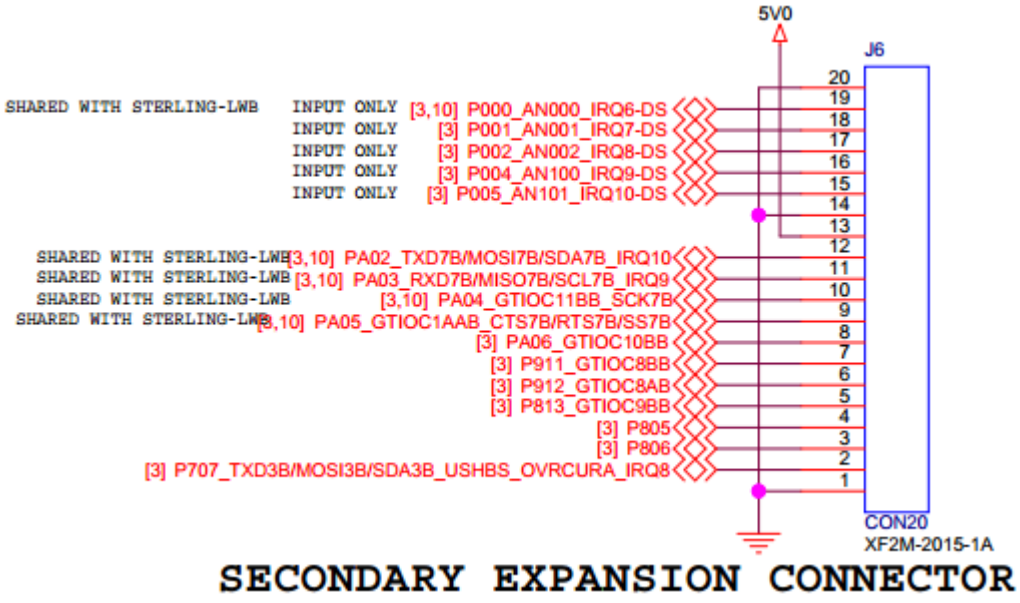
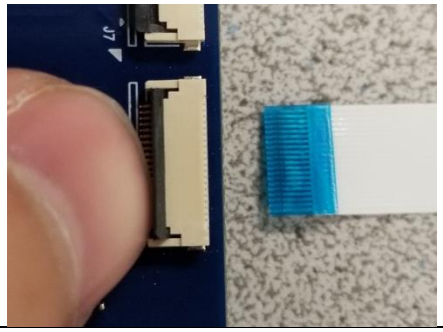
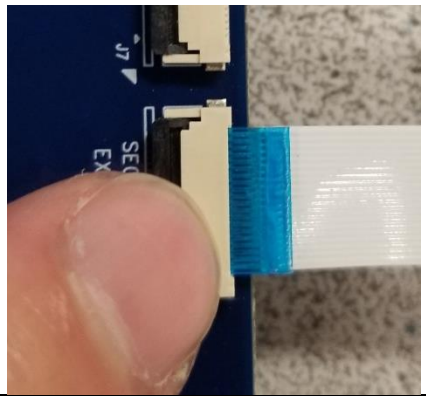
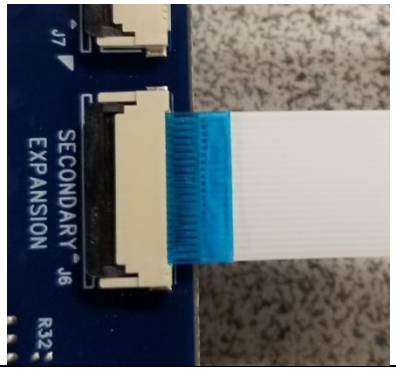
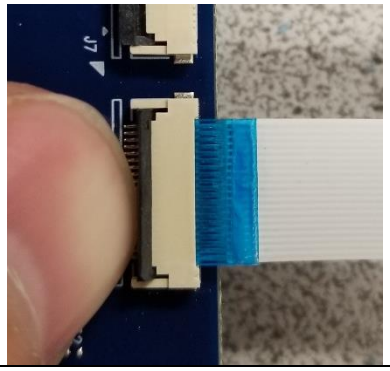
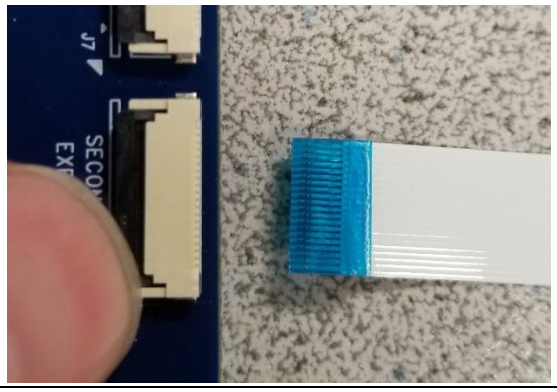


Figure 46 - Secondary Expansion Connector Schematic

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1) Prepare to insert the 20-pin cable by orienting the cable to where the pins are face down. 	2) Flip up the black locking tab to prepare the socket to accept the cable. 
3) Insert the cable into the port as far as it will easily go. 	4) Press down on the black locking tab until it locks the cable firmly in place. 

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1) The cable black locking tab should be down initially. 	2) Flip up the black locking tab to prepare to remove the cable. 
3) Remove the cable from the socket. 	4) Press down on the black locking tab so the tab will not get damaged. 

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7.13.5 10 Pin Alternate Power & Comm Interface

The SYG-70CP-BA/SYG-70CR-BA features a 10 pin alternate power & communication interface (Hirose DF13) to allow for I2C, SPI, IRQ, and Power to be quickly connected externally. This connector provides enhanced flexibility for your design.

1	**P202_MISO9A_MISOBA_IRQ3-DS**	**6**	**Ground**
2	**P203_MOSI9A_MOSIBA_IRQ2-DS**	**7**	**Ground**
3	**P204_SCK9A_RSPCKBA**	**8**	**P511_CRX1B_RXD4B/SCL4B_SDA2_IRQ15**
4	**5V Input**	**9**	**P512_CTX1B_TXD4B/SDA4B_SCL2_IRQ14**
5	**5V Input**	**10**	**P015_AN006_DA1_IRQ13**

Note: If connecting devices to this connector, the 5V power (J5 pins 4 and 5) should be a power INPUT to the SYG-70CP-BA/SYG-70CR-BA only. Do not use this connector to power external devices.

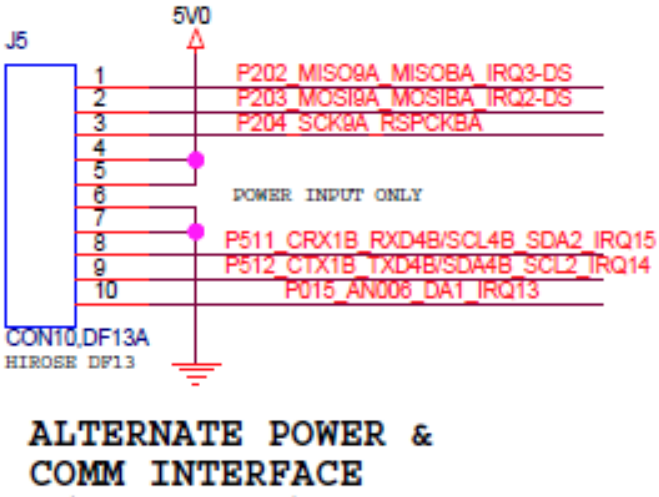


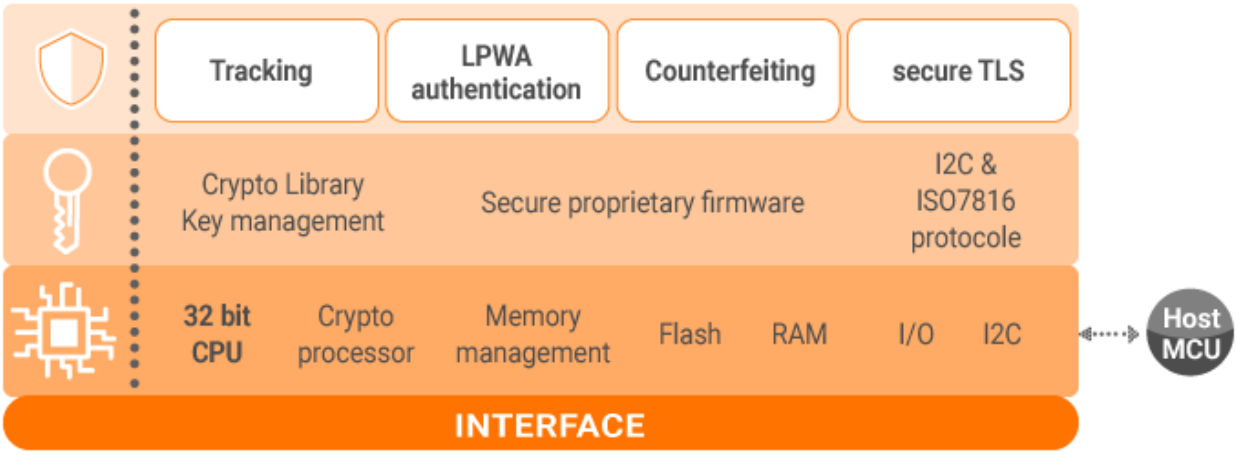
Figure 47 - Alternate Power & Communication Schematic

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8 Security – TO136 Secure Element

The TO136 Secure Element is connected as an I2C peripheral to the Renesas Synergy S7G2 MCU (Microcontroller Unit) of the SYG GUI, and features:

- Securely hosting certificates, secret keys and other customer data
- Handling of cryptography functions
- Personalization with certificates and secret keys



The TO136 is based on the state-of-the-art secure hardware designed for connected devices, featuring:

- 136KB secure flash / 4KB secure RAM
- 2.8mA active mode
- Tiny DFN6 3x3mm package
- I2C fast mode plus
- Mutual authentication to server (TLS and derivatives) or to off-line device
- TRNG: True Random Generator
- Asymmetric Cryptography: Elliptic Curves P256
- Symmetric Cryptography: AES, 3DES and SHA
- On-board Key generation
- MAC / HASH / signature

The SYG product family provides licensed drivers and other software from ubiquiOS Technology, https://www.ubiquiostechnology.com/, to make interfacing with the TO136 extremely easy, thus reducing your time to market.

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9 Programming Methods

The SYG-70CP-BA/SYG-70CR-BA features two programming headers allowing for JTAG, Single Wire Debug (SWD), or SCI Boot mode. This allows for a flexible and fast programming of software onto the SYG-70CP-BA/SYG-70CR-BA. The Boot mode is determined by the state of the MD pin, which is available on the 9-pin Cortex-M Mini JTAG header.

SCI Boot mode must be done via the 9-pin Cortex-M Mini JTAG Header.

JTAG and SWD modes can use both the 9-pin Cortex-M Mini JTAG Header and the Tag-Connect TC2050-IDC footprint.

9.1 JTAG / SWD

The MCU debug system includes two CoreSight™ Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD register

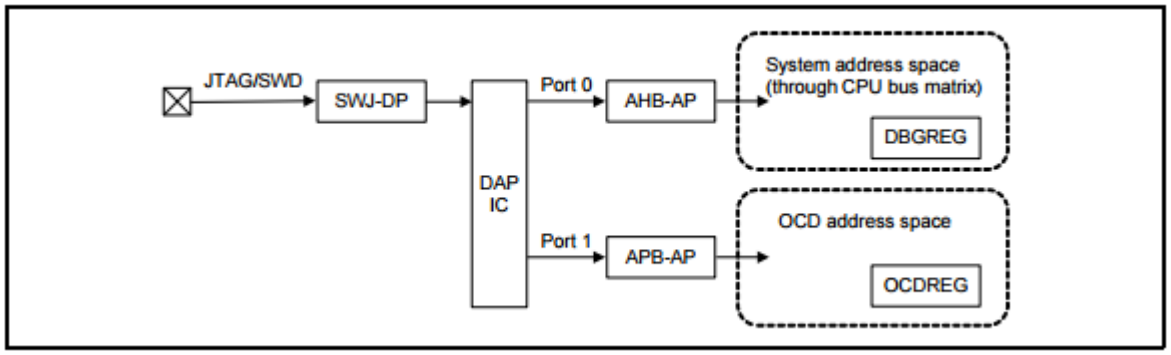


Figure 62- JTAG Block Diagram

The MCU must be in Single Chip Mode for JTAG / SWD to operate (MD = 1).

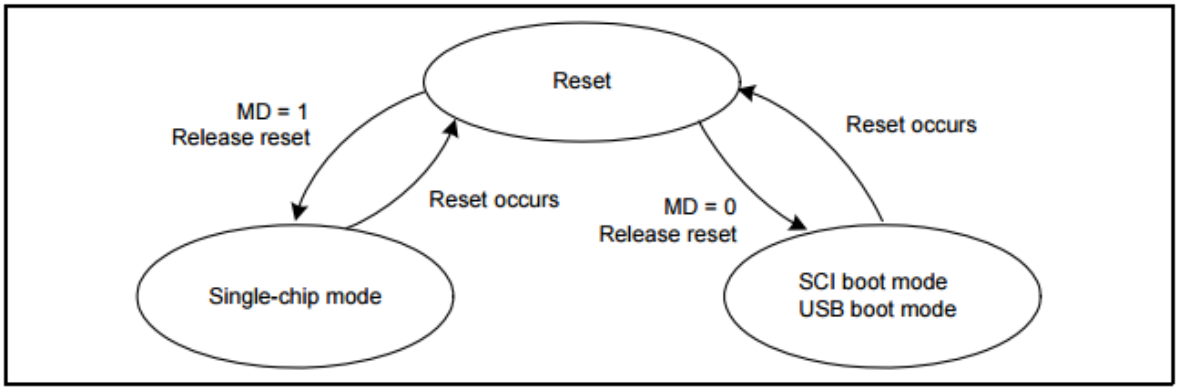


Figure 48 - JTAG Mode Selection Diagram

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Name	I/O	P/N	Width	Function	When not in use
TCK/SWCLK	Input	Pos.	1 bit	JTAG Clock Pin	Pull-up
TMS/SWDIO	I/O	Neg.	1 bit	JTAG TMS Pin Serial Wire Data in/out pin	Pull-up
TDI	Input	Pos.	1 bit	JTAG TDI Pin	Pull-up
TDO/SWO	Output	Neg	1 bit	JTAG TDO Pin Multiplexed with Serial Wire output	Open

9.2 SCI Boot

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in a dedicated area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI.

In boot mode, the host sends control commands and data for programming, and the code and data flash memory area are programmed or erased accordingly. An on-chip SCI handles transfer between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host. When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host.

The USB cable must not be connected on reset release.

Pin Name	I/O	Applicable Modes	Function
MD	Input	SCI Boot Mode USB Boot Mode (Serial Programming Mode)	Selection of Operating Mode
P110/RXD9	Input	SCI Boot Mode	For host communication, to receive data through SCI
P109/TXD9	Output	SCI Boot Mode	For host communication, to transmit data through SCI

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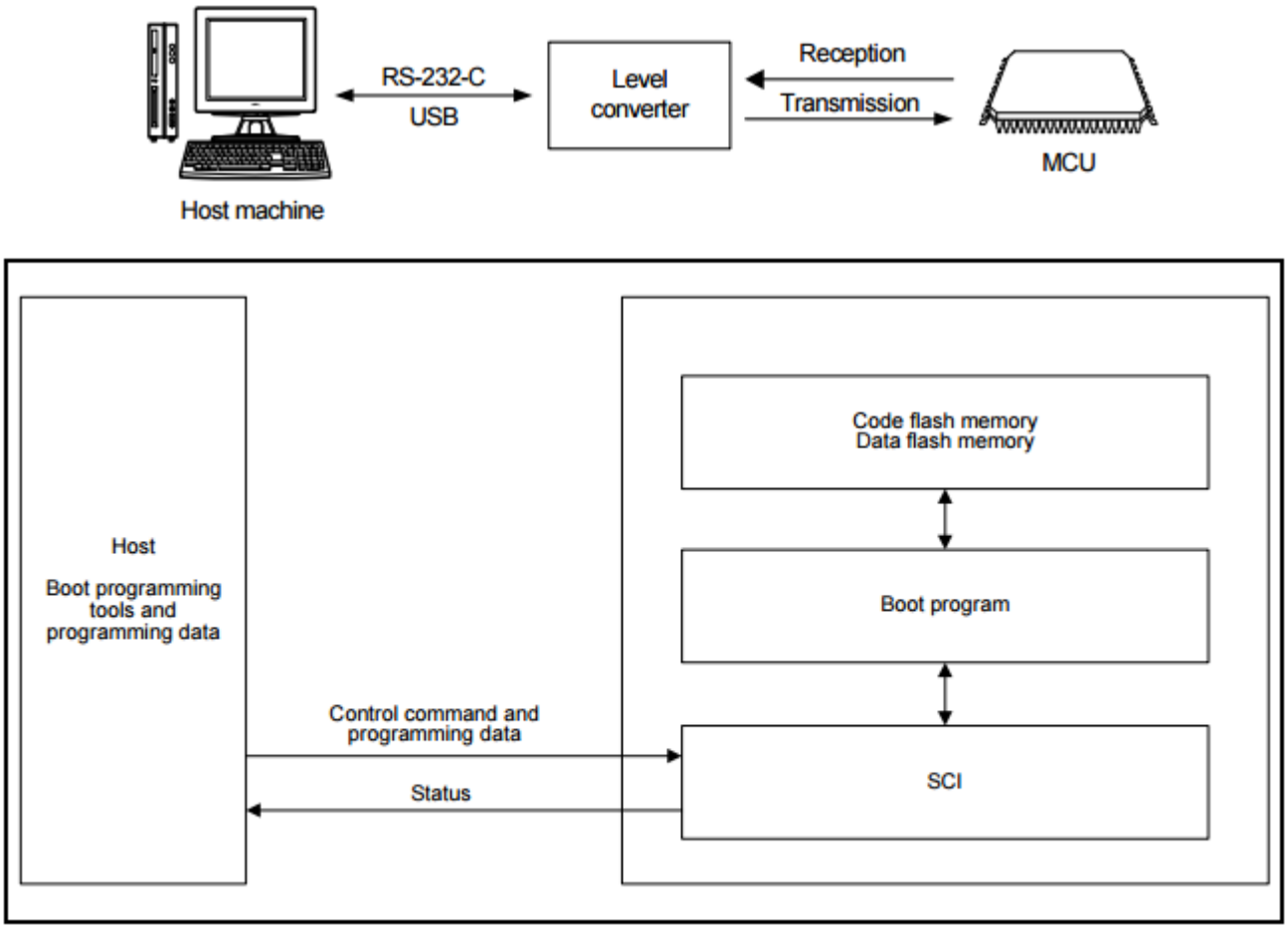


Figure 49 - SCI Programming Flow Diagram

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10 Additional Information

10.1 UbiquiOS Wireless Stack

The SYG-70CP-BA/SYG-70CR-BA features modules powered in part by software solutions from UbiquiOS™ Technology Limited. They provide a compact, integrated, interoperable, secure and easy-to-use embedded wireless stack that shortens time-to-market for applications implementing low-cost and low-power wireless connectivity. The ubiquiOS™ stack supports a wide range of microcontrollers, radio technologies, real-time operating systems (RTOS), including bare metal environments, and cloud solutions. UbiquiOS™ is based in Silicon Valley and New Zealand. For more information, please visit www.ubiquiostechnology.com

ubiquiOS™ provides a broad spectrum of functionality, including:

- Efficient embedded interface drivers for low-cost high-performance Wi-Fi transceivers
- Flexible Wireless LAN (Wireless LAN) upper Medium Access Control (MAC) and MAC Sublayer Management Entity (MLME) implementations, providing standards-based WLAN connectivity in various device roles
- A 2/3/4G cellular modem manager and Point-to-Point Protocol (PPP) endpoint
- Ethernet networking support
- A full low-resource TCP/IP network stack, including key auxiliary protocols for both client and server roles
- Broad range of upper-layer network protocols and services, including Network Time Protocol (NTP) client, Hypertext Transfer Protocol (HTTP) client/server, Universal Plug and Play (UPnP), Zeroconf/Bonjour (DNS-SD/mDNS), Domain Name System (DNS) resolver, Message Queue Telemetry Transfer (MQTT) client and others
- Cloud connectivity agents allowing simple integration with platforms such as Microsoft Azure IoT Hub, Amazon AWS IoT, IBM Bluemix, etc.
- Strong cryptography, link and transport layer security (including TLS v1.2 with Online Certificate Status Protocol (OCSP) and hardware secure element integration) for authentication and privacy in network communications, and for application-specific requirements
- An extensible "test engine" which allows implementation of scripted test of ubiquiOS-based products for validation, interoperability test, and certification
- Powerful libraries to facilitate easy application and protocol development in a resource- constrained environment, including for packet and stream management
- An efficient and lightweight operating system abstraction layer including memory management, and timer/task services to enable fastest time to market on an otherwise bare-metal system, or easy integration within a third-party operating system or application framework

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10.1.1 ubiquiOS License Key

During factory production of the SYG modules, FDI programs a ubiquiOS License Key into the S7G2 Data Flash. This License Key enables all functionality of the ubiquiOS software. The license key is located at address 0x4010FF80 (Data Flash Block 1022). If you somehow erase the license key from this location, you must replace it prior to using ubiquiOS software. If you do not know how to determine your ubiquiOS License Key, send a support email to support@TeamFDI.com and ask.

10.2 70-pin Breakout Expansion Board

The SYG-70CP-DK/SYG70-CR-DK Development Kit includes a 70-pin breakout expansion board (UEZGUI-EXP-BRKOUT) with optional RS232. This board allows for easy prototyping of hardware for use with FDI's GUI Family of products. The expansion board features an optional RS232 port for PC communications, and has load options to support the use of Flash Magic as an ISP programmer. Optional Power status LEDs, and DC Power Jack are also available.

Also included is a 50 pin & 20 pin flex cable to connect the EXP-BRKOUT board to the SYG-70CP-BA/SYG-70CR-BA.

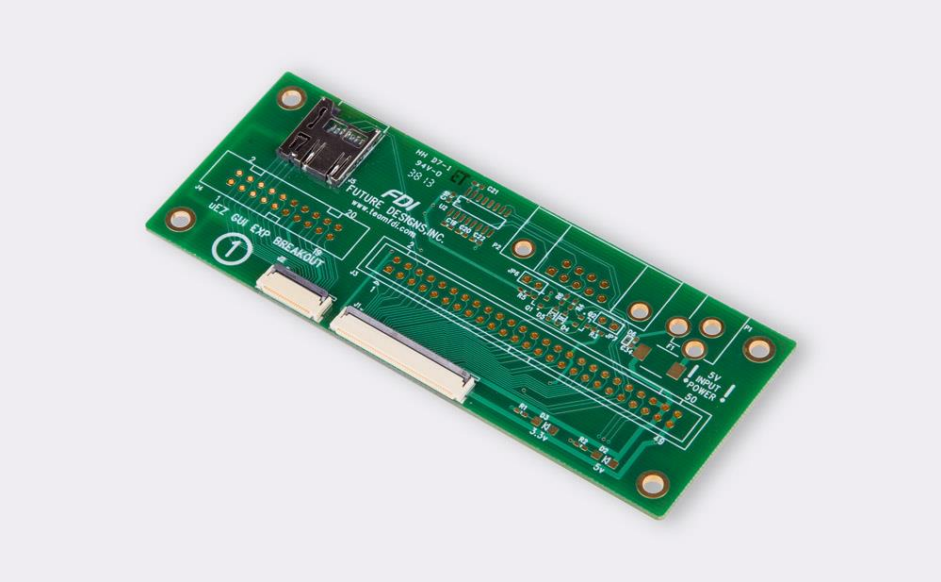


Figure 504 - EXP BRKOUT Board

Note: The EXP-BRKOUT board includes a microSD card slot. However, this microSD card slot is NOT compatible with the SYG-70CP-BA/SYG-70CR-BA, so just use the microSD card slot native to the SYG-70CP-BA/SYG-70CR-BA.

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10.3 Additional Expansion Board Support

FDI offers additional expansion boards for our GUI based products, with compatibility determined on a per-product basis.

The EXP1 Expansion board (available from www.teamfdi.com/product-details/uezgui-exp1) is one example expansion board that provides:

- 50-pin I/O Connection
- RS232/RS485 Serial Communication via DB9
- USB Host and USB Device
- 10/100 Ethernet with status LEDs
- DC Power Jack for external wall power
- 3.3V and 5V Power LEDs

Other expansion boards may be available to meet the needs of your project. For more information, visit https://www.teamfdi.com/ or contact us at https://www.teamfdi.com/support/

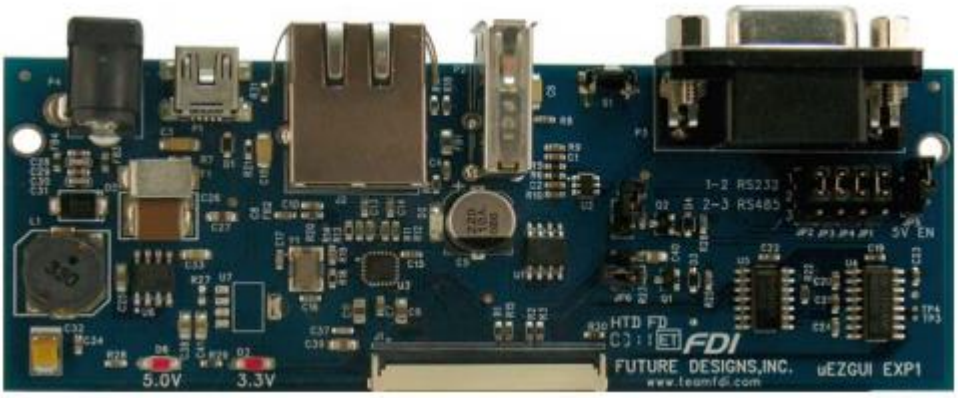


Figure 65- EXP1 Expansion Board

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10.3.1 Configuration Data in Data Flash

The following information is put into non-volatile flash during factory programming:

- ubiquiOS License Key (99 bytes)
- Valid Configuration (1 byte)
- Major Hardware Version (1 byte)
- Minor Hardware Version (1 byte)
- MAC Address (1 byte)
- ubiquiOS Key Number (9 bytes)
- Serial Number (6 bytes)
- Reserved (5 bytes)

This data is saved in the following structure:

```
typedef struct {
   uint8_t iUbiquiosKey[99];          // 99
   uint8_t iValidConfigurations;      // 100
   uint8_t iHWMajor;                  // 101
   uint8_t iHWMinor;                  // 102
   uint8_t iMACAddress[6];            // 108 Not Assigned to SYG units yet
   uint8_t iUbiquiosKeyNumber[9];  // 117
   uint8_t iUnitSerialNumber[6]; // 123
   uint8_t iReserved[5];              // 128
}T_ConfigurationData;
```

Configuration data is stored at the first 128 bytes starting at 0x4010FF80.

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11 Support

11.1 Where to Get Help

Online technical support is available at https://www.teamfdi.com/support/

11.2 Useful Links

- SYG-70CP-BA Product Page: https://www.teamfdi.com/product-details/syg-70cp-ba
- SYG-70CP-DK Product Page: https://www.teamfdi.com/product-details/syg-70cp-dk
- SYG-70CR-BA Product Page: https://www.teamfdi.com/product-details/syg-70cr-ba
- SYG-70CR-DK Product Page: https://www.teamfdi.com/product-details/syg-70cr-dk
- Future Designs, Inc. Forums: https://www.teamfdi.com/?post_type=forum
- Renesas Synergy Gallery: https://synergygallery.renesas.com
- SEGGER J-Link LITE: https://www.segger.com/jlink-lite-cortexm.html
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