IS31FL3747

12×12 DOTS MATRIX LED DRIVER

November 2024

GENERAL DESCRIPTION

The IS31FL3747 is a general purpose 12 × n (n=1~12) LED Matrix programmed via 12MHz SPI or 30MHz VSB compatible interface. Each LED can be dimmed individually with 8-bit PWM or 12-bit PWM data and 8-bit DC scaling data which allowing 256 steps or 4096 steps of linear PWM dimming and 256 steps of DC current adjustable level.

Additionally, each LED open and short state can be detected, IS31FL3747 store the open or short information in Open-Short Registers. The Open-Short Registers allowing MCU to read out via VSB or SPI interface, inform MCU whether there are LEDs open or short and the locations of open or short LEDs.

The IS31FL3747 operates from 2.7V to 5.5V and features a very low shutdown and operational current.

IS31FL3747 is available in QFN-40 (5mm×5mm) and WLCSP-36 packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

APPLICATIONS

- LED display for hand-held devices
- Gaming device (Keyboard, mouse etc.)
- LED in white goods application

FEATURES

- Supply voltage range: 2.7V to 5.5V
- Support 12 × n (n=1~12) LED matrix configurations
- Dual IS31FL3747 cascade connection support 24 × n (n=1~24) LED matrix configurations.
- Individual 12-bit, 8-bit and 8+4-bit PWM control steps
- Individual 8-bit DC current steps
- Global 8-bit current setting
- Maximum 32MHz with spread spectrum (SSP).
- 12MHz SPI or 30MHz VSB
- State lookup registers
- Individual open and short detect function
- 180-degree phase delay operation to reduce power noise
- De-Ghost
- ±7.5% (Max.) at 47.8mA channel to channel matching
- ±4% (Max.) at 47.8mA device to device accuracy
- Operating temperature: -40°C to 125°C
- QFN-40 (5mm×5mm) and WLCSP-36 packages
- RoHS & Halogen-Free Compliance
- TSCA Compliance

TYPICAL APPLICATION CIRCUIT

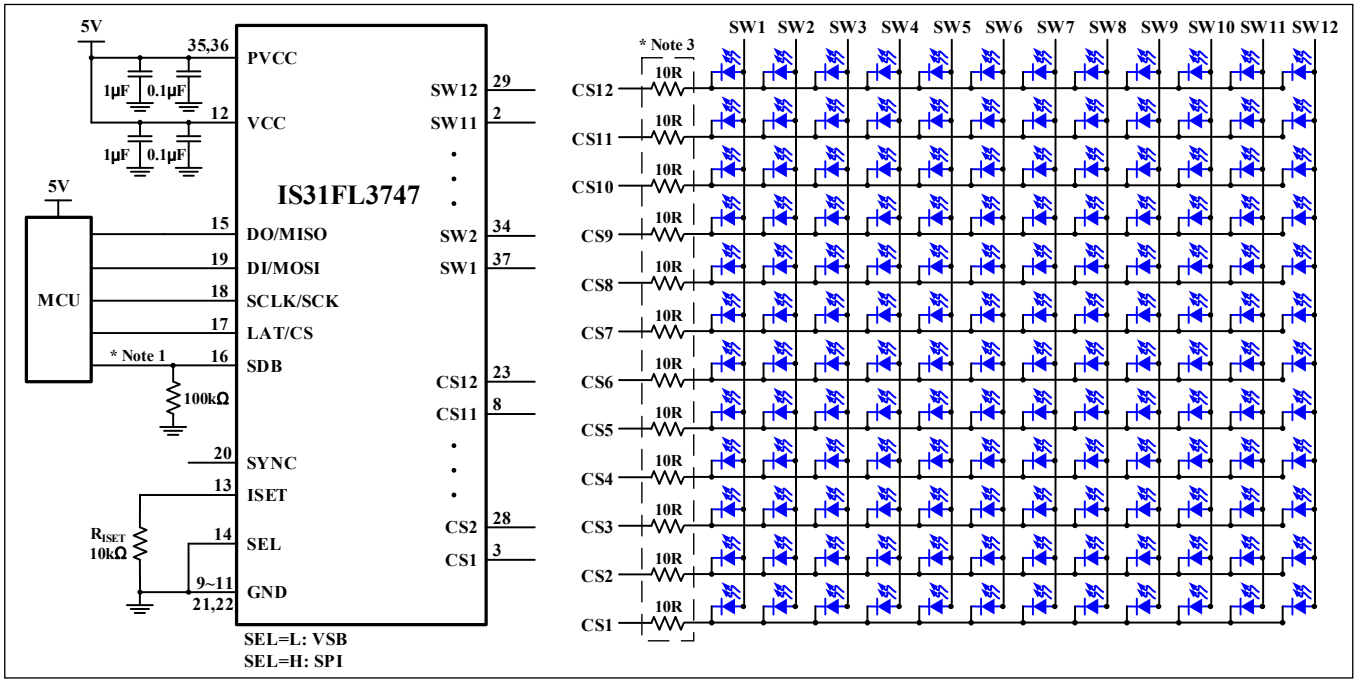


Figure 1 Typical Application Circuit: VSB/SPI Interface, 12×12 Array

TYPICAL APPLICATION CIRCUIT (CONTINUED)

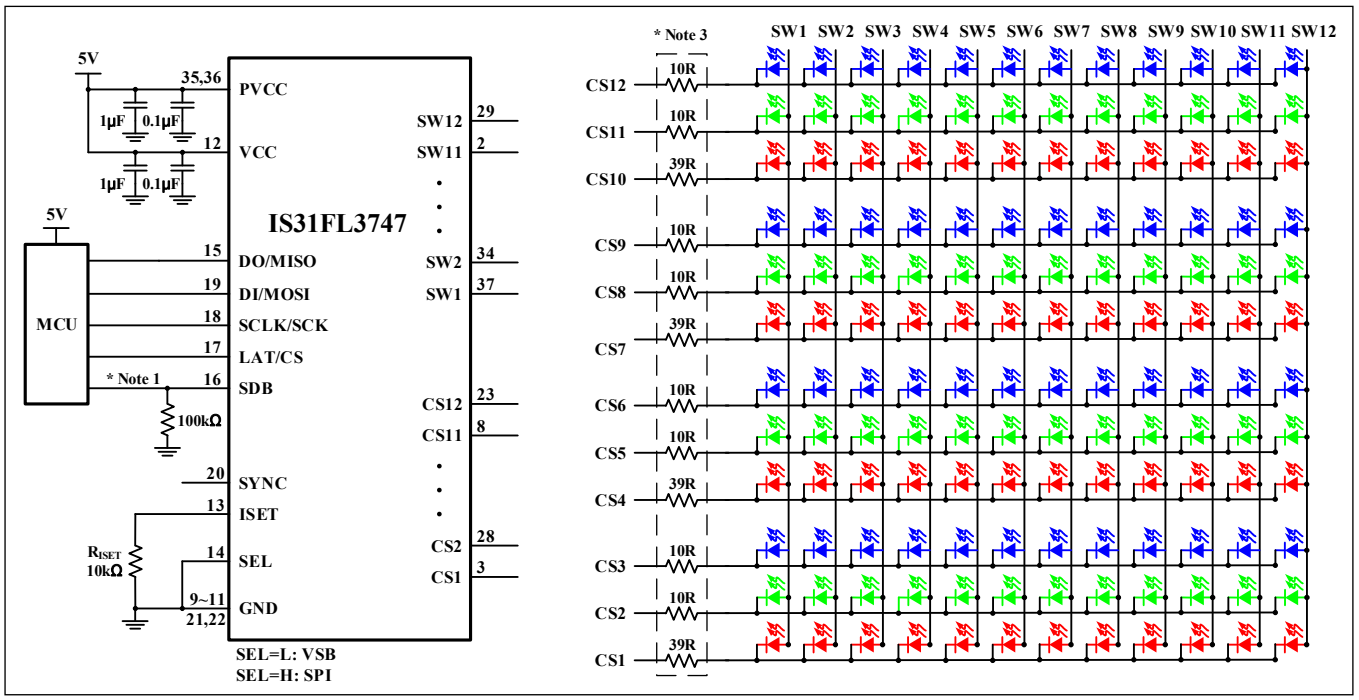


Figure 2 Typical Application Circuit: VSB/SPI Interface, 48 RGBs

Note 1: SDB Logic "1" input voltage is $0.8V_{CC}$, if the MCU V_{OH} is 3.3V, need to connect the SDB pin to 5V.

Note 2: PVCC and VCC should use same power supply to avoid the additional I_{SD}, it is recommended to use PV_{CC}=V_{CC}=5V.

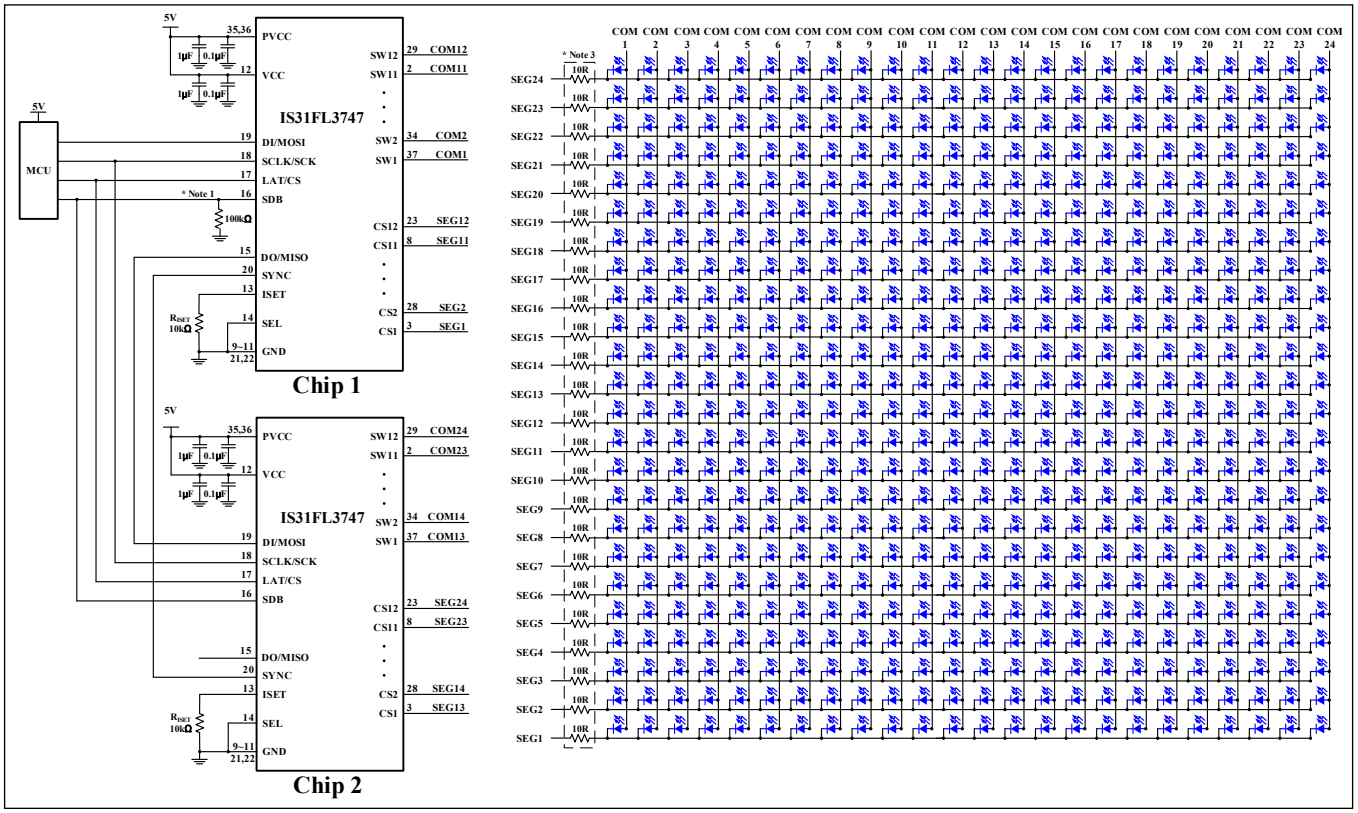


Figure 3 Typical Application Circuit: VSB Interface, 24×24 Array

TYPICAL APPLICATION CIRCUIT (CONTINUED)

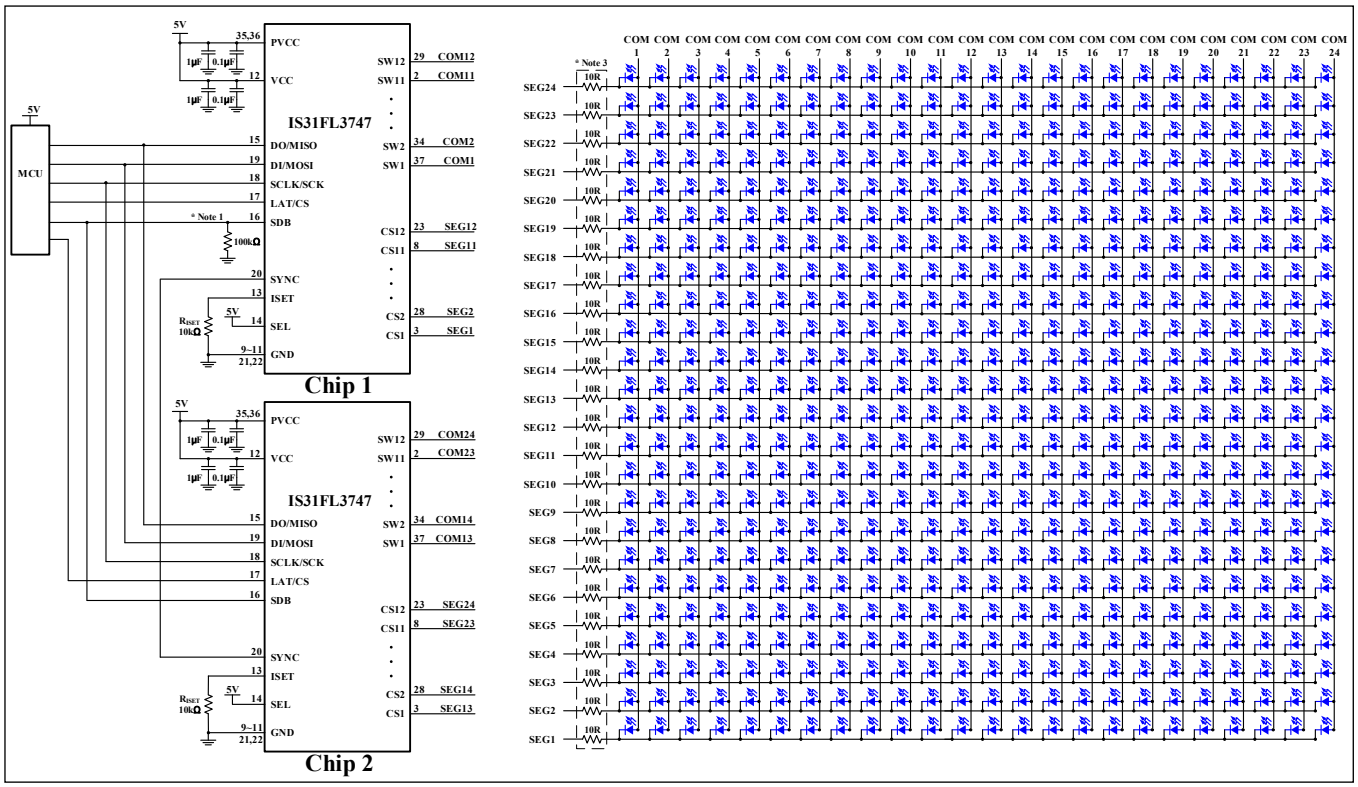
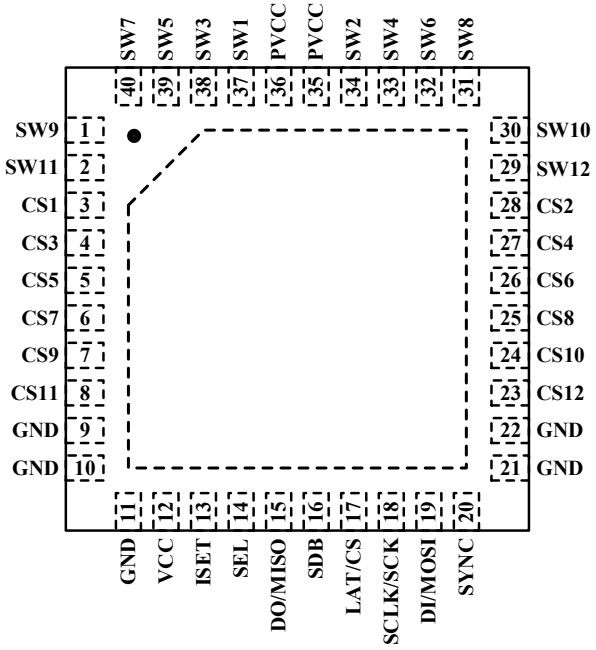
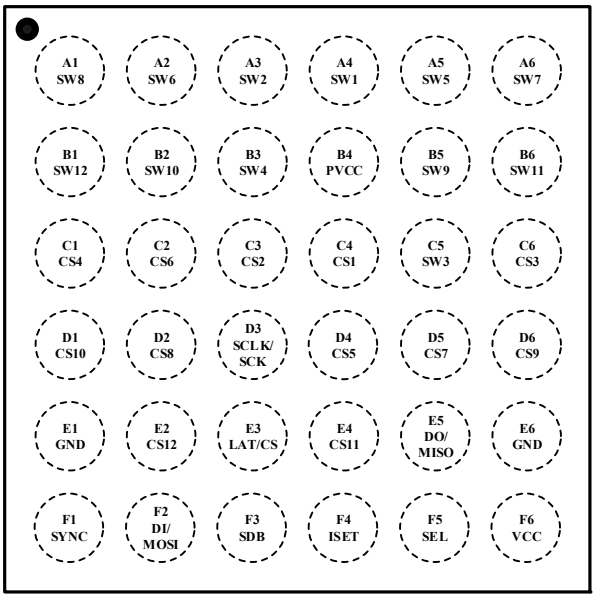


Figure 4 Typical Application Circuit: SPI Interface, 24×24 Array

Note 3: These optional resistors are for offloading the thermal dissipation ($P=I^2R$) away from the IS31FL3747, it is optional or 10Ω for white/blue/green LEDs, 39Ω recommended for red/yellow/orange LEDs.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-40	
WLCSP-36	

PIN DESCRIPTION (QFN)

No.	Pin	Description
37, 34, 38, 33, 39,32, 40, 31, 1, 30, 2, 29	SW1~SW12	Power SW.
3,28,4,27,5,26,6,25, 7,24,8,23	CS1~CS12	Current sink pin for LED matrix.
9~11, 21,22	GND	Analog GND.
12	VCC	Analog and digital circuits.
13	ISET	Set the maximum IOUT current.
14	SEL	Select SPI or VSB.
15	DO/MISO	VSB output data / MISO of SPI.
16	SDB	Shutdown pin.
17	LAT/CS	VSB latch / CS of SPI.
18	SCLK/SCK	VSB clock / SPI clock.
19	DI/MOSI	VSB input data / SPI input data.
20	SYNC	Synchronization.
35,36	PVCC	Power for current source SW.
	Thermal Pad	Need to connect to GND.

PIN DESCRIPTION (WLCSP)

No.	Pin	Description
A4, A3, C5, B3, A5, A2, A6, A1, B5, B2, B6, B1	SW1~SW12	Power SW.
C4, C3, C6, C1, D4, C2, D5, D2, D6, D1, E4, E2	CS1~CS12	Current sink pin for LED matrix.
E1, E6	GND	Analog GND.
F6	VCC	Analog and digital circuits.
F4	ISET	Set the maximum IOUT current
F5	SEL	Set SPI or VSB
E5	DO/MISO	VSB output data / MISO of SPI.
F3	SDB	Shutdown pin.
E3	LAT/CS	VSB latch / CS of SPI.
D3	SCLK/SCK	VSB clock / SPI clock.
F2	DI/MOSI	VSB input data / SPI input data.
F1	SYNC	Synchronization.
B4	PVCC	Power for current source SW.

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS31FL3747-QFLS4-TR	QFN-40, Lead-free	2500
IS31FL3747-CLS4-TR	WLCSP-36, Lead-free	

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a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~+150°C
Operating temperature range, T_A=T_J	-40°C ~ +125°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	31°C/W (QFN) 52.7°C/W (WLCSP)
ESD (HBM) ESD (CDM)	±8kV ±750V

Note 4: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC}=5V, V_{SDB}=V_{CC}, normal operation, GCC=0xFF, PWM=0x00, OSC=16MHz, SWx Pull Down Voltage= floating, CSy Pull Up Voltage= floating, C8h (Update Register) written "0000 0000"		3.8	5	mA
		V_{CC}=3.6V, V_{SDB}=V_{CC}, normal operation, GCC=0xFF, PWM=0x00, OSC=16MHz, SWx Pull Down Voltage= floating, CSy Pull Up Voltage= floating, C8h (Update Register) written "0000 0000"		2.9	4	mA
I_{SD}	Shutdown current	V_{CC}=5V, V_{SDB}=0V		2.2	3.0	µA
		V_{CC}=5V, V_{SDB}= V_{CC}, Configuration Register written "0000 0000"		2.2	3.0	
		V_{CC}=3.6V, V_{SDB}=0V		1	1.7	
		V_{CC}=3.6V, V_{SDB}= V_{CC}, Configuration Register written "0000 0000"		1	1.7	
I_{OUT}	Maximum constant current of CSy	R_{ISET}=10kΩ, GCC=0x0FF, SL=0xFF, V_{OUT}= 0.6V	43.5	47.8	52.1	mA
ΔI_{OUT}	I_{OUT} mismatch between channels	R_{ISET} = 10kΩ, GCC= 0xFF, Scaling= 0xFF (Note 5)	-7.5		7.5	%
ΔI_{MAT}	I_{OUT} accuracy between devices	R_{ISET} = 10kΩ, GCC= 0xFF, Scaling= 0xFF (Note 6)	-4		4	%

ELECTRICAL CHARACTERISTICS (CONTINUE)

The following specifications apply for V_{CC}= 5V, T_A= 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{HR}	Current switch headroom voltage SWx	I_{SWITCH}=400mA R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF		200	400	mV
	Current switch headroom voltage SWx (only for QFN-40 Package)	I_{SWITCH}=800mA, R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF		350	650	
	Current sink headroom voltage CSy	I_{SINK}=47.8mA, R_{ISET}=10kΩ		290	510	
t_{CSON}	CS-ON time during scan, the CSy are all on during this time	R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF, OSC=16MHz, 8bit PWM Mode	14.5	17.1	20.5	µs
		R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF, OSC=16MHz, 12bit PWM Mode	233	273	313	µs
t_{CSOFF}	CS-OFF time during scan, the CSy are all off during this time	R_{ISET}=10kΩ, GCC=0xFF, SL=0xFF, OSC=16MHz	1.45	1.85	2.25	µs
t_{NOL}	Delay total time for CS1 to CS 12, during this time, the SWx is on but CSy is not all turned on	(Note 7)	0.105	0.125	0.145	µs
T_{SD}	Thermal shutdown	(Note 7)		165		°C
T_{SD_HY}	Thermal shutdown hysteresis	(Note 7)		20		°C
V_{OD}	LED open detect threshold	V_{CC}=5V, R_{ISET}=10kΩ, I_{OUT}≥0.1mA, measured at CSy	0.065	0.12		V
V_{SD}	LED short detect threshold	V_{CC}=5V, R_{ISET}=10kΩ, I_{OUT}≥0.1mA, measured at CSy (V_{CC}-V_{CSy})	0.65	0.95		V
Logic Electrical Characteristics (SCLK/SCK, DO/MISO, DI/MOSI, LAT/CS, SDB, SYNC)						
V_{IL}	Logic “0” input voltage (SCLK/SCK, DO/MISO, DI/MOSI, LAT/CS, SYNC)	V_{CC}=2.7V~5.5V			V_{CC}×0.2	V
	Logic “0” input voltage (SDB)	V_{CC}=2.7V~5.5V			V_{CC}×0.4	V
V_{IH}	Logic “1” input voltage (SCLK/SCK, DO/MISO, DI/MOSI, LAT/CS, SYNC)	V_{CC}=2.7V~5.5V	V_{CC}×0.5			V
	Logic “1” input voltage (SDB)	V_{CC}=2.7V~5.5V	V_{CC}×0.8			V
V_{OH}	H level MISO/DO pin output voltage	I_{OH}= -8mA	V_{CC}-0.4V		V_{CC}	V
V_{OL}	L level MISO/DO pin output voltage	I_{OL}= 8mA	0		0.4	V
V_{HYS}	Input Schmitt trigger hysteresis	V_{CC}=3.6V (Note 7)		0.2		V
I_{IL}	Logic “0” input current	SDB=L, V_{INPUT} = L (Note 7)		5		nA
I_{IH}	Logic “1” input current	SDB=L, V_{INPUT} = H (Note 7)		5		nA

DIGITAL INPUT SPI SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		12	MHz
t_{SLCH}	CS active set-up time	34			ns
t_{SHCH}	CS not active set-up time	17			ns
t_{SHSL}	CS detect time	167			ns
t_{CHSH}	CS active hold time	34			ns
t_{CHSL}	CS not active hold time	17			ns
t_{CH}	Clock high time	34			ns
t_{CL}	Clock low time	34			ns
t_{CLCH}	Clock rise time			9	ns
t_{CHCL}	Clock fall time			9	ns
t_{DVCH}	Data in set-up time	7			ns
t_{CHDX}	Data in hold time	9			ns
t_{SHQZ}	Output disable time			34	ns
t_{CLQV}	Clock low to output valid			39	ns
t_{CLQX}	Output hold time	0			ns
t_{QLQH}	Output rise time			17	ns
t_{QLQH}	Output fall time			17	ns

DIGITAL INPUT VSB SWITCHING CHARACTERISTICS (NOTE 7)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock frequency	-		30	MHz
t_{WH0}	SCLK High Pulse duration	10			ns
t_{WL0}	SCLK Low Pulse duration	10			ns
t_{SU0}	DI to SCLK rising edge Setup time	5			ns
t_{SU1}	LAT falling edge to SCLK rising edge	30			ns
t_{H0}	SCLK rising edge to DI Hold time	2			ns
t_{H1}	SCLK rising edge to LAT rising edge Hold time	5			ns
t_{R0}	DO rise time		3	5	ns
t_{R1}	DO fall time		3	5	ns
t_{D0}	SCLK rising edge to DO recommend delay time		20	30	ns

Note 5: I_{OUT} mismatch (between channels) is calculated:

$$\Delta I_{MAT} = \left(\frac{I_{OUTn}(n=12)}{\left(\frac{I_{OUT1} + I_{OUT2} + ... + I_{OUT12}}{12} \right)} - 1 \right) \times 100\%$$

Note 6: I_{OUT} accuracy (between devices) is calculated:

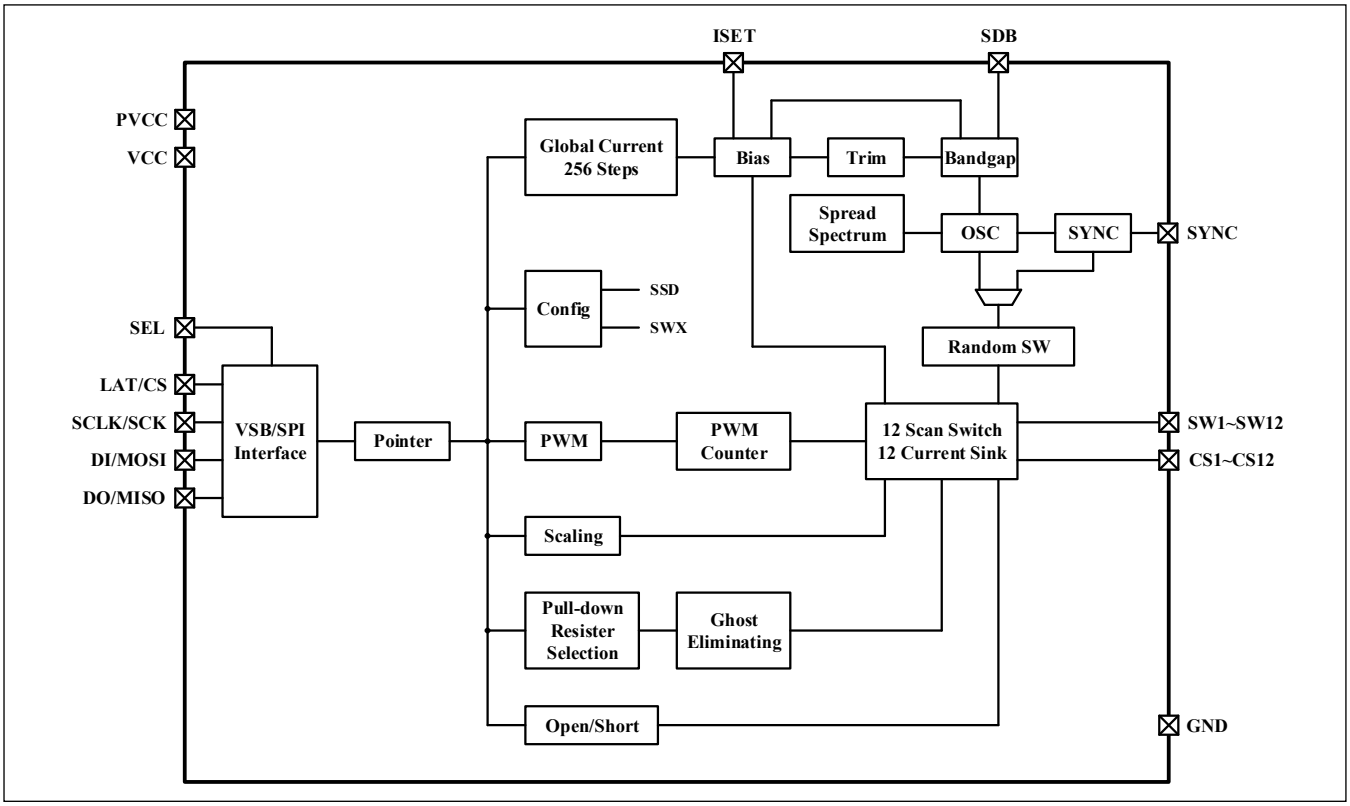
$$\Delta I_{MAX} = \left(\frac{\left(\frac{I_{OUT1} + I_{OUT2} + ... + I_{OUT12}}{12} - I_{OUT(IDEAL)} \right)}{I_{OUT(IDEAL)}} \right) \times 100\%$$

Where $I_{OUT(IDEAL)}$= 47.8mA (R_{ISET}= 10kΩ, GCC= 0xFF, Scaling= 0xFF, PWM= 0xFF).

Note 7: Guaranteed by design.

Note 8: The recommended minimum value of R_{ISET} is 10kΩ.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

SPI INTERFACE

IS31FL3747 uses a SPI protocol to control the chip's function with four wires: CS, SCK, MOSI and MISO. SPI transfer starts form CS pin from high to low controlled by Master (Microcontroller), and IS31FL3747 latches data when clock rising.

SPI data format is 8-bit length. The first command byte composite of 1-bit R/W bit, 3-bit chip ID bit and 4-bit page bit. The command byte must be sent first, and is followed by register address byte then the register data. If the R/W bit is "0", it will be writing operation and Master (Micro-controller) can write the register data into the register.

The maximum SCK frequency supported in IS31FL3747 is 12MHz.

Table 1 SPI Command Byte

Name	R/W	ID bit	Page No.
Bit	D7	D6:D4	D3:D0
Value	0: Write 1: Read	101	0x00: Point to Page 0 0x01: Point to Page 1 0x02: Point to Page 2 0x03: Point to Page 3 0x04: Point to Page 4 0x05: Point to Page 5

ADDRESS AUTO INCREMENT

To write multiple bytes of data into IS31FL3747, load the address of the data register that the first data byte is intended for. During the 8th rising edge of receiving the data byte, the internal address pointer will increment by one. The next data byte sent to IS31FL3747 will be placed in the new address, and so on. The auto increment of the address will continue as long as data continues to be written to IS31FL3747 (Figure 9).

READING OPERATION

Page 0~Page 5 registers can be read by SPI.

To read the registers of Page 0 thru Page 5, The D7 of the Command Byte need to be set to "1" and select the page number. If read one register, as shown in Figure 10, read the MISO data after sending the command byte and register address. If read more registers, as shown in Figure 10, the register address will auto increase during the 8th rising edge of receiving the last bit of the previous register data.

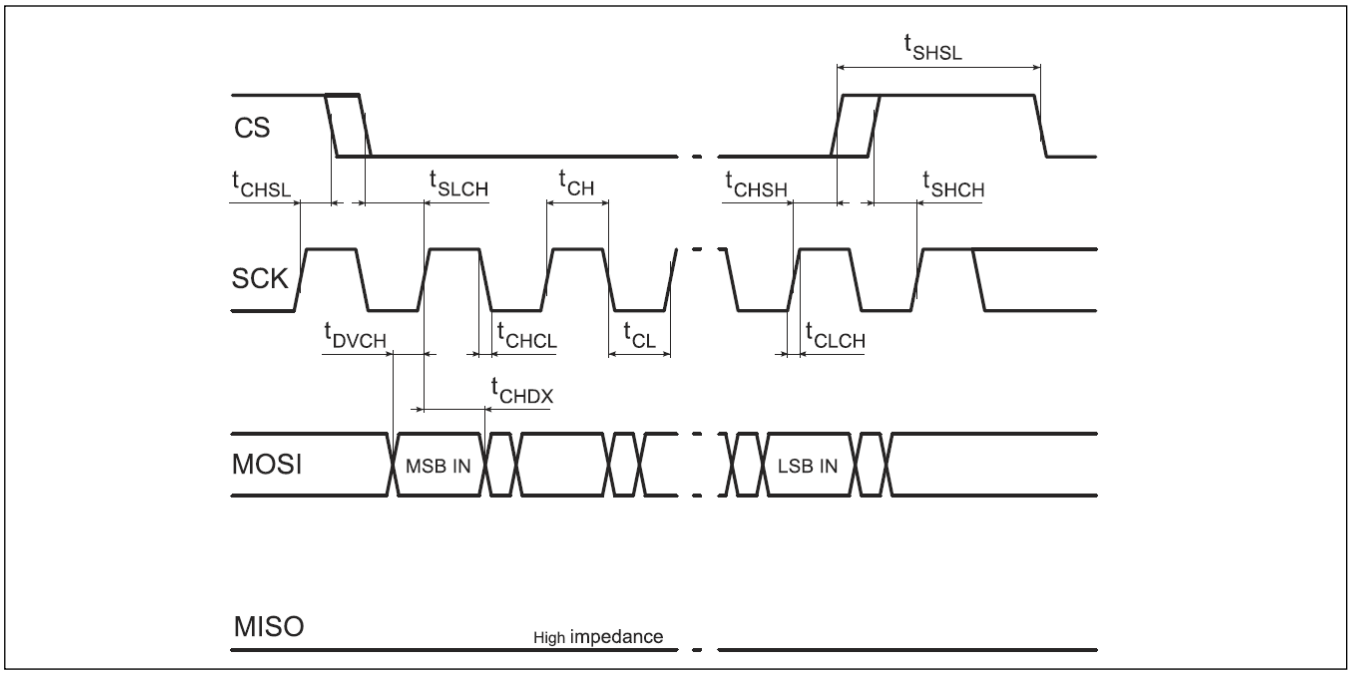


Figure 5 SPI Input Timing

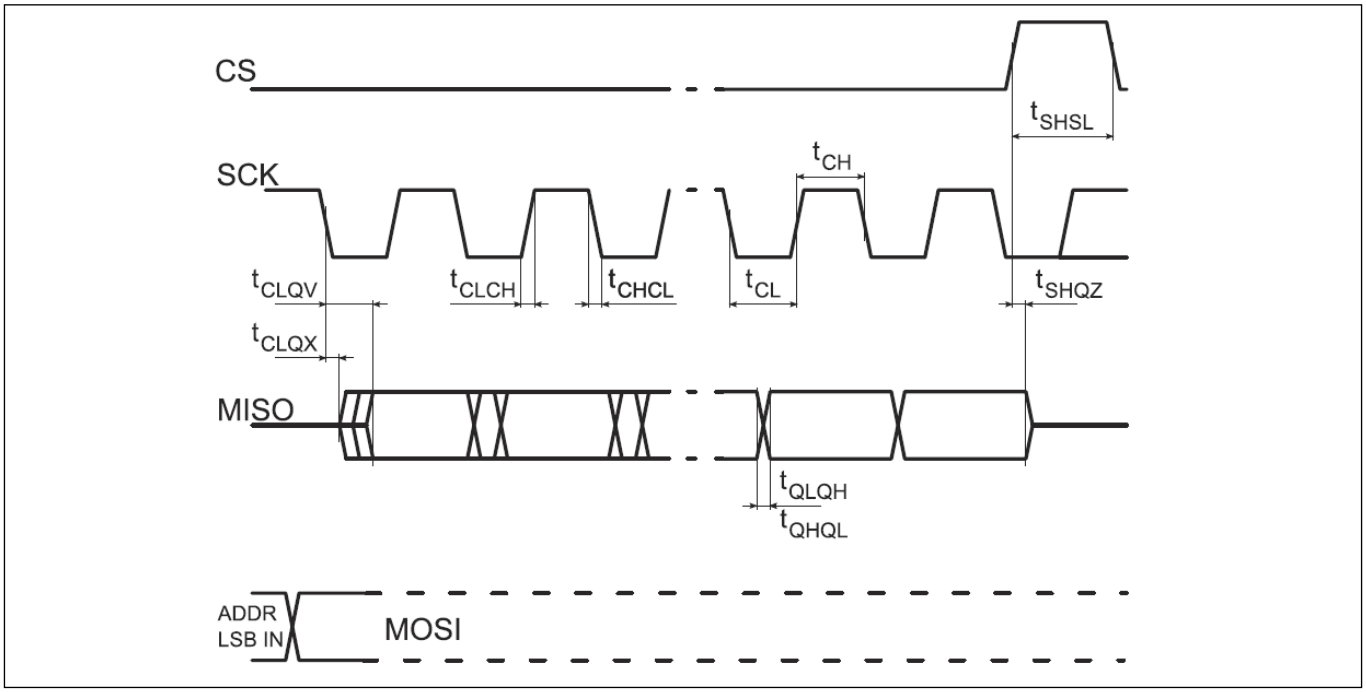


Figure 6 SPI Input Timing

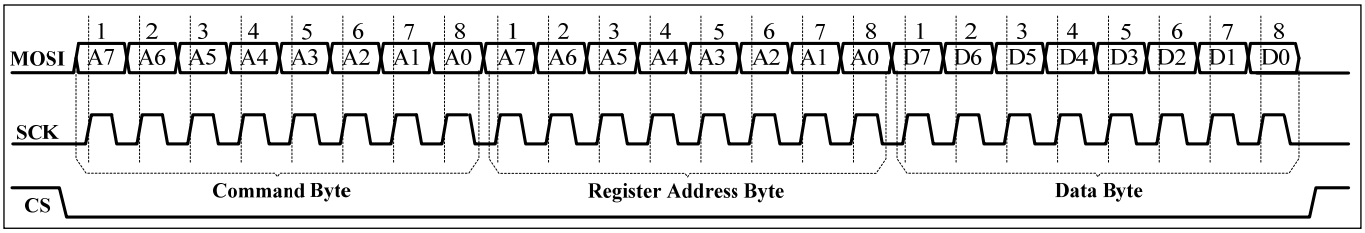


Figure 7 SPI Writing to IS31FL3747 (Typical)

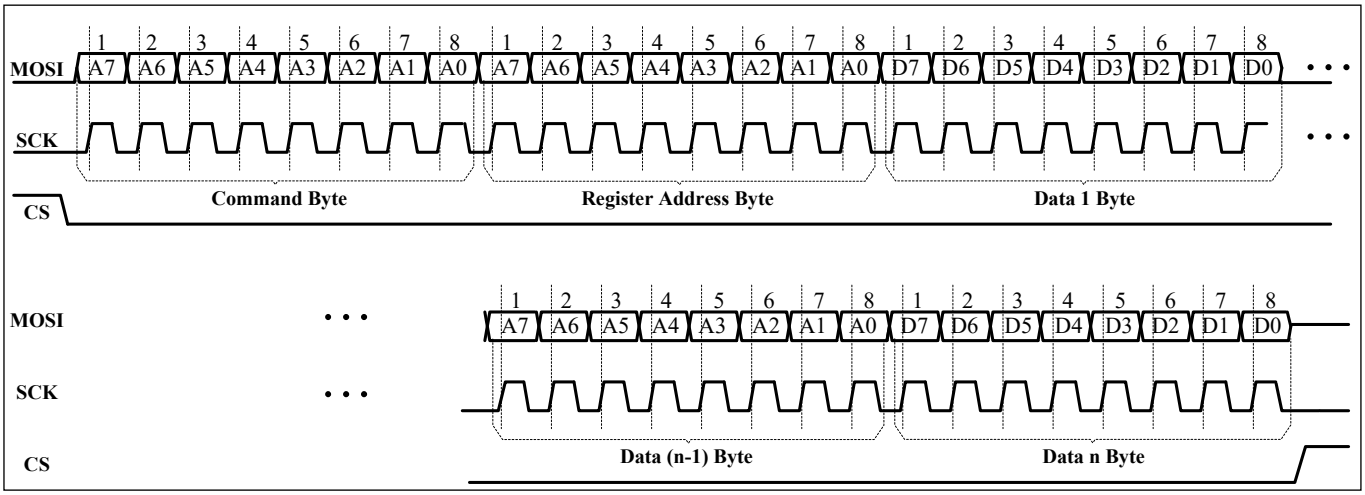


Figure 8 SPI Writing to IS31FL3747 (Automatic Address Increment)

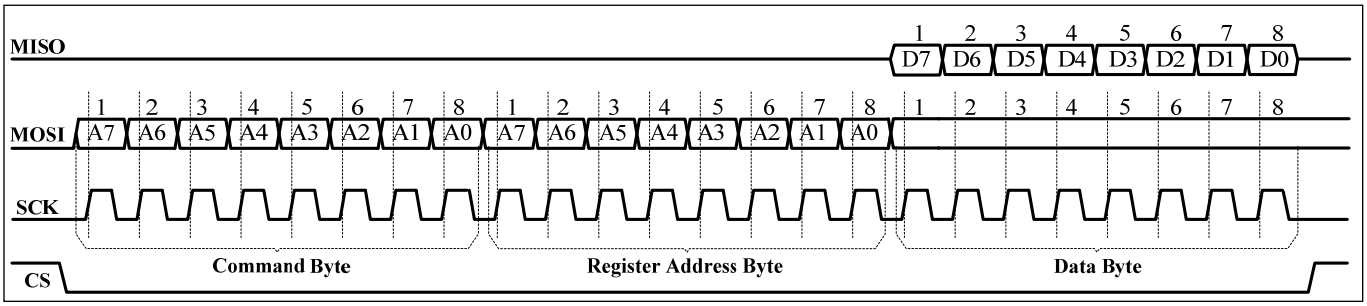


Figure 9 SPI Reading from IS31FL3747 (Typical)

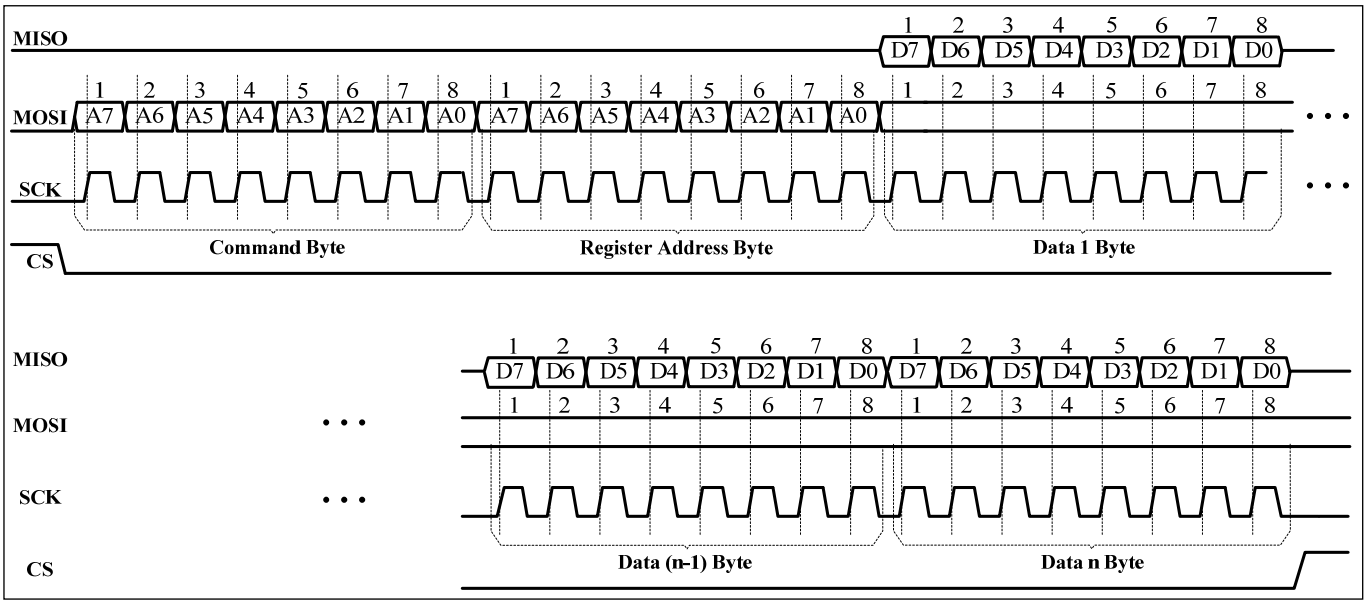


Figure 10 SPI Reading from IS31FL3747 (Automatic Address Increment)

Table 2 Register Definition-SPI

SPI Address	Name	Function	Table	R/W	Default
Page 0 (0x50): PWM Register (SW1~SW8)					
01h~C0h	PWM Register	Set PWM for each LED	3	R/W	0000 0000
Page 1 (0x51): PWM Register (SW9~SW16)					
01h~C0h	PWM Register	Set PWM for each LED	4	R/W	0000 0000
Page 2 (0x52): PWM Register (SW17~SW24)					
01h~C0h	PWM Register	Set PWM for each LED	5	R/W	0000 0000
Page 3 (0x53): Scaling Register (SW1~SW12)					
01h~90h	Scaling Register	Set Scaling for each LED	6	R/W	1111 1111
Page 4 (0x54): Scaling Register (SW13~SW24)					
01h~90h	Scaling Register	Set Scaling for each LED	7	R/W	1111 1111
Page 5 (0x55): Function Register					
00h	Configuration Register	Configure the operation mode	9	R/W	0100 0001
01h	SWx scan & SYNC function Register	Set SWx scan and SYNC function	10	R/W	0000 0000
02h	Global Current Control Register	Set global current for each channel	11	R/W	1111 1111
03h	Spread Spectrum & pull up /down time Register	Set spread spectrum and select CSy/SWx pull up/down time	12	R/W	0000 0000
04h	Temperature Status & Open/short detect & De ghost time Register	Set temperature thermal roll off and Open/short detect enable and De ghost time select	13	R/W	0000 0000
05h	Pull Down Voltage Selection Register 1	Set the pull-down voltage for SW1~SW4	14	R/W	0000 0000
06h	Pull Down Voltage Selection Register 2	Set the pull-down voltage for SW5~SW8	15	R/W	0000 0000
07h	Pull Down Voltage Selection Register 3	Set the pull-down voltage for SW9~SW12	16	R/W	0000 0000
08h	Group Pull Up Voltage Selection Register	Set the pull-up voltage for CSy	17	R/W	0000 0000
09h~38h	Open short detect result Register	Store the open/short information of LED	18	R	0000 0000
C8h	Update Register	Update the PWM data	-	W	0000 0000
DFh	Reset Register	Reset all registers	-	W	0000 0000

SPI Page 0, Page 1, Page 2 (0x50, 0x51, 0x52): PWM Register

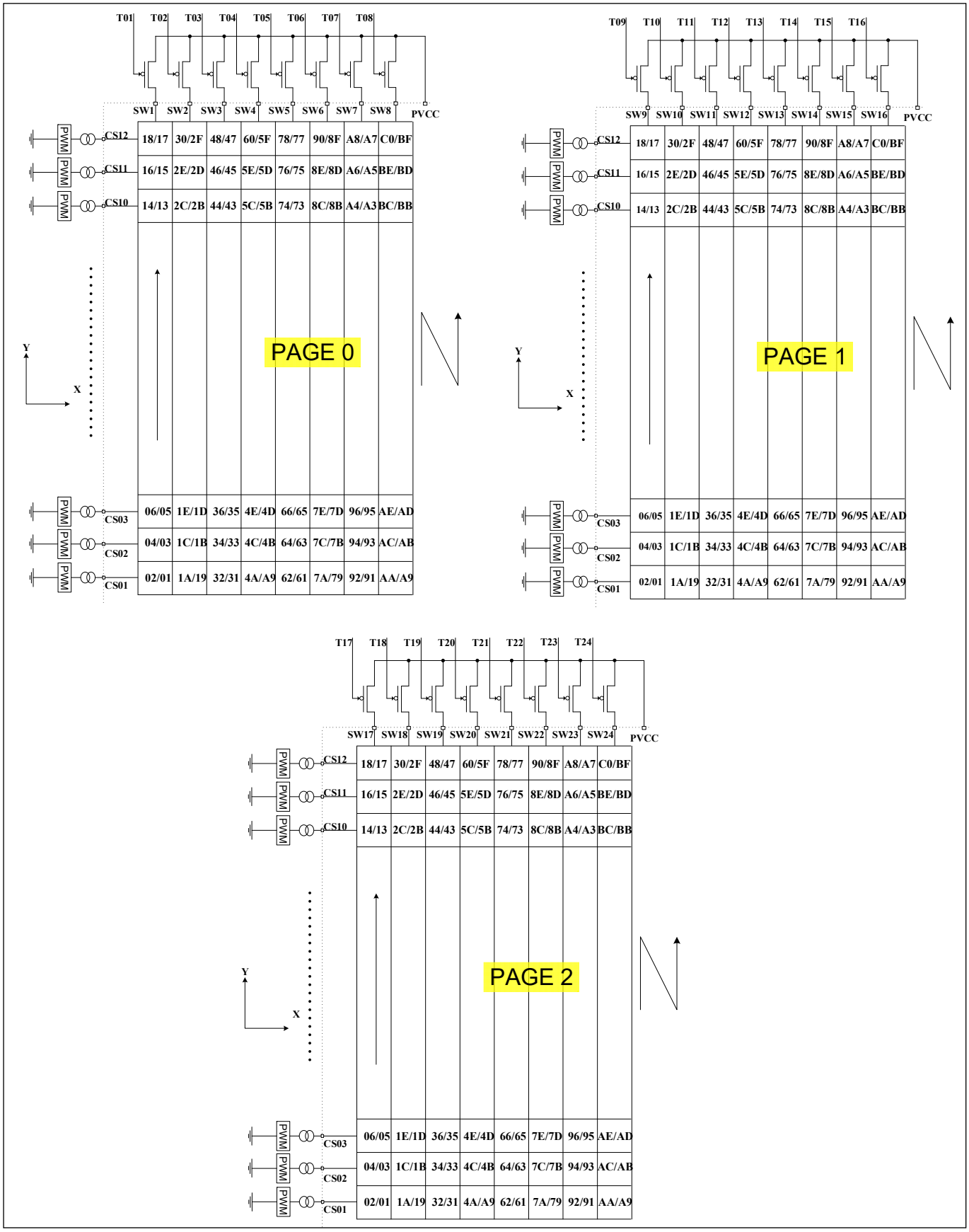


Figure 11 SPI PWM Register

Table 3 SPI Page 0: 01h ~ C0h PWM Register

Reg	02h (04h, 06h…)		01h (03h, 05h…)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

Table 4 SPI Page 1: 01h ~ C0h PWM Register

Reg	02h (04h, 06h…)		01h (03h, 05h…)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

Table 5 SPI Page 2: 01h ~ C0h PWM Register

Reg	02h (04h, 06h…)		01h (03h, 05h…)
Bit	D7:D4	D3:D0	D7:D0
Name	-	PWM_H	PWM_L
Default	0000	0000	0000 0000

Each dot has a byte to modulate the PWM duty in 256/4096 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED}=\frac{PWM}{N}\times I_{OUT(PEAK)}\times Duty \qquad (1)$$

N=256: $PWM=\sum_{n=0}^{7}D[n]\cdot 2^n$ (8-bit mode)

N=4096: $PWM=\sum_{n=0}^{11}D[n]\cdot 2^n$ (12-bit mode)

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

When SWS= “00000” and in 8bits + 4bits dithering/8bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty=\frac{17.1\mu s}{(17.1\mu s+1.85\mu s)}\times\frac{1}{12}=\frac{1}{13.38}$$ (2, 8-bit mode)

When SWS= “00000” and in 12-bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty=\frac{273\mu s}{(273\mu s+17.1\mu s)}\times\frac{1}{12}=\frac{1}{12.08}$$ (2,12-bit mode)

I_{OUT} is the output current of CSy (y=1~12),

$$I_{OUT(PEAK)}=\frac{478}{R_{ISET}}\times\frac{GCC}{256}\times\frac{SL}{256} \qquad (3)$$

GCC is the Global Current Control register (Page 5, 02h) value, SL is the Scaling register value as Table 6/Table 7 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, PWM register D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED}=\frac{478}{10k\Omega}\times\frac{255}{256}\times\frac{255}{256}\times\frac{1}{13.38}\times\frac{218}{256}$$

SPI Page 3, Page 4 (0x53, 0x54): Scaling Register

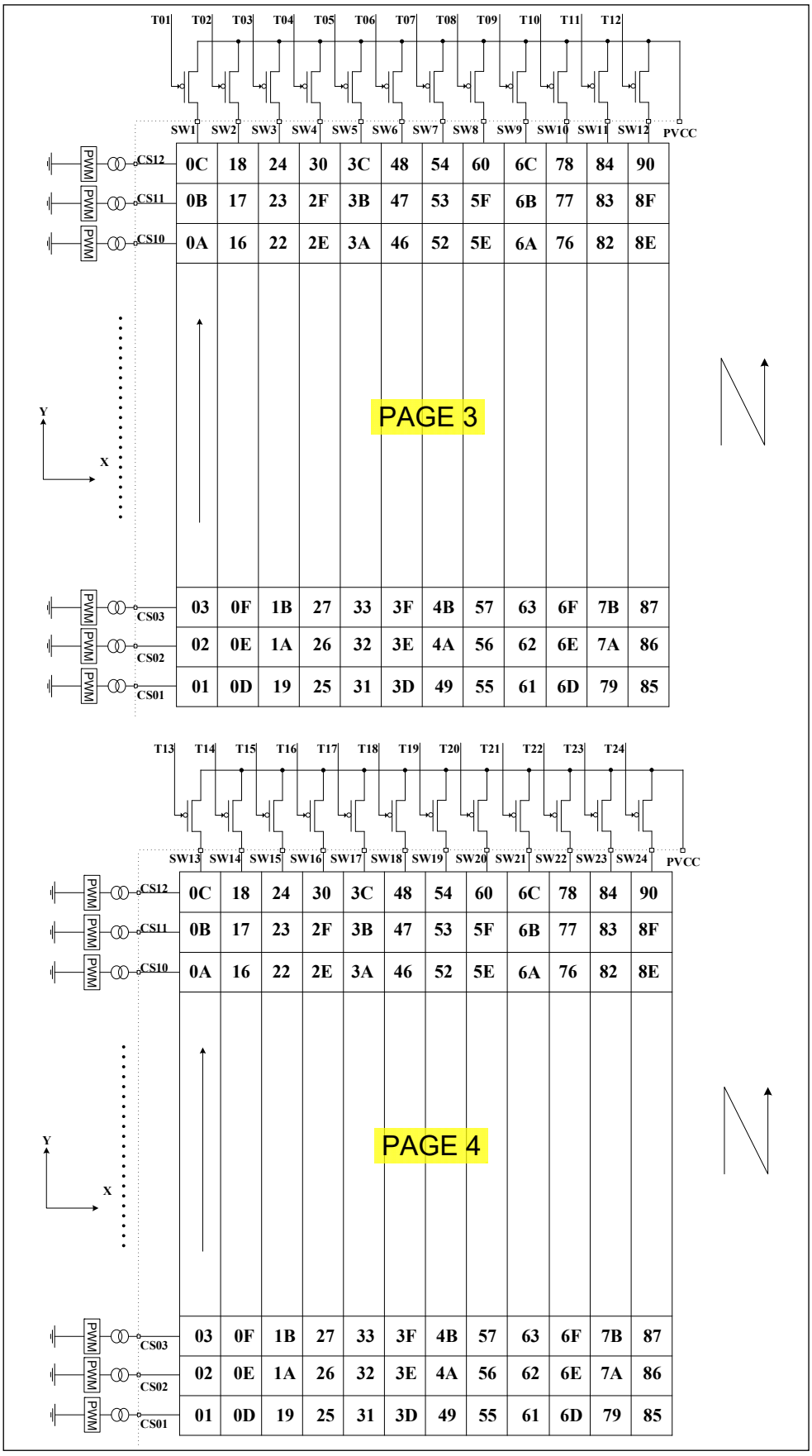


Figure 12 SPI Scaling Register

Table 6 SPI Page 3: 01h ~ 90h Scaling Register

Reg	01h (03h, 05h…)
Bit	D7:D0
Name	SL
Default	1111 1111

Table 7 SPI Page 4: 01h ~ 90h Scaling Register

Reg	01h (03h, 05h…)
Bit	D7:D0
Name	SL
Default	1111 1111

Scaling Register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{478}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \times 2^n$$

I_{OUT} is the output current of CSy (y=1~12), GCC is the Global Current Control Register (Page 5, 02h) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, R_{ISET}=10kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \times 2^n = 127$$

$$I_{OUT} = \frac{478}{10k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 23.6mA$$

$$I_{LED} = 23.6mA \times \frac{1}{13.38} \times \frac{PWM}{256}$$

Table 8 Page 5 (0x55): Function Register-SPI

SPI Address	Name	Function	Table	R/W	Default
00h	Configuration Register	Configure the operation mode	9	R/W	0100 0001
01h	SWx scan & SYNC function Register	Set SWx scan and SYNC function	10	R/W	0000 0000
02h	Global Current Control Register	Set global current for each channel	11	R/W	1111 1111
03h	Spread Spectrum & pull up /down time Register	Set spread spectrum and select CSy/SWx pull up/down time	12	R/W	0000 0000
04h	Temperature Status & Open/Short detect & De ghost time Register	Set temperature thermal roll off and Open/Short detect enable and De ghost time select	13	R/W	0000 0000
05h	Pull Down Voltage Selection Register 1	Set the pull-down voltage for SW1~SW4	14	R/W	0000 0000
06h	Pull Down Voltage Selection Register 2	Set the pull-down voltage for SW5~SW8	15	R/W	0000 0000
07h	Pull Down Voltage Selection Register 3	Set the pull-down voltage for SW9~SW12	16	R/W	0000 0000
08h	Group Pull Up Voltage Selection Register	Set the pull-up voltage for CSy	17	R/W	0000 0000
09h~38h	Open/Short detect result Register	Store the open or short information of LED	18	R	0000 0000
C8h	Update Register	Update the PWM data	-	W	0000 0000
DFh	Reset Register	Reset all registers	-	W	0000 0000

Table 9 SPI 00h Configuration Register

Bit	D7	D6	D5	D4:D3	D2:D1	D0
Name	CCS	EPS	OPS	OSC	PMS	SSD
Default	0	1	0	00	00	1

The Configuration Register sets operating mode of IS31FL3747.

When two IS31FL3747 are cascaded, the first chip needs to be set as “chip 1”, and second one as “chip 2”. When CCS is “0”, IS31FL3747 is “chip 1”. When CCS is “1”, IS31FL3747 is “chip 2”. When two IS31FL3747 are cascaded, “chip 1” and “chip 2” must update(C8h) at the same time during initialization.

Set EPS and OPS to change the clock phase of odd channels and even channels. It is helpful for reduction power noise.

The OSC bit selects the oscillator clock frequency. when OSC set “00”, the oscillator clock frequency is 16MHz, when OSC set “01”, the oscillator clock frequency is 32MHz, when OSC set to “10”, the oscillator clock frequency is 8MHz, when OSC set to “11”, the oscillator clock frequency is 4MHz.

The PMS bit selects PWM resolution mode, when PMS set “00”, the PWM mode is 8bits + 4bits dithering, when PFS set to “10”, the PWM mode is 8bits, when PFS set to “01” or “11”, the PWM mode is 12bits.

When SSD is “0”, IS31FL3747 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

CCS Cascading Chip Select
0 Chip 1
1 Chip 2

EPS Even Channels Clock Phase Select
0 All even channels work as scheme of Clock Phase 1
1 All even channels work as scheme of Clock Phase 2

OPS Odd Channels Clock Phase Select
0 All odd channels work as scheme of Clock Phase 1
1 All odd channels work as scheme of Clock Phase 2

OSC Oscillator Clock Frequency Select
00 16MHz
01 32MHz
10 8MHz
11 4MHz

PMS PWM Mode Select
00 8bits + 4bits dithering
10 8bits
01/11 12bits

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

Table 10 SPI 01h SWx Scan & SYNC Function Register

Bit	D7:D6	D5:D1	D0
Name	SYNC	SWS	RDM
Default	00	00000	0

When SYNC bits are set to “11”, the IS31FL3747 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device’s SYNC bits must be set to “10”.

SWS control the duty cycle of the SW, default mode is 1/12.

Random SW function is design for get better EMI test results. When RDM set to “1”, SWx will pull up randomly from 12 time points in a scan cycle.

SYNC Synchronize Configuration
00/01 High Impedance
11 Master
10 Slave

SWS SWx Setting
00000 SW1~SW12, 1/12
00001 SW1~SW11, 1/11, SW12 no-active
00010 SW1~SW10, 1/10, SW11~SW12 no-active
00011 SW1~SW9, 1/9, SW10~SW12 no-active
00100 SW1~SW8, 1/8, SW9~SW12 no-active
00101 SW1~SW7, 1/7, SW8~SW12 no-active
00110 SW1~SW6, 1/6, SW7~SW12 no-active
00111 SW1~SW5, 1/5, SW6~SW12 no-active
01000 SW1~SW4, 1/4, SW5~SW12 no-active
01001 SW1~SW3, 1/3, SW4~SW12 no-active
01010 SW1~SW2, 1/2, SW3~SW12 no-active
01011 All CSy work as current sinks only, no scan
10000 SW1~SW24, 1/24
10001 SW1~SW23, 1/23, SW24 no-active
10010 SW1~SW22, 1/22, SW23~SW24 no-active
10011 SW1~SW21, 1/21, SW22~SW24 no-active
10100 SW1~SW20, 1/20, SW21~SW24 no-active
10101 SW1~SW19, 1/19, SW20~SW24 no-active
10110 SW1~SW18, 1/18, SW19~SW24 no-active
10111 SW1~SW17, 1/17, SW18~SW24 no-active
11000 SW1~SW16, 1/16, SW17~SW24 no-active
11001 SW1~SW15, 1/15, SW16~SW24 no-active
11010 SW1~SW14, 1/14, SW15~SW24 no-active
11011 SW1~SW13, 1/13, SW14~SW24 no-active
Others No allowed

RDM Random SW Setting
0 Random SW disable
1 Random SW enable, not recommend in 24 × n cascade connection (CCS= “1”)

Table 11 SPI 02h Global Current Control Register

Bit	D7:D0
Name	GCC
Default	1111 1111

The Global Current Control Register modulates all CSy (y=1~12) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{478}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 12 SPI 03h Spread Spectrum & Pull Up /Down Time Register

Bit	D7	D6	D5	D4	D3:D2	D1:D0
Name	SPT	CPT	SSY	SSP	-	-
Default	0	0	0	0	00	00

Set SPT and CPT to select SW pull down time and CS pull up time.

When SSY enable, spread spectrum frequency will be synchronized with PWM frequency, the LED matrix flick at low current can be solved.

When SSP enable, it will adjust the range (±5%) and cycle time (1980μs) of spread spectrum function.

SPT SW Pull Down Time Select
0 SW pull down during off time
1 SW pull down during de ghost time

CPT CS Pull Up Time Select
0 CS pull up during off time
1 CS pull up during de ghost time

SSY Spread Spectrum Synchronize Enable
0 SYNC Spread Spectrum disable
1 SYNC Spread Spectrum enable

SSP Spread Spectrum Enable
0 Disable
1 Enable

Table 13 SPI 04h Temperature Status & Open/Short detect & De-ghost Time Register

Bit	D7	D6:D5	D4:D3	D2:D1	D0
Name	DGT	OSDE	TSP	TROF	TSE
Default	0	00	00	00	0

OSDE enables the open or short LED channel detection with the result stored in 09h~38h, note either open or short information is saved not both.

When TSE are set to "0", the thermal shutdown function enables. If environment temperature higher than maximum safe working temperature, IS31FL3747 will work in shutdown mode automatically, and it will go back in normal operation when the temperature drops.

TSP stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal roll-off function.

DGT De ghost time select
0 35 cycle
1 51 cycle

OSDE Open/Short Detect Enable
00/01 Detect disable
10 Short detect enable
11 Open detect enable

TSP Temperature Point, Thermal roll off start point
00 140°C
01 120°C
10 100°C
11 90°C

TROF Thermal roll off percentage of output current
00 100%
01 75%
10 55%
11 30%

TSE Thermal Shutdown Enable
0 Thermal shutdown enable
1 Thermal shutdown disable

Table 14 SPI 05h Pull Down Voltage Selection Register 1

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	PDV4	PDV3	PDV2	PDV1
Default	00	00	00	00

Table 15 SPI 06h Pull Down Voltage Selection Register 2

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	PDV8	PDV7	PDV6	PDV5
Default	00	00	00	00

Table 16 SPI 07h Pull Down Voltage Selection Register 3

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	PDV12	PDV11	PDV10	PDV9
Default	00	00	00	00

Set pull down voltage for SWx.

PDVx SWx Pull Down Voltage Select
00 floating
01 0V
10 1.4V
11 2.8V

Table 17 SPI 08h Group Pull Up Voltage Selection Register

Bit	D7:D6	D5:D4	D3:D2	D1:D0
Name	GUV4	GUV3	GUV2	GUV1
Default	00	00	00	00

Set pull up voltage for 4 group CSy.

GUV1 1st group (CS1/5/9) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

GUV2 2nd group (CS2/6/10) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

GUV3 3rd group (CS3/7/11) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

GUV4 4th group (CS4/8/12) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

Table 18 SPI 09h~38h Open/Short detect result Register (Read Only)

Bit	D7:D6	D5:D0
Name	-	CS06:CS01 of SWx
Default	00	00 0000
Bit	D7:D6	D5:D0
Name	-	CS12:CS07 of SWx
Default	00	00 0000

When OSDE (Page5, 04h) is set to “11”, open detection will be trigger once, and the open information will be stored at 09h~38h.

When OSDE (Page5, 04h) set to “10”, short detection will be trigger once, and the short information will be stored at 09h~38h.

Before set OSDE, the GCC should set to 0x0F, please check OPEN/SHORT DETECT FUNCTION section for more information.

After set OSDE, there should be 1ms delay before reading the open and short operation from registers.

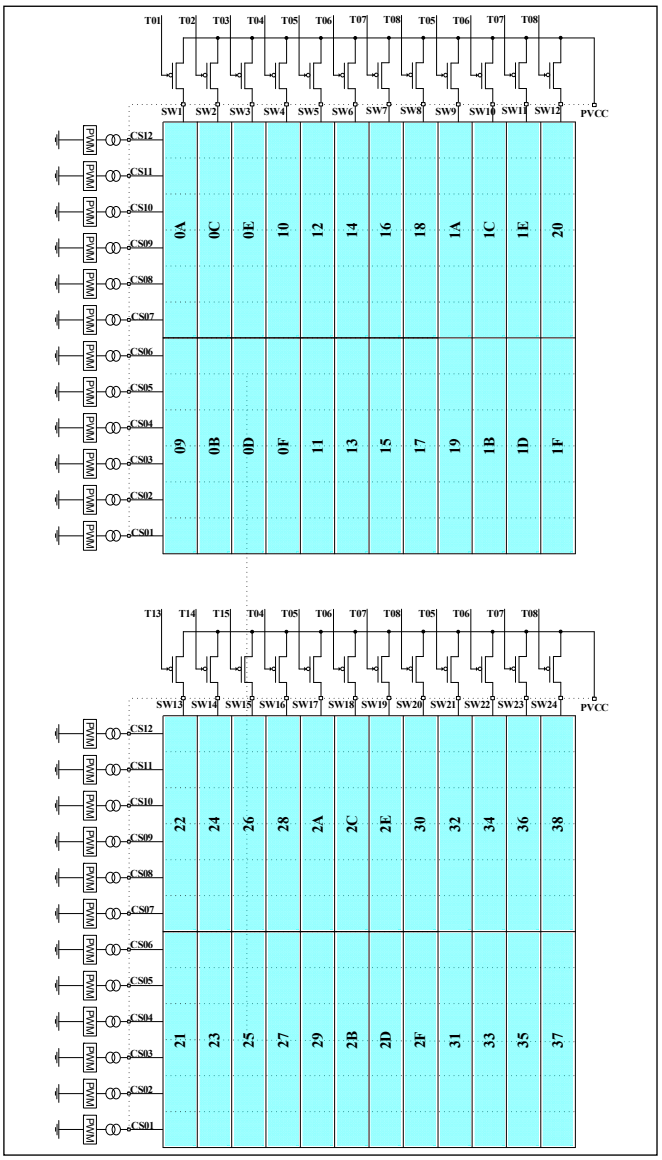


Figure 13 SPI Open/Short Register

C8h Update Register

When SDB= “H” and SSD= “1”, a writing of “0000 0000” to C8h will update the PWM register (Page 0/1/2 01h~C0h) values.

DFh Reset Register

When power on, all registers values are reset to default. A write of “0000 0000” to DFh will also reset all registers to their default values.

VSB INTERFACE

IS31FL3747 uses a VSB protocol to control the chip's function with four wires: DI, SCLK, LAT and DO. VSB transfer starts from DI and SCLK controlled by Master (Microcontroller), and IS31FL3747 latches data when LAT set to high.

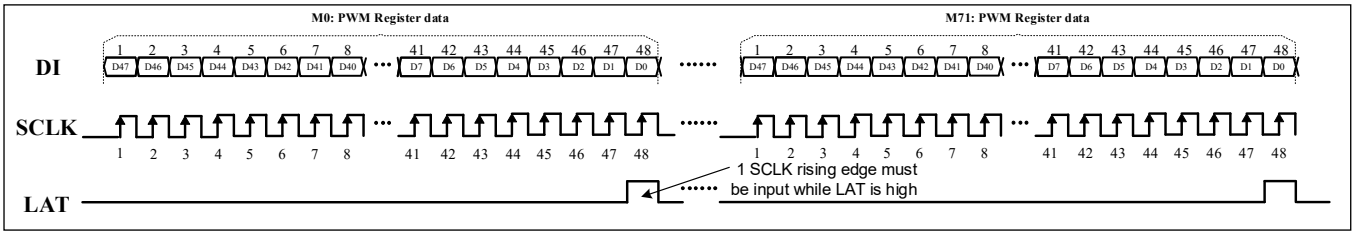


Figure 14 VSB Input Timing: M0~M71 PWM Register Data Write Command

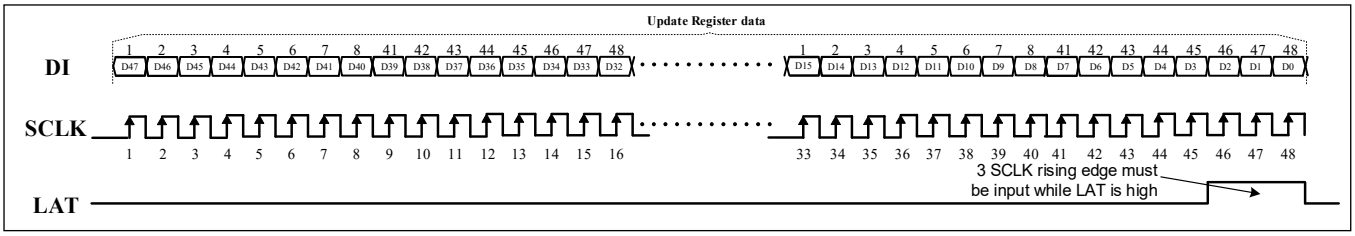


Figure 15 VSB Input Timing: Update Register Data Write Command

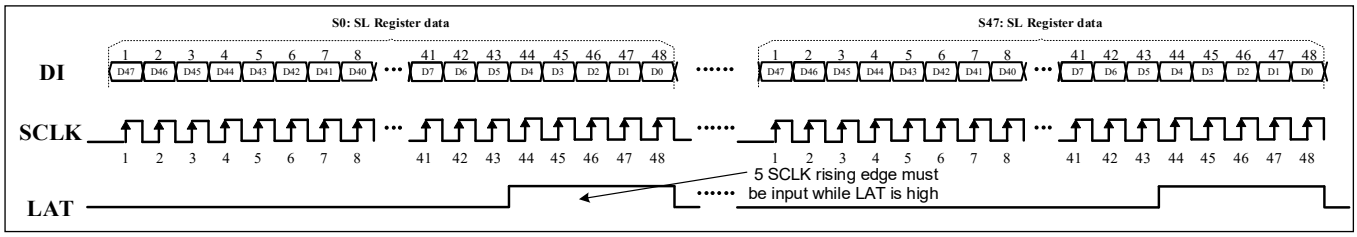


Figure 16 VSB Input Timing: SL Register Data Write Command

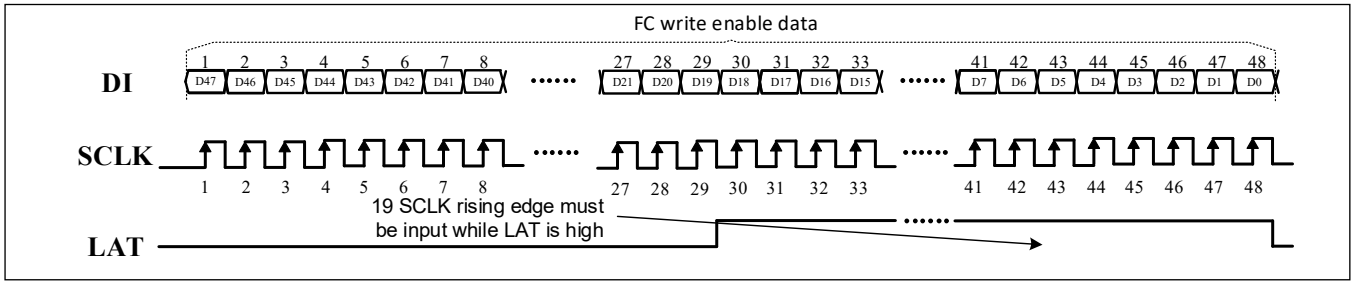


Figure 17 VSB Input Timing: FCxh Write Enable Command

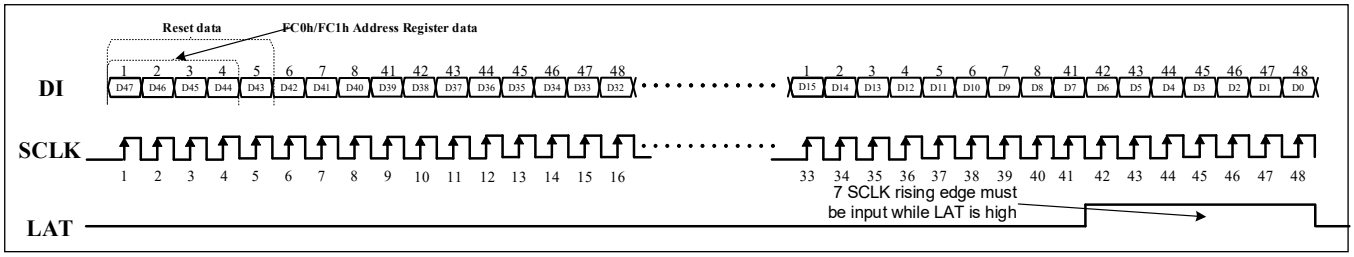


Figure 18 VSB Input Timing: FCxh Register Data Write Command

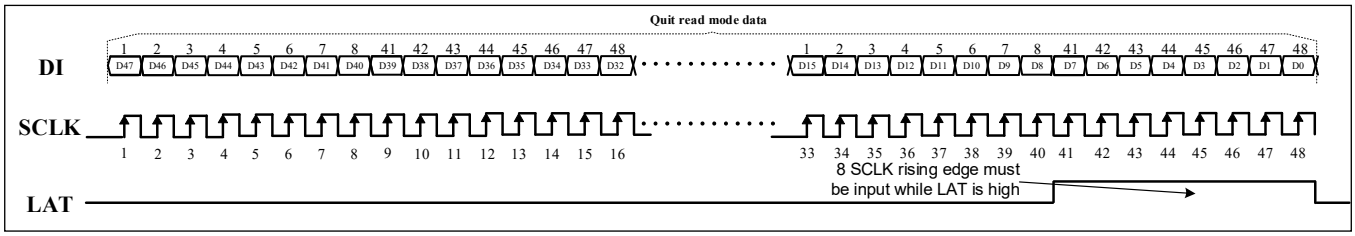


Figure 19 VSB Input Timing: Quit Read Mode Command

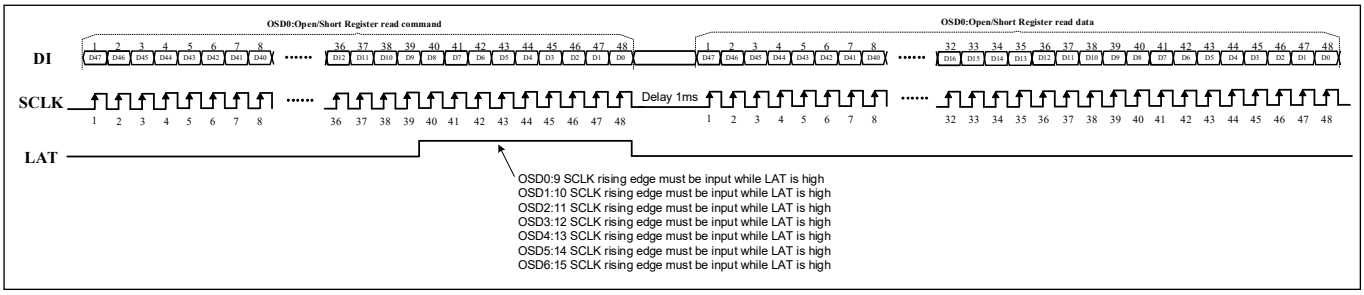


Figure 20 VSB Input Timing: OSDx Open/Short Detect Data Read Command

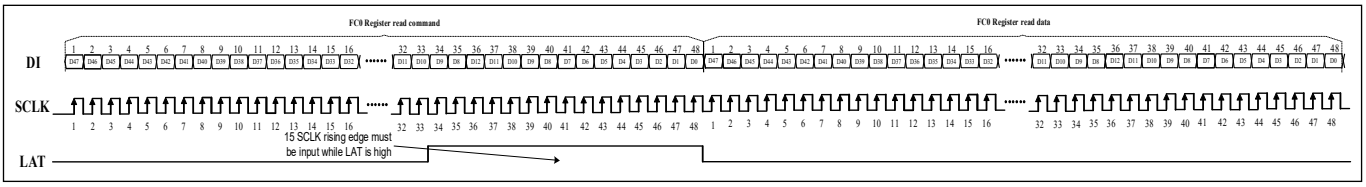


Figure 21 VSB Input Timing: FC0h Register Data Read Command

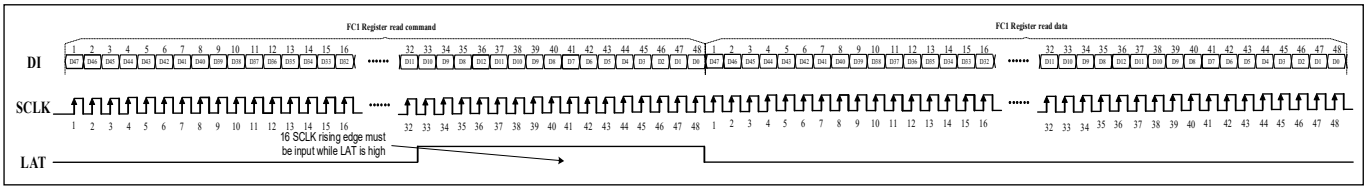


Figure 22 VSB Input Timing: FC1h Register Data Read Command

Table 19 VSB Protocol

Command name	SCLK rising edges when LAT is high	Description
WRT_PWM (48-bit PWM data write)	1	The 48-bit data in the common shift register are copied to the PWM memory unit selected by channel address counter, SW write counter.
UPDATE (Update PWM Data)	3	The 48-bit data is update PWM Register signal. When SDB= “H” and SSD= “1” and this command is received (all data are set to 0.) will update the PWM register (M0~M7) values.
WRT_SL (48-bit SL data write)	5	The 48-bit data in the common shift register are copied to the SL memory unit selected by channel address counter, SW write counter.
WRT_FC (FC data write)	7	The lower 39-bit data or the lower 29-bit data in the common shift register are copied to the FC0 or FC1 register. Bit 47–44 of the common shift register are used to choose which FC register is written to. If “1010b” is received for bit 47–44 of the common shift register, then the lower 44-bits in the common shift register are copied to the FC0 register. If “0101b” is received for bit 47–44 of the common shift register, then the lower 37 bits in the common shift register are copied to the FC1 register. If “11001b” is received for bit 47–43 of the common shift register, all the registers will be reset.
Quit read mode	8	The 48-bit data is quit read mode. When this command is received (all counters are reset to 0.) will quit read mode and return to write mode.
READ_OSD0 (OSD0 data read)	9	The 48-bit OSD0 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_OSD1 (OSD1 data read)	10	The 48-bit OSD1 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_OSD2 (OSD2 data read)	11	The 48-bit OSD2 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_OSD3 (OSD3 data read)	12	The 48-bit OSD3 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_OSD4 (OSD4 data read)	13	The 48-bit OSD4 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_OSD5 (OSD5 data read)	14	The 48-bit OSD5 data are copied to the 48-bit shift register. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_FC0 (FC0 data read)	15	The 44-bit data in the FC0 register are copied to the lower 44 bits of the shift register. Other bits in the shift register are reset to 0. The loaded data can be read out from DI synchronized with the SCLK rising edge.
READ_FC1 (FC1 data read)	16	The 32-bit data in the FC1 register are copied to the lower 32 bits of the shift register. Other bits in the shift register are reset to 0. The loaded data can be read out from DI synchronized with the SCLK rising edge.
FCWRTEN (FC write enable)	19	FC writes are enabled by this command (all date is set to 0). This command must always be input before the FC data write occurs.

Table 20 Register Definition-VSB

VSB Unit	Name	Function	Table	R/W	Default
PWM Register (SW1~SW8)					
M0~M23	PWM Register	Set PWM for each LED	21	R/W	0000 0000
PWM Register (SW9~SW16)					
M24~M47	PWM Register	Set PWM for each LED	21	R/W	0000 0000
PWM Register (SW17~SW24)					
M48~M71	PWM Register	Set PWM for each LED	21	R/W	0000 0000
Scaling Register (SW1~SW12)					
S0~S23	Scaling Register	Set Scaling for each LED	22	R/W	1111 1111
Scaling Register (SW13~SW24)					
S24~S47	Scaling Register	Set Scaling for each LED	22	R/W	1111 1111
Function Register					
FC0/FC1	Configuration Register	Configure the operation mode	24	R/W	0100 0001
	SWx scan & SYNC function Register	Set SWx scan and SYNC function	25	R/W	0000 0000
	Global Current Control Register	Set global current for each channel	26	R/W	1111 1111
	Spread Spectrum & pull up /down time Register	Set spread spectrum and select CSy/SWx pull up/down time	27	R/W	0000 0000
	Temperature Status & Open/short detect & De ghost time Register	Set temperature thermal roll off and Open/short detect enable and De ghost time select	28	R/W	0000 0000
	Address Register	Write 1010(47:44) to choose which FC0 register is written to	-	W	0000
	Reset Register	Write 11001(47:43) to reset all registers	-	W	00000
	Pull Down Voltage Selection Register 1	Set the pull-down voltage for SW1~SW4	29	R/W	0000 0000
	Pull Down Voltage Selection Register 2	Set the pull-down voltage for SW5~SW8	29	R/W	0000 0000
	Pull Down Voltage Selection Register 3	Set the pull-down voltage for SW9~SW12	29	R/W	0000 0000
	Group Pull Up Voltage Selection Register	Set the pull-up voltage for CSy	30	R/W	0000 0000
	Address Register	Write 0101(47:44) to choose which FC1 register is written to	-	W	0000
	Reset Register	Write 11001(47:43) to reset all registers	-	W	00000
OSD0~OSD5	Open short detect result Register	Store the open information of LED	31	R	0000 0000
UPDATE	Update Register	Update the PWM data	-	W	0000 0000

VSB M0~M71: PWM Register

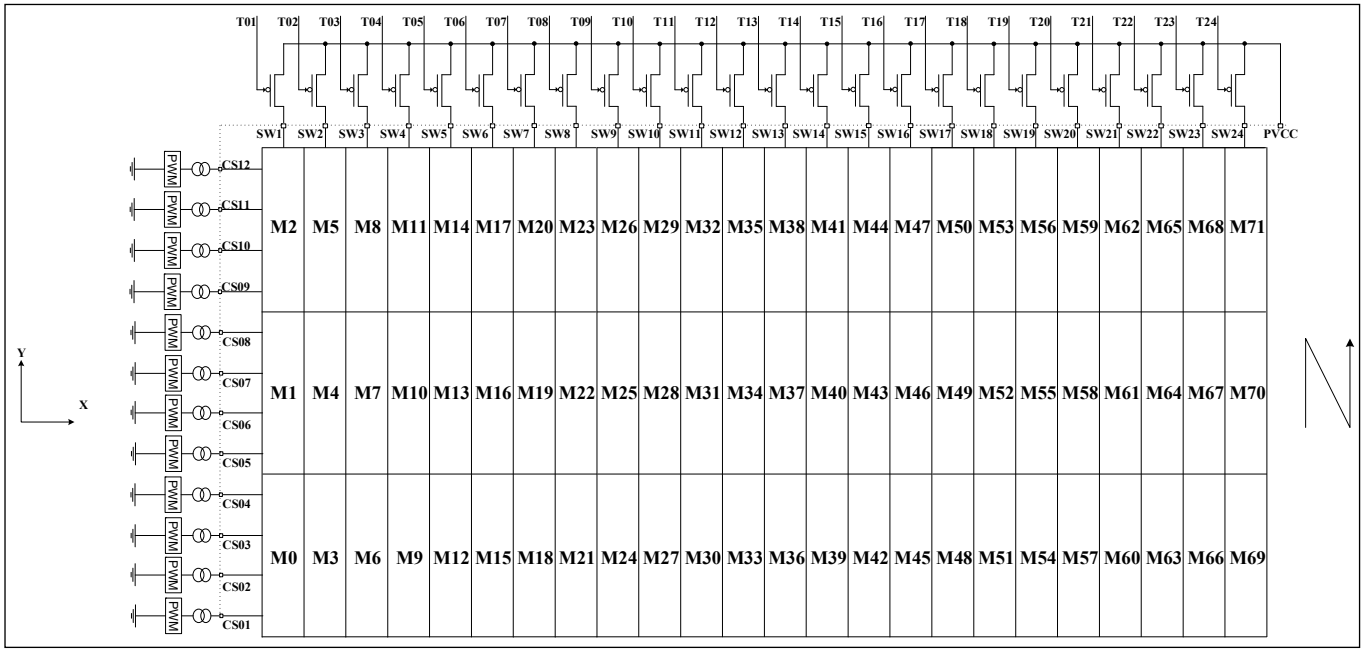


Figure 23 VSB PWM Register

Table 21 VSB M0 ~ M71 Unit

Unit	M0 (M1, M2…M71)				
Bit	47:44	43:36	…	11:8	7:0
Name	PWM_H	PWM_L	…	PWM_H	PWM_L
Default	0000	0000 0000	…	0000	0000 0000

Each dot has a byte to modulate the PWM duty in 256/4096 steps.

The value of the PWM Registers decides the average current of each LED noted I_{LED}.

I_{LED} computed by Formula (1):

$$I_{LED} = \frac{PWM}{N} \times I_{OUT\ (PEAK\ )} \times Duty \quad (1)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (8-bit mode)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (12-bit mode)

Where Duty is the duty cycle of SWx, see SCANING TIMING section for more information.

When SWS= “00000” and in 8-bits + 4bits dithering/ 8-bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty = \frac{17.1\mu s}{(17.1\mu s + 1.85\mu s)} \times \frac{1}{12} = \frac{1}{13.38}$$ (2, 8-bit mode)

When SWS= “00000” and in 12-bit PWM mode (OSC=16MHz), Duty is computed as below:

$$Duty = \frac{273\mu s}{(273\mu s + 17.1\mu s)} \times \frac{1}{12} = \frac{1}{12.08}$$ (2,12-bit mode)

I_{OUT} is the output current of CSy (y=1~12),

$$I_{OUT(PEAK)} = \frac{478}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \quad (3)$$

GCC is the Global Current Control register (FC0 Unit (23:16)) value, SL is the Scaling register value as Table 4 and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, PWM register D7:D0=1011 0101 (0xB5, 181), GCC=1111 1111, R_{ISET}=10kΩ, SL=1111 1111:

$$I_{LED} = \frac{478}{10k\Omega} \times \frac{255}{256} \times \frac{255}{256} \times \frac{1}{13.38} \times \frac{218}{256}$$

VSB S0~S47: Scaling Register

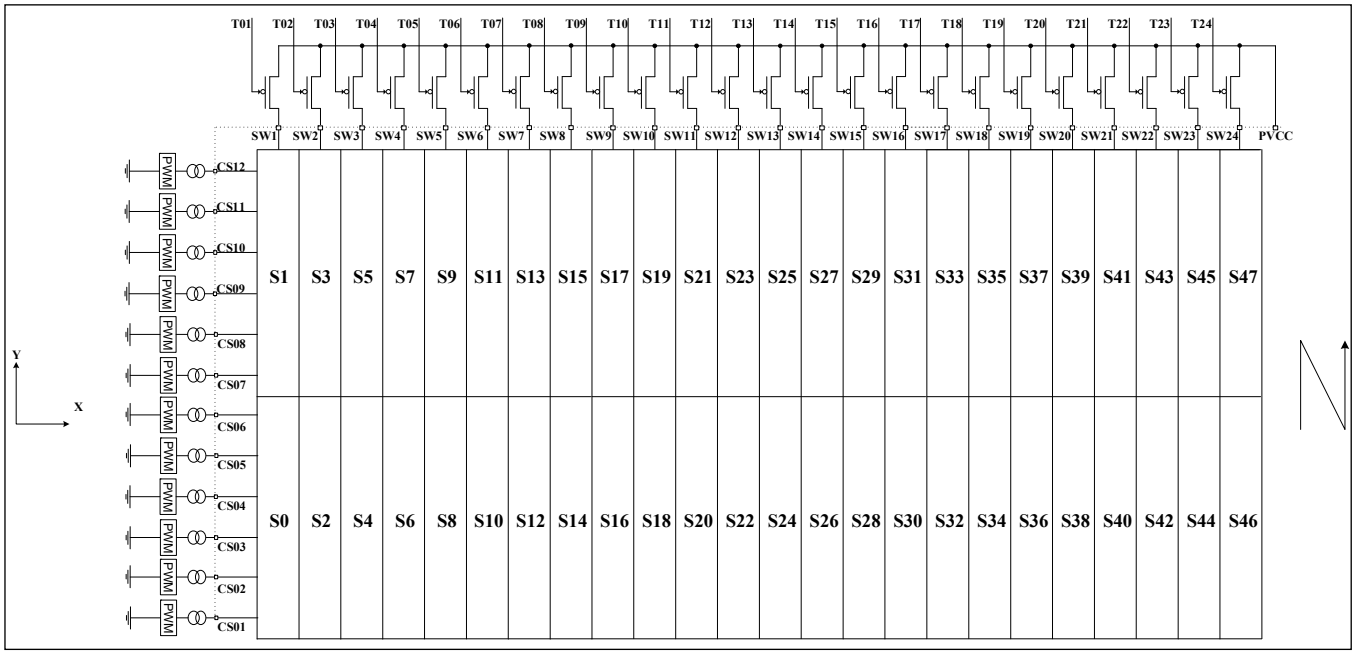


Figure 24 VSB Scaling Register

Table 22 VSB S0 ~ S47 Unit

Unit	S0 (S1, S2…S47)				
Bit	47:40	39:32	…	15:8	7:0
Name	SL	SL	…	SL	SL
Default	1111 1111	1111 1111	…	1111 1111	1111 1111

Scaling register control the DC output current of each dot. Each dot has a byte to modulate the scaling in 256 steps.

The value of the Scaling Register decides the peak current of each LED noted $I_{OUT(PEAK)}$.

$I_{OUT(PEAK)}$ computed by Formula (3):

$$I_{OUT(PEAK)} = \frac{478}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$SL = \sum_{n=0}^{7} D[n] \times 2^n$$

I_{OUT} is the output current of CSy (y=1~12), GCC is the Global Current Control Register (FC0 Unit (23:16)) value and R_{ISET} is the external resistor of ISET pin. D[n] stands for the individual bit value, 1 or 0, in location n.

For example: if in 8-bit PWM mode, R_{ISET}=10kΩ, GCC=1111 1111, SL=0111 1111:

$$SL = \sum_{n=0}^{7} D[n] \times 2^n = 127$$

$$I_{OUT} = \frac{478}{10k\Omega} \times \frac{255}{256} \times \frac{127}{256} = 23.6mA$$

$$I_{LED} = 23.6mA \times \frac{1}{13.38} \times \frac{PWM}{256}$$

Table 23 Function Register-VSB

VSB Unit	Bits	Name	Function	Table	R/W	Default
FC0	7~0	Configuration Register	Configure the operation mode	24	R/W	0100 0001
	15~8	SWx scan & SYNC function Register	Set SWx scan and SYNC function	25	R/W	0000 0000
	23~16	Global Current Control Register	Set global current for each channel	26	R/W	1111 1111
	31~24	Spread Spectrum & pull up /down time Register	Set spread spectrum and select CSy/SWx pull up/down time	27	R/W	0000 0000
	39~32	Temperature Status & Open/Short detect & De ghost time Register	Set temperature thermal roll off and Open/Short detect enable and De ghost time select	28	R/W	0000 0000
	43-47	Reset Register	Reset all registers	-	W	00000
FC1	7~0	Pull Down Voltage Selection Register 1	Set the pull-down voltage for SW1~SW4	29	R/W	0000 0000
	15~8	Pull Down Voltage Selection Register 2	Set the pull-down voltage for SW5~SW8	29	R/W	0000 0000
	23~16	Pull Down Voltage Selection Register 3	Set the pull-down voltage for SW9~SW12	29	R/W	0000 0000
	31~24	Group Pull Up Voltage Selection Register	Set the pull-up voltage for CSy	30	R/W	0000 0000
	43-47	Reset Register	Reset all registers	-	W	00000
OSD0 ~OSD5	47~0	Open/Short detect result Register	Store the open or short information of LED	31	R	000~000
UPDATE	47~0	Update Register	Update the PWM data	-	W	000~000

Table 24 VSB FC0 Unit (7:0) Configuration Register

Bit	7	6	5	4:3	2:1	0
Name	CCS	EPS	OPS	OSC	PMS	SSD
Default	0	1	0	00	00	1

The Configuration Register sets operating mode of IS31FL3747.

When two IS31FL3747 are cascaded, the first chip needs to be set as “chip 1”, and second one as “chip 2”. When CCS is “0”, IS31FL3747 is “chip 1”. When CCS is “1”, IS31FL3747 is “chip 2”.

Set EPS and OPS to change the clock phase of odd channels and even channels. It is helpful for reduction power noise.

The OSC bit selects the oscillator clock frequency. when OSC set “00”, the oscillator clock frequency is 16MHz, when OSC set “01”, the oscillator clock frequency is 32MHz, when OSC set to “10”, the oscillator clock frequency is 8MHz, when OSC set to “11”, the oscillator clock frequency is 4MHz.

The PMS bit selects PWM resolution mode, when PMS set “00”, the PWM mode is 8bits + 4bits dithering, when PFS set to “10”, the PWM mode is 8bits, when PFS set to “01” or “11”, the PWM mode is 12bits.

When SSD is “0”, IS31FL3747 works in software shutdown mode and to normal operate the SSD bit should set to “1”.

CCS Cascading Chip Select
0 Chip 1
1 Chip 2

EPS Even Channels Clock Phase Select
0 All even channels work as scheme of Clock Phase 1
1 All even channels work as scheme of Clock Phase 2

OPS Odd Channels Clock Phase Select
0 All odd channels work as scheme of Clock Phase 1
1 All odd channels work as scheme of Clock Phase 2

OSC Oscillator Clock Frequency Select
00 16MHz
01 32MHz
10 8MHz
11 4MHz

PMS PWM Mode Select
00 8bits + 4bits dithering
10 8bits
01/11 12bits

SSD Software Shutdown Control
0 Software shutdown
1 Normal operation

Table 25 VSB FC0 Unit (15:8) SWx Scan & SYNC Function Register

Bit	15:14	13:9	8
Name	SYNC	SWS	RDM
Default	00	00000	0

When SYNC bits are set to "11", the IS31FL3747 is configured as the master clock source and the SYNC pin will generate a clock signal distributed to the clock slave devices. To be configured as a clock slave device and accept an external clock input the slave device's SYNC bits must be set to "10".

SWS control the duty cycle of the SW, default mode is 1/12.

Random SW function is design for get better EMI test results. When RDM set to "1", SWx will pull up randomly from 12 time points in a scan cycle.

SYNC Synchronize Configuration
00/01 High Impedance
11 Master
10 Slave

SWS SWx Setting
00000 SW1~SW12, 1/12
00001 SW1~SW11, 1/11, SW12 no-active
00010 SW1~SW10, 1/10, SW11~SW12 no-active
00011 SW1~SW9, 1/9, SW10~SW12 no-active
00100 SW1~SW8, 1/8, SW9~SW12 no-active
00101 SW1~SW7, 1/7, SW8~SW12 no-active
00110 SW1~SW6, 1/6, SW7~SW12 no-active
00111 SW1~SW5, 1/5, SW6~SW12 no-active
01000 SW1~SW4, 1/4, SW5~SW12 no-active
01001 SW1~SW3, 1/3, SW4~SW12 no-active
01010 SW1~SW2, 1/2, SW3~SW12 no-active
01011 All CSy work as current sinks only, no scan
10000 SW1~SW24, 1/24
10001 SW1~SW23, 1/23, SW24 no-active
10010 SW1~SW22, 1/22, SW23~SW24 no-active
10011 SW1~SW21, 1/21, SW22~SW24 no-active
10100 SW1~SW20, 1/20, SW21~SW24 no-active
10101 SW1~SW19, 1/19, SW20~SW24 no-active
10110 SW1~SW18, 1/18, SW19~SW24 no-active
10111 SW1~SW17, 1/17, SW18~SW24 no-active
11000 SW1~SW16, 1/16, SW17~SW24 no-active
11001 SW1~SW15, 1/15, SW16~SW24 no-active
11010 SW1~SW14, 1/14, SW15~SW24 no-active
11011 SW1~SW13, 1/13, SW14~SW24 no-active
Others No allowed

RDM Random SW Setting
0 Random SW disable
1 Random SW enable, not recommend in 24 × n cascade connection (CCS= "1")

Table 26 VSB FC0 Unit (23:16) Global Current Control Register

Bit	23:16
Name	GCC
Default	1111 1111

The Global Current Control Register modulates all CSy (y=1~12) DC current which is noted as I_{OUT} in 256 steps.

I_{OUT} is computed by the Formula (3):

$$I_{OUT(PEAK)} = \frac{478}{R_{ISET}} \times \frac{GCC}{256} \times \frac{SL}{256} \qquad (3)$$

$$GCC = \sum_{n=0}^{7} D[n] \cdot 2^n$$

Where D[n] stands for the individual bit value, 1 or 0, in location n.

Table 27 VSB FC0 Unit (31:24) Spread Spectrum & Pull Up /Down Time Register

Bit	31	30	29	28	27:26	25:24
Name	SPT	CPT	SSY	SSP	-	-
Default	0	0	0	0	00	00

Set SPT and CPT to select SW pull down time and CS pull up time.

When SSY enable, spread spectrum frequency will be synchronized with PWM frequency, the LED matrix flick at low current can be solved.

When SSP enable, it will adjust the range (±5%) and cycle time (1980μs) of spread spectrum function.

SPT SW Pull Down Time Select
0 SW pull down during off time
1 SW pull down during de-ghost time

CPT CS Pull Up Time Select
0 CS pull up during off time
1 CS pull up during de-ghost time

SSY Spread Spectrum Synchronize Enable
0 SYNC Spread Spectrum disable
1 SYNC Spread Spectrum enable

SSP Spread Spectrum Enable
0 Disable
1 Enable

Table 28 VSB FC0 Unit (39:32) Temperature Status & Open/Short Detect & De-ghost Time Register

Bit	39	38:37	36:35	34:33	32
Name	DGT	OSDE	TSP	TROF	TSE
Default	0	00	00	00	0

OSDE enables the open or short LED channel detection with the result stored in 09h~38h, note either open or short information is saved not both.

When TSE are set to “00”, the thermal shutdown function enables. If environment temperature higher than maximum safe working temperature, IS31FL3747 will work in shutdown mode automatically, and it will go back in normal operation when the temperature drops.

TSP stores the temperature/thermal roll-off point. TROF stores percentage of output current of the thermal roll-off function.

DGT De-ghost Time Select
0 35 cycle
1 51 cycle

OSDE Open/Short Detect Enable
00/01 Detect disable
10 Short detect enable
11 Open detect enable

TSP Temperature Point, Thermal Roll Off Start Point
00 140°C
01 120°C
10 100°C
11 90°C

TROF Thermal Roll Off Percentage Of Output Current
00 100%
01 75%
10 55%
11 30%

TSE Thermal Shutdown Enable
0 Thermal shutdown enable
1 Thermal shutdown disable

Table 29 VSB FC1 Unit (23:0) Pull Down Voltage Selection Register

Bit	7:6	5:4	3:2	1:0
Name	PDV4	PDV3	PDV2	PDV1
Default	00	00	00	00
Bit	15:14	13:12	11:10	9:8
Name	PDV8	PDV7	PDV6	PDV5
Default	00	00	00	00
Bit	23:22	21:20	19:18	17:16
Name	PDV12	PDV11	PDV10	PDV9
Default	00	00	00	00

Set pull down voltage for SWx.

PDVx SWx Pull Down Voltage Select
00 floating
01 0V
10 1.4V
11 2.8V

Table 30 VSB FC1 Unit (31:24) Group Pull Up Voltage Selection Register

Bit	31:30	29:28	27:26	25:24
Name	GUV4	GUV3	GUV2	GUV1
Default	00	00	00	00

Set pull up voltage for 4 groups CSy.

GUV1 1st group (CS1/5/9) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

GUV2 2nd group (CS2/6/10) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

3GUV 3rd group (CS3/7/11) Pull Up Voltage Select
00 floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

GUV4 4th group (CS4/8/12) Pull Up Voltage Select
00 Floating
01 V_{CC}
10 V_{CC}-1.4V
11 V_{CC}-2.8V

Table 31 VSB OSD0~OSD5 Unit (47:0) Open/Short Detect Result Register (Read Only)

Bit	11:6	5:0
Name	CS12:CS7 of SWx	CS06:CS1 of SWx
Default	0000 00	00 0000
……		
Bit	47:42	41:36
Name	CS12:CS7 of SWx+4	CS06:CS1 of SWx+4
Default	0000 00	00 0000

When OSDE (FC0 Unit (39:32)) is set to “11”, open detection will be trigger once, and the open information will be stored at OSD0~OSD5 Unit (47:0).

When OSDE (FC0 Unit (39:32)) set to “10”, short detection will be trigger once, and the short information will be stored at OSD0~OSD5 Unit (47:0).

Before set OSDE, the GCC should set to 0x0F, please check OPEN/SHORT DETECT FUNCTION section for more information.

After set OSDE, there should be 1ms delay before reading the open and short operation from registers.

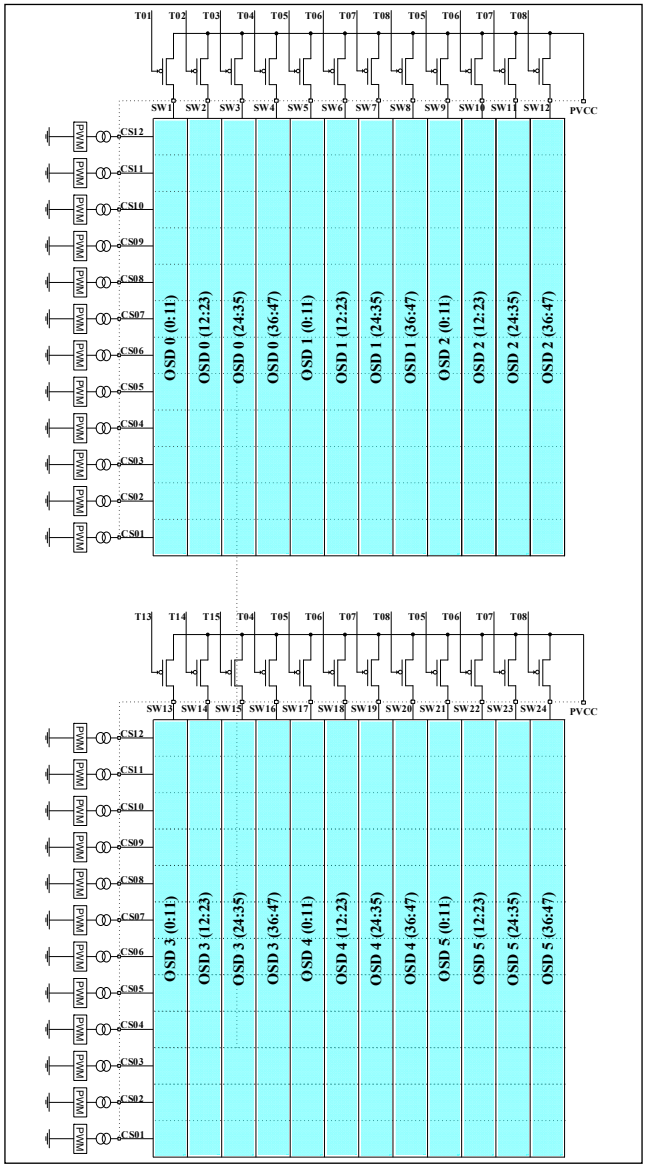


Figure 25 VSB Open/Short Register

Update Register

When SDB= “H” and SSD= “1”, a write of 48-bit data (all data are set to 0) to Update register will update the PWM register (M0~M71) values.

Reset Register

When power on, all registers values are reset to default. And write of “11001b” (bit 47~43) to FC register will also reset all registers to their default values.

APPLICATION INFORMATION

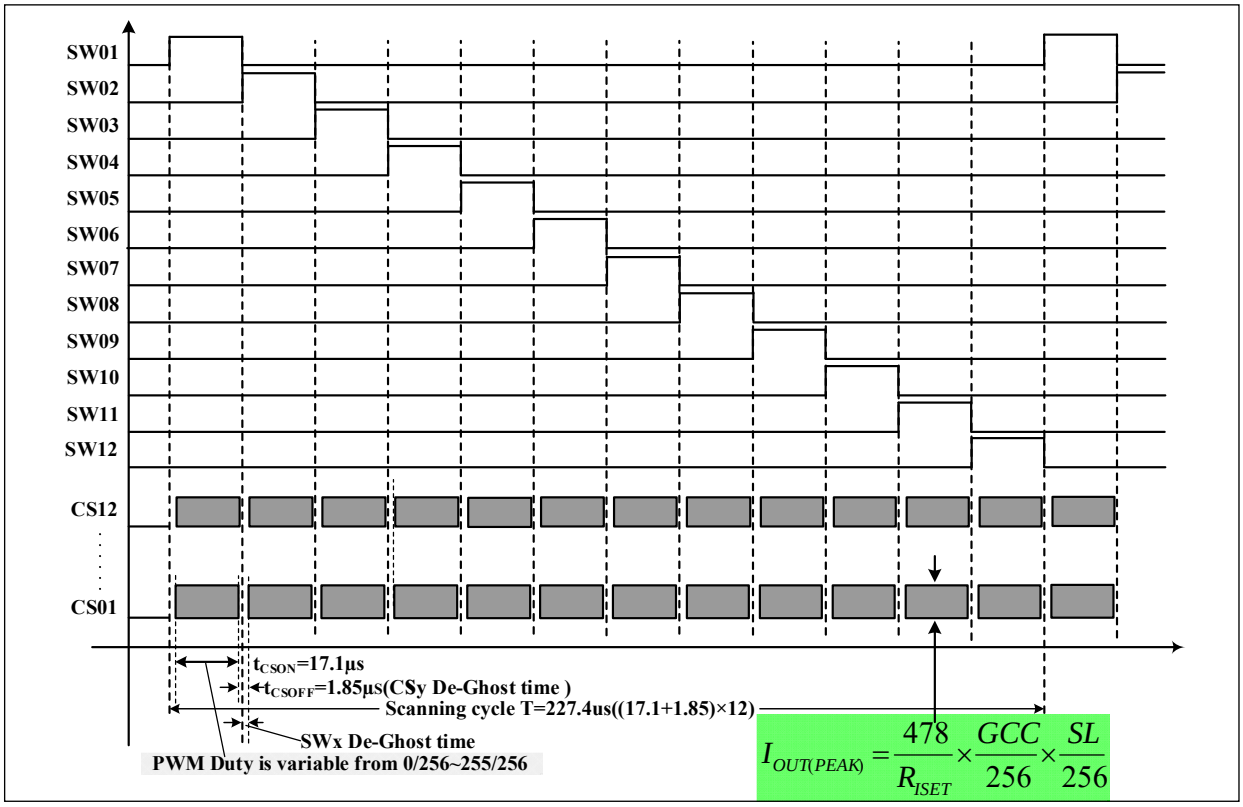


Figure 26 Scanning Timing (8-bit PWM Mode)

SCANNING TIMING

As shown in Figure above, the SW1~SW12 is turned on by serial, LED is driven 12 by 12 within the SWx (x=1~12) on time (SWx, x=1~12 is source and it is high when LED on), including the non-overlap blanking time during scan, the duty cycle of SWx (active high, x=1~12) is:

$$Duty = \frac{17.1\mu s}{(17.1\mu s + 1.85\mu s)} \times \frac{1}{12} = \frac{1}{13.38} \quad \text{(2, 8-bit mode)}$$

Where 17.1μs is t_{CSON},1.85μs is t_{CSOFF}.

PWM CONTROL

After setting the I_{OUT} and GCC, the brightness of each LEDs (LED average current (I_{LED})) can be modulated with 256 steps by PWM Register, as described in Formula (1).

$$I_{LED} = \frac{PWM}{N} \times I_{OUT\ (PEAK)} \times Duty \quad (1)$$

N=256: $PWM = \sum_{n=0}^{7} D[n] \cdot 2^n$ (8-bit mode)

N=4096: $PWM = \sum_{n=0}^{11} D[n] \cdot 2^n$ (12-bit mode)

Where PWM is PWM Registers data showing in SPI INTERFACE Table 3/4/5 or VSB INTERFACE Table 3.

For example, if in 8-bit PWM mode, R_{ISET}= 10kΩ, PWM= 127, and GCC= 255, Scaling= 255, then

$$I_{OUT(PEAK)} = \frac{478}{10k\Omega} \times \frac{127}{256} \times \frac{255}{256} \times \frac{255}{256} = 23.5mA$$

$$I_{LED} = 23.5mA \times \frac{1}{13.38} \times \frac{PWM}{256}$$

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected PWM value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Since the IS31FL3747 can modulate the brightness of the LEDs with 256 steps, a gamma correction function can be applied when computing each subsequent LED intensity setting such that the changes in brightness matches the human eye's brightness curve.

Table 32 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	4	6	10	13	18
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
22	28	33	39	46	53	61	69
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
78	86	96	106	116	126	138	149
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
161	173	186	199	212	226	240	255

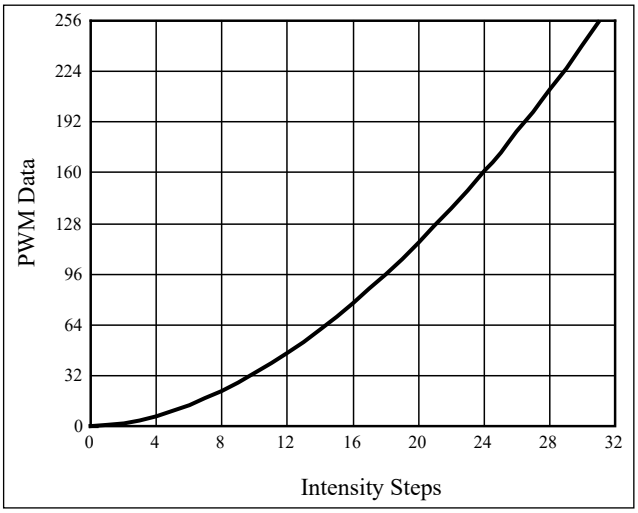


Figure 27 Gamma Correction (32 Steps)

Choosing more gamma steps provides for a more continuous looking breathing effect. This is useful for very long breathing cycles. The recommended configuration is defined by the breath cycle T. When T=1s, choose 32 gamma steps with 256 PWM steps, when T=2s, choose 64 gamma steps with 256 PWM steps, when T=24s, choose 128 gamma steps with 4096 PWM steps. The user must decide the final number of gamma steps not only by the LED itself, but also based on the visual performance of the finished product.

Table 33 64 Gamma Steps With 256 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	6	7
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
8	10	12	14	16	18	20	22
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
24	26	29	32	35	38	41	44
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
47	50	53	57	61	65	69	73
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
77	81	85	89	94	99	104	109
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
114	119	124	129	134	140	146	152
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
158	164	170	176	182	188	195	202
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
209	216	223	230	237	244	251	255

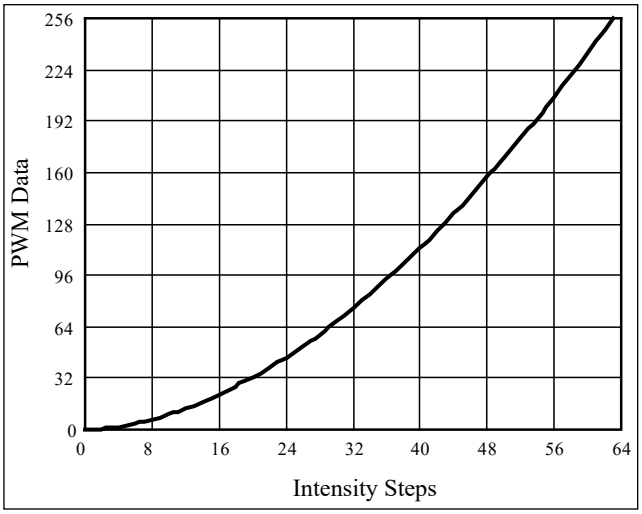


Figure 28 Gamma Correction (64 Steps)

Table 34 128 Gamma Steps With 4096 PWM Steps

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	1	2	3	4	5	7	8
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
10	13	15	18	21	25	29	33
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
37	42	47	53	59	65	72	79
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
87	94	103	112	121	130	141	151
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
162	174	186	198	211	224	238	253
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
268	283	299	316	333	350	369	387
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
407	426	447	468	489	512	534	558
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	C(63)
582	606	631	657	683	710	738	766
C(64)	C(65)	C(66)	C(67)	C(68)	C(69)	C(70)	C(72)
795	825	855	886	917	949	982	1016
C(73)	C(74)	C(75)	C(76)	C(77)	C(78)	C(79)	C(80)
1050	1085	1121	1157	1194	1231	1270	1309
C(81)	C(82)	C(83)	C(84)	C(85)	C(86)	C(87)	C(88)
1349	1389	1430	1472	1515	1558	1602	1647
C(89)	C(90)	C(90)	C(91)	C(92)	C(93)	C(94)	C(95)
1693	1739	1786	1834	1883	1932	1983	2034
C(96)	C(97)	C(98)	C(99)	C(100)	C(101)	C(102)	C(103)
2085	2138	2191	2245	2300	2356	2412	2470
C(104)	C(105)	C(106)	C(107)	C(108)	C(109)	C(110)	C(111)
2646	2587	2646	2707	2768	2831	2894	2958
C(112)	C(113)	C(114)	C(115)	C(116)	C(117)	C(118)	C(119)
3022	3088	3154	3221	3290	3358	3428	3499
C(120)	C(121)	C(122)	C(123)	C(124)	C(125)	C(126)	C(127)
3571	3643	3716	3790	3866	3941	4018	4096

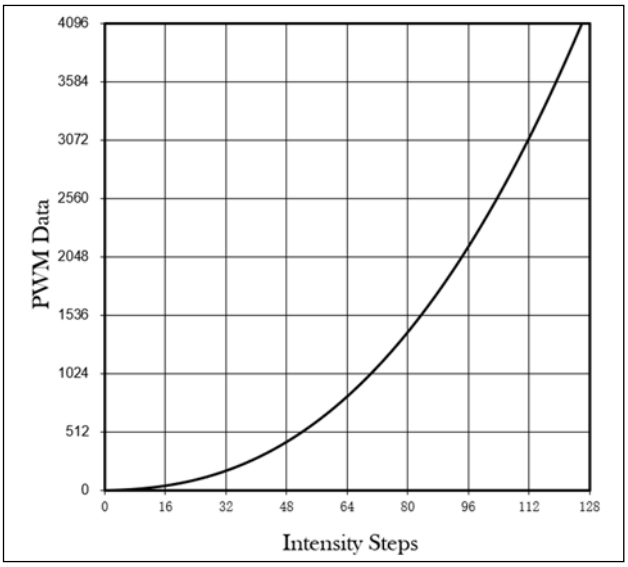


Figure 29 Gamma Correction (128 Steps)

Note 9: The data of 32 gamma steps is the standard value and the data of 64 gamma steps and 128 gamma steps is the recommended value.

OPERATING MODE

IS31FL3747 can only operate in PWM Mode. The brightness of each LED can be modulated with 256 steps by PWM registers. For example, if the data in PWM Register is “0000 0100”, then the PWM is the fourth step.

Writing new data continuously to the registers can modulate the brightness of the LEDs to achieve a breathing effect.

OPEN/SHORT DETECT FUNCTION

IS31FL3747 has open and short detect bit for each LED.

By setting the OSDE bits of the Open/Short Register from “00” to “10” or “11”, the LED Open/Short Register will start to store the open/short information and after at least 2 scanning cycles and the MCU can get the open/short information by reading the 09h~38h, for those dots are turned off via LED Scaling Registers, the open/short data will not get refreshed when setting the OSDE bit of the Open/Short Register.

The two configurations need to set before setting the OSD bits:

1 0x0F≤GCC≤0x40
2 SWx Pull Down Voltage = floating,
CSy Pull Up Voltage = floating,

Where GCC is the Global Current Control Register and the Pull Down/Up Voltage Selection Register set to 0x00 is set SWx pull-down voltage and CSy pull-up voltage to floating.

The detect action is one-off event and each time before reading out the open/short information, the OSDE bit of the Open/Short Register need to be set from “00” to “01” or “11” (clear before set operation).

DE-GHOST FUNCTION

The “ghost” term is used to describe the behavior of an LED that should be OFF but instead glows dimly when another LED is turned ON. A ghosting effect typically can occur when multiplexing LEDs. In matrix architecture any parasitic capacitance found in the constant-current outputs or the PCB traces to the LEDs may provide sufficient current to dimly light an LED to create a ghosting effect.

To prevent this LED ghost effect, the IS31FL3747 has integrated Pull down voltage for each SWx (x=1~12) and Pull up voltage for each CSy (y=1~12). Select the right SWx Pull down voltage and CSy Pull up voltage which eliminates the ghost LED for a particular matrix layout configuration.

Typically, selecting the 1.4V (V_{CC}-1.4V) will be sufficient to eliminate the LED ghost phenomenon.

When IS31FL3747 works in hardware shutdown mode, the de-ghost function should be disabled, otherwise it will be extra about 1μA shutdown current.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SSD bit of the Configuration Register to "0", the IS31FL3747 will operate in software shutdown mode. When the IS31FL3747 is in software shutdown, all current sources are switched off, so that the matrix is blanked. All registers can be operated. Typical current consume is 2.2μA when V_{CC}=5V.

Hardware Shutdown

The chip enters hardware shutdown when the SDB pin is pulled low. All analog circuits are disabled during hardware shutdown, typical the current consume is 2.2μA when V_{CC}=5V.

The chip releases hardware shutdown when the SDB pin is pulled high. During hardware shutdown state Function Register can be operated.

If V_{CC} has risk drop below 1.75V but above 0.1V during SDB pulled low, please re-initialize all Function Registers before SDB pulled high.

LAYOUT

As described in external resistor (R_{ISET}), the chip consumes lots of power. Please consider below factors when layout the PCB.

1. The V_{CC} (PVCC, VCC) capacitors need to close to the chip and the ground side should well connected to the GND of the chip.

2. R_{ISET} should be close to the chip and the ground side should well connect to the GND of the chip.

3. The thermal pad should connect to ground pins and the PCB should have the thermal pad too, usually this pad should have 16 or 25 via thru the PCB to other side's ground area to help radiate the heat. About the thermal pad size, please refer to the land pattern of each package.

4. The CSy pins maximum current is 47.8mA (R_{ISET}=10kΩ), and the SWx pins maximum current is larger, the width of the trace, SWx should have wider trace then CSy.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

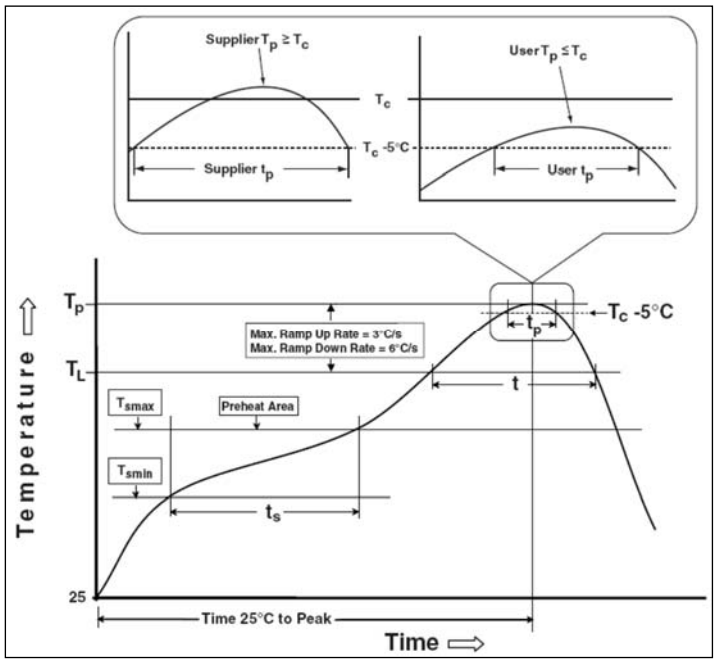
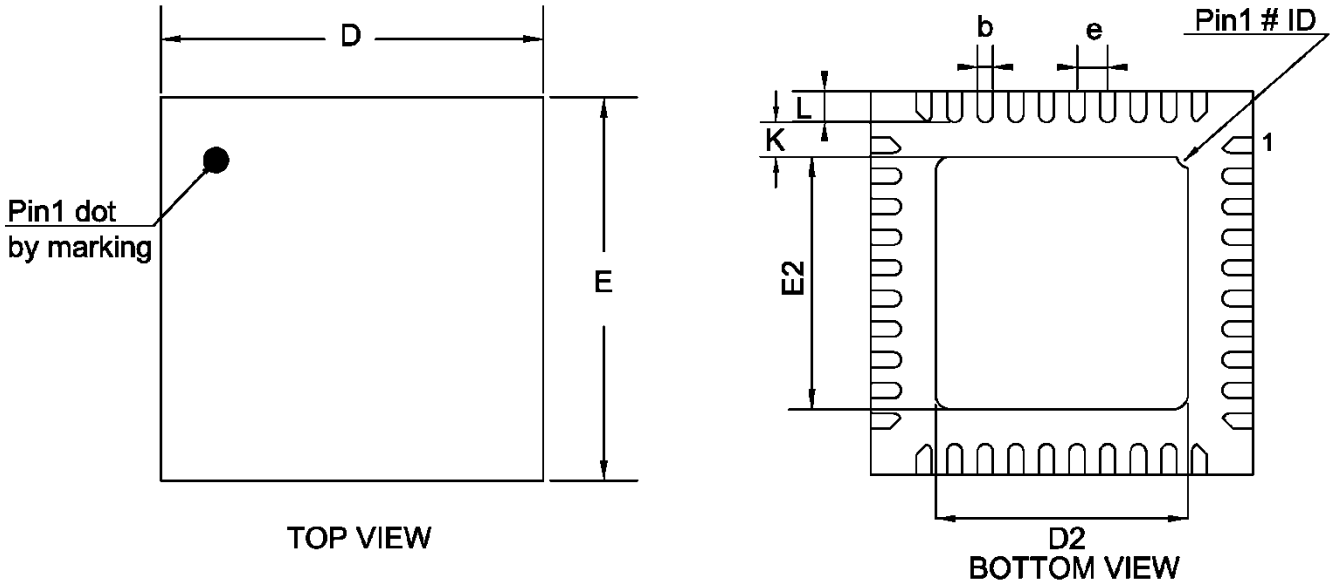
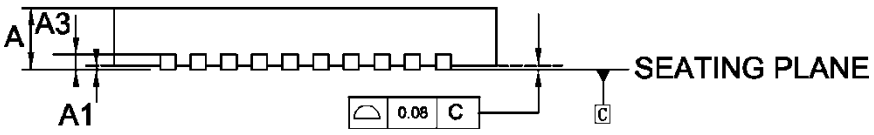


Figure 30 Classification Profile

PACKAGE INFORMATION

QFN-40





SIDE VIEW

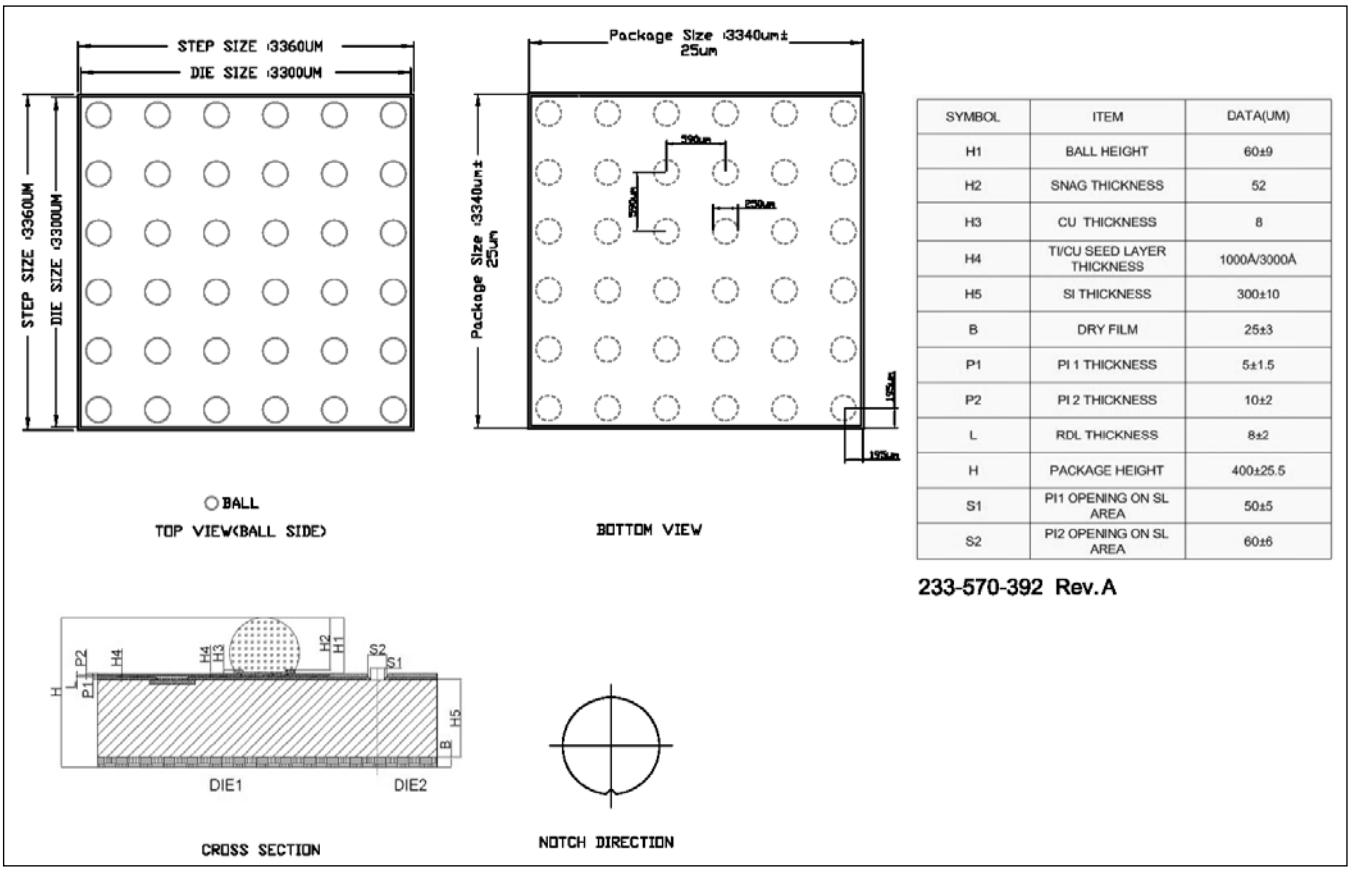
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.18	0.20	0.25
K	0.20	-	-
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.15	-	3.80
E2	3.15	-	3.80
L	0.30	0.40	0.50
e	0.40BSC		

NOTE:

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220
3. THE PIN'S SHARP AND THERMAL PAD SHOWS DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

233-570-291 Rev.B

WLCSP-36

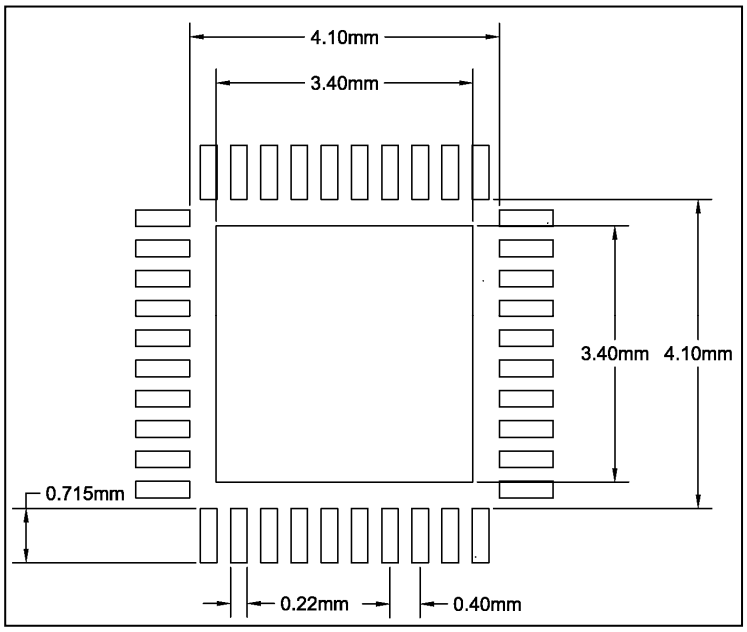


SYMBOL	ITEM	DATA(UM)
H1	BALL HEIGHT	60±9
H2	SNAG THICKNESS	52
H3	CU THICKNESS	8
H4	TI/CU SEED LAYER THICKNESS	1000Å/3000Å
H5	SI THICKNESS	300±10
B	DRY FILM	25±3
P1	PI 1 THICKNESS	5±1.5
P2	PI 2 THICKNESS	10±2
L	RDL THICKNESS	8±2
H	PACKAGE HEIGHT	400±25.5
S1	PI1 OPENING ON SL AREA	50±5
S2	PI2 OPENING ON SL AREA	60±6

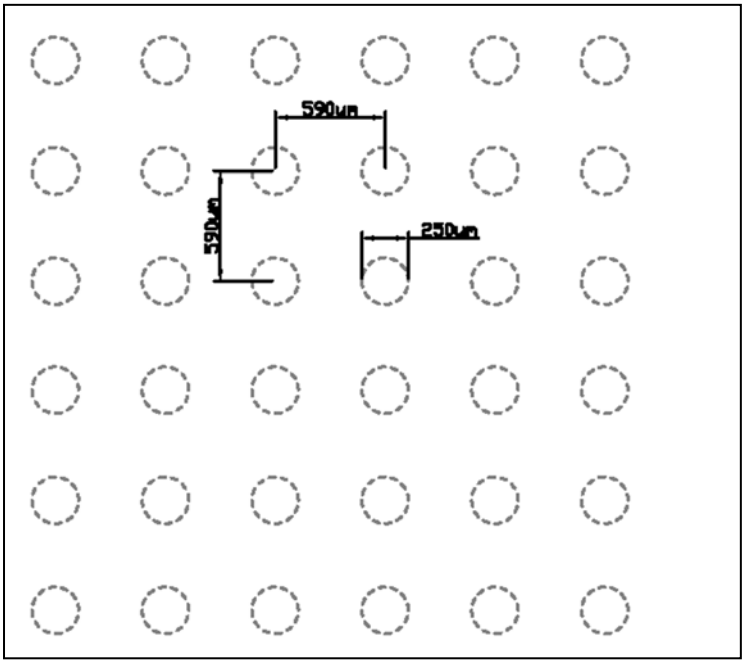
233-570-392 Rev.A

RECOMMENDED LAND PATTERN

QFN-40



WLCSP-36



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2021.09.08
B	1.Update EC table 2.Update Typical Application Circuit 3.Add WLCSP-36 package	2021.12.01
C	1. Update to new Lumissil logo and add RoHS 2. Update RJA value	2024.11.05