FCU900N60Z

MOSFET, N-Channel, SuperFET® II

600 V, 4.5 A, 900 mΩ

ON Semiconductor®

www.onsemi.com

Description

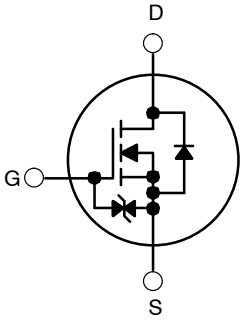
SuperFET® II MOSFET is ON Semiconductor's brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

Features

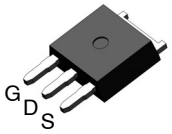
- 675 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 820 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 13 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 48.6 pF)
- 100% Avalanche Tested
- ESD Improved Capacity
- RoHS Compliant

Applications

- LCD/LED/PDP TV and Monitor Lighting
- Solar Inverter
- Charger

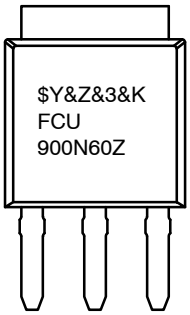


N−Channel



DPAK3
CASE 369AP

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCU900N60Z	= Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping
FCU900N60Z	FCU900N60Z	DPAK3	70 Units/ Tube

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	DC	±20	V
		AC (f > 1 Hz)	±30	
I_D	Drain Current	Continuous (T_C = 25°C)	4.5	A
		Continuous (T_C = 100°C)	2.8	
I_{DM}	Drain Current	Pulsed (Note 1)	13.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		47.5	mJ
I_{AR}	Avalanche Current (Note 1)		1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.52	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	52	W
		Derate above 25°C	0.42	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 1.0 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 2.3 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	100	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V, T_J = 25°C	625	–	–	V
		I_D = 1 mA, V_{GS} = 0 V, T_J = 150°C	675	–	–	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, referenced to 25°C	–	0.67	–	V/°C
BV_{DS}	Drain to Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 4.5 V	–	700	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 600 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.5	–	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.3 A	–	0.82	0.90	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2.3 A	–	4.6	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	534	710	pF
C_{oss}	Output Capacitance		–	399	530	pF
C_{rss}	Reverse Transfer Capacitance		–	19.7	30	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1 MHz	–	11.1	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	48.6	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 380 V, I_D = 2.3 A, V_{GS} = 10 V (Note 4)	–	13.1	17	nC
Q_{gs}	Gate to Source Gate Charge		–	2.2	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	4.5	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	2.4	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 380 V, I_D = 2.3 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	10.9	32	ns
t_r	Turn−On Rise Time		–	5.3	21	ns
$t_{d(off)}$	Turn−Off Delay Time		–	33.6	77	ns
t_f	Turn−Off Fall Time		–	11.9	34	ns
DRAIN−SOURCE DIODE CHARACTERISTIC						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	13.5	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2.3 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2.3 A, dI_F/dt = 100 A/μs	–	156	–	ns
Q_{rr}	Reverse Recovery Charge		–	1.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature.

TYPICAL PERFORMANCE CHARACTERISTICS

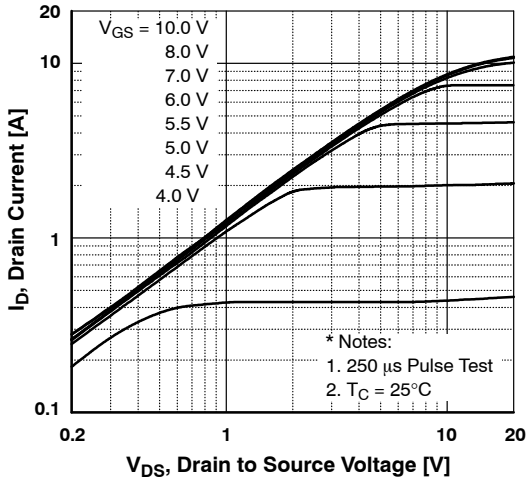


Figure 1. On−Region Characteristics

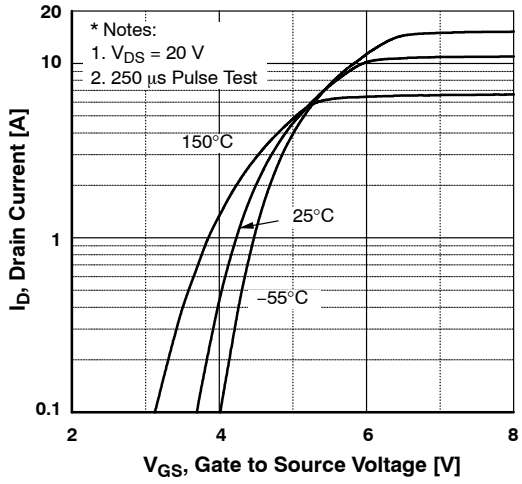


Figure 2. Transfer Characteristics

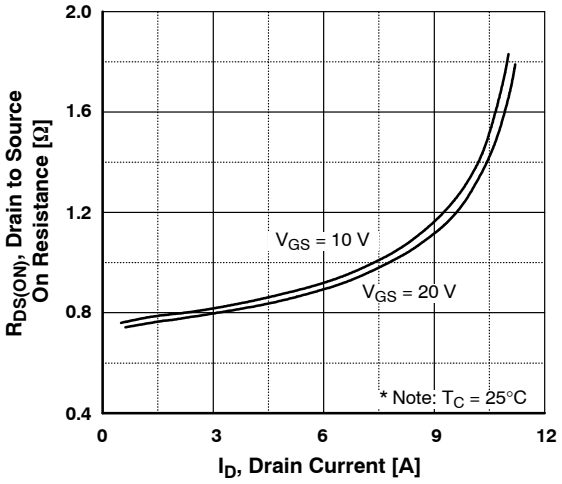


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

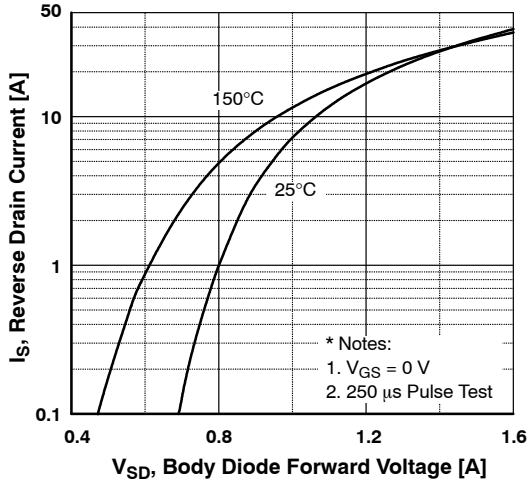


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

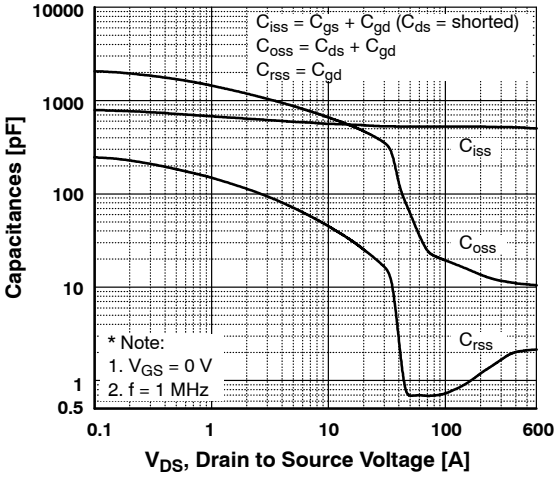


Figure 5. Capacitance Characteristics

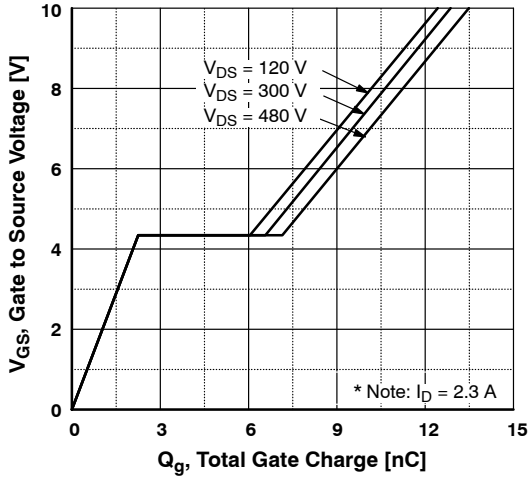


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

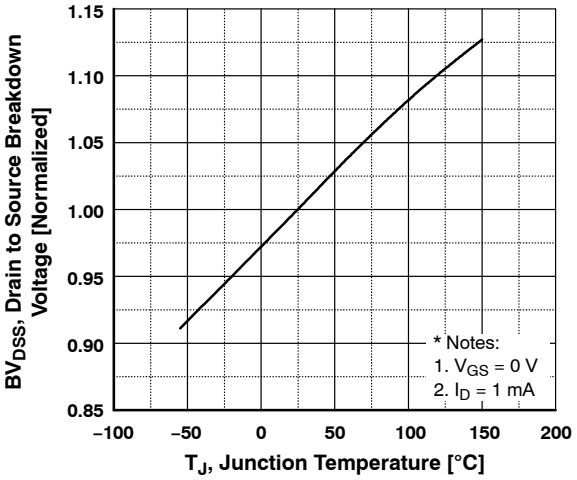


Figure 7. Breakdown Voltage Variation vs. Temperature

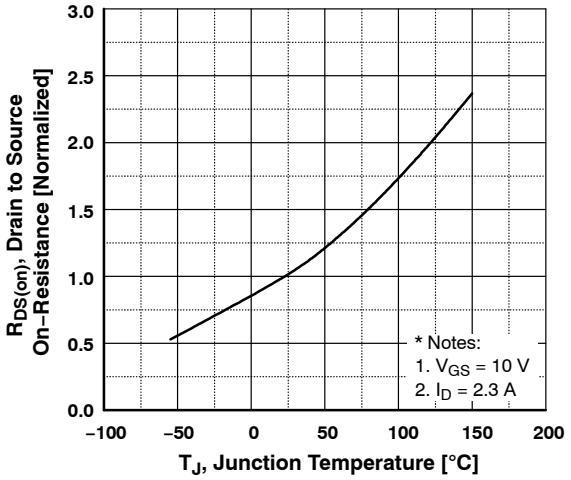


Figure 8. On−Resistance Variation vs. Temperature

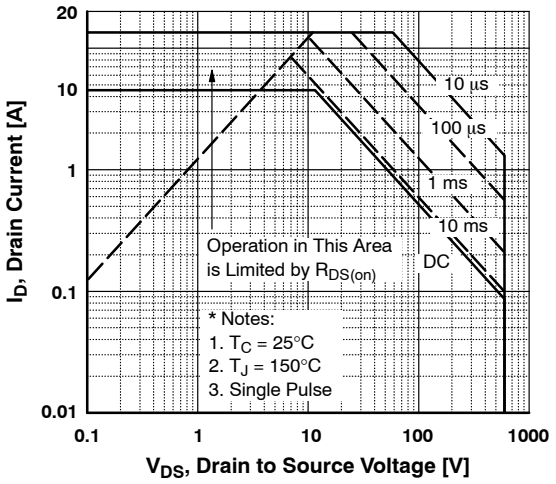


Figure 9. Maximum Safe Operating Area

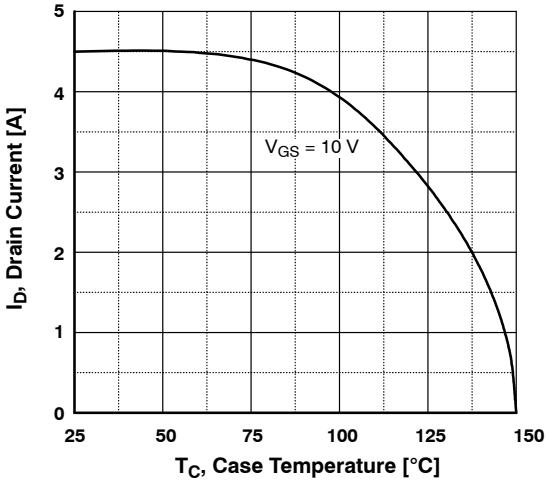


Figure 10. Maximum Drain Current vs. Case Temperature

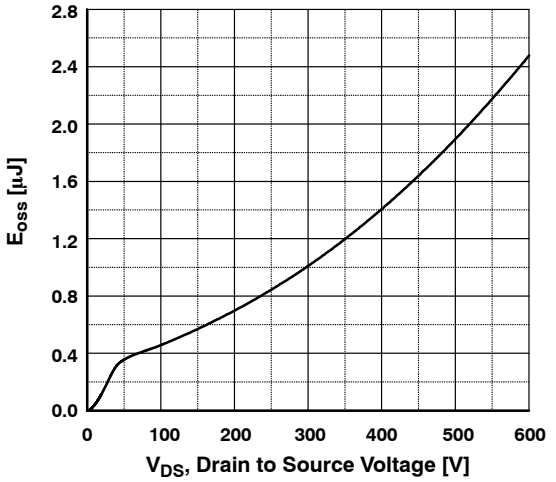


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

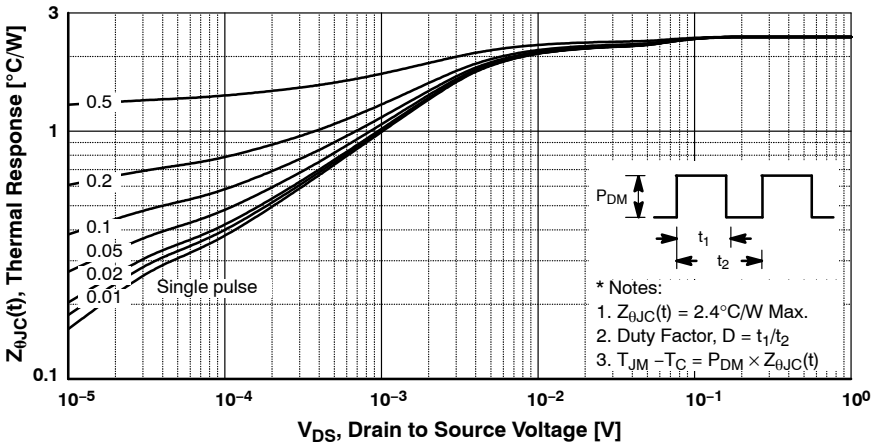


Figure 12. Transient Thermal Response Curve

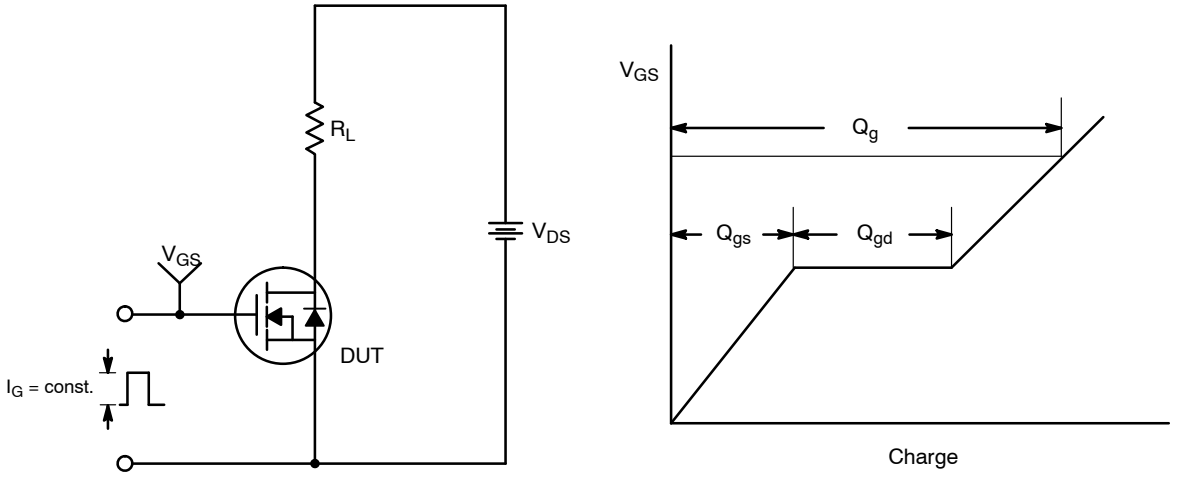


Figure 13. Gate Charge Test Circuit and Waveform

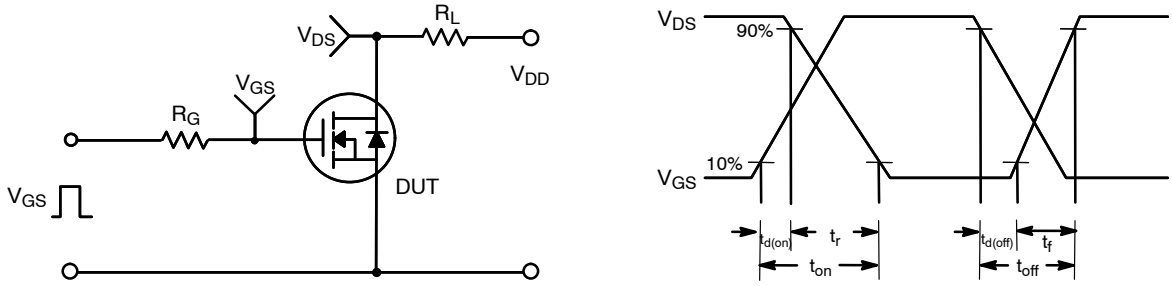


Figure 14. Resistive Switching Test Circuit and Waveforms

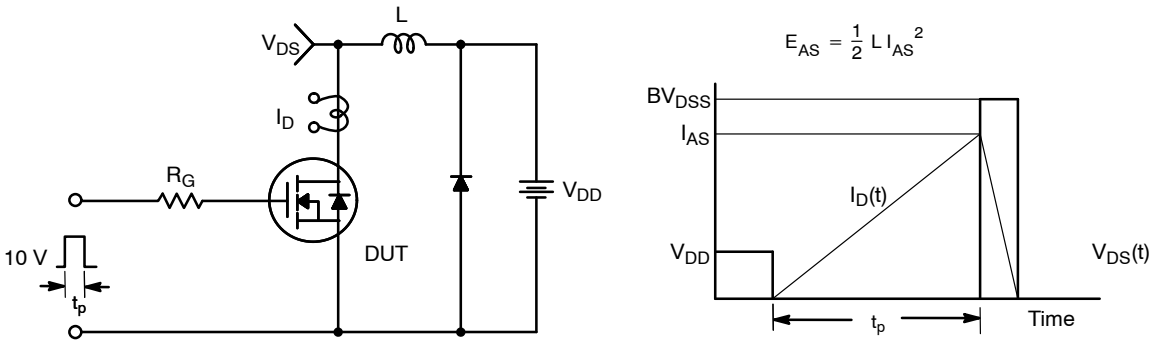


Figure 15. Unclamped Inductive Switching Test Circuit and Waveforms

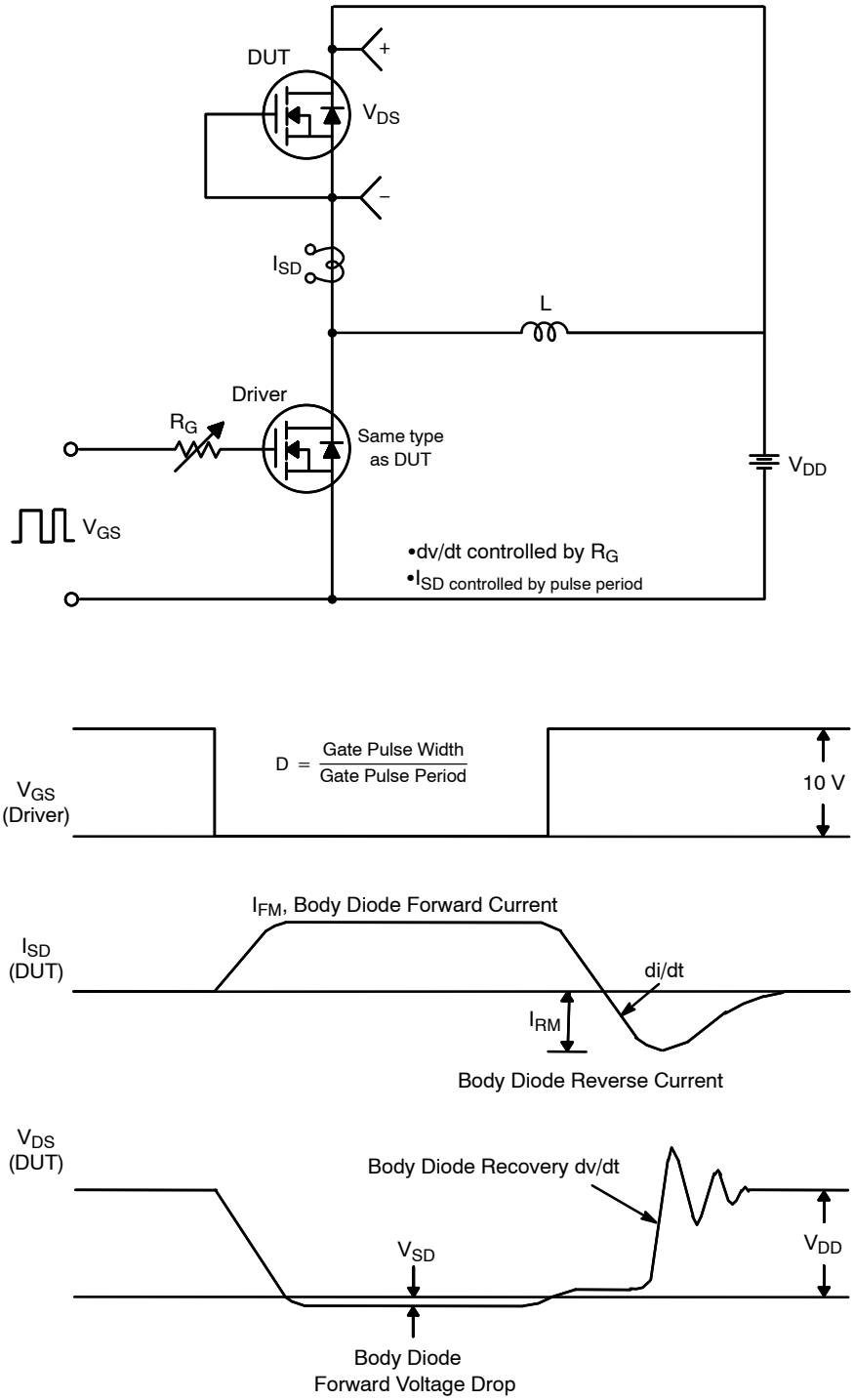
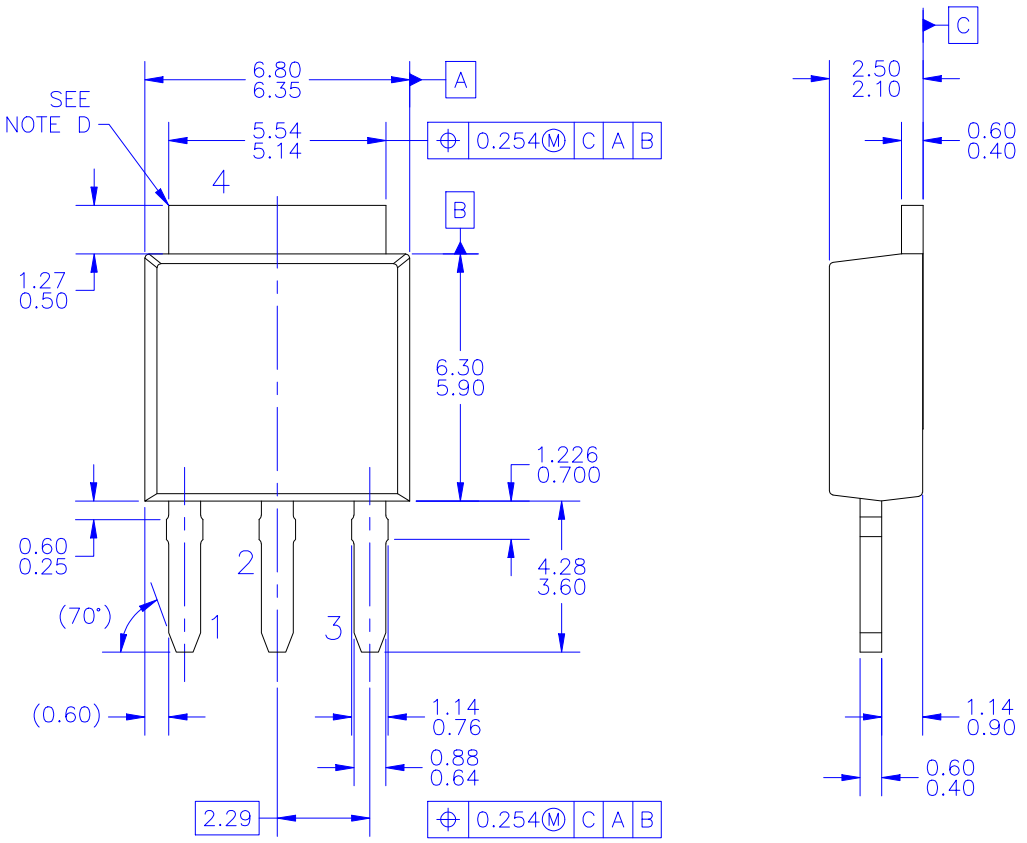


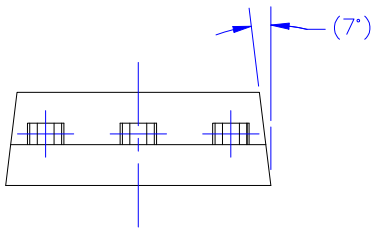
Figure 16. Peak Diode Recovery dv/dt Test Circuit and Waveforms

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DPAK3 (STRAIGHT LEADS)
CASE 369AP
ISSUE O

DATE 30 SEP 2016





NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) PACKAGE BODY REFERENCE: JEDEC, TO−251, ISSUE D, VARIATION AA, DATED JUNE 2002.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

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