UM12043

IMX91LP4EVK-11 Board User Manual

Rev. 1.0 — 15 November 2024 User manual

Document information

Information	Content
Keywords	UM12043, i.MX91 applications processor, IMX91LP4EVK-11 board, 91LP4EVK-11SOM (SOM board), 91LP4EVK-11BB (Base board)
Abstract	The i.MX 91 evaluation kit (IMX91LP4EVK-11 board) is a hardware platform designed to display the commonly used features of the i.MX 91 applications processor in a small and low-cost package.

1 IMX91LP4EVK-11 overview

The i.MX 91 Evaluation Kit (IMX91LP4EVK-11 board) is a platform designed to display the most commonly used features of the i.MX 91 applications processor. The IMX91LP4EVK-11 board is an entry-level development board with a small and low-cost package. The board enables developers to be familiar with the processor before investing a large amount of resources in more specific designs.

The IMX91LP4EVK-11 board is assembled with two separate boards:

- 91LP4EVK-11SOM: referred to as the "SOM board" in this document.
- 91LP4EVK-11BB: referred to as the "Base board" in this document.

This document includes system setup and configurations, and provides detailed information on the overall design and usage of the IMX91LP4EVK-11 board from a hardware system perspective.

1.1 Block diagram

Figure 1 shows the IMX91LP4EVK-11 block diagram.

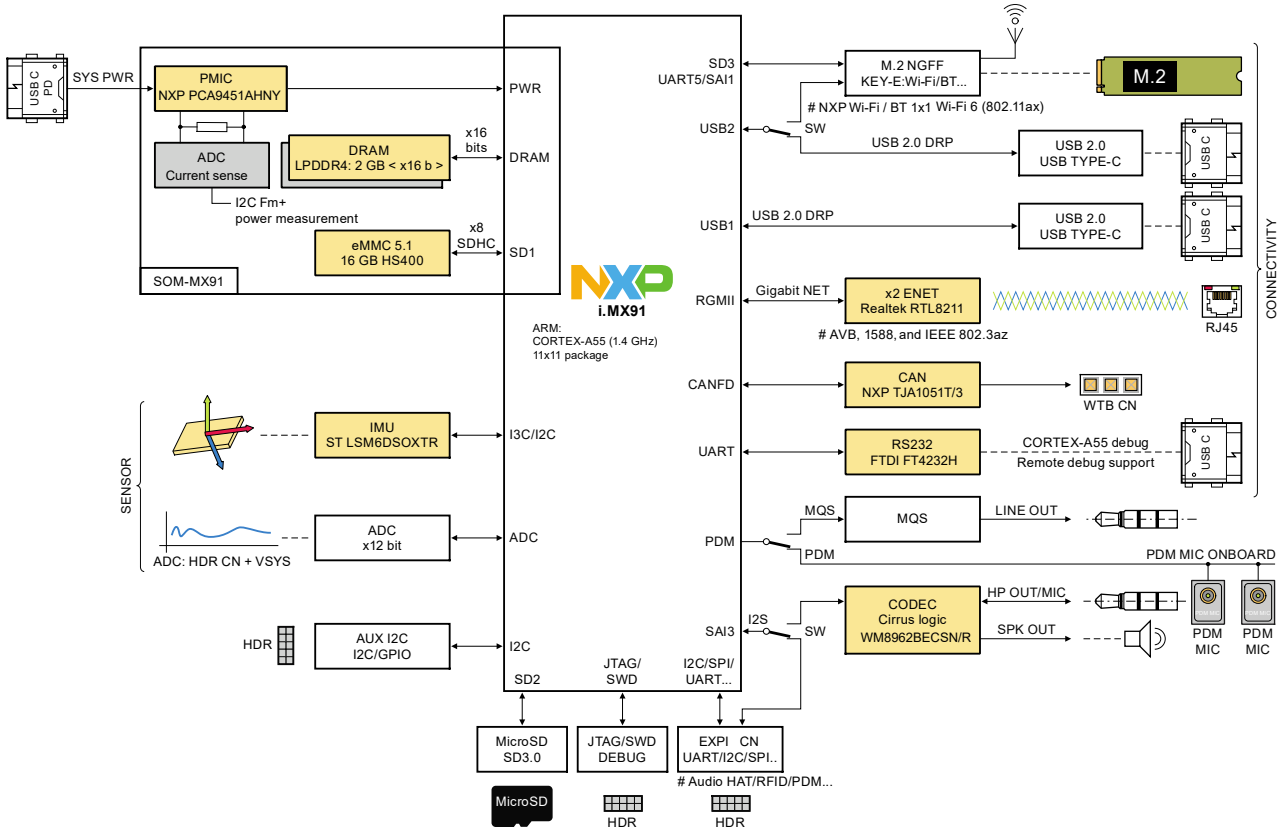


Figure 1. IMX91LP4EVK-11 block diagram

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1.2 Board kit contents

Table 1 lists the items included in the IMX91LP4EVK-11 board kit.

Table 1. Board kit contents

Item description	Quantity
IMX91LP4EVK-11 board assembled with two separate boards, 91LP4EVK-11SOM (SOM board) and 91LP4EVK-11BB (Base board)	1
USB Type-C 45 W Power Delivery Supply, 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 2.25 A supported	1
USB 3.0 Type-C Male to Type-A Male assembly cable	1
USB 3.0 Type-C Male to Type-A Female adapter	1
IMX91LP4EVK-11 Quick Start Guide	1

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1.3 Board pictures

Figure 2 shows the onboard connectors on the IMX91LP4EVK-11 board.

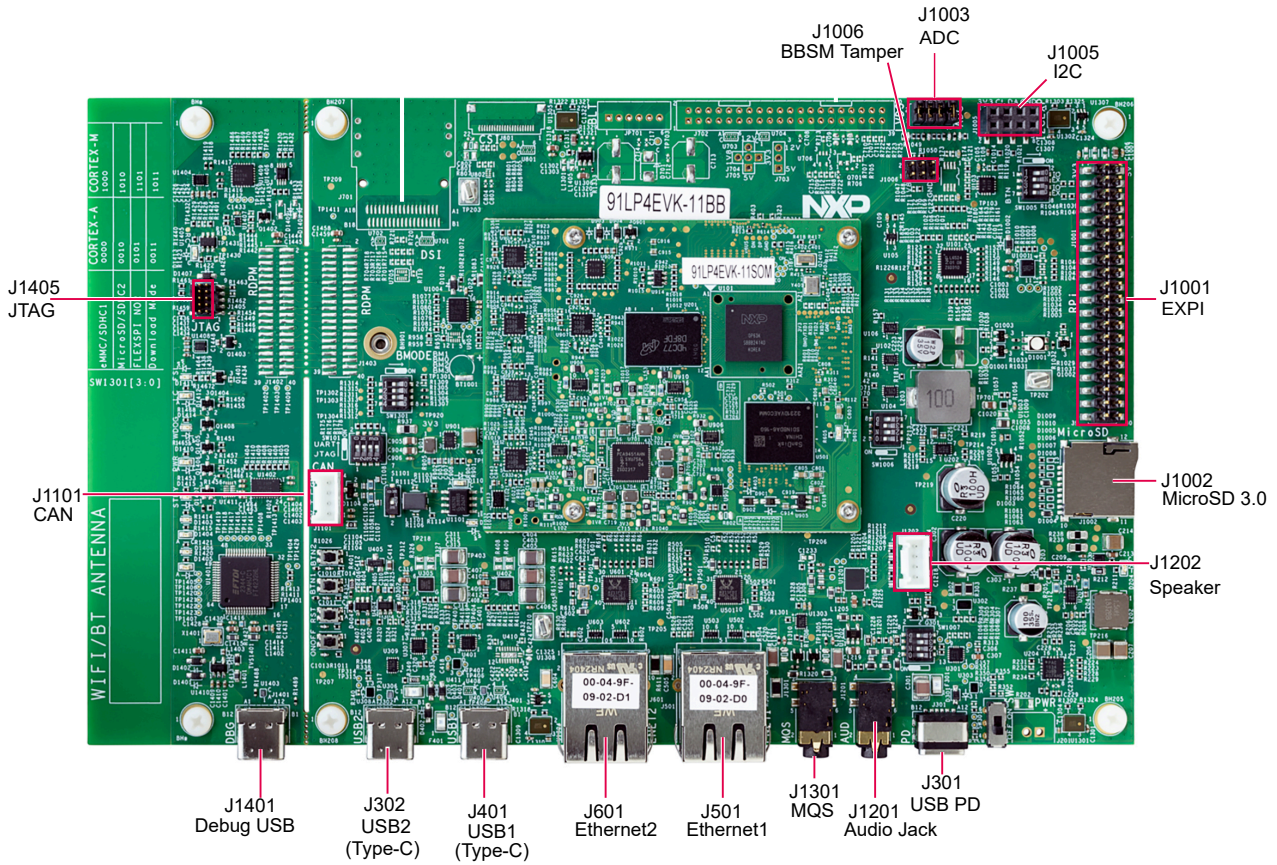


Figure 2. IMX91LP4EVK-11 onboard connectors

Figure 3 shows the onboard jumpers, switches, buttons, and LEDs available on the IMX91LP4EVK-11 board.

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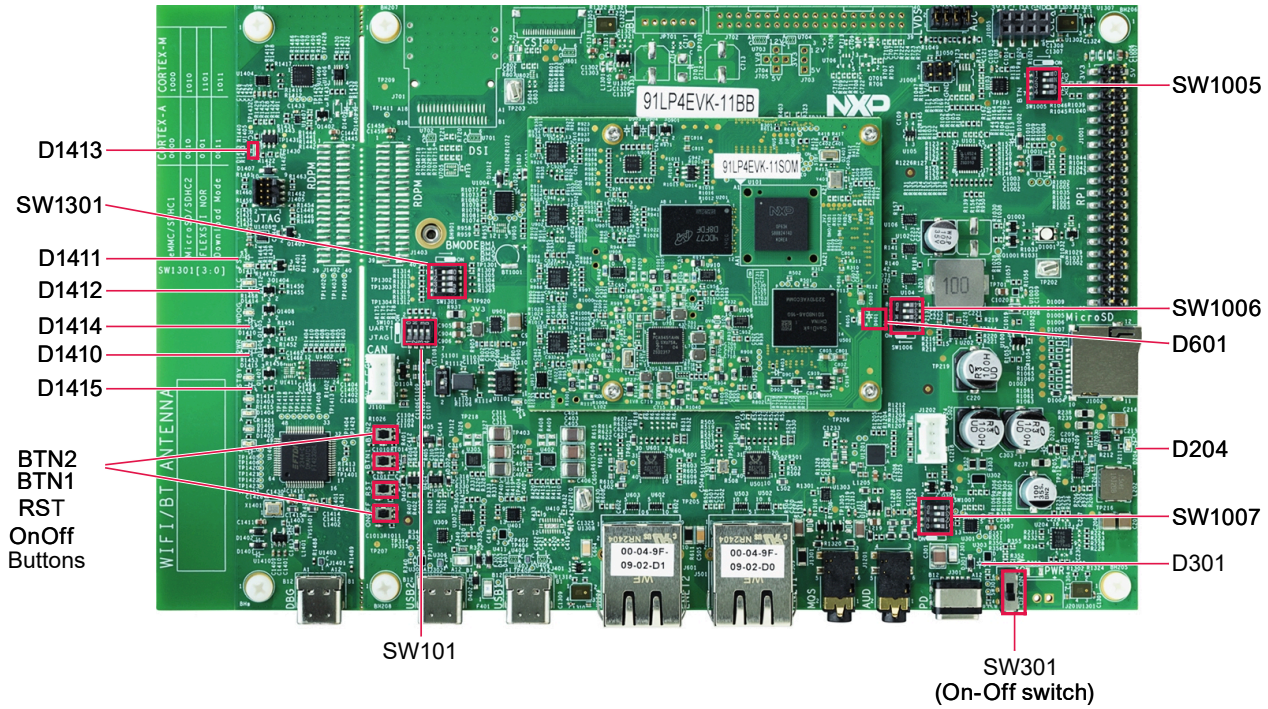


Figure 3. Switches, buttons, and LEDs on the IMX91LP4EVK-11 board

Figure 4 shows the bottom-side view of the IMX91LP4EVK-11 board.

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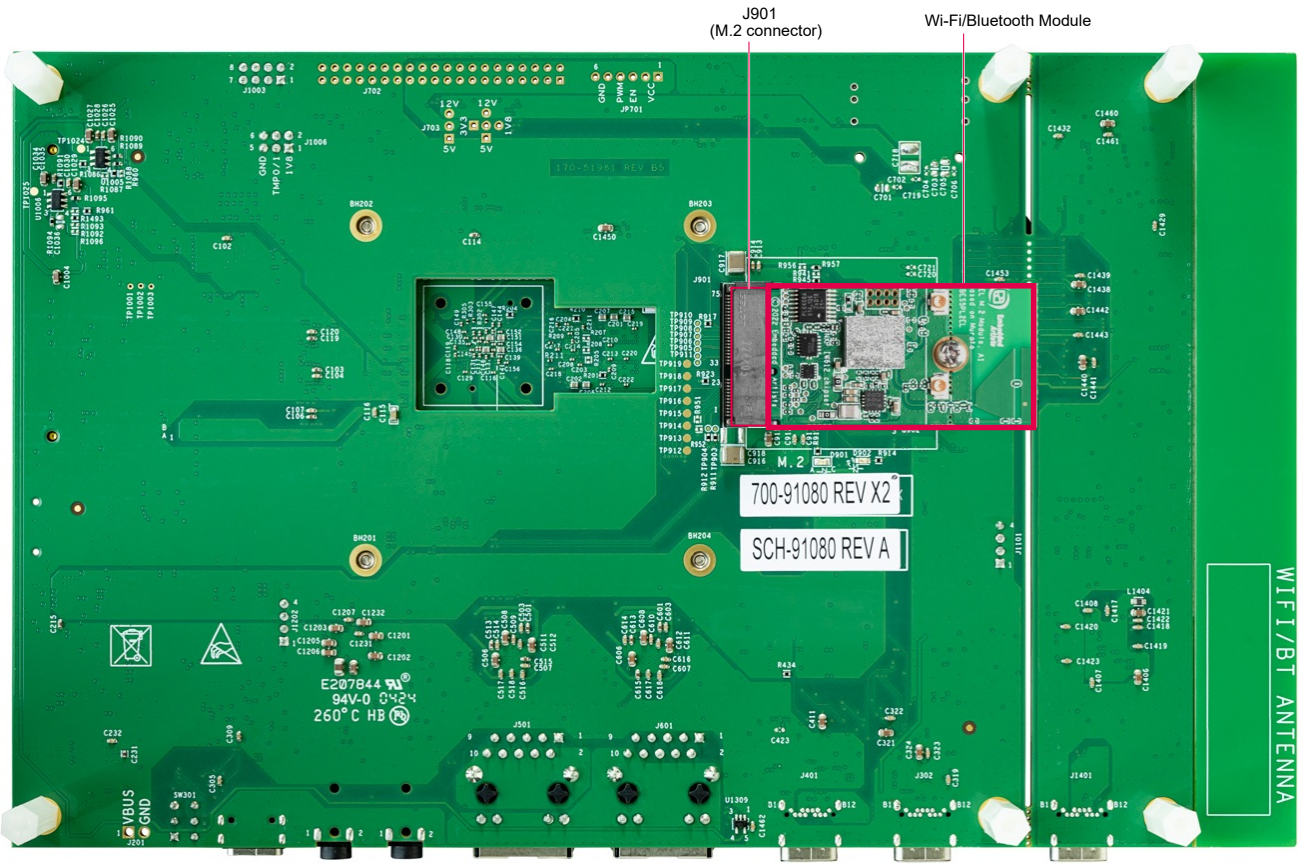


Figure 4. Bottom-side view of the IMX91LP4EVK-11 board

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1.4 Board features

Table 2 lists the features of IMX91LP4EVK-11.

Table 2. IMX91LP4EVK-11 features

Board feature	Target processor feature used	Description
Applications processor		The i.MX 91 applications processor features an Arm Cortex-A55 core that can operate at speeds of up to 1.4 GHz. ***Note:*** *For more details on the i.MX 91 processor, refer to the i.MX 91 Applications Processor Reference Manual and datasheet. See Section 6 "Related documentation"*
USB interface	USB 2.0 high-speed host and device controller	Two USB 2.0 Type C connectors
DRAM memory	DRAM controller and PHY	2 GB LPDDR4 (Micron MT53E1G16D1ZW-046 AAT:C)
Mass storage	uSDHC	• 16 GB eMMC5.1 (SanDisk SDINBDA6-16G-I(3D TLC)) • MicroSD card connector (SD3.0 supported)
Boot configuration		• Default boot mode is single boot from the eMMC device • The board supports three other boot devices listed below: – QSPI NOR Flash (M2-NOR-Flash) – QSPI NAND Flash (M2-NAND-Flash) – SD card (MicroSD connector)
Ethernet interface	Two Ethernet controllers	• 10/100/1000 Mbit/s RGMII Ethernet supporting TSN connected with external PHY, RTL8211 through an RJ45 connector (J501) • 10/100/1000 Mbit/s RGMII Ethernet connected with external PHY, RTL8211, through an RJ45 connector (J601)
CAN interface	CAN	One high-speed CAN transceiver NXP TJA1057GT/3 (U1101) and a 4-pin CAN FD connector (J1101)
Wi-Fi/Bluetooth interface	USB, SDIO, I2S, UART, I2C, and GPIO	• One M.2/NGFF Key E mini card 75-pin connector (J901) supporting SDIO, I2S, UART, I2C, and vendor-defined SPI interfaces • Murata Wi-Fi/Bluetooth module. It is based on NXP IW612/IW610 SoC, which supports dual-band (2.4 GHz /5 GHz) 1x1 Wi-Fi 6, Bluetooth 5.4, and IEEE 802.15.4
Audio	SAI/I2S	• 3.5 mm audio jack for headset, microphone, headphone output support, J1201 • Audio codec WM8962BECSN/R (U1201) can support 24-bit I2S data and 48 kHz sampling rate
	PDM	• Four onboard PDM microphone support • 3.5 mm audio jack for headset, microphone, headphone output support, J1301
	MQS	MQS support
Sensors	I2C/I3C	• LSM6DSOXTR (U1001) Inertial module—a 3D digital accelerometer and gyroscope
ADC interface	ADC	Four-channel ADC support
TAMPER	Battery backed non-secure module (BBNSM)	x2 Tamper function support

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Table 2. IMX91LP4EVK-11 features*...continued*

Board feature	Target processor feature used	Description
Debug interface		• USB-to-UART/MPSSE ICs device, FT4232H • One USB 2.0 Type-C connector (J1401) of FT4232H provides four COM ports: – The first and second ports are reserved. – The third port is connected to UART1 for Cortex A55 system debugging. – The fourth port is connected to UART2 for general communication. • FT4232H is used for remote debug of JTAG, boot mode, ONOFF, SYS_nRST, and power measurement board communication
EXPI		2x20 pin expansion interface J1001 for I2S, parallel display, parallel camera, UART, I2C, and GPIO expansion
I2C connector	I2C	8-pin dual-row pin header J1005 for I2C expansion
I/O expanders		• One I/O expander to provide remote I/O expansion for the target processor via the I2C-bus interface • One I/O expander to provide I/O expansion for FT4232H device for boot configuration, ONOFF, POR_B, and SYS_nRST
Power supply		• One USB 2.0 Type-C connector for power delivery only • PCA9451AHNY PMIC • Discrete DCDC/LDO
Power monitoring		Six quad-channel power monitors (PAC1934T-I/JQ) for power and energy monitoring (U902, U904, U907, U911, U912 on SOM board and U2014 on Base board)
PCB		• 91LP4EVK-11SOM: 2.4 inch × 2.9 inch, 6-layer • 91LP4EVK-11BB: 5 inch × 7.45 inch, 8-layer
Orderable part number		IMX91LP4EVK-11

1.5 Connectors

Table 3 describes the 91LP4EVK-11BB board connectors. See Figure 2 for the position of connectors on the board.

Table 3. 91LP4EVK-11BB connectors

Connector	Description	Connector type	Reference section
J302, J401	USB connectors	USB 2.0 Type C	Section 2.13 "USB interface"
J501, J601	Ethernet connectors	RJ45 jack	Section 2.14 "Ethernet"
J101, J103	DF40C-80DS-0.4V	2x40-pin socket	Board-to-board connector for SOM board
J102	DF40C-100DS-0.4V	2x50-pin socket	Board-to-board connector for SOM board
J901	M.2 socket KEY-E	75-pin connector	Section 2.10 "M.2 connector and Wi-Fi/ Bluetooth module"
J1001	EXPI	2x20-pin connector	Section 2.15 "EXPI"
J1002	MicroSD 3.0	Micro SD push-push connector	Section 2.8 "SD card interface"

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Table 3. 91LP4EVK-11BB connectors*...continued*

Connector	Description	Connector type	Reference section
J1003	ADC x4 channel	2x4-pin connector	Four pins connect to the ADC_IN[3:0] pins of the target processor
J1005	I2C connector	2x4-pin connector	Section 2.4 "I2C interface"
J1006	BBSM tamper	2x3-pin connector	The header can be used for tamper different mode test
J1101	CAN bus	4-pin connector	Section 2.12 "CAN interface"
J1201	Audio codec	3.5 mm headphone jack	Section 2.6 "Audio interface"
J1202	Speaker connector	1x4-pin plug	Section 2.6 "Audio interface"
J1301	KJ366EYS MQS connector	3.5 mm audio jack	Section 2.6 "Audio interface"
J1401	USB debug connector	USB Type-C connector	Section 3.1 "USB debug interface"
J1404	DF40B-12DS-0.4V(51)	12-pin board-to- board receptacle for power measurement	Section 2.2.2 "Power measurement board connector"
J1405	FTSH-105-01-L-DV-K JTAG header	2x5-pin connector	Section 3.2 "JTAG interface"

Table 4 describes the connectors available on the 91LP4EVK-11SOM board.

Table 4. 91LP4EVK-11SOM board connectors

Connector	Description	Connector type
J801, J802	DF40C-80DP-0.4V SOM-to-Base board connectors	2x40-pin connectors
J803	DF40C-100DP-0.4V SOM-to-Base board connector	2x50-pin connector

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1.6 User LEDs

The IMX91LP4EVK-11 board has light-emitting diodes (LEDs) to monitor system functions, such as power-on, reset, board faults. The information collected from LEDs can be used for debugging purposes.

Figure 3 shows the LEDs available on the board. Table 5 describes the IMX91LP4EVK-11 LEDs.

Table 5. IMX91LP4EVK-11 LEDs

Part identifier	LED color	LED name	Description (When LED in ON)
D204	Red	PWR LED	LED for main power supply. When ON, indicates that VDD_5V power supply is ON, and board is powered on.
D1403	Orange	Cortex A55 UART1	• D1404 ON – The UART data transmitted to host computer. • D1403 ON – The UART data received from host computer.
D1404	Green		
D1405	Green	UART2	• D1405 ON – The UART2 data transmitted to host computer. • D1406 ON – The UART2 data received from host computer.
D1406	Orange		
D1410	Red	System LED	• ON: FT4232H IC power is ON • OFF: FT4232H IC power is OFF
D1411	Orange		• ON: FT4232H function is suspended • OFF: FT4232H function is running
D1412	Red		• ON: Local JTAG for debug • OFF: Remote JTAG for debug
D1413	Green		• ON: Remote JTAG for debug • OFF: Local JTAG for debug
D1414	Orange		• ON: WDOG_B trigger to PCA9451AHNY PMIC • OFF: Normal
D1415	Orange		• ON: System Monitor is suspended • OFF: System Monitor is running

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1.7 Push buttons

Figure 3 shows the push buttons available on the board.

Table 6 describes the push buttons available on IMX91LP4EVK-11.

Table 6. IMX91LP4EVK-11 push buttons

Part identifier	Switch name	Description
SW1001	Power button	The i.MX 91 applications processor supports the use of a button input signal to request main SoC power state changes (that is, ON or OFF) from the PMIC. The ON/OFF button is connected to the ON/OFF pin of the i.MX 91 processor. • In the ON state: – If ON/OFF button is held longer than the debounce time, the power off interrupt is generated – If the button is held longer than defined max timeout, the state transits from ON to OFF, and send PMIC_ON_REQ signal to turn off the powers of PMIC. • In the OFF state: – If the ON/OFF button is held longer than the OFF-to-ON time, the state transits from OFF to ON, and send PMIC_ON_REQ signal to turn on the powers of PMIC
SW1002	Reset button (RESET)	The button is directly connected to the PMIC PCA9451AHNY. Holding the RESET button forces a reset of the PMIC power outputs except NVCC_SNVS_1V8 on the EVK board. The i.MX 91 applications processor is immediately turned off and reinitiates a boot cycle from the OFF state.
SW1003, SW1004	User button	The User buttons are kept for customized use cases.

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1.8 DIP switches

As shown in Table 7, three 4-bit DIP switches (SW1005, SW1006, and SW1007) are used on the IMX91LP4EVK-11 board for signal path selection for the below signals:

- SW1005 is used for RFU_BTN1 and RFU_BTN2 signals path selection. These signals are used as buttons (SW1003, SW1004) interrupts. By default, RFU_BTN1 and RFU_BTN2 signals connect with EXP_GPIO_IO23 and EXP_GPIO_IO24 from EXP GPIO connector (J1001).
- SW1006 is used for ENET1_nINT and ENET2_nINT signals, which are used as Ethernet PHY interrupts. By default, the signals connect with EXP_BTN1 and EXP_BTN2 from I2C IO expander (U101).
- SW1007 is used for USB_I2C_SDA and USB_I2C_SCL signals, which are USB-related peripherals configuration signals of the USB I2C bus. SW1007 connects these signals with GPIO_IO28 and GPIO_IO29 for I2C3 port by default.

Table 7. IMX91LP4EVK-11 DIP switches

Value SW	Signal name	4'b0101	4'b1010
SW1005	RFU_BTN1	EXP_BTN1	EXP_GPIO_IO23 (default)
	RFU_BTN2	EXP_BTN2	EXP_GPIO_IO24 (default)
SW1006	ENT1_nINT	GPIO_IO28	EXP_BTN1 (default)
	ENT2_nINT	GPIO_IO29	EXP_BTN2 (default)
SW1007	USB_I2C_SDA	GPIO_IO28 (default, used as I2C3_SDA)	I2C_SDA_BUF
	USB_I2C_SCL	GPIO_IO29 (default, used as I2C3_SCL)	I2C_SCL_BUF

See Figure 3 for the DIP switch positions on the board.

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2 Functional description

This chapter describes the features and functions of the IMX91LP4EVK-11 board components. It includes information about the processor, boot modes, storage devices, clocks, board interfaces, and debug support.

2.1 Processor

The i.MX 91 applications processor includes an Arm Cortex-A55 processor with speed up to 1.4 GHz. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbit/s Ethernet controllers, one supporting time sensitive networking (TSN), drive gateway applications with low latency. The part number used is MIMX9131CVVXJAA. (U101). This part is qualified for Industrial applications (-40C to 105C).

The i.MX 91 is useful for applications such as:

- Smart home
- Building control
- Contactless HMI
- Commercial
- Healthcare
- Media IoT

The processor provides a 16-bit LPDDR4 memory interface and other interfaces for connecting peripherals, such as WLAN, Bluetooth, USB2.0, uSDHC, Ethernet, CAN, ADC, and multi-sensors.

For more detailed information about the processor, see the *i.MX 91 data sheet* and *i.MX 91 Reference Manual* at https://www.nxp.com/imx91.

2.2 Power supply

The primary power supply to the IMX91LP4EVK-11 board is VBUS_IN (12 V - 20 V) through a USB-Type C power delivery (PD) connector (J301).

To switch on or off the VBUS_IN supply, one system power slider switch M096H-A020RT21A (SW301), is provided on the board. Table 8 describes the SW4 configuration.

Table 8. Power switch (SW301) configuration

SW301 switch	Description
Pin 1-2 and 4-5 closed	VBUS_IN power supply is OFF on the board (default setting)
Pin 2-3 and 5-6 closed	VBUS_IN power supply is ON

One DC buck switching regulator is used:

- MP8759GD (U201) switches VBUS_IN supply to SYS_5V (5 V) power supply, which is the input power supply for PCA9451AHNY PMIC and other discrete devices on the board.
  Note: *J201 connector is reserved for power input test. When the USB PD charger is not in use, user can provide 15 V power on J201 and short R202 to power up the system (For test purpose only). Figure 5 shows the IMX91LP4EVK-11 power supply block diagram.*

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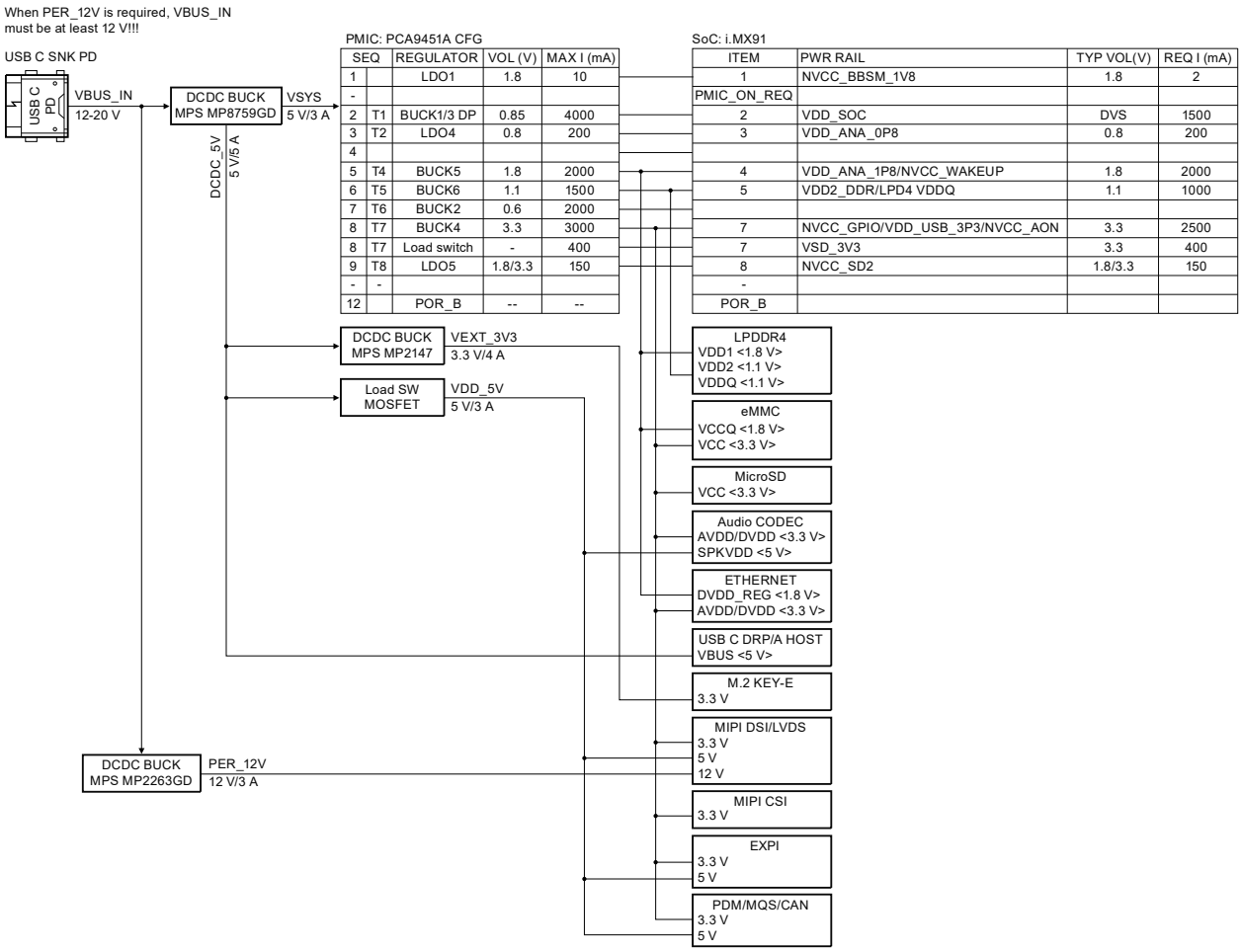


Figure 5. IMX91LP4EVK-11 power tree

Table 9 describes different power sources available on the board.

Table 9. IMX91LP4EVK-11 power supply devices

Part identifier designator	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
U201	MP8759GD	Monolithic Power Systems Inc.	• DCDC_5V • VSYS_5V	• 5 V at 8 A	Supplies power to: • NX20P3483UK USB PD and Type-C switches (U305 and U402) • PMIC PCA9451AHNY • DC buck MP2147GD (U901) • Always-ON LDO for load switch (U905)
U901	MP2147GD	Monolithic Power Systems Inc.	VEXT_3V3	3.3 V at 4 A	Supplies power to M.2 / NGFF interface
U701	PCA9451AHNY	NXP Semiconductors	BUCK2: LPD4/ x_VDDQ_0V6	0.6 V at 2 A	Not used for i.MX 91, i.MX 91 only supports LPDDR4.

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Table 9. IMX91LP4EVK-11 power supply devices*...continued*

Part identifier designator	Manufacturing part number	Part manufacturer	Power supply	Specifications	Description
			BUCK1/3[1][2]: VDD_ SOC_0 V85	0.65/0.8/0.85 V at 4 A dynamic voltage scaling (DVS) ***Note:*** *Refer to the i.MX 91 datasheet.*	VDD_SOC, power supply for SoC logic and Arm core
			BUCK4: • VDD_3V3	• 3.3 V at 3 A	Supplies power to: • Board-to-board connector for 91LP4EVK-11SOM board (J803) • 9 • NVCC_GPIO, power supply for GPIO when it is in 3.3 V mode • VDD_USB_3P3 pin for USB PHY power • eMMC 5.1 device
			BUCK5: • VDD_1V8	• 1.8 V at 2 A	Supplies power to: • Board-to-board connector for 91LP4EVK-11SOM (J801) • eMMC 5.1 device • VDD_ANA_1P8, analog core supply voltage • NVCC_WAKEUP, digital I/O supply
			BUCK6: • LPD4/x_ VDD2_1V1	• 1.1 V at 1.5 A	Supplies power to: • VDD2_DDR, DDR PHY supply voltage
			LDO1: NVCC_ BBSM_ 1V8	• 1.8 V at 10 mA	NVCC BBSM I/O supply
			LDO4: VDD_ ANA_0 P8	• 0.8 V at 200 mA	Analog core supply voltage
			LDO5: NVCC_ SD2	• 1.8 V/3.3 V	MicroSD card
			Switch: VSD2_3 V3	• 3.3 V	MicroSD card on base board
U203	DML3006LFDS-7 (Load switch)	Diodes Incorporated	VDD_5V	5 V at 10 A	• PDM/MQS/CAN interface • EXPI interface
U1306	NCP161ASN180 T1G (Load switch)	ON Semiconductor	VMIC_1V8	1.8 V	Supplies to four DMICs

1. BUCK1 and BUCK3 are configured in dual phase mode.
2. The PCA9451AHNY BUCK1/3 dual phase default output voltage is 0.85 V.

For further details of the power sequence required by the i.MX 91 processor, refer to section "Power sequence" in the *i.MX 91 Applications Processor Reference Manual.*

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2.2.1 Power monitoring

The IMX91LP4EVK-11 board includes six quad-channel current monitors for power and energy monitoring. See Table 10.

Table 10. Power monitoring devices

Part identifier	Manufacturing part number	FT4232 I2C address	Power rail
On SOM board			
U902	PAC1934T-I/JQ	0x11	• NVCC_BBSM_1V8 • VDD_SOC_0V85 • BB_VSYS_5V • S1_NVCC_BBSM_1V8
U904	PAC1934T-I/JQ	0x12	• LPD4/x_VDDQ_0V6 • S1_VDD_SOC_0V85 • NVCC_SD • S1_CPU_VDD2_DDR
U907	PAC1934T-I/JQ	0x13	• LPD4/x_VDDQ_0V6 • S1_CPU_VDDQ_DDR • LPD4/x_VDD2_1V1 • BUCK1_LSW4_CPU_1V8
U911	PAC1934T-I/JQ	0x14	• S1_VSYS_5V • VDD_3V3 • VDD_ANA_0V8
U912	PAC1934T-I/JQ	0x15	• VDD_1V8 • VDD_ANA_1V8 • VSD_3V3
On Base board			
U204	PAC1934T-I/JQ	0x16	• VEXT_3V3 • DCDC_5V_OUT • VBUS_IN

2.2.2 Power measurement board connector

One 12-pin board-to-board connector (J1404) is provided on the 91LP4EVK-11BB board to support Power Measurement Board connection, which you can use to evaluate the power consumption of most of the power rails in different user cases. Refer to Table 11.

Table 11 lists the J1404 connector pin definitions.

Table 11. J1404 pin definitions

Pins in Row1			Pins in Row 2		
Pin number	**Net name**	**Description**	**Pin number**	**Net name**	**Description**
1	VCC_FT_3V3	Power output, 3.3 V	2	GND	Ground
3	FT_SCL	FT4232 I2C clock signal, 3.3 V	4	FT_IO_nINT	FT4232 GPIO signal
5	FT_SDA	FT4232 I2C data signal, 3.3 V	6	FT_IO_nRST	FT4232 GPIO signal

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Table 11. J1404 pin definitions...*continued*

Pins in Row1			Pins in Row 2		
Pin number	**Net name**	**Description**	**Pin number**	**Net name**	**Description**
7	FT_EECLK	FT4232 EECLK signal, 3.3 V	8	Not connected	Not connected
9	FT_EEDATA	FT4232 EEDATA signal, 3.3 V	10	FT_EECS	FT4232 EECS signal, 3.3 V
11	VCC_FT_3V3	Power output, 3.3 V	12	GND	Ground

2.3 Clocks

IMX91LP4EVK-11 provides all the clocks required for the processor and peripheral interfaces. Table 12 summarizes the specifications of each clock and the component that provides it.

Table 12. IMX91LP4EVK-11 clocks

Part identifier	Clock generator	Clock	Specifications	Destination
Y401 (SOM board)	Crystal oscillator	XTALI_24M XTALO_24M	Frequency: 24 MHz	Target processor
QZ401 (SOM board)	Crystal oscillator	XTALI_32K XTALO_32K	Frequency: 32.768 kHz	NVCC_BBSM block of target processor
QZ701 (SOM board)	Crystal oscillator	XIN_32K XOUT_32K	Frequency: 32.768 kHz	PCA9451AHNY PMIC
X1401 (Base board)	Crystal oscillator	FT_OSCI FT_OSCO	Frequency: 12 MHz	FT4232H
Y501 (Base board)	Crystal oscillator	ETH1_XTALI ETH1_XTALO	Frequency: 25 MHz	Ethernet RGMII PHY1
Y601 (Base board)	Crystal oscillator	ETH2_XTALI ETH2_XTALO	Frequency: 25 MHz	Ethernet RGMII PHY2
U1004 (Base board)	PCF2131 (External RTC)	RTC_CLKO	Frequency: 32.768 kHz	I2C IO expansion header U101

2.4 I2C interface

The i.MX 91 processor supports a low-power inter-integrated circuit (I2C) module that supports an efficient interface to an I2C-bus as a master. The I2C provides a method of communication between various devices available on the IMX91LP4EVK-11 board.

One 8-pin dual-row pin header connector (J1005) is provided on the IMX91LP4EVK-11 board to support I2C connection. Developers can use the port for specific application development.

Table 13 explains the I2C header, J1005, pinout.

Table 13. I2C header (J1005) pinout

Pin	Signal name	Description
1, 2	VDD_3V3	Power output, 3.3 V
3, 4	I2C1_SCL	I2C clock signal, 3.3 V
5, 6	I2C1_SDA	I2C data signal, 3.3 V

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Table 13. I2C header (J1005) pinout...*continued*

Pin	Signal name	Description
7, 8	GND	Ground

Table 14 describes the I2C devices and their I2C addresses (7-bit) on the Base board.

Table 14. I2C devices on Base board

Part identifier	Device	I2C address (7-bit)	Port	Speed	Voltage	Description
U101	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2	1 MHz Fm+	3.3 V	I/O expander for IRQ / output
U103	ADP5585ACPZ-00-R7	0x34 (0b'01101[00]x)	MX-I2C2	1 MHz Fm+	3.3 V	I/O expander for output
U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C3	1 MHz Fm+	3.3 V	USB Type-C power delivery PHY
U307	PTN5110NHQZ	0x51 (0b'10100[01]x)	MX-I2C3	1 MHz Fm+	3.3 V	USB Type-C power delivery PHY
U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C13	1 MHz Fm+	3.3 V	USB Type-C power delivery PHY
U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C3	1 MHz Fm+	3.3 V	USB load switch
U305	NX20P3483UK	0x73 (0b'11100[11]x)	MX-I2C3	1 MHz Fm+	3.3 V	USB load switch
U1001	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1	I3C-12.5 Mbit/ s / I2C-400 kHz	3.3 V	IMU (I3C support)
U1201	WM8962BECSN/R	0x1A (0b'00110[10]x)	MX-I2C1	526 kHz	3.3 V	Audio codec
U1409	PCA9655EMTTXG	0x21 (0b'01000[01]x)	FTDI-I2C	1 MHz Fm+	3.3 V	Remote debug and power measurement interface I/O expander (DNP)
U204	PAC1934T	0x16 (0b'00101[10]x)	FTDI-I2C	1 MHz Fm+	3.3 V	Base board power monitor

Table 15 describes the I2C devices and their I2C addresses (7-bit) on SOM board.

Table 15. I2C devices on SOM board

Part identifier	Device	I2C address (7-bit)	Port	Speed	Voltage	Description
U701	PCA9451AHNY	0x25 (0b'0100101x)	MX-I2C2	1 MHz Fm+	3.3 V	PMIC
U902	PAC1934T	0x11 (0b'0010001x)	FTDI-I2C	1 MHz Fm+	3.3 V	Power monitor
U904	PAC1934T	0x12 (0b'0010010x)	FTDI-I2C	1 MHz Fm+	3.3 V	Power monitor
U907	PAC1934T	0x13 (0b'0010011x)	FTDI-I2C	1 MHz Fm+	3.3 V	Power monitor

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Table 15. I2C devices on SOM board...*continued*

Part identifier	Device	I2C address (7-bit)	Port	Speed	Voltage	Description
U911	PAC1934T	0x14 (0b'0010100x)	FTDI-I2C	1 MHz Fm+	3.3 V	Power monitor
U912	PAC1934T	0x15 (0b'0010101x)	FTDI-I2C	1 MHz Fm+	3.3 V	Power monitor
U909	ADP5585ACPZ-00-R7	0x34 (0b'0110100x)	FTDI-I2C	1 MHz Fm+	3.3 V	I/O expander
U913	PCT2075	0x48 (0b'1001000x)	FTDI-I2C	1 MHz Fm+	3.3 V	Temperature sensor

2.5 Boot mode and boot device configuration

The i.MX 91 processor offers multiple boot configurations that can be selected by using the SW1301 switch on the 91LP4EVK-11BB board. Alternatively, you can use the boot configuration stored in the internal eFUSE of the processor. You can also download a program image using a USB connection when the i.MX 91 processor is configured in Serial Download mode. The four dedicated BOOT MODE pins are used to select the various boot modes.

Figure 6 shows the boot mode selection switch.

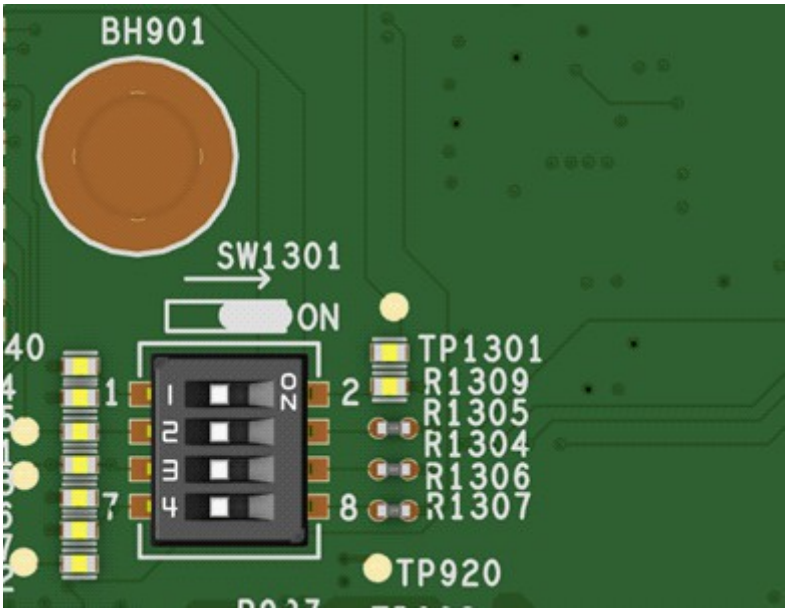


Figure 6. Boot mode selection switch

Table 16 describes the SW1301 values used in different boot modes.

Table 16. Boot mode settings

SW1301[3:0]	BOOT_MODE[3:0]	Boot core	Boot device
0001	0000	Cortex-A55 (Single boot)	From internal fuses
0011	0001		Serial downloader (USB)
0000	0010		uSDHC1 8-bit eMMC 5.1
0010	0011		uSDHC2 4-bit SD3.0

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Table 16. Boot mode settings...*continued*

SW1301[3:0]	BOOT_MODE[3:0]	Boot core	Boot device
0101	0100		FlexSPI Serial NOR
0111	0101		FlexSPI Serial NAND 2K page
0100	0110		Reserved
0110	0111		Reserved

On the IMX91LP4EVK-11 board, there are two onboard boot devices. The default one is an eMMC device. Another one is the microSD connector on the Base Board. The other two boot devices, QSPI NOR Flash and QSPI NAND Flash, are not present on the board. These devices can be supported through the M.2 card (**J901**) interface provided the related daughter cards are used.

Set SW1301[3:0] as 0000 to choose uSDHC3 (eMMC) as boot device, set 0010 to choose uSDHC2 (SD), set 0101 to choose QSPI NOR Flash, set 0111 to choose QSPI NAND Flash. Set 0011 to enter USB serial download.

Figure 7 shows the connection of SW1301 and i.MX 91 boot mode signals.

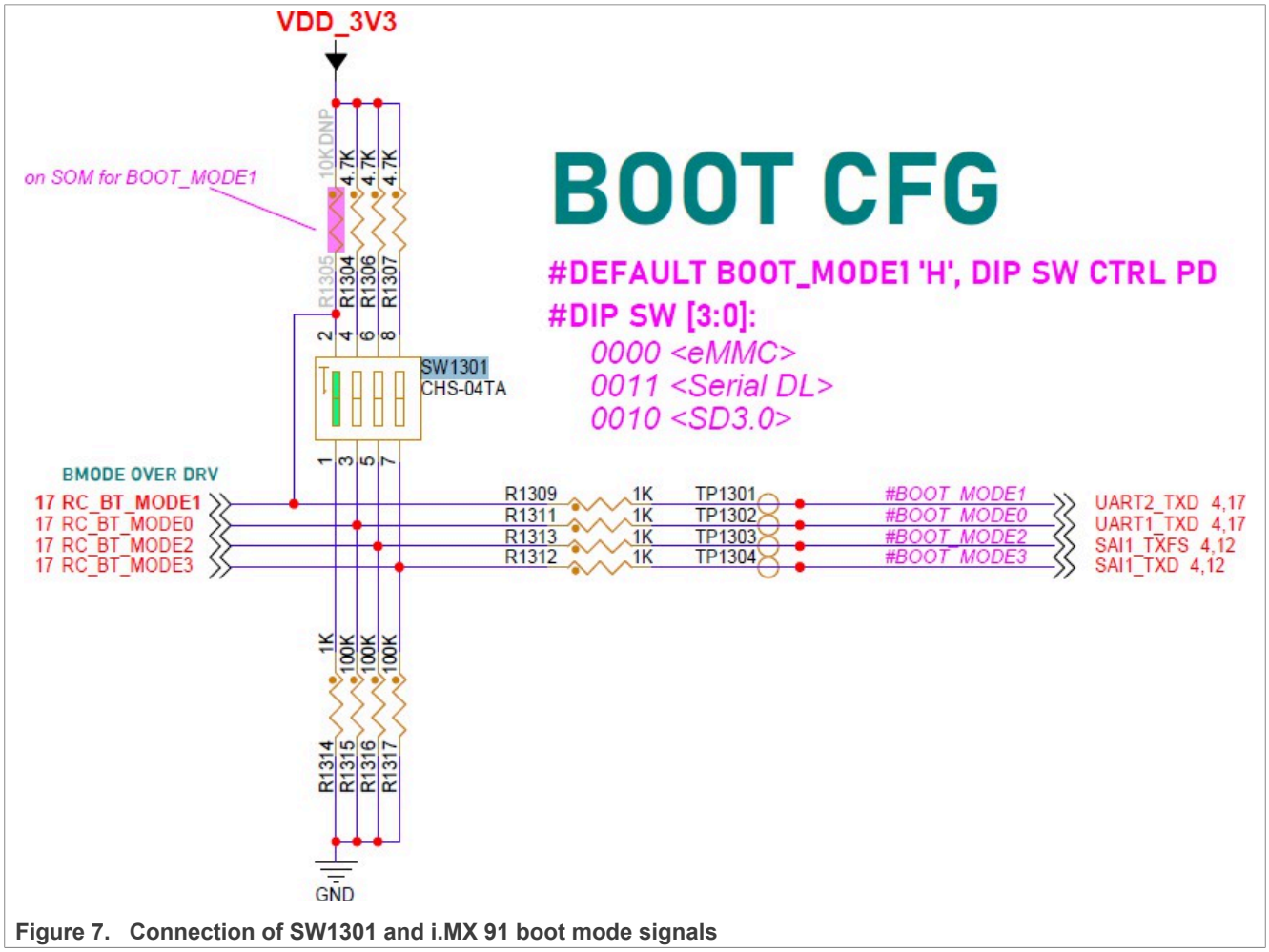


Figure 7. Connection of SW1301 and i.MX 91 boot mode signals

Note: *For more information about the boot modes and boot device configuration, see Chapter "System Boot" in the i.MX 91 Applications Processor Reference Manual.*

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2.6 Audio interface

The i.MX 91 processor's synchronous audio interface (SAI) supports an audio codec U1201 (WM8962BECSN/R) on IMX91LP4EVK-11 board. The audio codec is used for encoding/decoding audio data and supports 24-bit I2S data and 48 kHz sampling rate.

The audio codec is connected to a 3.5 mm 4-pole CTIA standard audio jack for audio input/output. The audio codec also allows connecting to a speaker via a 4-pin header (J1202) connector. The J1201 connector is

The pulse density modulated (PDM) microphone interface of the processor provides PDM Medium Quality sound (MQS) support on the IMX91LP4EVK-11 board. By using MQS, a user can connect stereo speakers or microphone without using an additional DAC. The MQS allows I2S audio data from SAI to be converted to PWM signals that can drive external speaker directly. Its audio source comes from SAI-3 and its output is connected to pads through IOMUX. The TMUX1574RSVR (U1303) four-channel switch is configured through PDM/ MQS_SEL configuration signal from I/O expander (ADP5585ACPZ-00-R7, I2C Address 0x34) to output either PDM CLK/Data or MQS data.

The J1301 audio jack is used for MQS output and two pairs of microphones (U1301/2 and U1304/5) are used for PDM interface.

Figure 8 shows the audio interface on the board. Table 17 describes the audio codec, audio jacks, and PDM microphones used on the board.

Table 17. Audio codec, audio jacks, and PDM microphones

Part identifier	Manufacturing part number	Description
J1201 and J1301	KJ366EYS	3.5 mm audio jacks for onboard audio codec and MQS analog input/output
U1201	Cirrus Logic WM8962 BECSN/R	Stereo audio codec. It receives analog audio from an input audio jack, encodes it as digital signals, decodes digital signals back to analog audio, and sends it to the output audio jack
U1301, U1302, U1304, and U1305	SPK0641HT4H-1	Digital microphones with respective single-bit PDM output
J1202	-	4-pin header for connecting speaker

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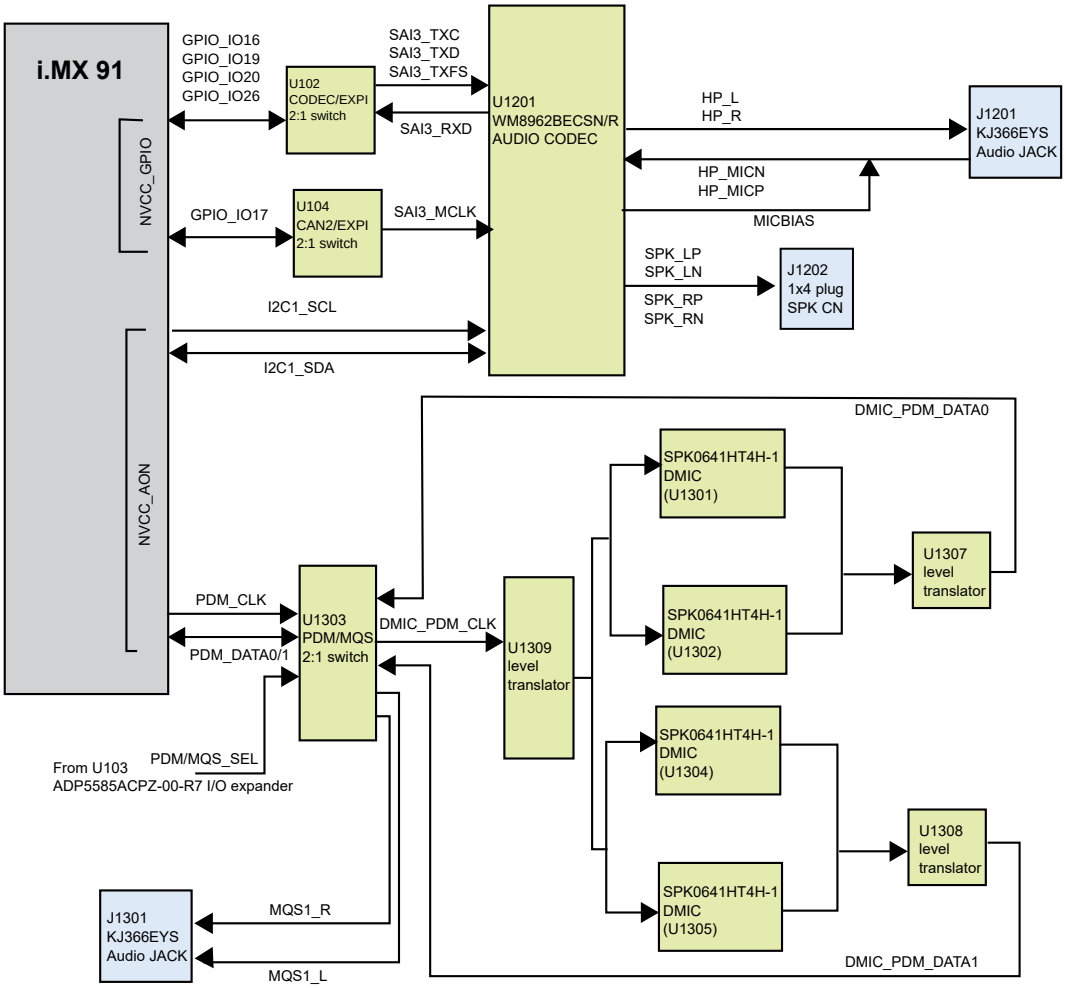


Figure 8. Audio interface connections

2.7 LPDDR44 DRAM memory

IMX91LP4EVK-11 features one 1 Gig × 16 (1 channel ×16 I/O × 1 rank) LPDDR4 DRAM chip (MT53E1G16D1ZW-046 AAT:C) for a total of 2 GB of RAM memory. The LPDDR4 DRAM memory is connected to the i.MX 91 DRAM controller.

The ZQ calibration resistor used by the LPDDR4 chip is 240 Ω 1% to LPD4/x_VDDQ and the ZQ calibration resistor DRAM_ZQ used at i.MX 91 SoC side is 120 Ω 1% to GND.

In the physical layout, the LPDDR4 chip is placed at the top side of the board. The data traces are not necessarily connected to the LPDDR4 chips in sequential order. Instead, the data traces are connected as best determined by the layout and other critical traces for the ease of routing.

2.8 SD card interface

The target processor has three ultra secured digital host controller (uSDHC) modules for SD/eMMC interface support. The uSDHC2 interface of i.MX 91 processor connects to the MicroSD card slot (J1002) on the IMX91LP4EVK-11 board. This connector supports one 4-bit SD3.0 MicroSD card. To select it as the boot device of the board, refer Section 2.5.

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2.9 eMMC memory

The eMMC memory (located at the SOM board) is connected to the uSDHC1 interface of i.MX 91, which can support eMMC 5.1 devices. It is the default boot device of the board. Table 16 shows the boot settings.

Table 18 describes the eMMC memory device that is supported by the uSDHC1 interface.

Table 18. Supported eMMC device

Part identifier	Part number	Configuration	FBGA	Manufacturer	Memory size
U501	SDINBDA6-16G-I	3D TLC	TFBGA-153	SanDisk	16 GB

2.10 M.2 connector and Wi-Fi/Bluetooth module

IMX91LP4EVK-11 supports M.2/NGFF Key E mini card 75-pin connector, J901. The M.2 mini card connector supports USB, SDIO, I2S, UART, I2C, and GPIO connections. The connector can be used for Wi-Fi/Bluetooth card, IEEE802.15.4 Radio, or 3G/4G cards.

Table 19 describes the pinout of the M.2 mini card connector (J901).

Table 19. M.2 mini card connector (J901) pinout

M.2 mini card connector pin	Connection details
3V3_1, 3V3_2, 3V3_3, 3V3_4	Connected to VPCIe_3V3 power supply
LED1	Connected to M.2 Green LED, D901
I2S_SCK	Connected to SAI1_TXC processor pin
I2S_WS	Connected to SAI1_TXFS processor pin
I2S_SD_IN	Connected to SAI1_RXD processor pin
I2S_SD_OUT	Connected to SAI1_TXD processor pin
LED2	Connected to M.2 Orange LED, D902
UART_WAKE	M2_UART_nWAKE input for I/O expander (PCAL6524HEAZ, P0_3, I2C address: 0x22)
UART_RXD	Connected to CHS-04TA switch, SW101. The signals are routed to the i.MX 91 processor pin DAP_TDI and processor interface DAP
UART_TXD	Connected to CHS-04TA switch, SW101. The signals are routed to the i.MX 91 processor pin DAP_TDO_TRACESWO and processor interface DAP
UART_CTS	Connected to CHS-04TA switch, SW101. The signals are routed to the i.MX 91 processor pin DAP_TCLK_SWCLK and processor interface DAP
UART_RTS	Connected to CHS-04TA switch, SW101. The signals are routed to the i.MX 91 processor pin DAP_TMS_SWDIO and processor interface DAP
VEN_DEF1	Connected to EN_SPI_TXD/UART_SOUT
VEN_DEF2	Connected to VEN_SPI_RXD/UART_SIN
VEN_DEF3	Connected to EN_SPI_CLK/UART_RTSO
SUSCLK	Connected to PMIC_32K_OUT, generated by PCA9451AHNY PMIC
PERST0	M2_nRST input for I/O expander (PCAL6524HEAZ, P2_2, I2C address: 0x22)
W_DISABLE2	M2_nDIS2 input for I/O expander (PCAL6524HEAZ, P2_3, I2C address: 0x22)
W_DISABLE1	M2_nDIS1 input for I/O expander (PCAL6524HEAZ, P2_4, I2C address: 0x22)

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Table 19. M.2 mini card connector (J901) pinout...*continued*

M.2 mini card connector pin	Connection details
I2C_DATA	Connected to SDAL pin of PCA9451AHNY PMIC
I2C_CLK	Connected to SCLL pin of PCA9451AHNY PMIC
ALERT	M2_nALERT input for I/O expander (PCAL6524HEAZ, P1_2, I2C address: 0x22)
USB_D+	Connected to M2_USB2_DP if R911 is populated
USB_D-	Connected to M2_USB2_DN if R912 is populated
SDIO_CLK	Connected to the SD3_CLK processor pin and processor interface SDHC3
SDIO_CMD	Connected to the SD3_CMD processor pin and processor interface SDHC3
SDIO_DATA0	Connected to the SD3_DATA0 processor pin and processor interface SDHC3
SDIO_DATA1	Connected to the SD3_DATA1 processor pin and processor interface SDHC3
SDIO_DATA2	Connected to the SD3_DATA2 processor pin and processor interface SDHC3
SDIO_DATA3	Connected to the SD3_DATA3 processor pin and processor interface SDHC3
SDIO_WAKE	Connected to the CCM_CLKO1 processor pin of NVCC_WAKEUP module
SDIO_RST	SD3_nRST output from I/O expander (PCAL6524HEAZ, P1_4, I2C address: 0x22)
PEWAKE0	PCIE_nWAKE input for I/O expander (PCAL6524HEAZ, P0_2, I2C address: 0x22)

For further details about i.MX 91 interfaces, see *i.MX 91 Reference Manual*.

2.11 QSPI NOR/NAND Flash

The QSPI memory is connected to the FlexSPI interface of i.MX 91, which is shared with SDHC3 interface, can support up to 166 MHz. The M.2 slot (J901) can also be used to insert the QSPI memory cards. These can support 166 MHz SDR and 90 MHz DDR operations. To select QSPI memory as the boot device of the IMX91LP4EVK-11 board, refer to the boot settings described in Section 2.5 "Boot mode and boot device configuration".

To support QSPI NOR Flash or NAND Flash boot, VPCIe_3V3 must be powered before POR_B, the following rework step must be taken on 91LP4EVK-11BB (Base board). See Figure 9.

1. DNP R922
2. Install R950 (1 kΩ/0402/5%)

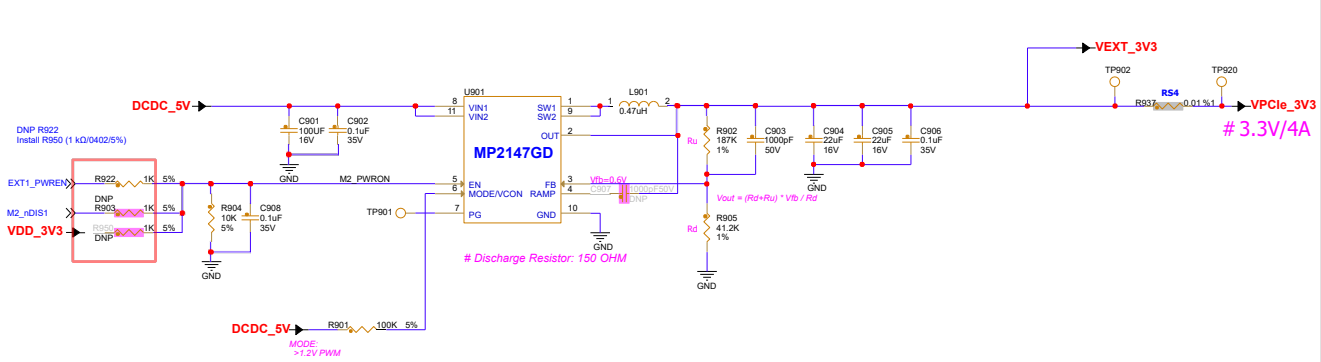


Figure 9. Rework required on 91LP4EVK-11BB for using QSPI memory as boot device

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2.12 CAN interface

The i.MX 91 processor supports a controller area network (CAN) module, which is a communication controller implementing the CAN protocol. The controller supports the CAN with flexible data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor supports two CAN FD controllers.

On the IMX91LP4EVK-11 board, one of the controllers is connected to the high-speed CAN transceiver TJA1057GT/3. The high-speed CAN transceiver drives CAN signals between the target processor and a 4-pin header connected to its physical two-wire CAN bus.

The HS-CAN transceiver and header are described in Table 20.

Table 20. High-speed CAN transceiver and header

Part identifier	Manufacturing part number	Description
U1101	TJA1057GT/3 (NXP Semiconductors)	High-speed CAN transceiver. Provides an interface between a CAN protocol controller and the physical two-wire CAN bus.
J1101	Not applicable	1x4 CAN header. It is connected to the CAN bus and allows external connection with the bus.

Note: *For details about the CAN Transceiver TJA1057, refer to the TJA1057 datasheet.*

Table 21 explains the pinout for CAN header, J1101.

Table 21. CAN header - pinout

Pin	Signal name	Description
1	VDD_5V	5 V power supply
2	CAN_H	CAN transceiver high signal
3	CAN_L	CAN transceiver low signal
4	GND	Ground

2.13 USB interface

The i.MX 91 processor features two USB 2.0 controllers, with two integrated USB PHYs. On the IMX91LP4EVK-11 board, one is used for the USB2.0 Type-C Port1 (J401) and the other is used for USB2.0 Type-C Port2 (J302).

Table 22 describes the USB ports available on the board. The USB debug connector J1401 is shown in Figure 2.

Table 22. USB ports

Part identifier	USB Port Type	Description
J401	USB2.0 Type-C	Connects to full-speed USB host and device controller (USB 1) of target processor. It can operate as a device or host. The USBC_VBUS signal controls the VBUS drive for the USB port.
J302	USB2.0 Type-C	Connects to full-speed USB host and device controller (USB 2) of target processor. It can operate as a device or host. The USBC2_VBUS signal controls the VBUS drive for the USB port. The USB2_DP and USB2_DN signals from the USB2 controller of the target processor are connected to a 2:1 CBTL02043A multiplexer (U309). Depending upon the USB2_SEL configuration signal from PCAL6524HEAZ

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Table 22. USB ports*...continued*

Part identifier	USB Port Type	Description
		I/O expander (U101, I2C address: 0x22), the multiplexer directs USB data to either USB2 Type C port (J302) or to M.2 card connecter (J901)
J301	USB 6 Type-C Power Delivery	It is used for power only. It does not support USB data transfer. It is the only power supply port therefore it must always be supplied for system power.
J1401	USB Type-C	It is used for system debug purpose and supports the UART, remote debug, and power measurement functions. For detail, see the Section 3 "Debug support". ***Note:*** *Remote debug and power measurement connectors are not populated on the IMX91LP4EVK-11 board.*

2.14 Ethernet

The i.MX 91 processor supports two Gigabit Ethernet controllers capable of simultaneous operation. The processor supports Energy-Efficient Ethernet (EEE), Ethernet Audio Video Bridging (AVB), and IEEE 1588.

The Ethernet subsystem of the board is provided by the Realtek RTL8211FDI-VD-CG Ethernet transceivers (U501 and U601) that support RGMII (10/100/1000 Mbit/s Ethernet) and connect to RJ45 connectors (J501 and J601). The Ethernet transceivers (or PHYs) receive standard RGMII Ethernet signals from i.MX 91. The RJ45 connectors integrate Magnetic transformer inside, so they can be directly connected to Ethernet transceivers (or PHYs).

Each Ethernet port has a unique MAC address, which is fused into i.MX 91. The Ethernet connectors are labeled clearly on the board. See Table 23

Table 23. Ethernet on IMX91LP4EVK-11 board

Part identifier	Part number (Manufacturer)	Description
U501 (ENET1)	RTL8211FDI-VD-CG (Realtek Semiconductor)	Ethernet transceiver that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. • Uses RGMII for transmission/ reception • Uses 25 MHz crystal Y501 for clock source • Operating voltage: 1.8 V (default) • Uses ESD protection devices (PUSB3FR4) U502 and U503
J501	-	RJ45 Ethernet connector for ENET1
U601 (ENET2)	RTL8211FDI-VD-CG (Realtek Semiconductor)	Ethernet transceiver that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. • Uses RGMII for transmission/ reception • Uses 25 MHz crystal Y601 for clock source • Operating voltage: 1.8 V (default) • Uses ESD protection devices (PUSB3FR4) U602 and U603
J601	-	RJ45 Ethernet connector for ENET2

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2.14.1 LED and LDO configuration

In order to reduce the pin count on the RTL8211F(I)-VD/RTL8211FD(I)-VD, the LED pins are duplexed with the CFG_EXT and CFG_LDO[1:0] pins. As the Hardware Configuration shares the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding CFG_EXT/CFG_LDO[1:0] inputs upon power-on/reset.

For example, as Figure 10 (left-side) shows, if a given CFG_EXT/CFG_LDO[1:0] inputs are resistively pulled high, then the corresponding LED outputs are configured as an active low driver.

On the right side, if a given CFG_EXT/CFG_LDO[1:0] inputs are resistively pulled low, then the corresponding output is configured as an active high driver. The Hardware Configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (for example, 4.7 KΩ). If no LED indications are needed, the components of the LED path (LED + 510 Ω) can be removed.

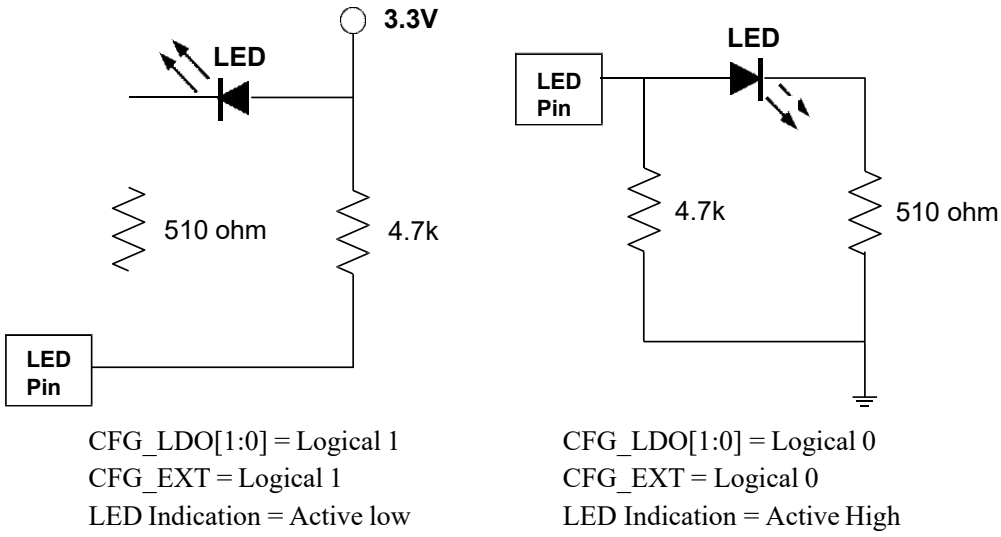


Figure 10. LDO configuration

2.15 EXPI

The IMX91LP4EVK-11 board has a 2x20 pin expansion interface (EXPI) (J1001) that supports I2S, UART, I2C, and GPIO connections. This interface can be used to access various pins or to plug in accessory cards, such as the 8MIC-RPI-MX8, MX93AUD-HAT, and TM050RDH03-41.

Table 24 lists the J1001 pin definitions.

Table 24. J1001 pin definitions

Pin number	Net name	Pin number	Net name
1	VEXPI_3V3	2	VEXPI_5V
3	GPIO_IO02	4	VEXPI_5V
5	GPIO_IO03	6	GND
7	GPIO_IO04	8	GPIO_IO14

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Table 24. J1001 pin definitions...*continued*

Pin number	Net name	Pin number	Net name
9	GND	10	GPIO_IO15
11	GPIO_IO17	12	GPIO_IO18
13	GPIO_IO27	14	GND
15	GPIO_IO22	16	GPIO_IO23
17	VEXPI_3V3	18	GPIO_IO24
19	GPIO_IO10	20	GND
21	GPIO_IO09	22	GPIO_IO25
23	GPIO_IO11	24	GPIO_IO08
25	GND	26	GPIO_IO07
27	GPIO_IO00	28	GPIO_IO01
29	GPIO_IO05	30	GND
31	GPIO_IO06	32	GPIO_IO12
33	GPIO_IO13	34	GND
35	GPIO_IO19	36	GPIO_IO16
37	GPIO_IO26	38	GPIO_IO20
39	GND	40	GPIO_IO21

The GPIO pads have very flexible IOMUX options, can be used as many interfaces, see Table 25.

Table 25. GPIO pad IOMUX options

IO PAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6
GPIO_IO00	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA
GPIO_IO01	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL
GPIO_IO02	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA
GPIO_IO03	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL
GPIO_IO04	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA
GPIO_IO05	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL
GPIO_IO06	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA
GPIO_IO07	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL
GPIO_IO08	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA
GPIO_IO09	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL

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Table 25. GPIO pad IOMUX options*...continued*

IO PAD	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6
GPIO_IO10	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA
GPIO_IO11	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL
GPIO_IO12	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA
GPIO_IO13	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL
GPIO_IO14	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX
GPIO_IO15	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX
GPIO_IO16	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B
GPIO_IO17	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B
GPIO_IO18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0	tpm5.CH2
GPIO_IO19	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm6.CH2
GPIO_IO20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm3.CH1
GPIO_IO21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm4.CH1
GPIO_IO22	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA
GPIO_IO23	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL
GPIO_IO24	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	TDO_SWO	spi6.PCS1
GPIO_IO25	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	TCLK_SWCLK	spi7.PCS1
GPIO_IO26	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	TDI	spi8.PCS1
GPIO_IO27	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	TMS_SWDIO	spi5.PCS1

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3 Debug support

The IMX91LP4EVK-11 board supports both USB and JTAG interfaces for debugging. These are described in the following sections.

3.1 USB debug interface

The i.MX 91 applications processor has eight independent UART ports (UART1 – UART8). On the IMX91LP4EVK-11 board, UART1 is used for Cortex-A55 core. A single chip USB to dual UART, JTAG, and I2C is used for UART debug and remote debug. The part number is FT4232H. The developers can download the driver from FTDI website.

After the driver for FT4232H is installed, the PC enumerates four COM ports when the USB cable is plugged into the J1401 connector. The first and second ports are reserved. The third port is connected to UART1 for A55 system debugging and the fourth port is connected to UART2 for general communication. Developers can use Putty, Tera Term, Xshell, or other terminal tools. Table 26 describes the required settings.

Table 26. Terminal setting parameters

Parameter	Value
Data rate	115,200 baud
Data bits	8
Parity	None
Stop bits	1

FT4232H is used for remote debug of JTAG, Bootmode, ONOFF, SYS_nRST, and power measurement board communication. Developers can load different images on the PC for associated applications. For example, the power measurement tool BCU from github project: nxp-imx/bcu.can be downloaded from the link below:

https://github.com/nxp-imx/bcu/releases

The USB debug connector J1401 is shown in Figure 2.

3.2 JTAG interface

The i.MX 91 Applications Processor has four JTAG signals on dedicated pins, and one HW reset input signal POR_B. Those signals are directly connected to the standard 10-pin 1.27 mm JTAG connector (J1405). The four JTAG signals used by the processor are:

- JTAG_TCK (TAP Clock)
- JTAG_TMS (TAP Machine State)
- JTAG_TDI (TAP Data In)
- JTAG_TDO (TAP Data Out)

The JTAG connector (J1405) is shown in Figure 2.

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4 PCB information

The IMX91LP4EVK-11 board comprises the 91LP4EVK-11SOM and 91LP4EVK-11BB boards. The material used is FR-4, and the PCB stack-up information is shown in Table 27 and Table 28. The CPU board uses 6-layer stack-up and the BB board uses 8-layer stack-up.

Table 27. 91LP4EVK-11SOM Board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	**Signal**	0.5+Plating			
	Dielectric		PP1080	3.49	2.8 mil
2	**GND**	1			
	Dielectric		Core 0.076 mm	3.97	3 mil
3	**Signal**	1			
	Dielectric		PP 1080*2 Core 0.8 mm PP 1080*2	4.15	42.88 mil
4	**Power**	1			
	Dielectric		Core 0.076 mm	3.97	3 mil
5	**GND**	1			
	Dielectric		PP 1080	3.49	2.8 mil
6	**Signal**	0.5+Plating			
Finished:	62.992(6.299/-6.299) mil			1.6(+0.16/-0.16) mm	
Designed:	58.268 mil			1.48 mm	
Material:	185HR				

Table 28. 91LP4EVK-11BB board stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	**Signal**	0.5+Plating			
	Dielectric		1080	3.75	2.646 mil
2	**GND**	1			
	Dielectric		Core 0.13 mm	4.13	5.12 mil
3	**Signal**	1			
	Dielectric		1080*2 2116	3.95	9.674 mil
4	**Power**	1			
	Dielectric		Core 0.8 mm	4.47	31.5 mil
5	**Power**	1			
	Dielectric		1080*2 2116	3.95	9.638 mil

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Table 28. 91LP4EVK-11BB board stack up information*...continued*

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
6	**Signal**	1			
	Dielectric		Core 0.13 mm	4.13	5.12 mil
7	**GND**	1			
	Dielectric		1080	3.75	2.646 mil
8	**Signal**	0.5+Plating			
Finished:	78.74(7.874/-7.874) mil			2(+0.2/-0.2) mm	
Designed:	75.236 mil			1.911 mm	
Material:	TU768				

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5 Acronyms and abbreviations

Table 29 lists and explains the acronyms and abbreviations used in this document.

Table 29. Acronyms

Term	Description
AVB	Audio video bridging
BGA	Ball grid array
BBNSM	Battery backed non-secure module
CAN	Controller area network
Codec	Coder/decoder
DRP	Dual Role Port
DNP	Do not populate
EEE	Energy efficient Ethernet
EXPI	2x20 pin expansion interface
FD	Flexible data-rate
GPIO	General-purpose input/output
HS	High-speed
I2C	Inter-integrated circuit
I2S	Inter-IC sound
I3C	Improved inter-integrated circuit
LDO	Low dropout regulator
LED	Light-emitting diode
MPSSE	Multi-protocol synchronous serial engine
MQS	Medium quality sound
NGFF	Next generation form factor
PDM	Pulse-density modulation
PMIC	Power management integrated circuit
POR	Power-on reset
QSPI	Quad serial peripheral interface
RDPM	Remote debug and power measurement
SDK	Software development kit
TSN	Time-sensitive networking
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
uSDHC	Ultra secured digital host controller

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6 Related documentation

Table 30 lists and explains the additional documents and resources that you can refer to for more information on the IMX91LP4EVK-11 board.

Table 30. Related documentation

Document	Description	Link / how to access
i.MX 91 Applications Processor Reference Manual (IMX91RM	Intended for system software and hardware developers and application programmers who want to develop products based on the i.MX 91 MPU	i.MX 91 Documentation
i.MX 91 Industrial Application Processors Data Sheet (IMX91 IEC)	Provides information about electrical characteristics, hardware design considerations, and ordering information	• IMX91IEC (Industrial datasheet) • IMX91CEC (Commercial datasheet)
i.MX 91 Hardware Developer's Guide	This document aims to help hardware engineers design and to test their i.MX 91 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoidance of board bring-up problems.	UG10147

Additional documents are available on the below URL: i.MX 91 Documentation

Note:

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

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7 Revision history

Table 31 summarizes the revisions to this document.

Table 31. Document revision history

Document ID	Release date	Description
UM12043 v.1.0	15 November 2024	Initial public release

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