MP6632A

50V, 3-Phase Brushless DC Motor Driver with 1A Gate Driver

DESCRIPTION

The MP6632A is a 3-phase brushless DC (BLDC) motor driver with up to 1A of driving current and a 6V to 50V input voltage (V_{IN}) range.

The MP6632A controls the motor speed through the pulse-width modulation (PWM) signal or the DC signal on the PWM/DC pin with closed-/open-loop speed control and a built-in, configurable speed curve function. The device features 120° modulation for good dynamic response and high-speed operation.

The motor driver also features a rotational speed detector. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the Hall output. Direction control is also achieved through the DIR pin.

Rich protections include under-voltage lockout (UVLO), locked-rotor detection, over-current protection (OCP), and thermal shutdown.

The MP6632A is available in a QFN-32 (4mmx4mm) package.

FEATURES

- 6V to 50V Input Voltage (V_{IN}) Range
- Up to 1A Driving Current Capacity
- 120° Modulation
- Supports 0V to 3.3V DC Input or 50Hz to 100kHz Pulse-Width Modulation (PWM) Input
- Supports External Triple-Hall Input
- Closed-/Open-Loop Speed Control
- Direction/Brake input
- Power-Save Mode (PSM)
- Locked-Rotor Detection
- Over-Current Protection (OCP)
- Rotational Speed Indicator
- 25kHz/50kHz Switching Frequency (f_{SW})
- Soft Start (SS) to Reduce Noise
- Available in a QFN-32 (4mmx4mm) Package

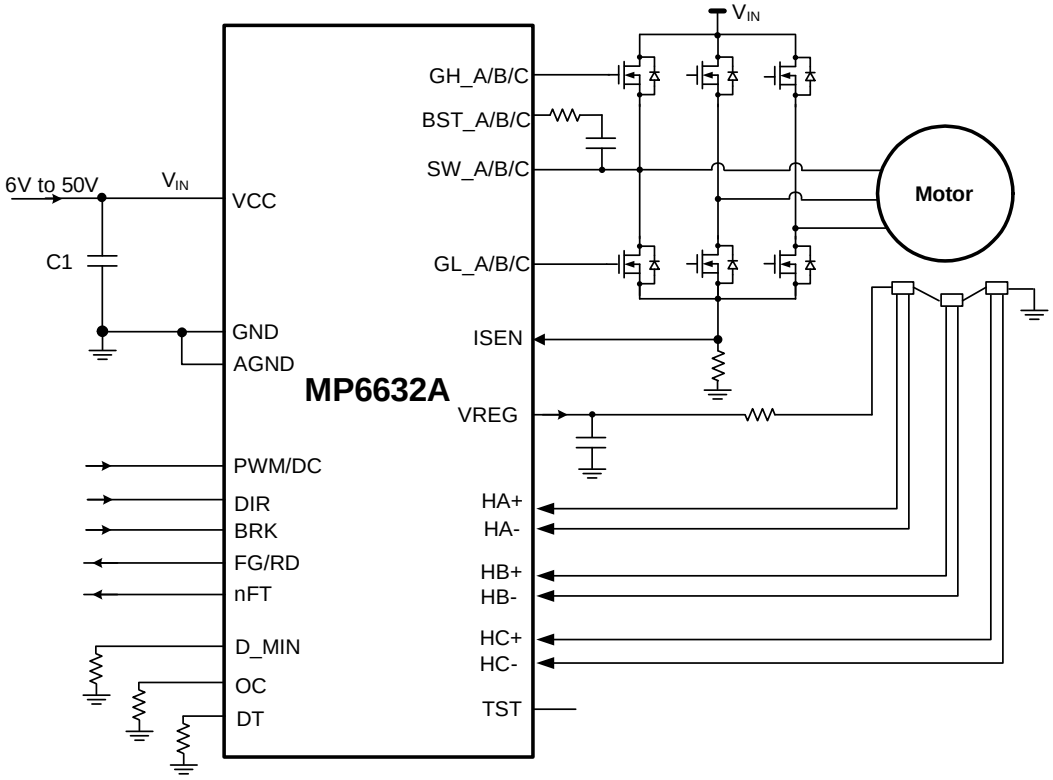
APPLICATIONS

- General 3-Phase Brushless DC (BLDC) Motors
- Fans
- Pumps

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6632AGR-xxxx**	QFN-32 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6632AGR-xxxx-Z).

** "-xxxx" is the configuration code identifier. The first four digits of the suffix (-xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for the non-default function option. -0001 is the default configuration.

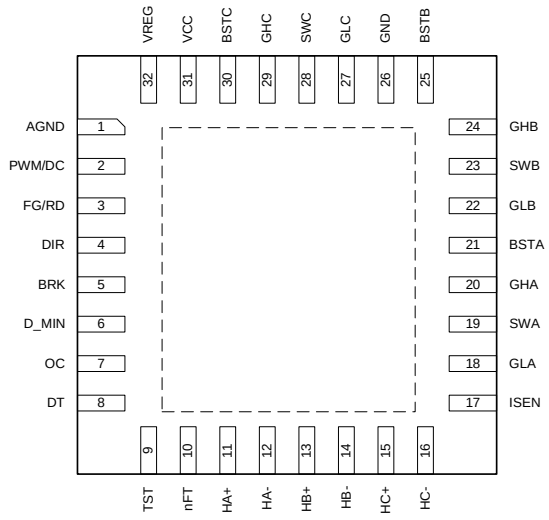
TOP MARKING

MPSYWW
M6632A
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M6632A: First four digits of the part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-32 (4mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog ground.**
2	PWM/ DC	**Rotational speed control input pin.** Pull the PWM/DC pin up internal using an 85kΩ resistor connected to the internal low-dropout (LDO) regulator. Apply a 50Hz to 100kHz pulse-width modulation (PWM) frequency (f_{PWM}) to this pin for speed control when PWM_DC = 0. Apply a DC voltage between 0V and 3.3V to this pin for speed control when PWM_DC = 1.
3	FG/RD	**Speed indication and locked-rotor detection.** The FG/RD pin is an open-drain output that should be pulled up externally.
4	DIR	**Direction control pin.** The DIR pin should be pulled down internally. If DIR is low, then the MP6632A operates in forward rotation, and the output is A → B → C. If DIR is high, then the MP6632A operates in reverse rotation, and the output is A → C → B.
5	BRK	**Brake.** Pull the BRK pin high to brake the motor. BRK should be pulled down internally.
6	D_MIN	**Input starting duty setting.** A resistor connected between the D_MIN and GND pins sets the starting duty. If D_MIN is floating, the starting duty is set by the internal register bits.
7	OC	**Over-current protection (OCP) setting.** A resistor connected between the OC and GND pins sets the OCP threshold. If the OC pin is floating, the OCP threshold is set by the internal register bits.
8	DT	**Dead time setting.** A resistor connected between the DT and GND pins sets the dead time (DT) of high-side (HS) gate driver and the low-side (LS) gate driver. If the DT pin is floating, the DT is set by the internal register bits.
9	TST	**Test pin.** The TST pin is floating by default.
10	nFT	**Fault indicator output.** The nFT pin is pulled active low when a fault is occurs. nFT is an open-drain output that should be pulled up externally.
11	HA+	**Phase A Hall positive input terminal.**
12	HA-	**Phase A Hall negative input terminal.** HA- is only active in differential mode.
13	HB+	**Phase B Hall positive input terminal.**
14	HB-	**Phase B Hall negative input terminal.** HB- is only active in differential mode.
15	HC+	**Phase C Hall positive input terminal.**
16	HC-	**Phase C Hall negative input terminal.** HC- is only active in differential mode.
17	ISEN	**Current-sense.** The ISEN pin senses the bus current using a current-sense resistor.
18	GLA	**Phase A LS gate driver pin.**
19	SWA	**Phase A switching node.**
20	GHA	**Phase A HS gate driver pin.**
21	BSTA	**Phase A HS gate driver bootstrap pin.**
22	GLB	**Phase B LS gate driver pin.**
23	SWB	**Phase B switching node.**
24	GHB	**Phase B HS gate driver pin.**
25	BSTB	**Phase B HS gate driver bootstrap pin.**
26	GND	**Ground.**
27	GLC	**Phase C LS gate driver pin.**
28	SWC	**Phase C switching node.**
29	GHC	**Phase C HS gate driver pin.**
30	BSTC	**Phase C HS gate driver bootstrap pin.**
31	VCC	**Input supply voltage.**
32	VREG	**10V reference output pin.**

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VCC .....-0.3V to +55V
SWA, SWB, SWC .....-0.3V to V_{CC} + 0.3V
GHx, BSTx..... -0.3V to V_{SWx} + 13V
PWM/DC, VREG, GLx .....-0.3V to +13V
All other pins .....-0.3V to +6.5V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
QFN-32 (4mmx4mm)..... 2.97W
T_J..... 150°C
Supply voltage (V_{CC}) .....6V to 55V
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....2000V

Recommended Operating Conditions (3)

Supply voltage (V_{CC}) .....6V to 50V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-32 (4mmx4mm)…...…....42…..9.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40 to 125°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
V_{CC} under-voltage lockout (UVLO) rising threshold	V_{UVLO}			5	5.2	V
Input UVLO Hysteresis				0.5		V
Operating supply current	I_{CC}			5		mA
Standby Current	$I_{STANDBY}$	PWM/DC pin pulls low for 100ms			200	µA
Logic Input Thresholds						
DIR input high voltage	V_{DIR_HIGH}		2			V
DIR input low voltage	V_{DIR_LOW}				0.8	V
DIR pull-down resistance	R_{DIR}			100		kΩ
BRK input high voltage	V_{BRK_HIGH}		2			V
BRK input low voltage	V_{BRK_LOW}				0.8	V
BRK pull-down resistance	R_{BRK}			100		kΩ
PWM input high voltage	V_{PWM_HIGH}	PWM_DC = 0	2			V
PWM input low voltage	V_{PWM_LOW}	PWM_DC = 0			0.8	V
PWM pull-up resistance	R_{PWM}	PWM_DC = 0		85		kΩ
DC input high voltage	V_{DC_HIGH}	PWM_DC = 1, T_J = 25°C	3.2	3.3	3.4	V
DC input low voltage	V_{DC_LOW}	PWM_DC = 1		6		mV
Logic Output Voltage						
FG/RD low-level output voltage	V_{FG_LOW}	I_{FG} = 3mA			0.3	V
nFT low-level output voltage	V_{nFT_LOW}	I_{nFT} = 3mA			0.3	V
Reference						
VREG output voltage			9.5	10	10.5	V
VREG maximum load		I_{VREG} = 30mA		9.95		V
Bias current; D_MIN, OC, and DT pins' output current	I_{BIAS}		47.5	50	52.5	µA
D_MIN duty threshold	D_{MIN}	R_{D_MIN} = 10kΩ		15.6		%
Gate Driver						
High-side (HS) gate driver output high voltage	V_{GATE_HS}			9.4		V
Low-side (LS) gate driver output high voltage	V_{GATE_LS}			10		V
Switching frequency	f_{SW}	T_J = 25°C	24.4	25	25.8	kHz
Gate source current (5)	I_{SOURCE}			1		A
Gate sink current (5)	I_{SINK}			1		A
Gate pull-up resistance	R_{UP}	T_J = 25°C			7	Ω
Gate pull-down resistance	R_{DOWN}	T_J = 25°C			5	Ω
Dead time (DT)	t_{DT}	R_{DT} = 28kΩ		300		ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40 to 125°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Hall Signal						
Hall differential input drive voltage	V_{HALL_DIFF}	HLOGIC=0, differential mode	±30			mV
Hall input common-mode voltage	V_{HALL_CM}	HLOGIC = 0, differential mode	0		4	V
Hall input offset voltage	V_{HALL_OFFSET}	HLOGIC = 0, V_{HCM} = 1V, differential mode		±1		mV
Hall input hysteresis voltage	V_{HALL_HYS}	HLOGIC = 0, V_{HCM} = 1V, differential mode		±13		mV
Hall input logic high threshold	V_{HALL_HIGH}	HLOGIC = 1, logic input mode	2			V
Hall input logic low threshold	V_{HALL_LOW}	HLOGIC = 1, logic input mode			0.8	V
Protections						
Over-current protection (OCP) threshold	I_{OCP}	R_{OC} = 28kΩ	90	100	110	mV
Locked-rotor detection time	t_{RD}			0.5		sec
Locked-rotor detection retry time	t_{RD_RETRY}			4.5		sec
Thermal shutdown threshold				170		°C
Thermal shutdown hysteresis				30		°C

Note:

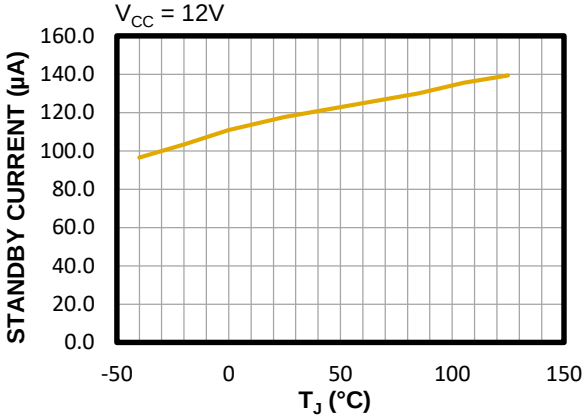
5) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

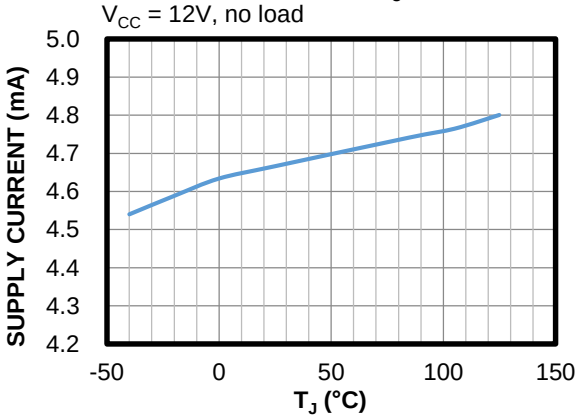
Standby Current vs. T_J

V_{CC} = 12V

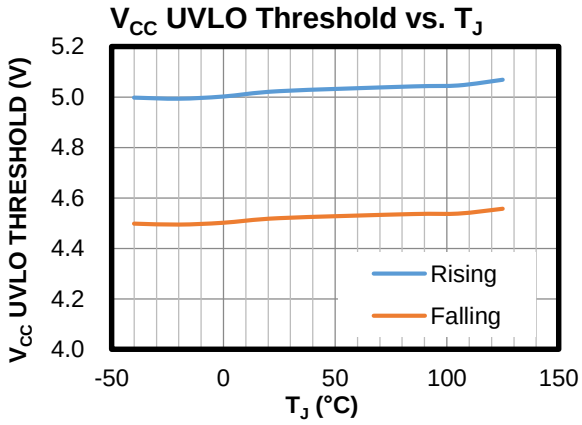


Supply Current Vs. T_J

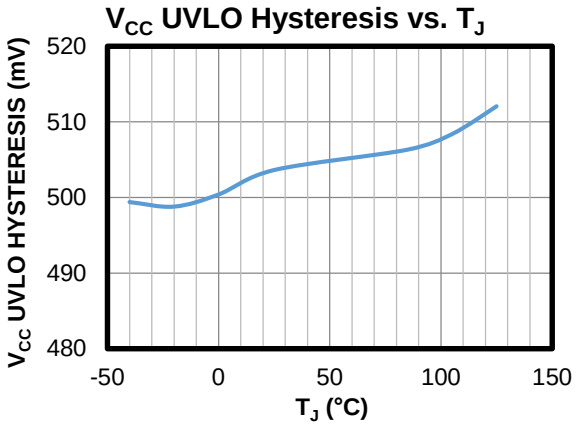
V_{CC} = 12V, no load



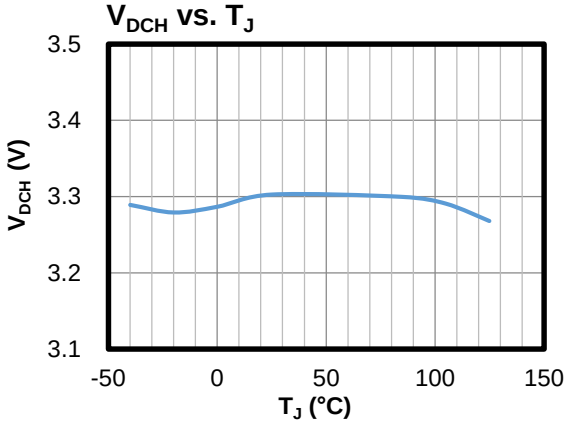
V_{CC} UVLO Threshold vs. T_J



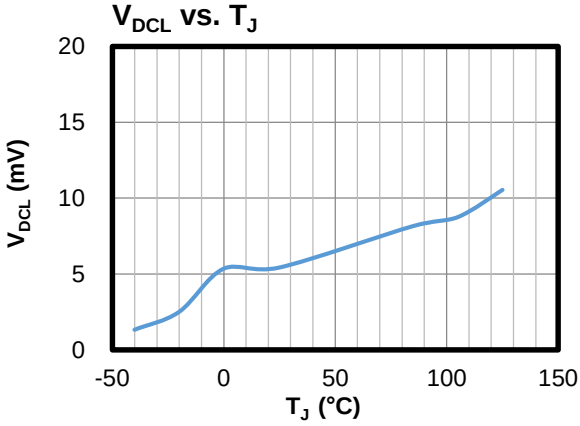
V_{CC} UVLO Hysteresis vs. T_J



V_{DCH} vs. T_J



V_{DCL} vs. T_J

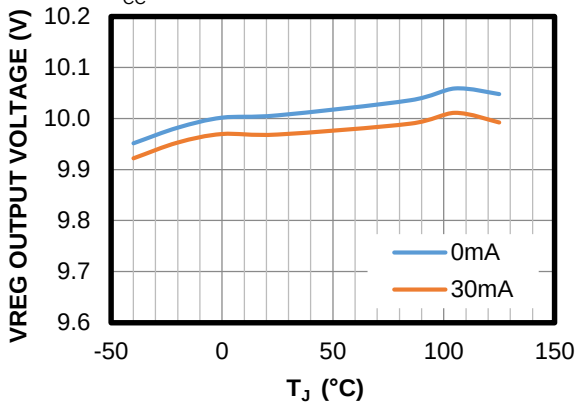


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

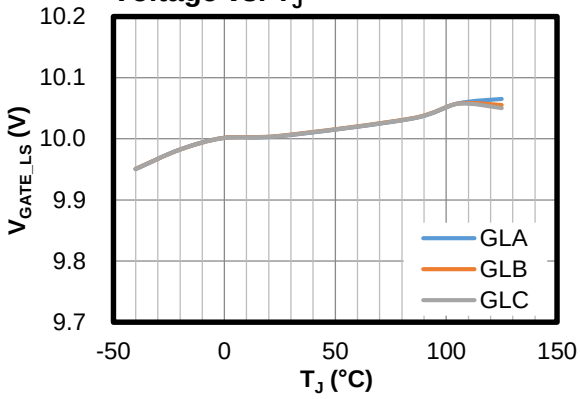
TYPICAL CHARACTERISTICS *(continued)*

VREG Output Voltage vs. T_J

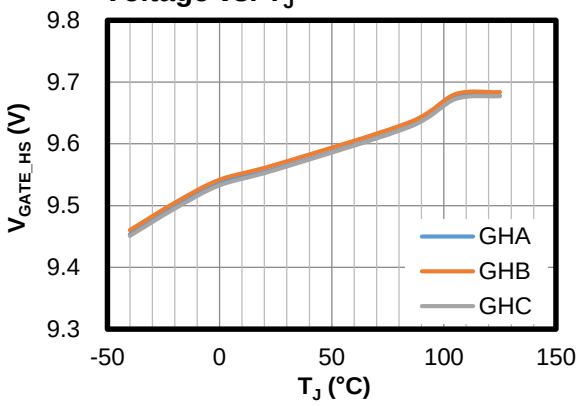
V_{CC} = 12V



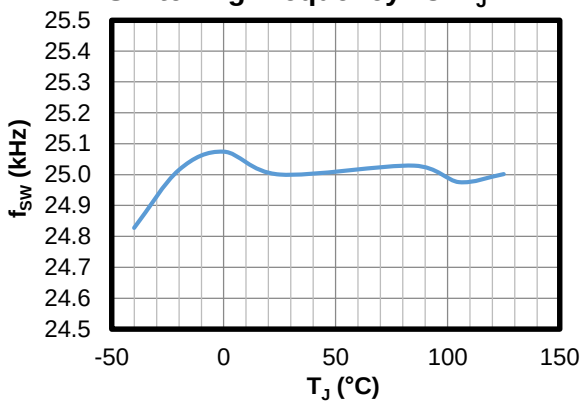
Low-Side Gate Driver High Voltage vs. T_J



High-Side Gate Driver High Voltage vs. T_J

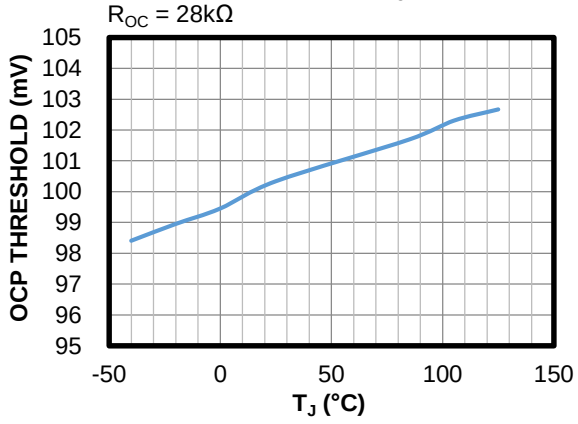


Switching Frequency vs. T_J



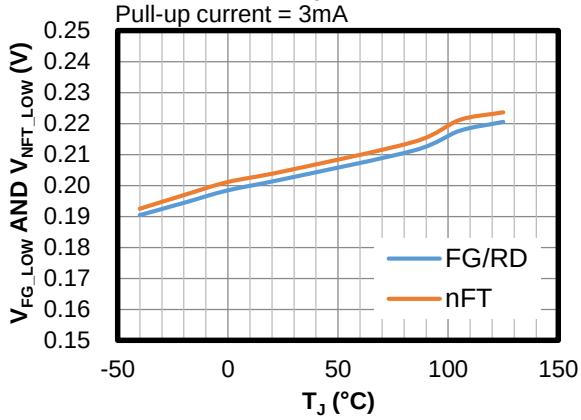
OCP Threshold vs. T_J

R_{OC} = 28kΩ



Logic Low-Level Output Voltages vs. T_J

Pull-up current = 3mA



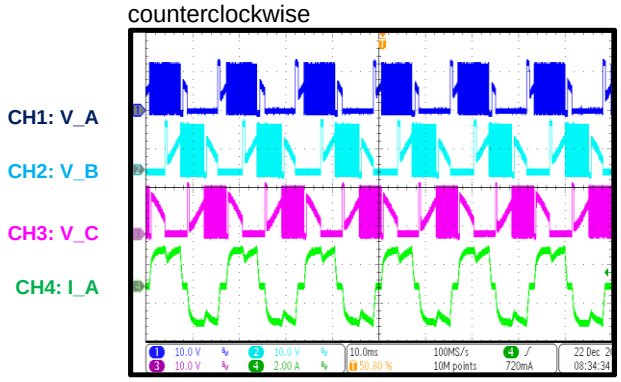
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, f_{PWM} = 20kHz, with three external Hall-effect sensors.

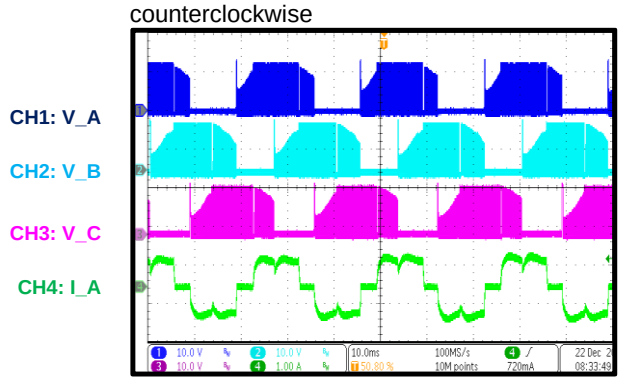
Steady State

PWM duty = 100%, DIR is low, counterclockwise



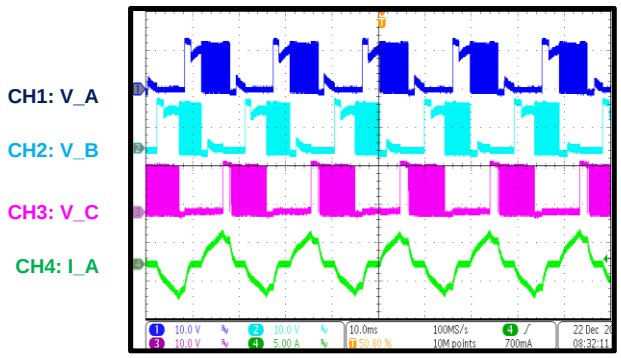
Steady State

PWM duty = 50%, DIR is low, counterclockwise



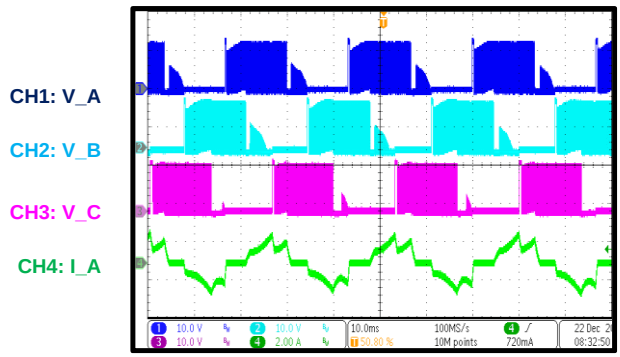
Steady State

PWM duty = 100%, DIR is high, clockwise



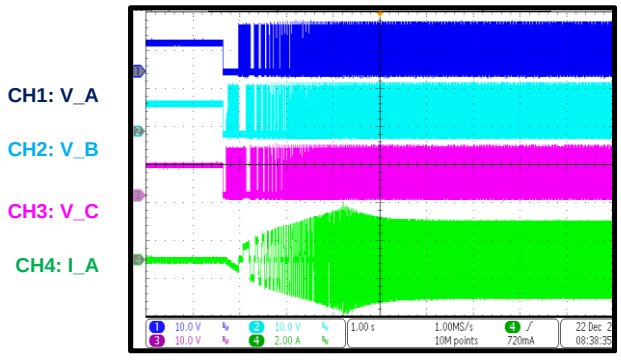
Steady State

PWM Duty = 50%, DIR is high, clockwise



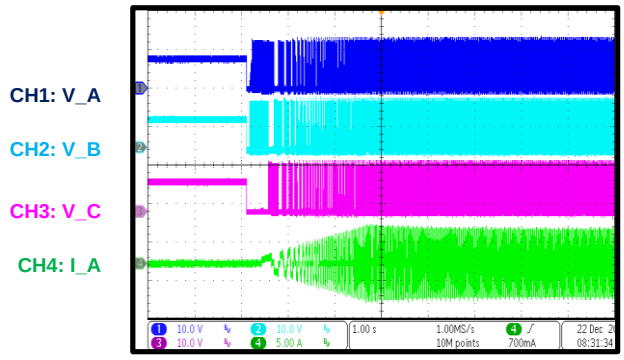
Start-Up through PWM

PWM duty = 0% to 100%, DIR is low, counterclockwise



Start-Up through PWM

PWM duty = 0% to 100%, DIR is high, counterclockwise



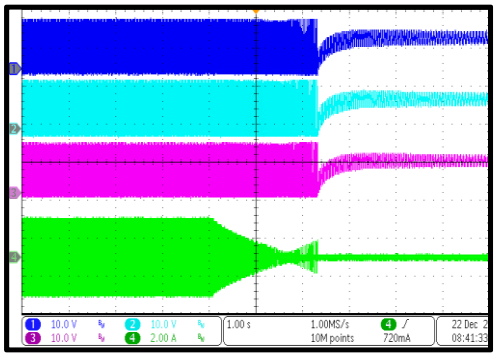
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. V_{IN} = 12V, f_{PWM} = 20kHz, with three external Hall-effect sensors.

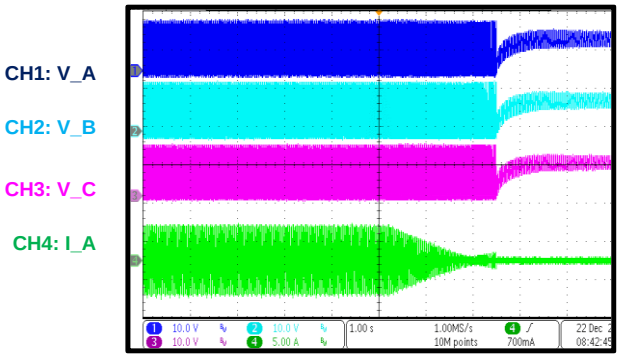
Shutdown through PWM

PWM duty = 100% to 0%, DIR is low, counterclockwise



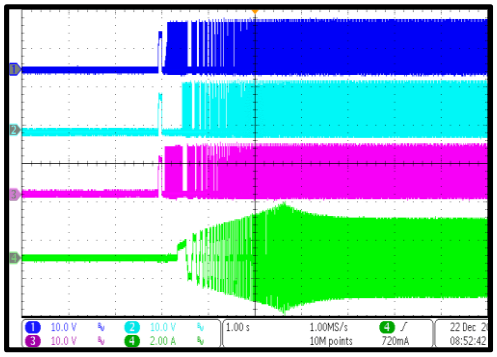
Shutdown through PWM

PWM duty 100% to 0%, DIR is high, counterclockwise



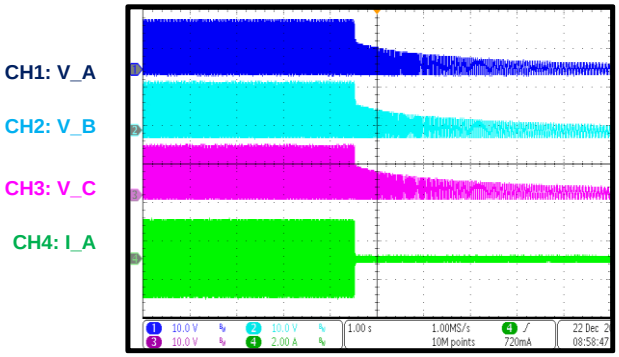
Start-Up

V_{CC} = 0V to 12V, PWM duty = 100%, DIR is low, counterclockwise



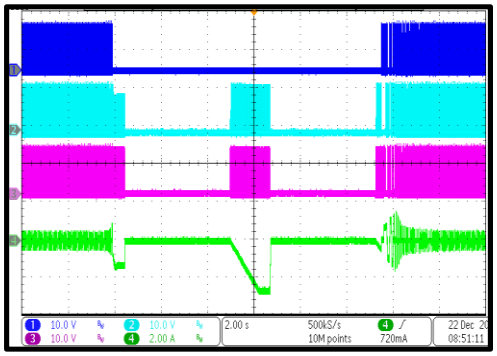
Shutdown

V_{CC} = 12V to 0V, PWM duty = 100%, DIR is low, counterclockwise



Lock and Retry

PWM duty = 25%, rotor is locked, and then released



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

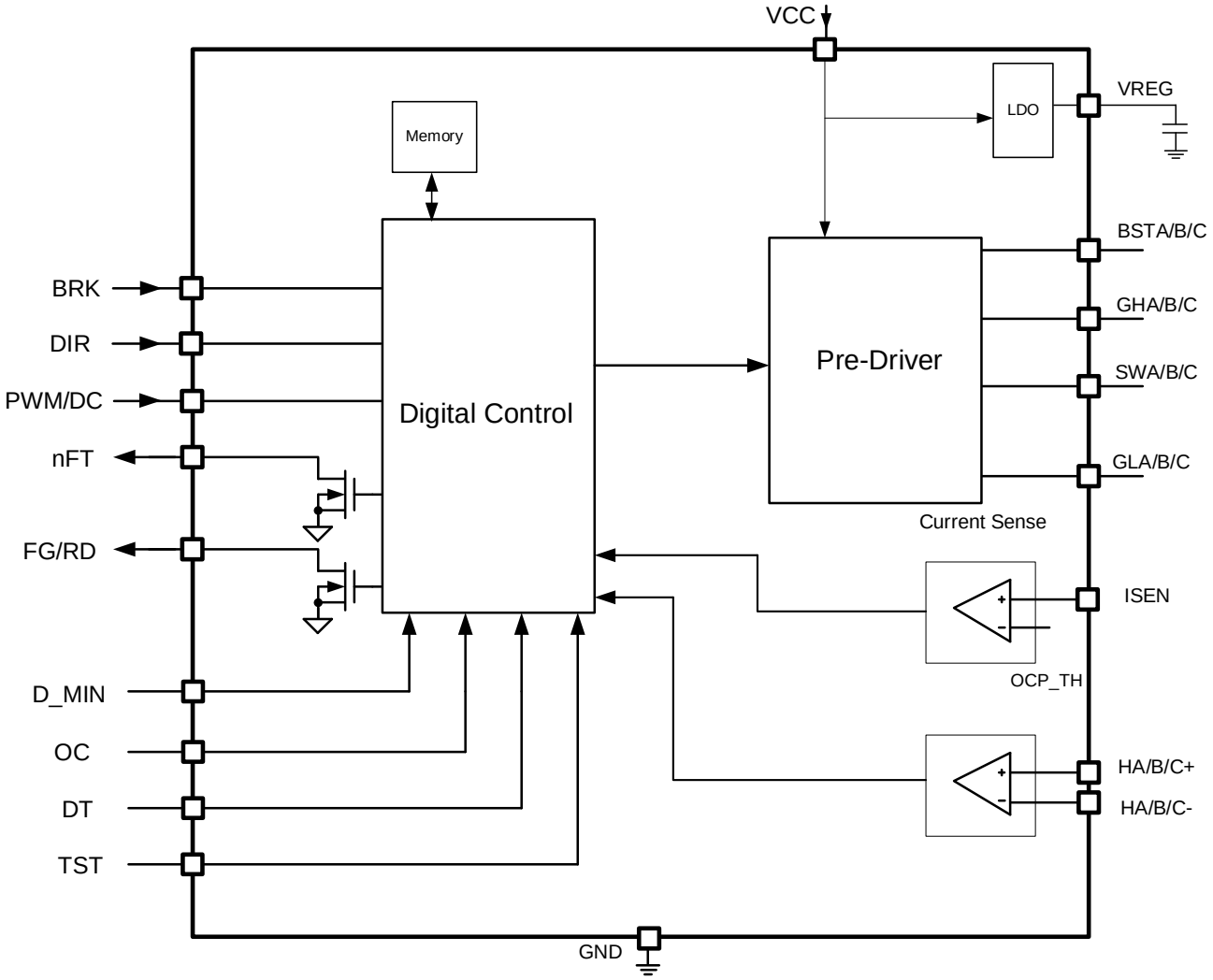


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

The MP6632A is a 3-phase, brushless DC (BLDC) motor driver that controls the motor speed through a pulse-width modulation (PWM) signal or the DC voltage on the PWM/DC pin with closed-/open-loop speed control, with a built-in, configurable speed curve function. It features 120° modulation for good dynamic response and high speed operation.

The MP6632A supports 120° modulation based on the external Hall sensor's signal (see Figure 2).

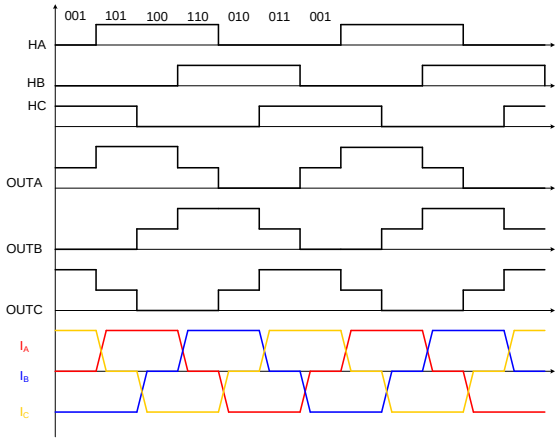


Figure 2: 120° Modulation

The MP6632A also features rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the external Hall signal. The direction control is also achieved through the DIR pin input and the BRK pin to brake the motor.

Rich protections include under-voltage lockout (UVLO), locked-rotor detection, over-current protection (OCP), and thermal shutdown.

Speed Control

The PWM/DC pin controls the motor speed by applying a PWM signal or a DC voltage.

If PWM_DC = 1, the motor speed is controlled by the DC voltage on the PWM/DC pin. The external DC voltage is linearly converted to a PWM input duty cycle internally. The DC voltage ranges between 0V and 3.3V.

If PWM_DC = 0, the motor speed is controlled by the PWM input signal duty cycle. The input PWM frequency is from 50Hz to 100kHz. The supported input PWM frequency range can be selected by register bit PWM_L.

Open-Loop and Closed-Loop Speed Control

The MP6632A supports either speed open-loop or closed-loop speed control (configured by register bits OPEN_L and CLOSE_H).

In closed-loop mode (OPEN_L = 0 and CLOSE_H = 1), the MP6632A internally detects the Hall signal speed and feedback in the control loop, then adjusts the PWM output duty to a closed loop. By doing this, the motor speed follows the reference exactly.

In open-loop mode (OPEN_L = 1), the OUTA, OUTB, and OUTC output duty cycles directly depend on the PWM input duty.

In mixed mode (OPEN_L = 0 and CLOSE_H = 0), the MP6632A operates in closed-loop mode when the PWM input duty is below 87.5% and open-loop mode when the input duty exceeds 87.5%.

Starting Duty and Minimum Speed

The starting input duty can be configured by the internal register (DIN_MIN) or the resistance on the external D_MIN pin. If the D_MIN pin is floating, the starting duty is set by the internal register; otherwise, the starting duty is set by the resistance on the D_MIN pin.

When the IC is enabled, it detects the D_MIN pin voltage (V_{D_MIN}), and then V_{D_MIN} is converted to the starting duty cycle. The value remains the same until the power is reset.

Table 1: Starting Duty Set by the Resistor

R (kΩ)	DIN_MIN (%)
2	3.125
4	6.25
6	9.375
8	12.5
10	15.625
12	18.75
14	21.875
16	25
20	28.125
24	31.25
28	34.375
32	37.5
38	40.625
44	43.75
50	46.875

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

The operation when the input duty is below the starting duty is configured by register bits SPD_ZERO and MAX_EN. The SPD_ZERO and MAX_EN can be set to the following configurations:

- If SPD_ZERO = 0 and MAX_EN = 0, then the speed maintains the minimum speed when the PWM input duty cycle is below the starting duty.
- If SPD_ZERO = 0 and MAX_EN = 1, then the speed rises to the maximum speed when the PWM input duty cycle is below the starting duty.
- If SPD_ZERO = 1 and MAX_EN = x, then the speed is 0rpm when the PWM input duty cycle is below the starting duty.

Speed Curve Configuration

The SPD_MAX registers configure the speed when the PWM input duty is at 100%. Otherwise, the MP6632A provides a five-point curve configuration function where the output speed can be configured when the input duty is 37.5%, 50%, 62.5%, 75%, or 87.5%. Linear interpolation occurs between the adjacent duty cycles.

Figure 3 shows the curve configuration when SPD_ZERO = 1.

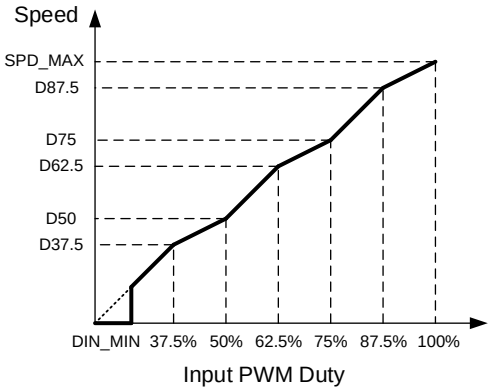


Figure 3: Curve Configuration when SPD_ZERO = 1

Figure 4 shows the curve configuration when SPD_ZERO = 0.

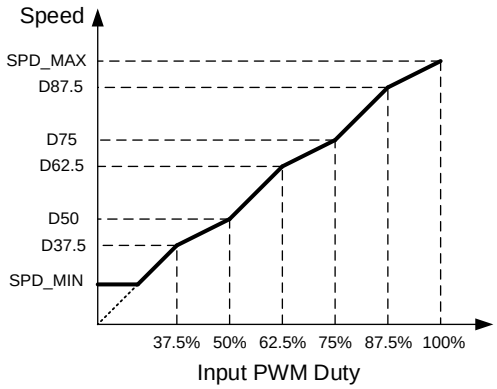


Figure 4: Curve Configuration when SPD_ZERO = 0

The DIN_MIN register sets the starting duty, and the SPD_MIN register sets the minimum output duty for open-loop control and the minimum speed for closed-loop speed control.

Direction Control

The direction is controlled by the DIR pin's polarity. When DIR is pulled low, the MP6632A operates in forward rotation in the following sequence: A → B → C → A…

When DIR is pulled high, the MP6632A operates in reverse rotation in the following sequence: A → C → B → A…

Pre Start-Up Timer

In the pre start-up stage, the IC increases the output duty cycle gradually before the speed is taken over by the PWM duty cycle, triggered by the timer set by bits DUTY_SLOPE[1:0]. This is used for smooth start-up and to provide enough torque.

A longer timer provides a lower soft pre-start current, but causes a longer pre start-up time.

Soft-Start Time (t_{SS})

To reduce the input inrush current during start-up, MP6632A provides a configurable soft-start time (t_{SS}) by setting register bits T_SS[1:0]. t_{SS} can be set between 1.3s and 10.4s.

Closed-Loop Integrator Gain

In closed-loop mode, the closed-loop integrator gain is dependent on the register bits KI[7:0] and KP[7:0].

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Higher KI and KP values lead to faster loop response when the loop is steady.

Oscillator Frequency Setting

The operating switching frequency (f_{SW}) can be set to either 25KHz or 50kHz by configuring register SW_SEL .

Speed Detection

The FG signal on the FG/RD pin outputs an internal Hall change signal for speed indication. The different FG signal frequencies include 1x, 1/2x, and 3x the Hall frequency. This is selected by setting the FGRD_SEL bit.

FG is an open-drain output that must be pulled up externally during normal operation.

Dead Time (DT)

To prevent shoot-through in any bridge phase, a dead time (DT) is necessary. The DT for all three phases is set by a single DT resistor (R_{DT}) on the DT pin or internal register. The DT has eight different selectable options (see Table 2).

Table 2: DT Set by the DT Resistor

R_{DT} (kΩ)	DT (ns)
0	800
4	700
8	600
12	500
16	400
24	300
32	200
44	100

Standby Mode

The MP6632A integrates standby mode to reduce power consumption.

If PWM_DC = 0, the PWM input duty is low and remains low for longer than 100ms, and all gate drivers stop. Then the IC enters standby mode. In standby mode, the most internal circuit is off, including the VREG LDO.

Locked-Rotor Detection

In the case of a locked motor rotor lock, all low-side (LS) gate drivers output high if there is no Hall signal edge during the 0.5s detection time. All low-side MOSFETs (LS-FETs) turn on and auto-restart after 4.5s, and then the IC tries to recover. nFT is pulled low when the locked rotor is detected, and is pulled high after recovery.

Over-Current Protection (OCP)

The MP6632A senses the bus current using a current-sense resistor. If during normal switching the bus current exceeds the OCP threshold set by the OC pin or register OCP_TH a after deglitch time, all LS-FETs turns on immediately. The part resumes normal switching in the next switching cycle. If the over-current (OC) fault lasts longer than the time set by register bits PTIME[2:0], then all gate drivers are disabled. The OCP fault response can be configured to either latch-off mode or retry mode.

Table 3: OCP Threshold Set by the OC Resistor

R (kΩ)	OCP Threshold (mV)
0 to 6	Disabled
16 to 28	100
8 to 14	50
32 to 80	200

Thermal Shutdown

The MP6632A's die temperature is monitored internally. If the die temperature exceeds 175°C, all of the gate drivers are disabled. Once the die temperature drops below 150°C, the device resumes normal operation automatically. The nFT pin pulls low when thermal shutdown is triggered.

Under-Voltage Lockout (UVLO)

When the VCC pin voltage (V_{CC}) falls below the UVLO threshold, all circuitry in the device is disabled and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the device resumes normal operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER DESCRIPTION

Register Map

Add	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00h (OTP/REG)	SPD_MAX[7:0]							
01h (OTP/REG)	SPD_MAX[15:8]							
02h (OTP/REG)	SPD_MIN[7:0]							
03h (OTP/REG)	HI_FREQ	BRK_MD	DIN_MIN[5:0]					
04h (OTP/REG)	WAIT_TM[1:0]		WAIT_PWM	MAX_EN	CLOSE_H	OPEN_L	LOCK_SEL[1:0]	
05h (OTP/REG)	DST	T_SS[1:0]		DUTY_SLOPE [1:0]		SPD_ZERO	RESERVED	
06h (OTP/REG)	OCP_BH	RESERVED	PWM_DC	FGRD_SEL[1:0]		OCP_TH[1:0]		RESERVED
07h (OTP/REG)	PWM_L	SW_SEL	RESERVED					
08h (OTP/REG)	KI[7:0]							
09h (OTP/REG)	KP[7:0]							
0Ah (OTP/REG)	RESERVED							
0Bh (OTP/REG)	D37.5							
0Ch (OTP/REG)	D50							
0Dh (OTP/REG)	D62.5							
0Eh (OTP/REG)	D75							
0Fh (OTP/REG)	D87.5							
10h (OTP/REG)	RESERVED	MIN_SEL	DT[2:0]			PTIME[2:0]		
11h (OTP/REG)	RESERVED	WAIT_BH	WAIT_SEL	WAIT_EN	RESERVED	OC_RTY	HLOGIC	RESERVED
12h (OTP/REG)	OCP_RED	RESERVED	HAL_POL	RESERVED		LOCK_LF	OCP_LF	RESERVED

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

MAX_SPEED_1 (00h)

The MAX_SPEED_1 command sets the maximum speed in close-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[7:0]	0xFF	Sets the maximum speed when the input duty is 100%. 8-bit least significant bit (LSB). Electrical speed = 7.5rpm / LSB.

MAX_SPEED_2 (01h)

The MAX_SPEED_2 command sets maximum speed in close-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MAX[15:8]	0x08	Sets the maximum speed when the input duty is 100%. 8-bit most significant bit (MSB). Combined with SPD_MAX[7:0] to set the maximum speed (electrical speed).

MIN_SPEED (02h)

The MIN_SPEED command sets minimum speed in close-loop speed control or the minimum output duty in open-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	SPD_MIN[7:0]	0x20	Sets the minimum speed or minimum output duty. In closed-loop mode, this bit sets the minimum speed (electrical speed), depending on the HI_FREQ bit, where: HI_FREQ = 0, 60rpm / LSB HI_FREQ = 1, 480rpm / LSB In open-loop mode, this bit sets the minimum output duty, where minimum output duty = SPD_MIN[7:0] / 255 and the default is 12.5%.

CFR_1 (03h)

The CFR_1 command refers to the control function register and sets the switching frequency (f_{SW}), brake mode, and starting duty.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	HI_FREQ	0	Selects the high frequency. 0: High frequency is not selected (default) 1: High frequency is selected The SW bit must be set to 1 if HI_FREQ = 1.
6	OTP/REG	BRK_MD	0	Selects the brake action after the BRK pin is pulled high. 0: The reference duty cycle reduces to DIN_MIN, then turns on the low-side MOSFETs (LS-FETs) 1: Turns on the LS-FETs
5:0	OTP/REG	DIN_MIN[5:0]	0x10	Sets the starting duty, where the starting duty = DIN_MIN / 128 and the default is 12.5%.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CFR_2 (04h)

The CFR_2 command sets the wait status, maximum speed below the starting duty, open-/closed-loop speed control, and lock detection time.

Bits	Access	Bit Name	Default	Description
7:6	OTP/REG	WAIT_TM[1:0]	00	Selects the waiting time or speed threshold at start-up. Combined with WAIT_SEL, these bits can select the fixed time that the IC waits before output switching or the motor speed threshold at which the IC starts driving the motor. When LOCK_SEL = 00, the waiting time or speed threshold can be selected as follows: If WAIT_SEL = 1, wait for a fixed time. The time setting is WAIT_TM = 00: 1.2s, 01: 1.8s, 10: 3s, 11: 4.2s. If WAIT_SEL = 0, wait for the motor speed to drop to a certain speed, where WAIT_TM = 00: 1000rpm (electrical speed), 01: 600rpm, 10: 150rpm, 11: 60rpm. This is also related to the LOCK_SEL register setting. If LOCK_SEL = 01, the wait time is doubled, and the corresponding speed threshold is reduced to half of its default speed. If LOCK_SEL = 1x, the wait time is increased by four times, and the speed threshold is reduced to a fourth of its default speed.
5	OTP/REG	WAIT_PWM	0	Enables the wait function for the PWM on/off control. 0: Disable the wait function for the PWM on/off control 1: Enable the wait function for the PWM on/off control
4	OTP/REG	MAX_EN	0	Enables the maximum speed when PWM input duty < DIN_MIN. 0: Disabled (default) 1: Maximum output speed or maximum output duty when PWM input duty < DIN_MIN This is active only when SPD_ZERO = 0.
3	OTP/REG	CLOSE_H	0	Enables closed-loop speed control when the PWM input duty > 87.5%. 0: Open-loop speed control when the PWM input duty > 87.5% (default) 1: Closed-loop speed control when the PWM input duty > 87.5%
2	OTP/REG	OPEN_L	1	Enables open-loop speed control. 1: Open-loop speed control (default) 0: Closed-loop speed control when the PWM input duty < 87.5%
1:0	OTP/REG	LOCK_SEL	00	Selects the lock detection time and retry time. 00: The detection time is 0.5s, and the retry time is 4.5s 01: The detection time is 1s, and the retry time is 9s 1x: The detection time is 2s, and the retry time is 18s

START_HALL (05h)

The START_HALL command sets the start-up operation and dynamic operation.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	DST	0	Sets the duty limit at pre start-up. 0: 50% 1: 93%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

6:5	OTP/REG	T_SS[1:0]	00	Sets the soft dynamic time. The output duty reference time ranges between 0% and 100%. 00: 1.3s (default) 01: 2.6s 10: 5.2s 11: 10.4s
4:3	OTP/REG	DUTY_SLOPE [1:0]	10	Pre start-up time bits. The output duty's time duration increases by 1 step. 00: 2.5ms 01: 5ms 10: 10ms (default) 11: 20ms
2	OTP/REG	SPD_ZERO	1	Enables zero speed. 0: Maintain the minimum speed when the PWM input duty cycle < DIN_MIN 1: Stops when the PWM input duty cycle < DIN_MIN
1:0	N/A	RESERVED	00	Reserved.

CFR_3 (06h)

The CFR_3 command sets the over-current protection (OCP) behavior and threshold, the pulse-width modulation (PWM) input, and the FG/RD output.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OCP_BH	0	Enables over-current protection (OCP) actions. 0: Turn on the LS-FETs 1: Floating
6	N/A	RESERVED	0	Reserved.
5	OTP/REG	PWM_DC	0	Selects the DC input or pulse-width modulation (PWM) input for the PWM/DC pin. 0: PWM input (default) 1: DC input
4:3	OTP/REG	FGRD_SEL[1:0]	00	Selects the FG/RD pin output. 00: 1x (default) 01: 1/2x 10: 3x 11: RD
2:1	OTP/REG	OCP_TH[1:0]	11	Selects the OCP threshold. 00: Disabled 01: 50mV 10: 100mV 11: 200mV
0	N/A	RESERVED	0	Reserved.

PWM_SW_COMP (07h)

The PWM_SW_COMP command sets the PWM frequency (f_{PWM}) range and switching frequency (f_{SW}).

Bits	Access	Bit Name	Default	Description
7	OTP/REG	PWM_L	0	Selects the PWM frequency (f_{PWM}). 0: 1kHz to 100kHz 1: 50Hz to 2kHz

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

6	OTP/REG	SW_SEL	0	Selects the output switching frequency (f_{SW}). 0: 25kHz (default) 1: 50kHz
5:0	N/A	RESERVED	0x01	Reserved.

KI (08h)

The KI command configures the integral parameter for closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KI[7:0]	0x01	Sets the integral parameter for closed-loop speed control.

KP (09h)

The KP command configures the gain parameter during closed-loop speed control.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	KP[7:0]	0x01	Sets the gain during closed-loop speed control.

SPEED_CURVE_1 (0Bh)

The SPEED_CURVE_1 command configures the speed when the PWM input duty cycle is at 37.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D37.5[7:0]	0x60	Sets the speed or output duty when the input PWM duty = 37.5%. For open-loop control, set the output duty when the PWM input duty = 37.5%. Output duty = D37.5[7:0] / 256. For closed-loop control, set the reference speed when the PWM input duty = 37.5%. Speed = D37.5[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_2 (0Ch)

The SPEED_CURVE_2 command configures the speed when the PWM input duty cycle is at 50%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D50[7:0]	0x80	Sets the speed or output duty when the input PWM duty = 50%. For open-loop control, set the output duty when the PWM input duty = 50%. Output duty = D50[7:0] / 256. For closed-loop control, set the reference speed when the PWM input duty = 50%. Speed = D50[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_3 (0Dh)

The SPEED_CURVE_3 command configures the speed when the PWM input duty cycle is at 62.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D62.5[7:0]	0xA0	Sets the speed or output duty when the PWM input duty = 62.5%. For open-loop control, set the output duty when the PWM input duty = 62.5%. Output duty = D62.5[7:0] / 256. For closed-loop control, set the speed reference when the PWM input duty = 62.5%. Speed = D62.5[7:0] / 256 x SPD_MAX[15:0].

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

SPEED_CURVE_4 (0Eh)

The SPEED_CURVE_4 command configures the speed when the PWM input duty cycle is at 75%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D75[7:0]	0xC0	Sets the speed or output duty when the PWM input duty = 75%. For open-loop control, set the output duty when the PWM input duty = 75%. Output duty = D75[7:0] / 256. For closed-loop control, set the speed reference when the PWM input duty = 75%. Speed = D75[7:0] / 256 x SPD_MAX[15:0].

SPEED_CURVE_5 (0Fh)

The SPEED_CURVE_5 command configures the speed when the PWM input duty cycle is at 87.5%.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	D87.5[7:0]	0xE0	Sets the speed or output duty when the PWM input duty = 87.5%. For open-loop control, set the output duty when the PWM input duty = 87.5%. Output duty = D87.5[7:0] / 256. For closed-loop control, set the speed reference when the PWM input duty = 87.5%. Speed = D87.5[7:0] / 256 x SPD_MAX[15:8].

GATE_DRIVE_PT (10h)

The GATE_DRIVE_PT command sets minimum on time, dead time (DT), and protection time.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	00	Reserved.
6	OTP/REG	MIN_SEL	0	Selects the minimum on time of the low-side MOSFETs (LS-FETs). 0: 400ns 1: 800ns
5:3	OTP/REG	DT[2:0]	000	Selects the dead time (DT). 000: 800ns 001: 700ns 010: 600ns 011: 500ns 100: 400ns 101: 300ns 110: 200ns 111: 100ns
2:0	OTP/REG	PTIME[2:0]	010	Selects the protection time. 000: 80ms 001: 160ms 010: 240ms 011: 320ms 100: 400ms 101: 480ms 110: 560ms 111: 640ms

CFR_4 (11h)

The CFR_4 command sets the wait configuration, OCP, and Hall sensor logic.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	0	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

6	OTP/REG	WAIT_BH	0	Selects coasting or brake during waiting. 0: Coasting during wait 1: Brake during wait
5	OTP/REG	WAIT_SEL	0	Selects the waiting function at start-up. 0: Coasting until the speed drops below the speed threshold during start-up (default) 1: Coasting for a fixed time during start-up
4	OTP/REG	WAIT_EN	1	Enables the waiting function at start-up. 0: Directly start up without wait 1: Wait until the speed drops to a set threshold or wait for a fixed time during start-up
3	N/A	RESERVED	0	Reserved.
2	OTP/REG	OC_RTY	0	Disables entering the retry state during OCP. 0: Enter retry state during OCP 1: Do not enter retry state during OCP
1	OTP/REG	HLOGIC	0	Selects the input Hall sensor signal. 0: Differential input 1: High/low logic input
0	N/A	RESERVED	0	Reserved.

CFR_5 (12h)

The CFR_5 command sets OCP, Hall sensor polarity and lock protection.

Bits	Access	Bit Name	Default	Description
7	OTP/REG	OC_RED	0	Enables the output duty cycle reduction during OCP. 0: Disabled 1: Enabled
6	N/A	RESERVED	0	Reserved.
5	OTP/REG	HAL_POL	0	Selects the Hall signal input polarity. 0: Original Hall signal 1: Inverse of the input Hall signal
4:3	N/A	RESERVED	00	Reserved.
2	OTP/REG	LCK_LF	0	Enables locked-rotor protection latch-off mode. 0: Disabled 1: Enabled
1	OTP/REG	OCP_LF	0	Enables OCP latch-off enable mode. 0: Disabled 1: Enabled
0	N/A	RESERVED	0	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

VCC Input

Place an input capacitor (C_{IN}) as close to VCC and GND as possible. VCC keep the input voltage (V_{IN}) stable and reduces the V_{IN} noise and ripple. The C_{IN} resistance must be low at the switching frequency (f_{SW}).

It is recommended to use an electrolytic capacitor in parallel with the ceramic capacitors with X7R dielectrics. The voltage rating should exceed the maximum V_{IN}.

To avoid high voltage spikes caused by energy stored in the motor charged back to the C_{IN} side, a voltage-clamping transient voltage suppressor (TVS) diode is recommended.

MOSFETs Selection

Six external N-channel MOSFETs are required for normal operation.

The drain-source breakdown voltage of the MOSFETs must exceed the supply voltage. Considering the voltage spike caused by parasitic inductance, the voltage margin needs to be taken in consideration to prevent MOSFETs from being damaged by the spike. A 10V to 15V margin is typically recommended. The voltage spike is related to the PCB layout and current; a larger margin is required for higher-current applications.

$R_{DS(ON)}$ is the resistance when the MOSFET is fully turned on. A lower $R_{DS(ON)}$ means lower power consumption and less generated heat. $R_{DS(ON)}$ should be selected so that the heat can be dissipated safely. An external heat sink or special PCB layout can be used for heat dissipation.

External Capacitor

A locally bypassed capacitor is required for the VREG pin to provide power to the gate driver. A ≥1μF ceramic capacitor with X7R or X5R dielectrics is recommended.

The BST capacitor (C_{BST}) is the power supply for high-side (HS) gate driver. ≥1μF ceramic capacitor with X7R or X5R dielectrics is recommended. C_{BST} must be connected in series with a 2.2Ω resistor.

Hall Sensor Connection

This operation is based on the Hall sensor signal from the external Hall-effect sensor. The MP6632A supports either Hall elements with differential inputs or a Hall-sensor IC with high-/low-logic inputs configured via the HLOGIC register bit.

Hall Elements Connection when HLOGIC = 0

When HLOGIC = 0, the Hall input acts as a differential input, and the MP6632A supports Hall elements with differential inputs. The Hall element has two outputs connected to Hx+ and Hx- as the differential inputs.

Figure 5 shows the Hall sensors connected in series.

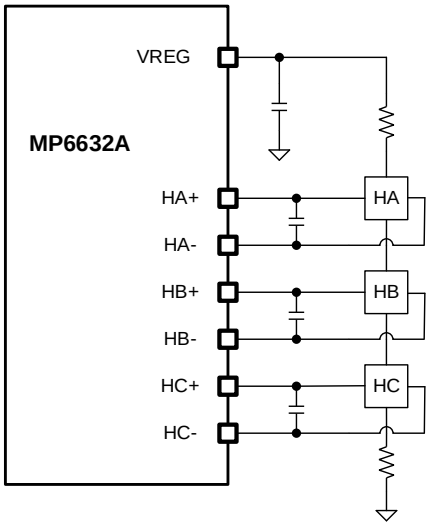


Figure 5: Series Hall Elements Connection

The voltage range of Hx+ and Hx- is recommended to be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 6 on page 25 shows the Hall sensors connected in parallel.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

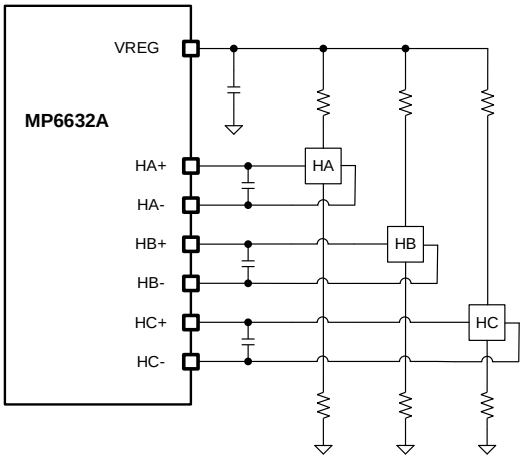


Figure 6: Parallel Hall Elements Connection

The voltage range of Hx+ and Hx- must be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 7 shows that supply voltage of the Hall element as a low-dropout (LDO) regulator.

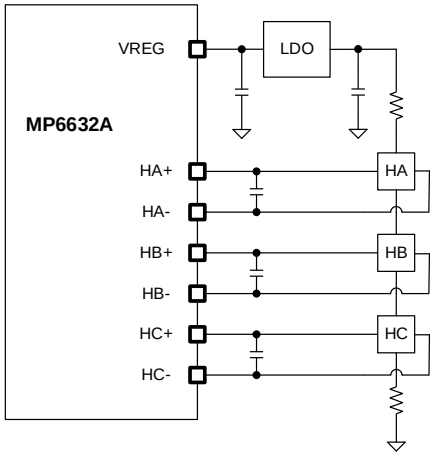


Figure 7: Hall Sensor Supplied by LDO

Hall IC Connection when HLOGIC = 0

In Hall differential input mode, the MP6632A can support a Hall-sensor IC with Hx- connected to a bias voltage. The bias voltage must be within the Hall sensor's common-mode voltage.

The voltage range of Hx+ and Hx- must be within the Hall sensor's common-mode voltage. Otherwise, the wrong result may occur where the comparator's high output becomes low, or vice versa.

Figure 8 shows the Hall-sensor IC connection in differential mode.

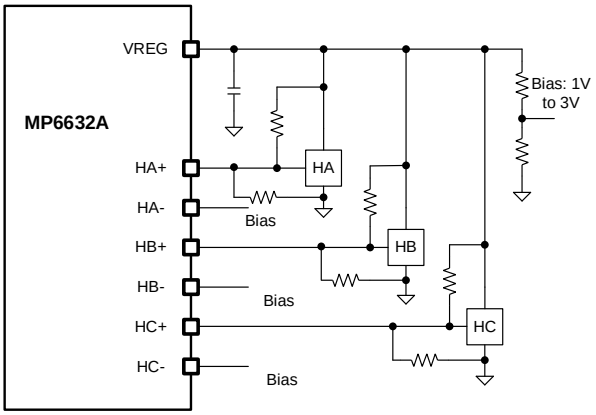


Figure 8: Hall-Sensor IC Connection in Differential Input Mode

Hall IC Connection when HLOGIC = 1

If Hall input mode is configured as the high-/low-logic input mode via register bit HLOGIC, the Hall-sensor IC is used as the Hall sensor. Connect the Hall-sensor IC's output to Hx+ and float Hx-.

Figure 9 shows the Hall-sensor IC connection configured as the Hall sensor high-/low-logic input.

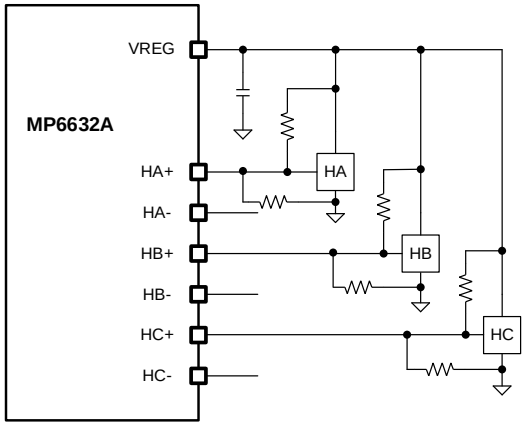


Figure 9: Hall-Sensor IC Connection with High/Low Logic Input Mode

Hall Sensor Placement Example

Consider the Hall sensor placement for a 4-pole, 6-slot motor. There are two conditions to evaluate:

1. When the current flows into the stator phase winding, the south magnetic field is generated (see figure 10 on page 26).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

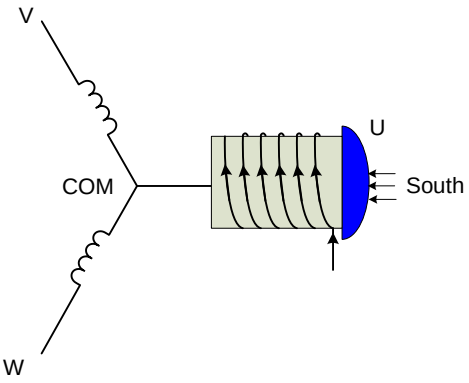
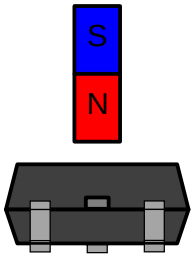


Figure 10: Magnetic South with Winding Direction

2. If the Hall sensor output is high when the north pole is close to the Hall sensor's branded side.



Hall Output High

Figure 11: Hall Output High with North Pole Approaching

The following placement is recommended if both of the above conditions are satisfied, or if neither of the two condition is satisfied.

- Hall A is aligned with the central line of phase A and phase C.
- Hall B is aligned with the central line of phase A and phase B.
- Hall C is aligned with the central line of phase B and phase C.

If one of the two conditions is not satisfied, the hall polarity can be configured to inverse using register bit HAL_POL.

Figure 12 shows the Hall sensor placement.

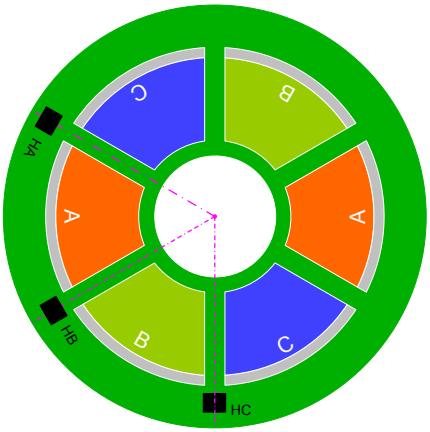


Figure 12: Hall Sensor Placement

Truth Table for Hall Output with Phase Drive

If the Hall sensor placement is correct, the Hall output and phase driver satisfies Table 4 for forward rotation and Table 5 for reverse rotation.

Table 4: Truth Table for Forward Rotation

HA	HB	HC	SWA	SWB	SWC
1	0	0	Switch	Float	LS on
1	1	0	Float	Switch	LS on
0	1	0	LS on	Switch	Float
0	1	1	LS on	Float	Switch
0	0	1	Float	LS on	Switch
1	0	1	Switch	LS on	Float

Table 5: Truth Table for Reverse Rotation

HA	HB	HC	SWA	SWB	SWC
1	0	0	LS on	Float	Switch
1	0	1	LS on	Switch	Float
0	0	1	Float	Switch	LS on
0	1	1	Switch	Float	LS on
0	1	0	Switch	LS on	Float
1	1	0	Float	LS on	Switch

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 13 and Figure 14, and follow the guidelines below:

1. Place the input capacitor as close to the VCC and GND pins as possible.
2. Place the VREG bypass capacitor as close to the VREG and GND pins as possible.
3. Place a capacitor for each Hall input signal to filter the signal from the external Hall sensor. Place this capacitor as close to IC as possible.
4. Place the Hall signal's two wires close to each other to avoid noise coupling.
5. Place a capacitor close to the ISEN pin to filter noise. Two-wire routing is recommended. Place the two wires close to each other.
6. To reduce switching noise, use a ceramic capacitor for each half-bridge to minimize the switching loop trace. Figure 14 shows an example of dual MOSFETs in an SOIC-8 package.

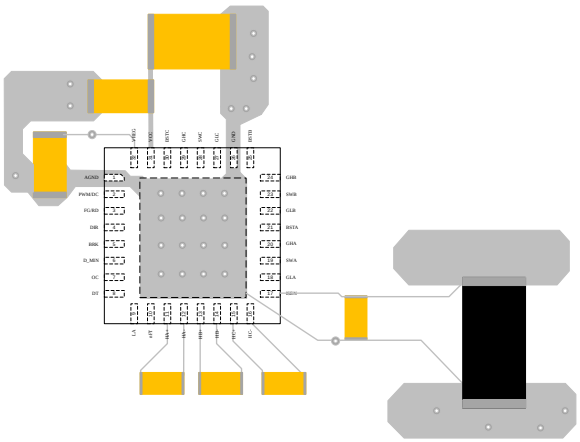


Figure 13: Recommended PCB Layout

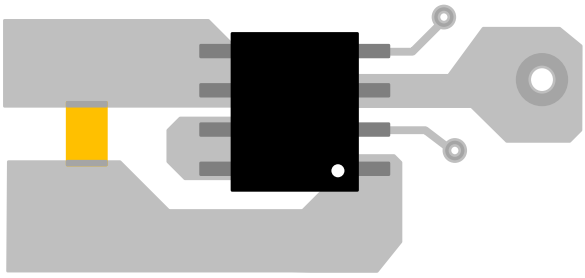


Figure 14: A Bypass Capacitor for Each Half-Bridge

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

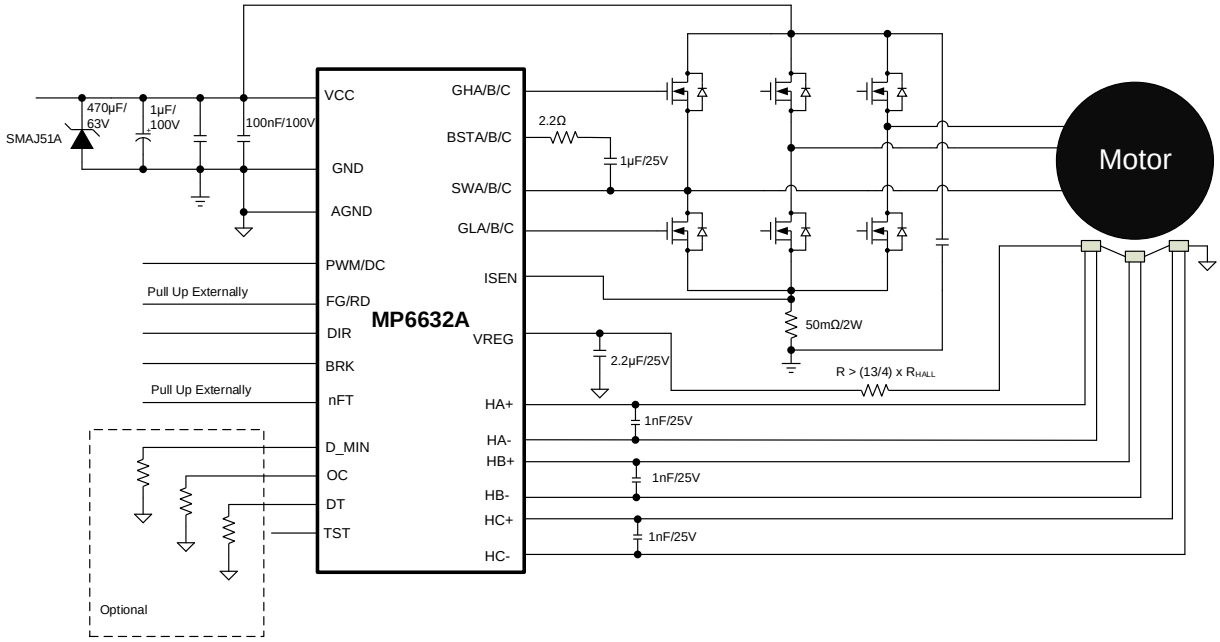
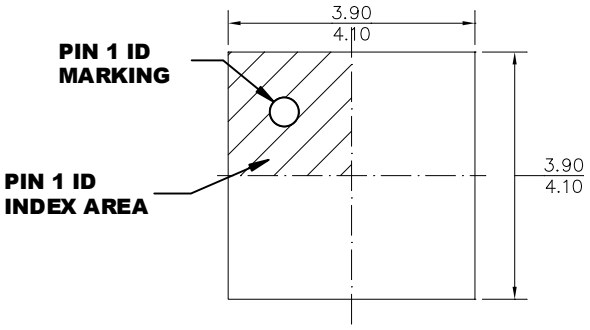


Figure 15: Typical Application Circuit

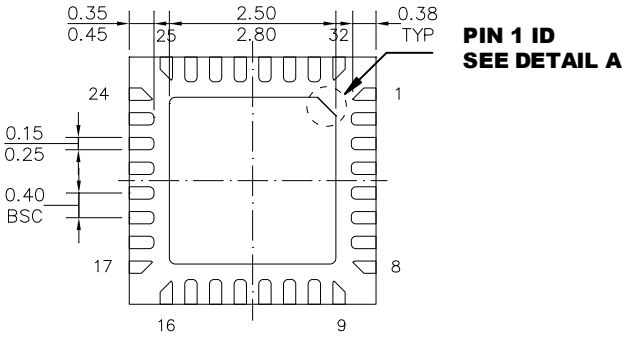
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

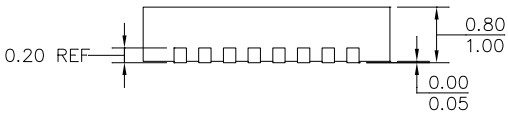
QFN-32 (4mmx4mm)



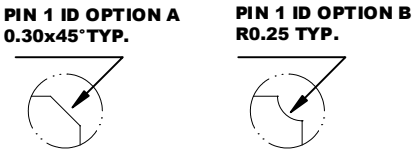
TOP VIEW



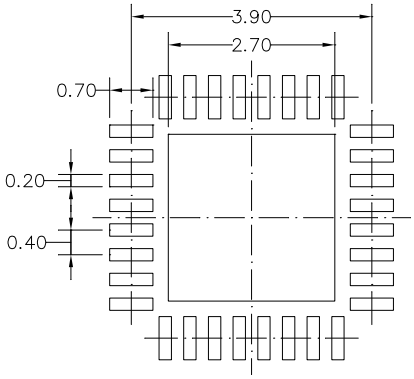
BOTTOM VIEW



SIDE VIEW



DETAIL A



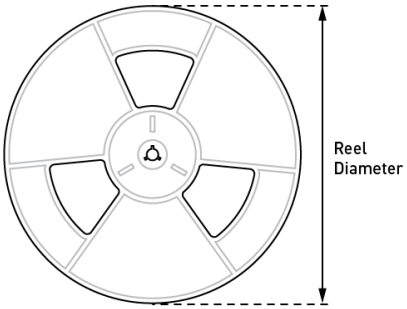
RECOMMENDED LAND PATTERN

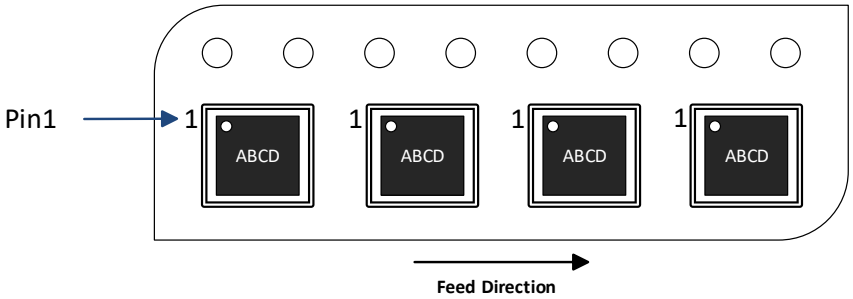
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6632AGR-xxxx-Z	QFN-32 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/13/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.