

BUK9520-100B

N-channel TrenchMOS logic level FET

Rev. 01 — 6 May 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC-Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

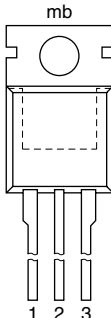
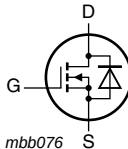
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	-	63	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	203	W
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 63\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	222	mJ
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 ; see Figure 12	-	16.4	22.3	m Ω
		$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 12 ; see Figure 11	-	16.2	20	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		
			SOT78A (3-lead TO-220AB; SC-46; SFM3)	

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9520-100B	3-lead TO-220AB; SC-46; SFM3	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

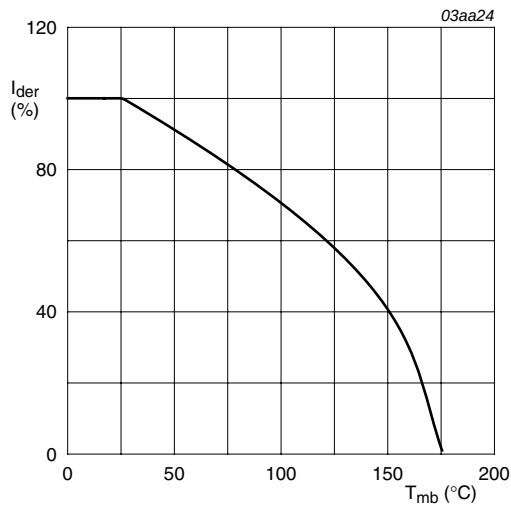
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-15	15	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; see Figure 1 ; see Figure 3	-	63	A
		T _{mb} = 100 °C; V _{GS} = 5 V; see Figure 1	-	45	A
I _{DM}	peak drain current	T _{mb} = 25 °C; t _p ≤ 10 μs; pulsed; see Figure 3	-	253	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	203	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C

Source-drain diode

I _S	source current	T _{mb} = 25 °C	-	63	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	253	A

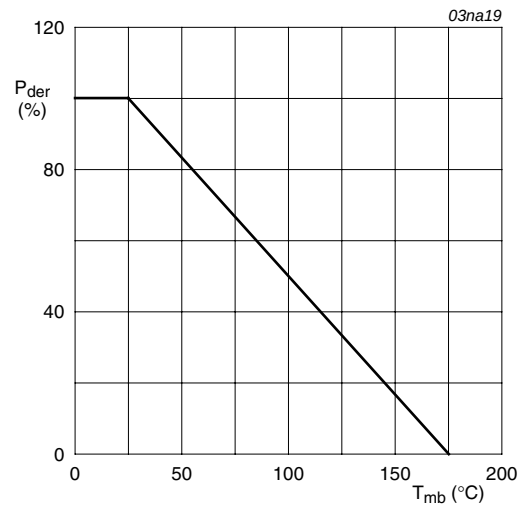
Avalanche ruggedness

E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 63 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped	-	222	mJ
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$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

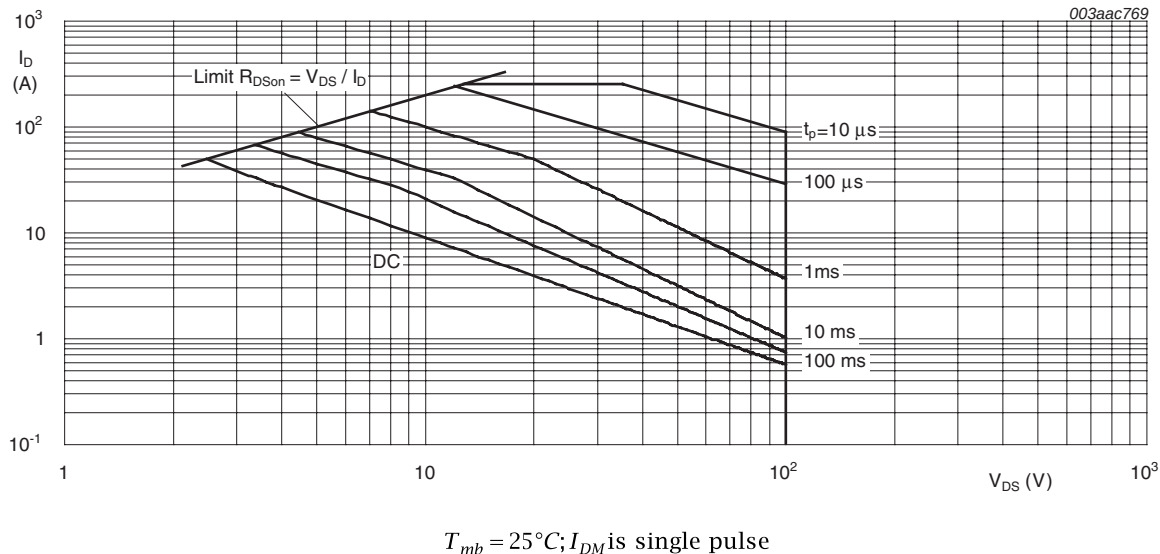


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.75	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	-	60	-	K/W

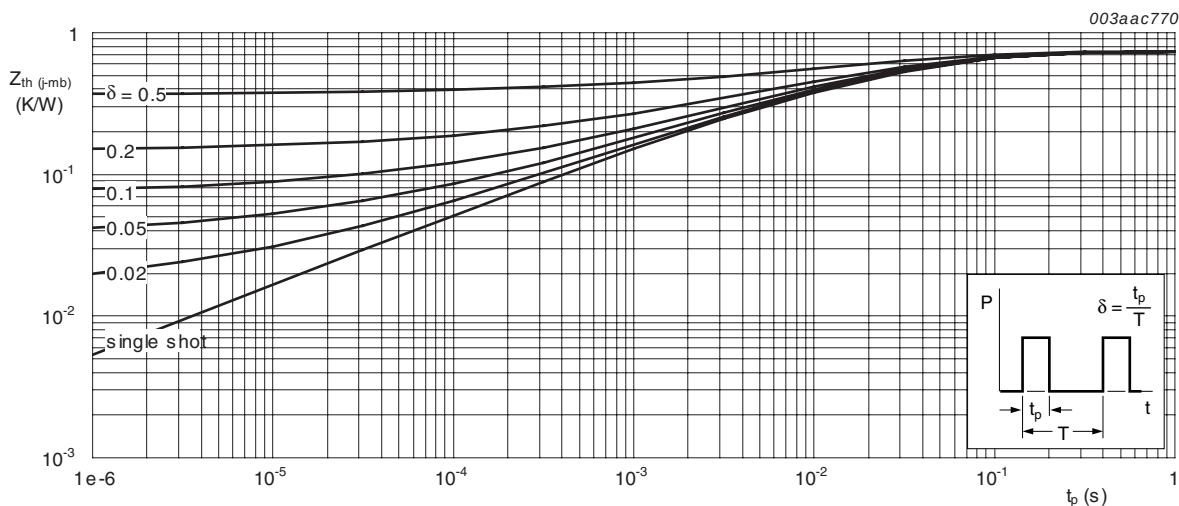


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	1	1.58	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 10	-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μA
I _{GSS}	gate leakage current	V _{DS} = 0 V; V _{GS} = -10 V; T _j = 25 °C	-	2	100	nA
		V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	16.4	22.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 ; see Figure 12	-	15.6	18.5	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 12 ; see Figure 11	-	-	50	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 12 ; see Figure 11	-	16.2	20	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 80 V; V _{GS} = 5 V; T _j = 25 °C; see Figure 14 ; see Figure 15	-	53.4	-	nC
Q _{GS}	gate-source charge		-	9.5	-	nC
Q _{GD}	gate-drain charge		-	21.2	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; T _j = 25 °C; see Figure 16	-	4300	5657	pF
C _{oss}	output capacitance		-	340	411	pF
C _{rss}	reverse transfer capacitance		-	150	201	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	45	-	ns
t _r	rise time		-	116	-	ns
t _{d(off)}	turn-off delay time		-	173	-	ns
t _f	fall time		-	77	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to centre of die; T _j = 25 °C	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	from source lead to source bond pad; T _j = 25 °C	-	7.5	-	nH

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 13	-	0.86	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	80	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$	-	272	-	nC

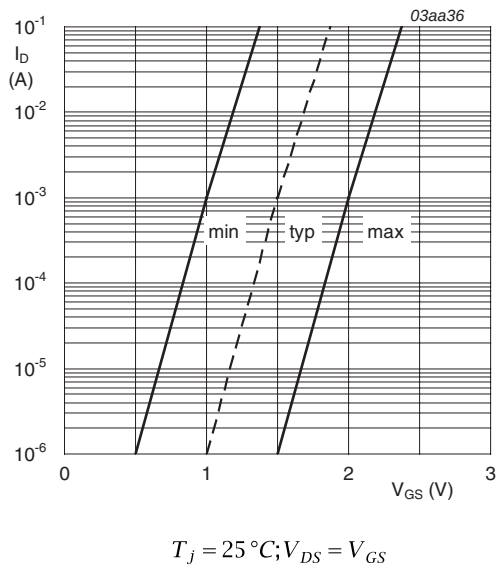


Fig 5. Sub-threshold drain current as a function of gate-source voltage

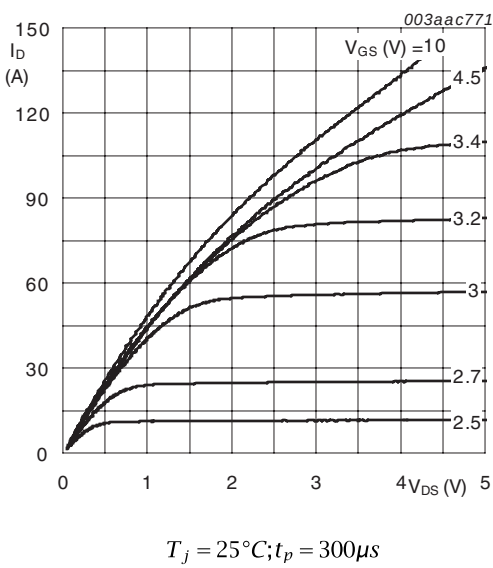


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

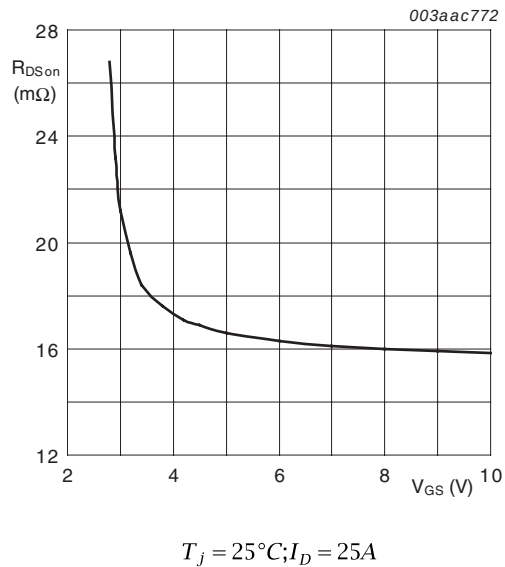


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values.

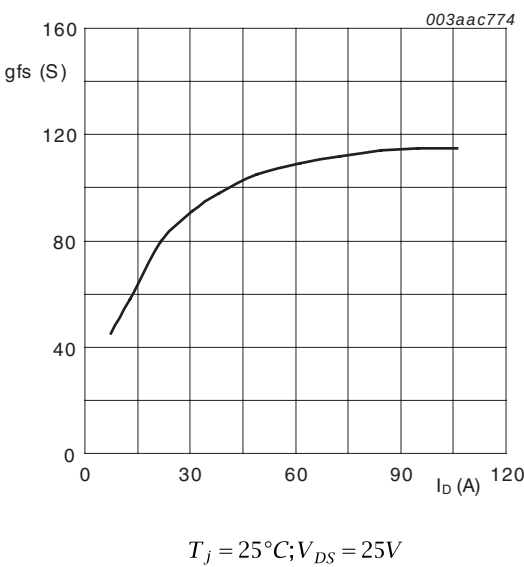


Fig 8. Forward transconductance as a function of drain current; typical values.

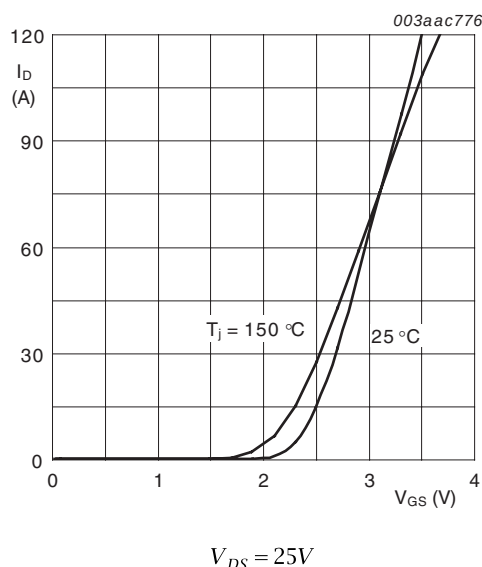


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.

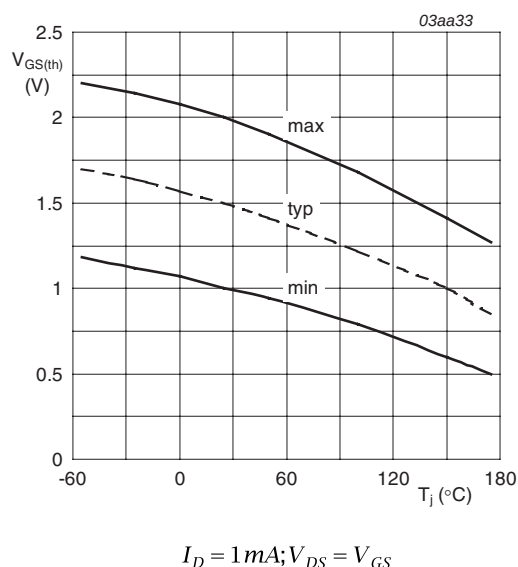


Fig 10. Gate-source threshold voltage as a function of junction temperature

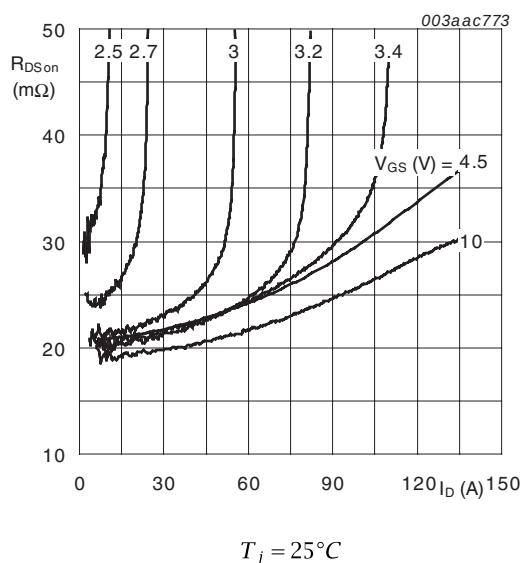


Fig 11. Drain-source on-state resistance as a function of drain current; typical values.

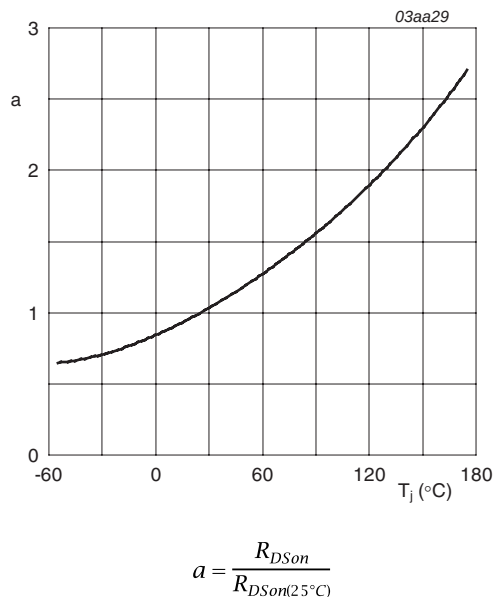


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

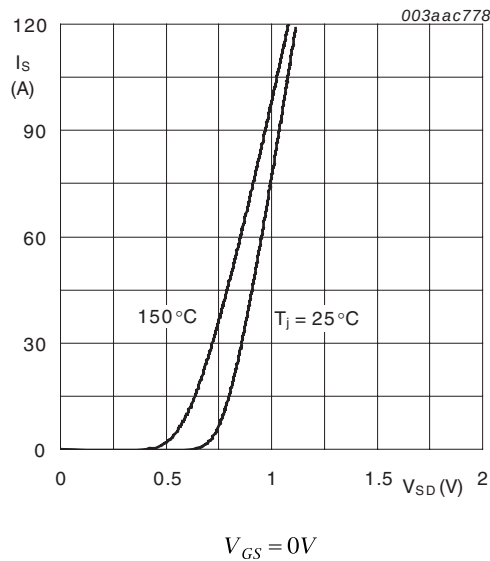


Fig 13. Source current as a function of source drain voltage; typical values.

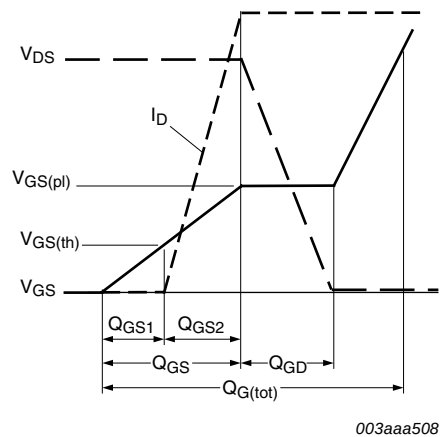


Fig 14. Gate charge waveform definitions

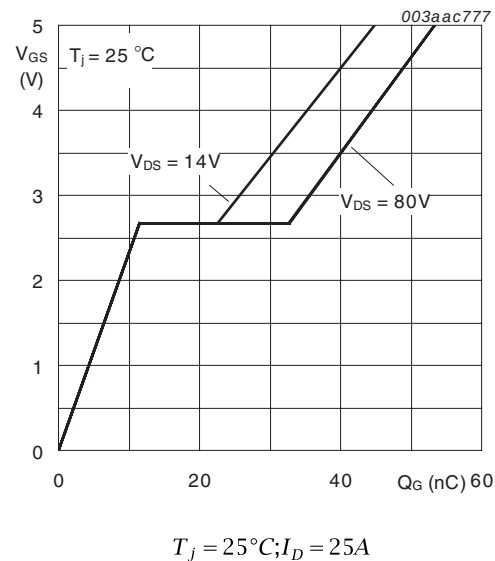


Fig 15. Gate-source voltage as a function of turn-on gate charge; typical values.

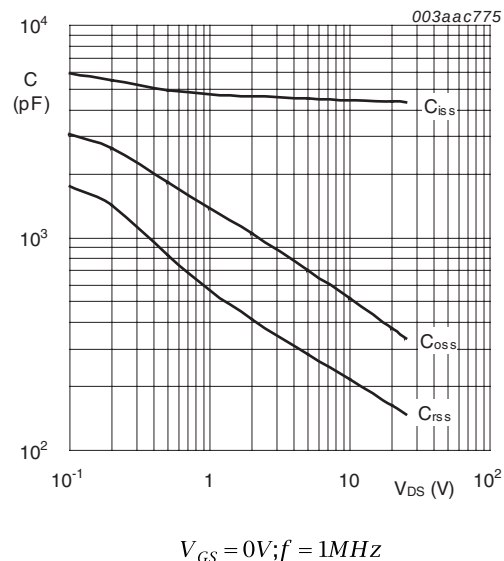


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A

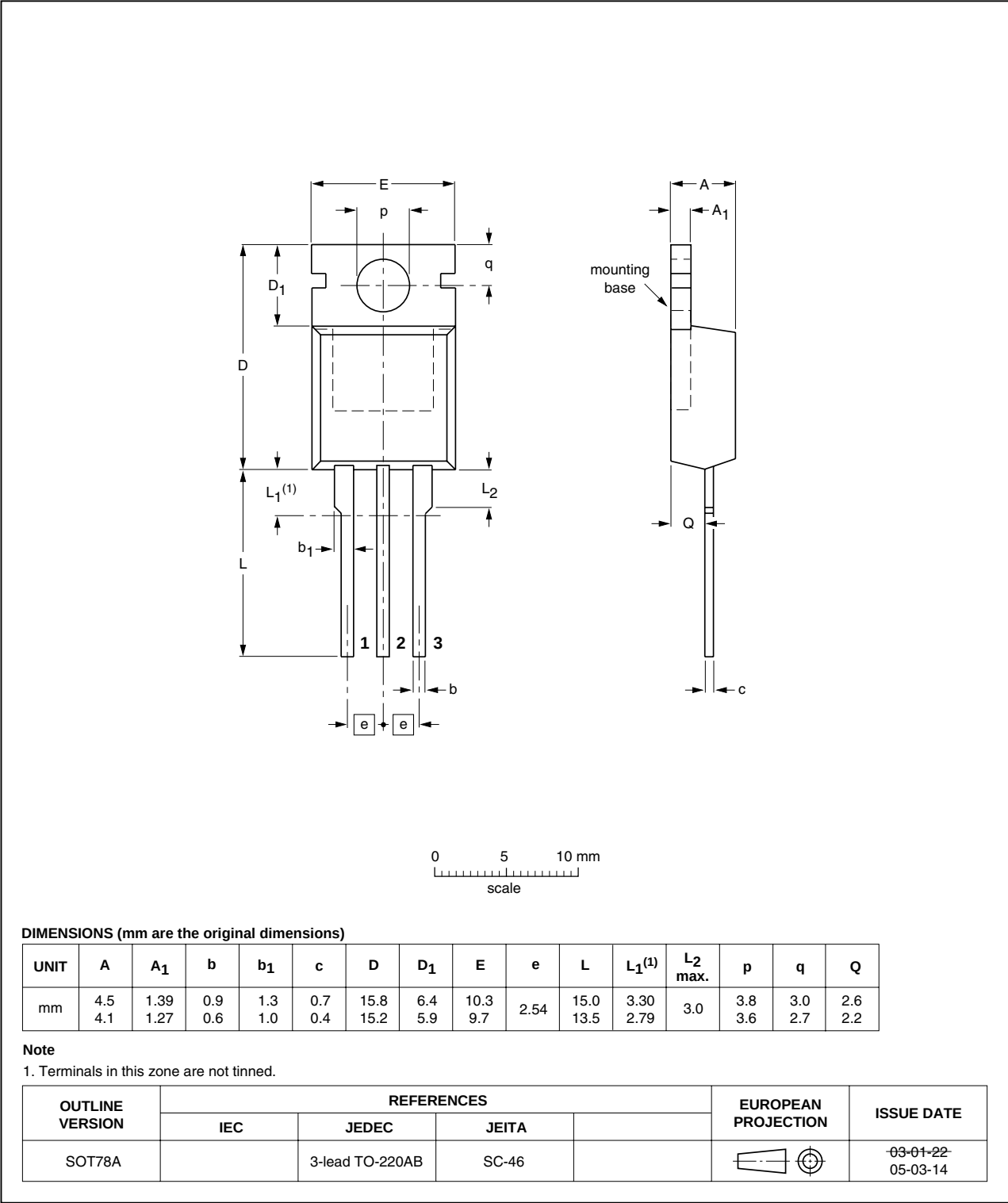


Fig 17. Package outline SOT78A (3-lead TO-220AB; SC-46; SFM3)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9520-100B_1	20090506	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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11. Contents

1 Product profile1

1.1 General description1

1.2 Features and benefits1

1.3 Applications1

1.4 Quick reference data1

2 Pinning information2

3 Ordering information2

4 Limiting values3

5 Thermal characteristics4

6 Characteristics5

7 Package outline9

8 Revision history10

9 Legal information11

9.1 Data sheet status11

9.2 Definitions11

9.3 Disclaimers11

9.4 Trademarks11

10 Contact information11



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