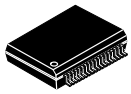
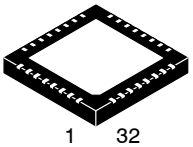
Power Ballast and Dual LED Driver for Automotive Front Lighting 2nd Generation

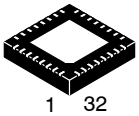
NCV78763



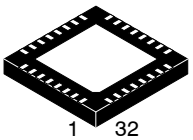
SSOP36 EP
CASE 940AB



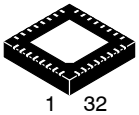
QFN32 7x7
CASE 485ED



QFN32
CASE 488AM



QFNW32 7x7
CASE 484AG



QFNW32 5x5
CASE 484AB

The NCV78763 is a single−chip and high efficient smart Power ballast and Dual LED DRIVER designed for automotive front lighting applications like high beam, low beam, daytime running light (DRL), turn indicator, fog light, static cornering and so on.

The NCV78763 is a best fit for high current LEDs and provides a complete solution to drive two strings up to 60 V, by means of two internal independent buck switch channel outputs, with a minimum of external components. For each individual LED channel, the output current and voltage can be customized according to the application requirements. An on−chip diagnostic feature for automotive front lighting is provided, easing the safety monitoring from the microcontroller. The device integrates a current−mode voltage booster controller, realizing a unique input current filter with a limited BOM.

When more than two LED channels are required on one module, then two, three or more NCV78763 devices can be combined, with the possibility for the booster circuits to operate in multiphase−mode. This helps to further optimize the filtering effect of the booster circuit and allows a cost effective dimensioning for mid to high power LED systems.

Due to the SPI programmability, one single hardware setup can support multiple system configurations for a flexible platform solution approach.

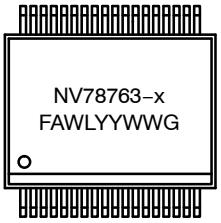
Features

- Single Chip Boost−Buck Solution
- Two LED Strings up to 60 V
- High Current Capability up to 1.6 A DC per Output
- High Overall System Efficiency
- Minimum of External Components
- Active Input Filter with Low Current Ripple from Battery
- Integrated Switched Mode Buck Current Regulator
- Integrated Boost Current−mode Controller
- Programmable Input Current Limitation
- Average Current Regulation Through the LEDs
- High Operating Frequencies to Reduce Inductor Sizes
- Integrated PWM Dimming with Wide Frequency Range
- Low EMC Emission for LED switching and dimming
- SPI Interface for Dynamic Control of System Parameters
- Please Look Further in the Document for the NV78763−9 Device Regarding its New Features
- These are Pb−Free Devices

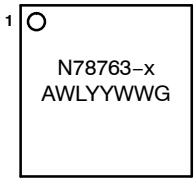
Typical Applications

- Front Lighting High Beam and Low Beam
- Day time Running Light (DRL)
- Position or Park light
- Turn Indicator
- Fog Light and Static Cornering

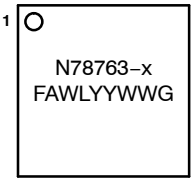
MARKING DIAGRAMS



SSOP36



QFN32



QFNW32

F	= Fab Location
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 46 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 46.

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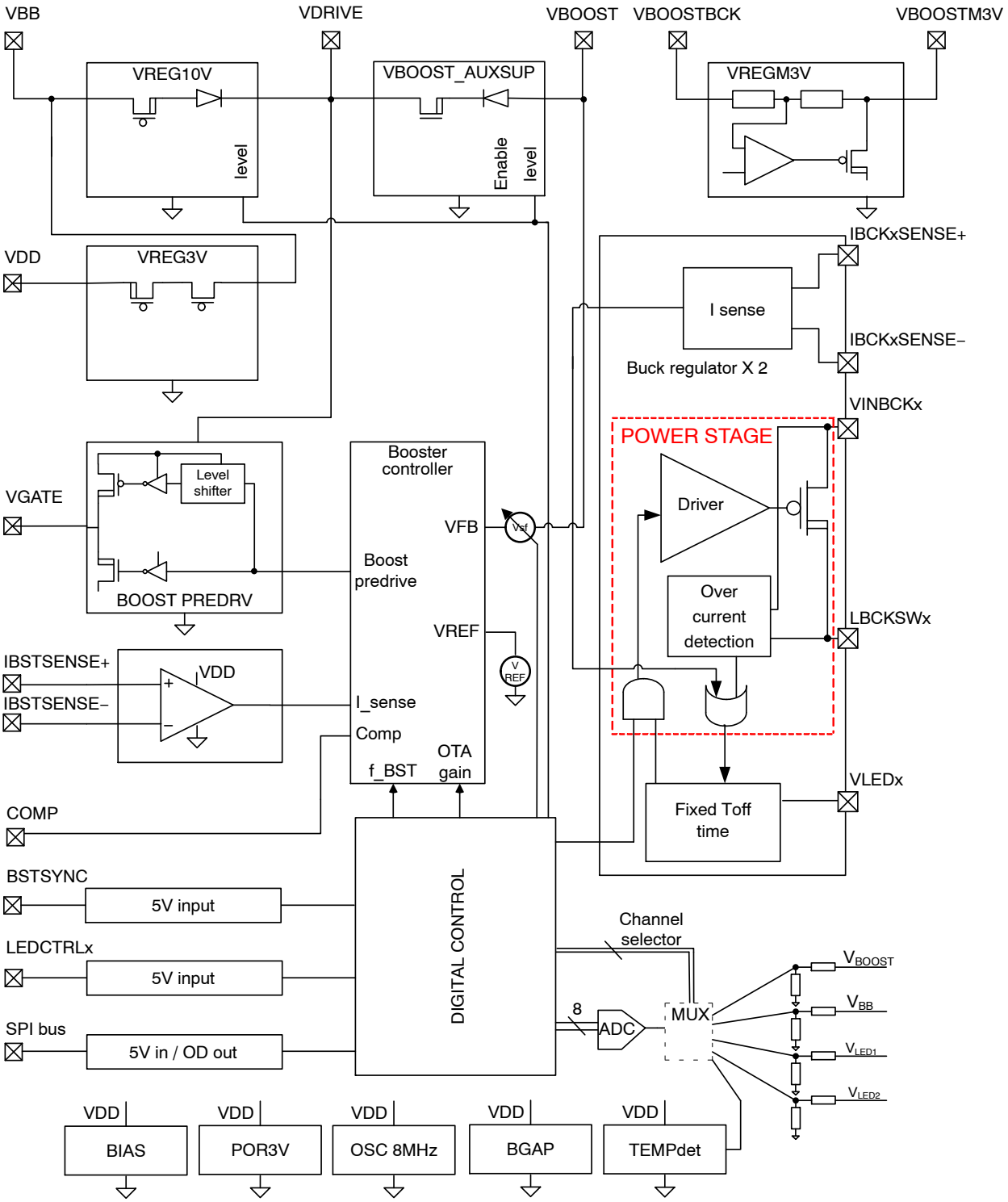


Figure 1. Internal Block Diagram

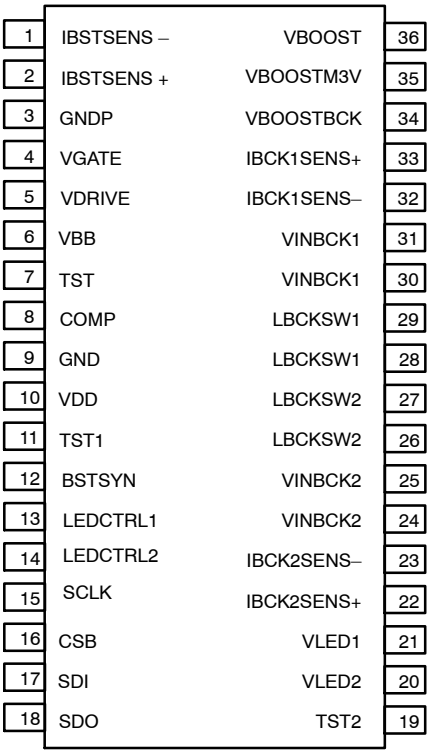


Figure 2. Pin Connections (SSOP36 EP)

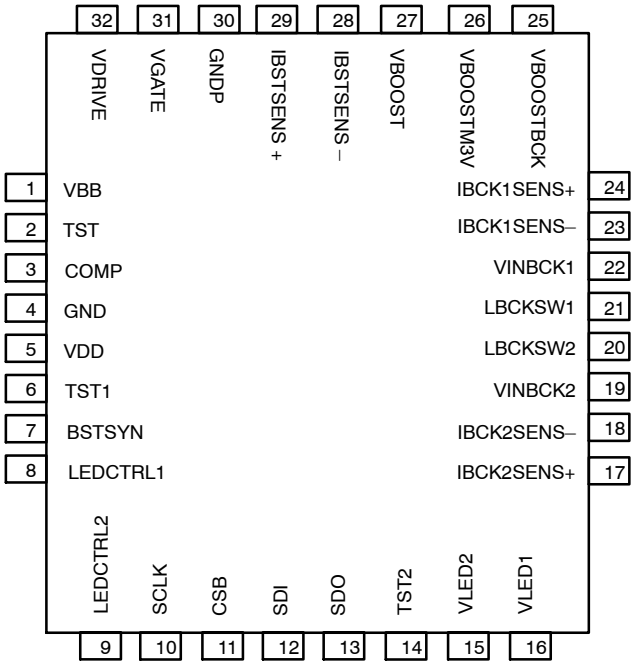


Figure 3. Pin Connections (QFN32)

Table 1. PIN DESCRIPTION

Pin No. SSOP36−EP	Pin No. QFN32	Pin Name	Function	I/O Type
1	28	IBSTSENSE−	Battery current negative feedback input	LV in/out
2	29	IBSTSENSE+	Battery current positive feedback input	LV in/out
3	30	GNDP	Power ground	Ground
4	31	VGATE	Booster MOSFET gate pre−driver	MV out
5	32	VDRIVE	10V supply	MV supply
6	1	VBB	Battery supply	HV supply
7	2	TST	Internal function. To be tied to GND.	LV in/out
8	3	COMP	Compensation for the Boost regulator	LV in/out
9	4	GND	Ground	Ground
10	5	VDD	3V logic supply	LV supply
11	6	TST1	Internal function. To be tied to GND.	LV in/out
12	7	BSTSYN	External clock for the boost regulator	MV in
13	8	LEDCTRL1	LED string 1 enable	MV in
14	9	LEDCTRL2	LED string 2 enable	MV in
15	10	SCLK	SPI clock	MV in
16	11	CSB	SPI chip select (chip select bar)	MV in
17	12	SDI	SPI data input	MV in
18	13	SDO	SPI data output	MV open−drain
19	14	TST2	Internal function. To be tied to GND.	LV in/out
20	15	VLED2	LED string 2 forward voltage input	HV in
21	16	VLED1	LED string 1 forward voltage input	HV in
22	17	IBCK2SENSE+	Buck 2 positive sense input	HV in
23	18	IBCK2SENSE−	Buck 2 negative sense input	HV in
24	19	VINBCK2	Buck 2 high voltage supply	HV in
25	X	VINBCK2	Buck 2 high voltage supply	HV in
26	20	LBCKSW2	Buck 2 switch output	HV out
27	X	LBCKSW2	Buck 2 switch output	HV out
28	21	LBCKSW1	Buck 1 switch output	HV out
29	X	LBCKSW1	Buck 1 switch output	HV out
30	22	VINBCK1	Buck 1 high voltage supply	HV in
31	X	VINBCK1	Buck 1 high voltage supply	HV in
32	23	IBCK1SENSE−	Buck 1 negative sense input	HV in
33	24	IBCK1SENSE+	Buck 1 positive sense input	HV in
34	25	VBOOSTBCK	High voltage for the BUCK switches	HV supply
35	26	VBOOSTM3V	VBOOST−3V regulator output	HV out (supply)
36	27	VBOOST	Boost voltage feedback input	HV in

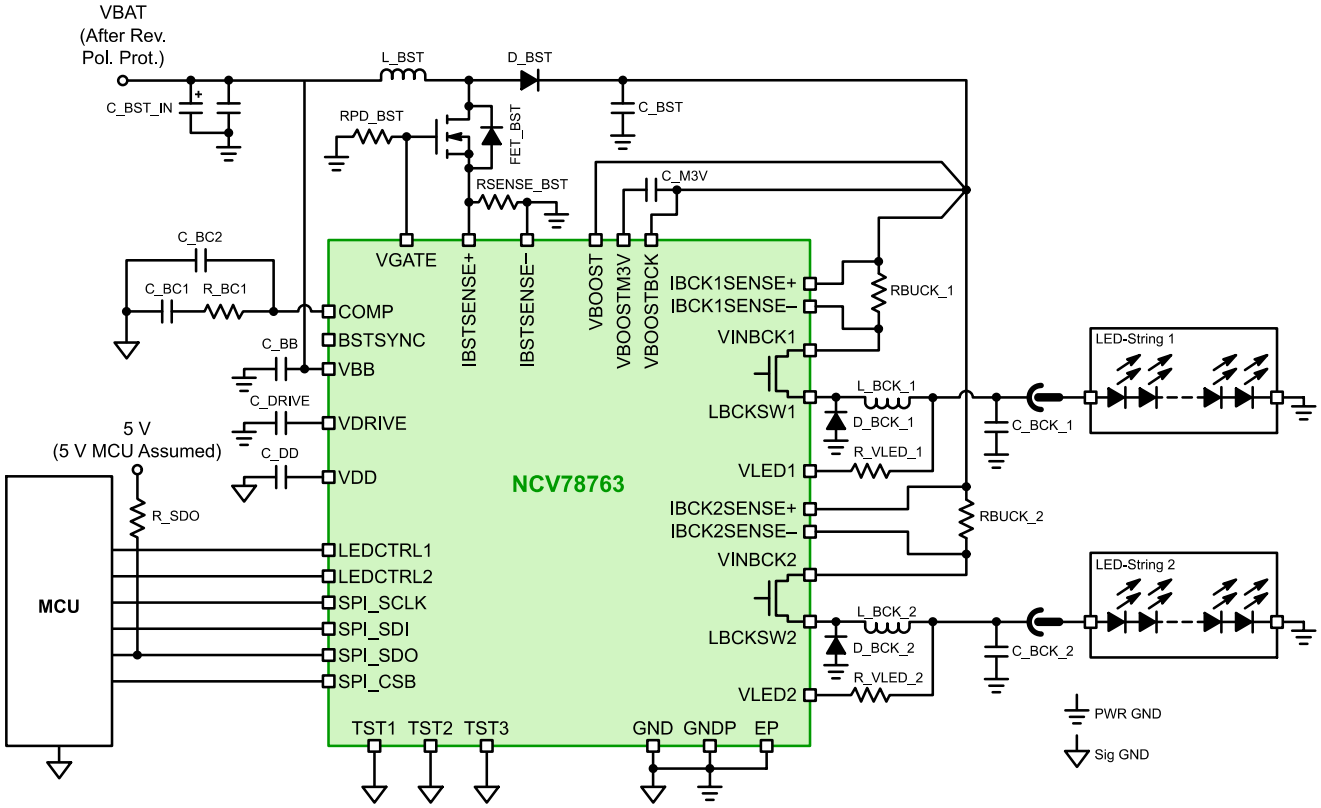


Figure 4. NCV78763 Application Diagram

Note A: as reported in the application diagram, the device pins TST, TST2 & TST1 must be connected to the signal ground GND.
Note B: external capacitors or RC may be added to these SPI lines for stable communication in case of application noise. The selection of these components must be done so that the resulting waveforms are respecting the limits reported in Table 19.
Note C: recommended values for the external MOSFET pull down resistor RPD_BST range from 10 kΩ to 33 kΩ.
Note D: the minimum value for the LED feedback resistors R_VLED_1 and R_VLED_2 is 1 kΩ.

Table 2. ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage (Note 1)	V_{BB}	−0.3	60	V
LED supply voltage (Note 2)	V_{BOOST}	−0.3	68	V
Logic Supply voltage (Note 3)	V_{DD}	−0.3	3.6	V
MOSFET Gate driver supply voltage (Note 4)	V_{DRIVE}	−0.3	12	V
Input current sense voltage pins	IBSTSENSE+, IBSTSENSE−	−1.0	12	V
Medium voltage IO pins (Note 5)	IOMV	−0.3	7.0	V
Relative voltage IO pins (Note 6)	ΔV_IO	VBOOSTM3V	VBOOSTBCK	V
Buck switch low side (Note 7)	LBCKSW1, LBCKSW2	−2.0	VBOOSTBCK	V
Current into or out of the VLED pin	$I_{VLEDpin}$	−30	30	mA
Series resistor on the VLED pin	R_{VLEDx}	1		kΩ
Storage Temperature (Note 8)	T_{strg}	−50	150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 9)	T_{SLD}		260	°C
Electrostatic discharge on component level (Note 10)	V_{ESD}	−2	+2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute maximum rating for pin VBB.
2. Absolute maximum rating for pins: VBOOST, VBOOSTM3V, IBCK1SENSE+, IBCK1SENSE−, VINBCK1, VLED1, IBCK2SENSE+, IBCK2SENSE−, VINBCK2, VLED2.
3. Absolute maximum rating for pins: VDD, TEST1, TEST2, COMP.
4. Absolute maximum rating for pins: VDRIVE, VGATE.
5. Absolute maximum rating for pins: SCLK, CSB, SDI, SDO, LEDCTRL1, LEDCTRL2, BSTSYNC. The device tolerates 5 V coming from the external logics (MCU) when in off state.
6. Relative maximum rating for pins: VINBCK1, VINBCK2, IBCK1SENSE+, IBCK2SENSE+, IBCK1SENSE−, IBCK2SENSE−.
7. Requirement: V(VINBCKx − LBCKSWx) < 70 V.
8. For limited time up to 100 hours, otherwise the max. storage temperature < 85°C.
9. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
10. This device series incorporates ESD protection and is tested by the following methods:
    ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
    ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
    Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

Table 3. RECOMMENDED OPERATING RANGES

The recommended operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the device outside the operating ranges described in this section is not warranted. Operating outside the recommended operating ranges for extended periods of time may affect device reliability. A mission profile (Note 11) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

Characteristic	Symbol	Min	Max	Unit
Battery Supply voltage	V_{BB}	4	40	V
Gate driver supply current (Note 12)	I_{DRIVE}		40	mA
Functional operating junction temperature (Note 13)	T_{JF}	−45	155	°C
Parametric operating junction temperature range	T_{JP}	−40	150	°C
Buck switch output current peak	$I_{LBUCKpeak}$		1.9	A

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. The parametric characteristics of the circuit are not guaranteed outside the Parametric operating junction temperature range. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
12. $I_{DRIVE} = Q_{Tgate} \times F_{BOOST}$ (external MOSFET total gate charge multiplied by booster driving frequency).
13. The circuit functionality is not guaranteed outside the functional operating junction temperature range. The maximum functional operating range can be limited by thermal shutdown "Tsd" (ADC_Tsd, see Table 10). Also please note that the device is verified on bench for operation up to 170°C but that the production test guarantees 155°C only.

Table 4. THERMAL RESISTANCE

Characteristic	Package	Symbol	Value	Unit
Thermal resistance package to Exposed Pad (Note 14)	SSOP36−EP	θJcbot	3.5	°C/W
Thermal resistance package to Exposed Pad (Note 14)	QFN32 7x7	θJcbot	3.4	°C/W
Thermal resistance package to Exposed Pad (Note 14)	QFN32 5x5	θJcbot	3.4	°C/W

14. Includes also typical solder thickness under the Exposed Pad (EP).

ELECTRICAL CHARACTERISTICS NOTE: Unless differently specified, all device Min and Max parameters boundaries are given for the full supply operating ranges and junction temperature (T_{JP}) range (−40°C; +150°C).

Table 5. VBB: BATTERY SUPPLY INPUT

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Nominal Operating Supply Range	V_{BB}		5		40	V
Device Current Consumption	I_{BB_0}	buck regulators off, gate drive off, outputs unloaded			8	mA

Table 6. VDRIVE: SUPPLY FOR BOOSTER MOSFET GATE DRIVE CIRCUIT

Characteristic	Symbol	Conditions		Min	Typ	Max	Unit
VDRIVE reg. voltage from VBB (Note 15)	$V_{DRV_BB_15}$	$V_{BB} - V_{DRIVE} > 1.65$ V @I_{DRIVE} = 25 mA	VDRIVE_ SETPOINT[3:0] = 1111	9.7	10.1	10.7	V
	$V_{DRV_BB_00}$	$V_{BB} - V_{DRIVE} > 1.65$ V @I_{DRIVE} = 25 mA	VDRIVE_ SETPOINT[3:0] = 0000	4.8	5	5.3	V
VDRIVE from VBB increase per code (Note 15)	ΔV_{DRV_BB}	Linear increase, 4Bits			0.34		V
VDRIVE reg. voltage from VBOOST (Note 15)	$V_{DRV_BST_15}$	$V_{BOOST} - V_{DRIVE} > 3$ V @I_{DRIVE} = 40 mA	VDRIVE_SETPOINT[3:0] = 1111	9.5	10.1	10.7	V
	$V_{DRV_BST_00}$	$V_{BOOST} - V_{DRIVE} > 3$ V @I_{DRIVE} = 40 mA	VDRIVE_SETPOINT[3:0] = 0000	4.7	5	5.3	V
VDRIVE from VBOOST increase per code (Note 15)	Δ_{VDRV_BST}	Linear increase, 4 Bits			0.34		V
VDRIVE Output current limitation from VBB input	$V_{DRV_BB_IL}$			40		400	mA
VDRIVE Output current limitation from VBOOST input	$V_{DRV_BB_IL}$			40		200	mA
VDRIVE decoupling capacitor	C_{VDRIVE}				470		nF
VDRIVE decoupling capacitor ESR	C_{VDRIVE_ESR}					100	mΩ

15. The VDRIVE voltage setpoint is in the same range if the current is either provided by VBB or VBOOST pin. The voltage headroom between VBB and VDRIVE or VDRIVE and VBOOST needs to be sufficient. For what concerns VDRIVE from VBB, in case of 25 mA current, the worst case headroom is 1.65V. The VBOOST_AUX regulator can be enabled by SPI (bit VDRIVE_BST_EN[0]).

Table 7. VDD: 3V LOW VOLTAGE ANALOG AND DIGITAL SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBB to VDD switch disconnection	V_{BB_LOW}		3.65		3.9	V
VDD regulator output voltage	V_{DD}	V_{BB} > 4 V	3.15		3.4	V
DC total current consumption including output	V_{DD_IOUT}	V_{BB} > 4 V			15	mA
DC current limitation	V_{DD_ILIM}	V_{BB} > 4 V	15		240	mA
VDD external decoupling cap.	C_{VDD}		0.3	0.47	2.2	μF
VDD ext. decoupling cap. ESR	C_{VDD_ESR}				200	mΩ
POR Toggle level on VDD rising	POR_{3V_H}		2.7		3.05	V
POR Toggle level on VDD falling	POR_{3V_L}		2.45		2.8	V
POR Hysteresis	POR_{3V_HYST}			0.2		V

Table 8. VBOOSTM3: HIGH SIDE MOSFETS AUXILIARY SUPPLY

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VBSTM3 regulator output voltage	V_{BSTM3}		−3.6	−3.3	−3.0	V
VBSTM3 DC output current consumption	V_{BSTM3_IOUT}			5		mA
VBSTM3 DC output current consumption on NV78763−9 device	V_{BSTM3_IOUT}			30		mA
VBSTM3 Output current limitation	V_{BSTM3_ILIM}				200	mA
VBSTM3 external decoupling capacitor	C_{VBSTM3}		0.3	0.47	2.2	μF
VBSTM3 external decoupling cap. ESR	C_{VBSTM3_ESR}				200	mΩ

Table 9. OSC8M: SYSTEM OSCILLATOR CLOCK

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
System oscillator frequency	FOSC8M	After device factory trimming	7.1	8.0	8.9	MHz

Table 10. ADC FOR MEASURING VBOOST, VBB, VLED1, VLED2, VTEMP

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
ADC Resolution	ADC_{RES}			8		Bits
Integral Nonlinearity (INL)	ADC_{INL}		−1.5		+1.5	LSB
Differential Nonlinearity (DNL)	ADC_{DNL}		−2.0		+2.0	LSB
Full path gain error for measurements via VBB, VLEDx, VBOOST	$ADC_{GAINERR}$		−3.25		3.25	%
Offset at output of ADC	ADC_{OFFSET}		−2		2	LSB
Time for 1 SAR conversion	ADC_{CONV_TIME}			8		μs

Table 10. ADC FOR MEASURING VBOOST, VBB, VLED1, VLED2, VTEMP (continued)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
ADC full scale for VBB measurement	ADC_{FS_VBB}			39.7		V
ADC full scale for VLED	ADC_{FS_VLED}			69.5		V
ADC full scale for Vboost	ADC_{FS_VBST}			69.5		V
ADC internal temperature measurement for thermal shutdown	ADC_{TSD}		163	169	175	°C
VLED input impedance	$VLED_{R_IN}$		255		710	kΩ

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
Booster overvoltage shutdown (Note 16)	BST_OV_07	ΔV to the reg. level, DC level	[BOOST_OV_SD = 111]	5.3	5.8	6.3	V
	BST_OV_06	ΔV to the reg. level, DC level	[BOOST_OV_SD = 110]	4.3	4.85	5.3	V
	BST_OV_05	ΔV to the reg. level, DC level	[BOOST_OV_SD = 101]	3.4	3.9	4.3	V
	BST_OV_04	ΔV to the reg. level, DC level	[BOOST_OV_SD = 100]	2.4	2.9	3.3	V
	BST_OV_03	ΔV to the reg. level, DC level	[BOOST_OV_SD = 011]	1.9	2.4	2.8	V
	BST_OV_02	ΔV to the reg. level, DC level	[BOOST_OV_SD = 010]	1.5	2	2.3	V
	BST_OV_01	ΔV to the reg. level, DC level	[BOOST_OV_SD = 001]	1.2	1.5	1.8	V
	BST_OV_00	ΔV to the reg. level, DC level	[BOOST_OV_SD = 000]	0.6	1	1.3	V
Booster overvoltage shutdown increase per code	ΔBST_OV	Linear increase, 2 bits, DC level			0.5/1	0.6/1.2	V
Booster overvoltage re−activation	BST_RA_3	ΔV to the VBOOST reg. overvoltage protection, DC level	[BOOST_OV_REACT = 11]	−1.8	−1.4	−1	V
Booster overvoltage re−activation	BST_RA_0	ΔV to the VBOOST reg. overvoltage protection, DC level	[BOOST_OV_REACT = 00]		0		V
Booster overvoltage re−activation decrease per code	ΔBST_RA	Linear decrease, 2 bits, DC level		−0.6	−0.5		V
VBOOST undervoltage shutdown on NV78763−9 device	BST_UV_THR			1.17	1.215	1.26	V
Booster regulation setpoint voltage	BST_REG_127	DC level	[BOOST_VSETPOINT = 1111111]	62.8	64.1	66	V
	BST_REG_001	DC level	[BOOST_VSETPOINT = 0000001]	14.4	15	15.6	V
	BST_REG_000	DC level	[BOOST_VSETPOINT = 0000000]	10.5	11	11.5	V
Booster regulation setpoint increase step per code	ΔBST_REG	Linear increase, 7 bits			0.39	0.55	V

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
Booster Error Amplifier (EA) Trans−conductance Gain G_m	EA_{Gm_3}	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 11]	63	90	117	μS
	EA_{Gm_2}	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 10]	42	60	78	μS
	EA_{Gm_1}	Seen from VBOOST pin input, DC value	[BOOST_OTA_GAIN = 01]	21	30	39	μS
	EA_{Gm_0}	Seen from VBOOST pin input, High impedance tri−state	[BOOST_OTA_GAIN = 00]		0		μS
EA max output current (positive/source)	$EA_{Iout_pos_max_03}$	EA_{Gm_03} is set	[BOOST_OTA_GAIN = 11]	150	180		μA
	$EA_{Iout_pos_max_02}$	EA_{Gm_02} is set	[BOOST_OTA_GAIN = 10]	100	120		μA
	$EA_{Iout_pos_max_01}$	EA_{Gm_01} is set	[BOOST_OTA_GAIN = 01]	50	60		μA
EA max output current (negative/sink)	$EA_{Iout_neg_max_03}$	EA_{Gm_03} is set	[BOOST_OTA_GAIN = 11]		−180	−150	μA
	$EA_{Iout_neg_max_02}$	EA_{Gm_02} is set	[BOOST_OTA_GAIN = 10]		−120	−100	μA
	$EA_{Iout_neg_max_01}$	EA_{Gm_01} is set	[BOOST_OTA_GAIN = 01]		−60	−50	μA
EA max output leakage current in tri−state	EA_{Iout_leak}	EA_{Gm_00} is set (EA disabled, high impedance tri−state)	[BOOST_OTA_GAIN = 00]	−1		1	μA
EA equivalent output resistance	EA_{ROUT}			0.7		2.9	MΩ
EA max output voltage (at VCOMP pin)	$COMP_{CLH3}$	(BST_SLPCTRL_3 or BST_SLPCTRL_2) & (BST_VLIMTH_3 or BST_VLIMTH_2)	[BOOST_SLP_CTRL = 1x] & [BOOST_VLIMTH = 1x]	2.1	2.26		V
	$COMP_{CLH2}$	BST_SLPCTRL_3 or BST_SLPCTRL_2) & (BST_VLIMTH_1 or BST_VLIMTH_0)	[BOOST_SLP_CTRL = 1x] & [BOOST_VLIMTH = x1]	1.8	1.98		V
	$COMP_{CLH1}$	BST_SLPCTRL_1 or BST_SLPCTRL_0) & (BST_VLIMTH_3 or BST_VLIMTH_2)	[BOOST_SLP_CTRL = x1] & [BOOST_VLIMTH = 1x]	1.5	1.64		V
	$COMP_{CLH0}$	BST_SLPCTRL_1 or BST_SLPCTRL_0) & (BST_VLIMTH_1 or BST_VLIMTH_0)	[BOOST_SLP_CTRL = x1] & [BOOST_VLIMTH = x1]	1.2	1.35		V
EA min output voltage (at VCOMP pin)	$COMP_{CLL}$					0.4	V
Division factor of VCOMP voltage towards the Current comparator input	$COMP_{DIV}$				7		
Voltage shift (offset) on VCOMP on Current comparator input	$COMP_{VSF}$				0.5		V
Booster skip cycle for low currents (Note 17)	BST_SKCL_3		[BOOST_SKCL = 11]		0.7 or 0.8		V
	BST_SKCL_2		[BOOST_SKCL = 10]		0.625 or 0.7		V
	BST_SKCL_1		[BOOST_SKCL = 01]		0.55 or 0.6		V
VGATE comparator to start BST_TOFF time	$BST_{VGATE_THR_1}$		[VBOOST_VGATE_THR = 1]		1.2		V
	$BST_{VGATE_THR_0}$		[VBOOST_VGATE_THR = 0]		0.4		V

Table 11. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI Setting	Min	Typ	Max	Unit
Booster PWM frequency (when from internal generation)	BST_{FREQ_31}	FOSC8M / 38	[BOOST_FREQ = 11111]	187	210	234	kHz
	BST_{FREQ_01}	FOSC8M / 8	[BOOST_FREQ = 00001]	890	1000	1110	kHz
	BST_{FREQ_00}	PWM clock disabled	[BOOST_FREQ = 00000]		0		kHz
Booster PWM freq. increase per code	ΔBST_{FREQ}	Nonlinear increase, 5 bits			5–112		kHz
Booster minimum OFF time (Note 18)	$BST_{TOFF_MIN_3}$		[VBOOST_TOFFMIN = 11]	100	155	210	ns
	$BST_{TOFF_MIN_2}$		[VBOOST_TOFFMIN = 10]	140	195	250	ns
	$BST_{TOFF_MIN_1}$		[VBOOST_TOFFMIN = 01]	30	75	120	ns
	$BST_{TOFF_MIN_0}$		[VBOOST_TOFFMIN = 00]	70	115	160	ns
Booster minimum ON time (Note 18)	$BST_{TON_MIN_3}$		[VBOOST_TONMIN = 11]	235	300	365	ns
	$BST_{TON_MIN_2}$		[VBOOST_TONMIN = 10]	200	260	320	ns
	$BST_{TON_MIN_1}$		[VBOOST_TONMIN = 01]	150	200	250	ns
	$BST_{TON_MIN_0}$		[VBOOST_TONMIN = 00]	100	150	200	ns

16. The following condition must always be respected: BST_REG_XX + BST_OV_X < 68 V.
17. The higher levels indicated in the cells are valid for BST_VLIMTH_2 and BST_VLIMTH_3 selection (BOOST_VLIMTH<1> = 1).
18. Rise and fall time of the VGATE is not included.

Table 12. BOOSTER CONTROLLER – CURRENT REGULATION PARAMETERS

Characteristic	Symbol	Conditions	SPI setting	Min	Typ	Max	Unit
Current comparator for Imax detection	BST_{VLIMTH_3}		[BOOST_VLIMTH = 11]	95	100	105	mV
	BST_{VLIMTH_2}		[BOOST_VLIMTH = 10]	75	80	85	mV
	BST_{VLIMTH_1}		[BOOST_VLIMTH = 01]	57	62.5	67	mV
	BST_{VLIMTH_0}		[BOOST_VLIMTH = 00]	45	50	55	mV
Current comparator for VBOOST regulation, offset voltage	BST_{OFFS}			–5	0	5	mV
Booster slope compensation	$BST_{SLPCTRL_3}$		[BOOST_SLPCTRL = 11]		20		mV/ μs
	$BST_{SLPCTRL_2}$		[BOOST_SLPCTRL = 10]		10		mV/ μs
	$BST_{SLPCTRL_1}$		[BOOST_SLPCTRL = 01]		5		mV/ μs
	$BST_{SLPCTRL_0}$	(no slope control)	[BOOST_SLPCTRL = 00]		0		mV/ μs
Booster Current Sense voltage common mode range	CMVSENSE			–0.1		1	V

Table 13. BOOSTER CONTROLLER – MOSFET GATE DRIVER

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High–side switch impedance	RON_{HI}			2.5	4	Ω
Low–side switch impedance	RON_{LO}			2.5	4	Ω

Table 14. BUCK REGULATOR – INTERNAL SWITCHES CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Buck switch On resistance	$R_{DS(on)}$	At room–temperature, I(VINBCKx) pin = 1.5 A, (VBOOST–VINBCKx) = 0.2 V			0.65	Ω
	$R_{DS(on)_hot}$	At Tj = 150°C, I(VINBCKx) pin = 1.5 A, (VBOOST–VINBCKx) = 0.2 V			0.9	Ω
Buck Overcurrent detection	OCD		1.9		3	A

Table 14. BUCK REGULATOR – INTERNAL SWITCHES CHARACTERISTICS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Buck Switching slope (ON phase)	Trise			3		V/ns
Buck Switching slope (OFF phase)	Tfall			2		V/ns
Slow Buck Switching Slope on NV78763−9 device (ON phase)	Trise_ls	BUCK_DRV_SLOW = 1		1.5		V/ns
Slow Buck Switching Slope on NV78763−9 device (OFF phase)	Tfall_ls	BUCK_DRV_SLOW = 1		1.5		V/ns

Table 15. BUCK REGULATOR – CURRENT REGULATION PARAMETERS

Characteristic	Symbol	Conditions		Min	Typ	Max	Unit
Buck current sense threshold voltage	VTHR_255		[BUCKx_VTHR = 11111111]		412		mV
Buck current sense threshold voltage	VTHR_000		[BUCKx_VTHR = 00000000]		31.5		mV
Buck current sense threshold voltage increase per code	ΔVTHR	exponential increase, 7.5 bits equivalent, DC level			1.013	1.5	%
Buck threshold voltage temperature stability	$VTHR_{TEMP}$	Without chopper function		−1.5 & −2		+1.5 & +2	% & mV / 100°C
Buck threshold voltage accuracy (Note 21)	$VTHR_{ERR}$	Without chopper function		−3 & −6		+3 & +6	% & mV
Buck TOFFxVLED constant setting for shortest OFF time	$T_{OFF_VLED_15}$		[BUCKx_TOFFVLED = 1111]		10		μs V
Buck TOFFxVLED constant setting for longest OFF time	$T_{OFF_VLED_00}$		[BUCKx_TOFFVLED = 0000]		50		μs V
Buck OFF time relative error	$BCK_{TOFF_ERR_REL}$	T_{OFF} xVLED @VLED > 2 V & T_{OFF} > 0.35 μs		−10	0	10	%
Buck OFF time absolute error	$BCK_{TOFF_ERR_ABS}$	T_{OFF} xVLED @VLED > 2 V & $T_{OFF} \le$ 0.35 μs		−35	0	35	ns
Buck OFF time setting decrease per code	ΔTC	exponential increase, 4 bits, DC level			11.33		%
Detection level for low VLED voltages	$VLED_{LMT}$			1.62	1.8	1.98	V
Buck ON too long time detection (OPEN LOAD)	BCK_{TON_OPEN}			44.3	50	55.7	μs
Buck minimum ON time mask in regulation (Note 20)	BCK_{TON_MIN}			50		250	ns
Buck OFF time for short circuit detected on VLEDx (Note 22)	BCK_{TOFF_SHORT}	VLEDx < $VLED_{LMT}$		63		90	μs
The zero−cross detection threshold level (Note 23)	ZCD_TH			−100	−60	−15	mV
The zero−cross detection filter time	ZCD_FT			15		170	ns

Table 15. BUCK REGULATOR − CURRENT REGULATION PARAMETERS

Characteristic	Symbol	Conditions		Min	Typ	Max	Unit
Delay from BUCK ISENS comparator input to BUCK switch going OFF (Note 21)	BCK_{CMP_DEL}	ISENS comparator over−drive ramp > 1 mV/10 ns			70		ns

19. Without use of buck chopper function (for sufficient coil current ripple, see buck section in the datasheet). With the buck chopper function, the offset is reduced to a level lower than ±|3 mV|.
20. The buck ISENSE comparator is active at the end of this mask time.
21. BCK_CMP_DEL < 120 ns, guaranteed by laboratory measurement, not tested in production.
22. Unless zero−cross detection stops the TOFF time on NV78763−9 device.
23. The voltage at LBCKSWx pin when the comparator toggles, rising edge.

Table 16. 5V TOLERANT DIGITAL INPUTS (SCLK, CSB, SDI, LEDCTRL1, LEDCTRL2, BSTSYNC)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input digital in leakage current (Note 24)	R_{PULL}		40		160	kΩ
LEDCTRLx to PWM dimming propagation delay	$BUCKx_{SW_DEL}$		3.6	4	4.9	μs

24. Pull down resistor ($R_{pulldown}$) for LEDCTRLx, BSTSYNC, SDI and SCLK, pull up resistor (R_{pullup}) for CSB to VDD.

Table 17. 5V TOLERANT OPEN−DRAIN DIGITAL OUTPUT (SDO)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Low−voltage output voltage	VOUTLO	I_{out} = −10 mA (current flows into the pin)			0.4	V
Equivalent output resistance	$R_{DS(on)}$	Low−side switch		20	40	Ω
SDO pin leakage current	SDO_{ILEAK}				2	μA
SDO pin capacitance (Note 25)	SDO_{C}			10		pF
CLK to SDO propagation delay (Note 26)	SDO_{DL}	Low−side switch activation/deactivation time			320	ns

25. Guaranteed by bench measurement, not tested in production.
26. Values valid for 1 kΩ external pull−up connected to 5 V and 100 pF to GND, when in case of falling edge the voltage on the SDO pin goes below 0.5 V. This delay is internal to the chip and does not include the RC charge at pin level when the output goes to high impedance.

Table 18. 3V TOLERANT DIGITAL PINS (TST1, TST2)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
High−level input voltage	VINHI		2			V
Low−level input voltage	VINLO				0.8	V
Input leakage current TST1 pin	$TST1_{Rpulldown}$	Internal pull−down resistance	19	32	47	kΩ
Input leakage current TST2 pin	$TST2_{Rpulldown}$	Internal pull−down resistance	1.6	4	5.9	kΩ

Table 19. SPI INTERFACE

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CSB setup time	t_{CSS}		500			ns
CSB hold time	t_{CSH}		250			ns
SCLK low time	t_{WL}		500			ns
SCLK high time	t_{WH}		500			ns
Data−in (DIN) setup time	t_{SU}		250			ns
Data−in (DIN) hold time	t_H		275			ns
SDO disable time	t_{DIS}		110		320	ns
SDO valid for high lo low transition	t_{SDO_HL}				320	ns
SDO valid for low lo high transition (Note 27)	t_{SDO_LH}				320 + t(RC)	ns
SDO hold time	t_{HO}		110			ns
CSB high time	t_{CS}		1000			ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
27. Time depends on the SDO load and pull−up resistor.

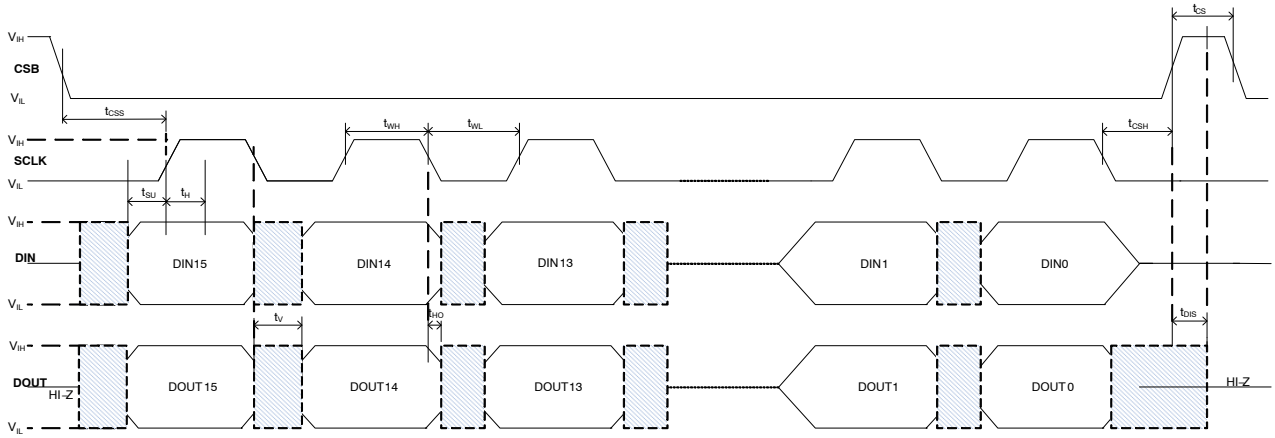


Figure 5. NCV78763 SPI Communication Timing

TYPICAL CHARACTERISTICS

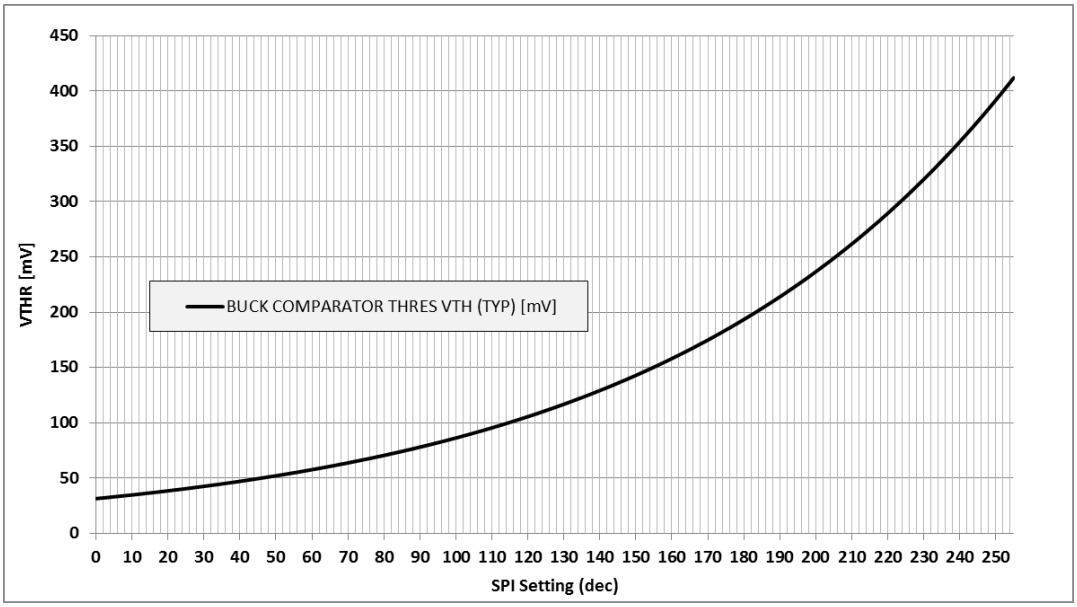


Figure 6. Buck Peak Comparator Threshold (Note 28)

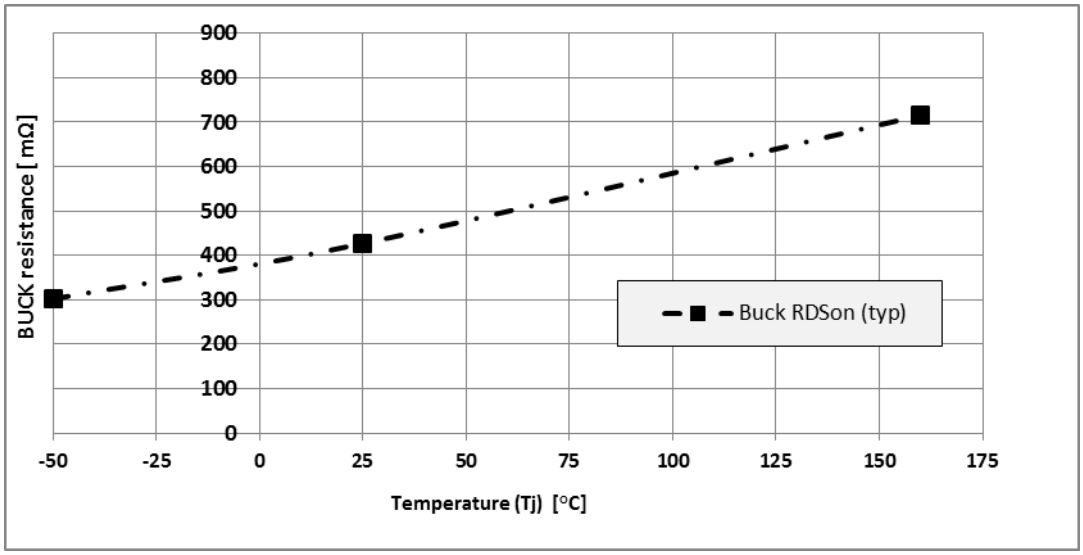


Figure 7. Buck MOSFET Typical $R_{DS(on)}$ Over Silicon Junction Temperature

28. Curve obtained by applying the typical exponential increase from the min value VTHR_000. Please see Table 15 for details.

DETAILED OPERATING AND PIN DESCRIPTION

SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78763 is designed to support power−up starting from V_{BB} = 5 V.

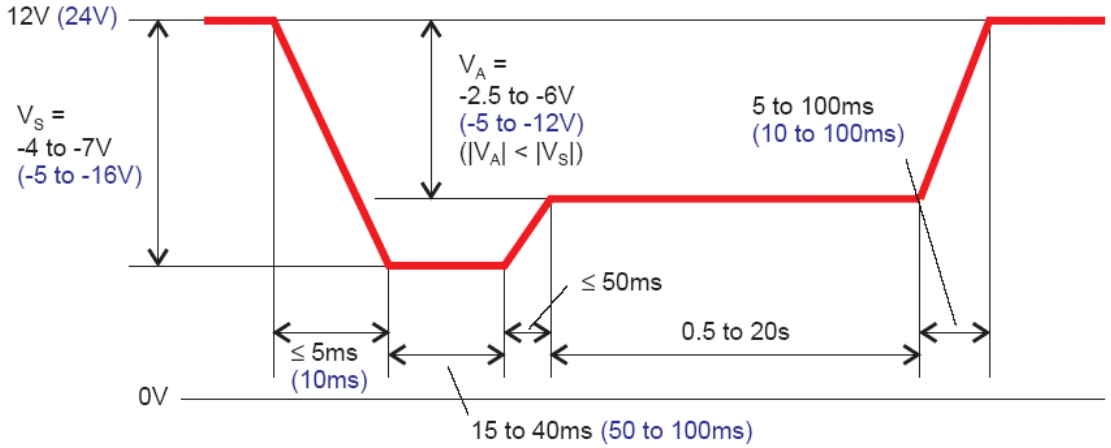


Figure 8. Cranking Pulse (ISO7637−1): System has to be Fully Functional (Grade A) from Vs = 5 V to 28 V

VDRIVE Supply

The VDRIVE supply voltage represents the power for the complete the BOOST PREDRV block, which generates the VGATE, used to switch the booster MOSFET. The voltage is programmable via SPI in 16 different values (register VDRIVE_SETPOINT[3:0], ranging from a minimum of 5 V typical to 10 V typical: see Table 6). This feature allows having the best switching losses vs. resistive losses trade off, according to the MOSFET selection in the application, also versus the minimum required battery voltage. The lowest settings can be exploited to drive logic gate drive MOSFETs. In order to support low VBB battery voltages and long crank pulse drops, the VDRIVE supply can take its energy from the source with the highest output voltage, either from (refer to Figure 1):

- the VREG10V supply, which derives its energy from the VBB input.
- the VBOOST_AUXSUP, which gets its energy from the VBOOST path. In order to enable this condition the bit VDRIVE_BST_EN[0] = 1. It is highly recommended to enable this function at module running mode in order to insure proper MOSFET gate drive even in case of large battery drop transients.

Under normal operating conditions, when the voltage headroom between VBB and VREG10V is sufficient, the gate driver energy is entirely supplied via the VBB path. In case the VBOOST_AUX regulator is enabled, it will start to draw part of the required current starting as from when the headroom reduces below the minimum requirement, then linearly increasing, until bearing 100% of the IDRIVE current when the VBB drops close or below the VDRIVE target and still enough energy can be supplied by the booster circuit. Please note that the full device functionality is not guaranteed for VBB voltages lower than 4 V and that for very low voltages a reset will be generated (see Table 7).

Note: powering the device via the VBOOST_AUXSUP will produce an extra power dissipation linked to the related linear drop (VBOOST − VBOOST_AUXSUP), which must be taken into account during the thermal design.

VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip and derives energy from VBB. Due to the low dropout regulator design, VDD is guaranteed already from low VBB voltages. The Power−On−Reset circuit (POR) monitors the VDD voltage and the VBB voltage to control the out−of−reset and reset entering state: an internal switch disconnects the VDD regulator from the VBB input as its voltage drops below the admitted threshold VBB_LOW (Table 7); this originates a VDD discharge that will result in a device reset either if the voltage falls below the PORL level or in general, if due to the drop, the VDD regulation target cannot be kept for more than typically 100 µs. At power-up, the chip will exit from reset state when VBB > VBB_LOW and VDD > PORH.

VBOOSTM3V Supply

The VBOOSTM3V is the high side auxiliary supply for the gate drive of the buck regulators' integrated high−side P−MOSFET switches. This supply receives energy directly from the VBOOSTBCK pin.

INTERNAL CLOCK GENERATION − OSC8M

An internal RC clock named OSC8M is used to run all the digital functions in the chip. The clock is trimmed in the factory prior to delivery. Its accuracy is guaranteed under full operating conditions and is independent from external component selection (refer to Table 9 for details).

ADC

General

The built−in analog to digital converter (ADC) is an 8−bit capacitor based successive approximation register (SAR). This embedded peripheral can be used to provide the following measurements to the external Micro Controller Unit (MCU):

- V_{BOOST} voltage: sampled at the VBOOST pin;
- V_{BB} voltage (linked to the battery line);
- $VLED1_{ON}$, $VLED2_{ON}$ voltages;
- VLED1 and VLED2 voltages;
- VTEMP measurement (chip temperature).

The internal NCV78763 ADC state machine samples all the above channels automatically, taking care for setting the analog MUX and storing the converted values in memory. The external MCU can readout all ADC measured values via the SPI interface, in order to take application specific decisions. Please note that none of the MCU SPI commands interfere with the internal ADC state machine sample and conversion operations: the MCU will always get the last available data at the moment of the register read.

The state machine sampling and conversion scheme is represented in the figure below.

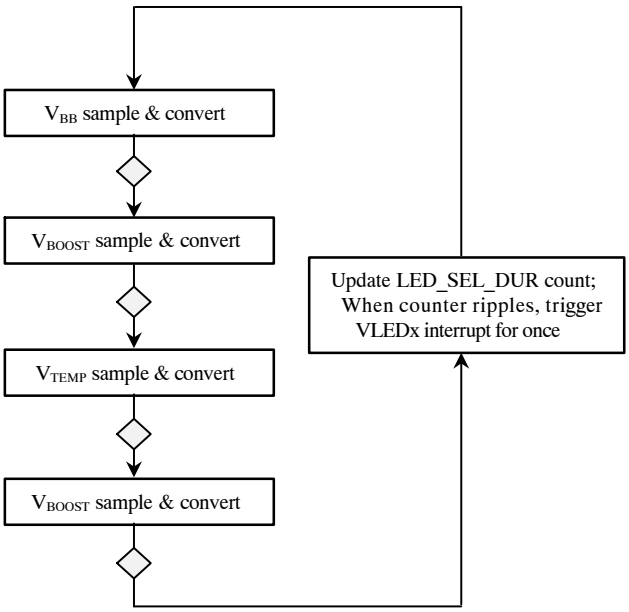


Figure 9. ADC Sample and Conversion Main Sequence

Referring to the figure above, the typical rate for a full SAR plus digital conversion per channel is 8 μs (Table 10). For instance, each new V_{BOOST} ADC converted sample occurs at 16 μs typical rate, whereas for both the V_{BB} and V_{TEMP} channel the sampling rate is typically 32 μs, that is to say a complete cycle of the depicted sequence. This time is referred to as T_{ADC_SEQ}.

If the SPI setting LED_SEL_DUR[8:0] is not zero, then interrupts for the VLEDx measurements are allowed at the points marked with a rhombus, with a minimum cadence corresponding to the number of the elapsed ADC sequences (forced interrupt). In formulas:

$$T_{VLEDx_INT_forced} = LED_SEL_DUR[8:0] \times T_{ADC_SEQ}$$

In general, prior to the forced interrupt status, the $VLEDx_{ON}$ ADC interrupts are generated when a falling edge on the control line for the buck channel "x" is detected by the device. In case of *external dimming*, this interrupt start signal corresponds to the LEDCTRLx falling edge together with a controlled phase delay (Table 16). When in *internal dimming*, the phase delay is also internally created, in relation with the falling edge of the dimming signal. The purpose of the phase delay is to allow completion the ongoing ADC conversion before starting the one linked to the VLEDx interrupt: if at the moment of the conversion LEDCTRLx pin is logic high, then the updated registers are VLEDxON[7:0] and VLEDx[7:0]; otherwise, if LEDCTRLx pin is logic low, the only register refreshed is VLEDx[7:0]. This mechanism is handled automatically by the NCV78763 logic without need of intervention from the user, thus drastically reducing the MCU cycles and embedded firmware and CPU cycles overhead that would be otherwise required.

To avoid loss of data linked to the ADC main sequence, one LED channel is served at a time also when interrupt requests from both channels are received in a row and a full sequence is required to go through to enable a new interrupt VLEDx. In addition, possible conflicts are solved by using a defined priority (channel pre−selection). Out of reset, the default selection is given to channel "1". Then an internal flag keeps priority tracking, toggling at each time between channels pre−selection. Therefore, up to two dimming periods will be required to obtain a full measurement update of the two channels. This not considered however a limitation, as typical periods for dimming signals are in the order of 1 ms period, thus allowing very fast failure detection.

A flow chart referring to the ADC interrupts is also displayed (Figure 10).

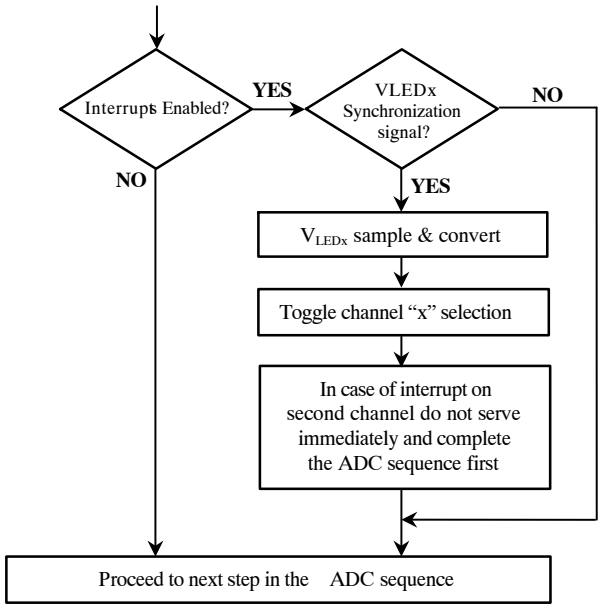


Figure 10. ADC VLEDx Interrupt Sequence

All NCV78763 ADC registers data integrity is protected by ODD parity on the bit 8 (that is to say the 9th bit if counting from the LSbit named "0"). Please refer to the SPI map section for further details.

Battery voltage ADC: V_{BB}

The battery voltage is sampled making use of the device supply V_{BB} pin. The (8−bit) conversion ratio is 40/255 (V/dec) = 0.157 (V/dec) typical. The converted value can be found in the SPI register VBB[7:0], with ODD parity protection bit in VBB[8]. The external MCU can make use of the measured VBB value to monitor the status of the module supply, for instance for a power de−rating algorithm.

Boost voltage ADC: V_{BOOST}

This measure refers to the boost voltage at the VBOOST pin, with an 8 bit conversion ratio of 70/255 (V/dec) = 0.274 (V/dec) typical, inside the SPI register VBOOST[7:0]. This measurement can be used by the MCU for diagnostics and booster control loop monitoring. The measurement is protected by parity (ODD) in bit VBOOST[8].

Device Temperature ADC: V_{TEMP}

By means of the VTEMP measurement, the MCU can monitor the device junction temperature (T_J) over time. The conversion formula is:

$$T_J = (VTEMP[7:0](dec) - 20)[^\circ C]$$

VTEMP[7:0] is the value read out directly from the related 8bit−SPI register (please refer to the SPI map). The value is also used internally by the device to for the *thermal warning* and *thermal shutdown* functions. More details on these two can be found in the dedicated sections in this document. The parity protection (ODD) is found on bit VTEMP[8].

LED String Voltages ADC: V_{LEDx}, V_{LEDxON}

The voltage at the pins VLEDx (1, 2) is measured. Their conversion ratio is 70/255 (V/dec) = 0.274 (V/dec) typical. This information, found in registers VLEDxON[7:0] and VLEDx[7:0], can be used by the MCU to infer about the LED string status. For example, individual shorted LEDs, or dedicated Open string and short to GND or short to battery algorithms. As for the other ADC registers, the values are protected by ODD parity, respectively in VLEDxON[8] and VLEDx[8].

Please note that in the case of constant LEDCTRLx inputs and no dimming (in other words dimming duty cycle equals to 0% or 100%) the VLEDx interrupt is forced with a rate equal to $T_{VLEDx_INT_forced}$, given in the ADC general section. This feature can be exploited by MCU embedded algorithm diagnostics to read the LED channels voltage even when in OFF state, before module outputs activation (module startup pre−check).

BOOSTER REGULATOR

General

The NCV78763 features one common booster stage for the two high−current integrated buck current regulators. In addition, optional external buck regulators, belonging to other NCV78x63 devices, can be cascaded to the same boost voltage source as exemplified in the picture below.

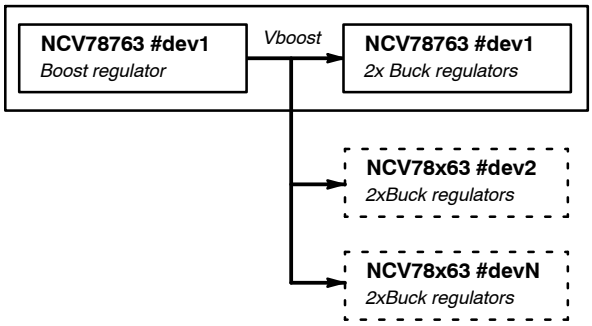


Figure 11. Cascading Multiple NCV78x63 Buck Channels on a Common Boost Voltage Source

The booster stage provides the required voltage source for the LED string voltages out of the available battery voltage. Moreover, it filters out the variations in the battery input current in case of LED strings PWM dimming.

For nominal loads, the boost controller will regulate in *continuous mode* of operation, thus maximizing the system power efficiency at the same time having the lowest possible input ripple current (with “continuous mode” it is meant that the supply current does not go to zero while the load is activated). Only in case of very low loads or low dimming duty cycle values, *discontinuous mode* can occur: this means the supply current can swing from zero when the load is off, to the required peak value when the load is on, while keeping the required input average current through the cycle. In such situations, the total efficiency ratio may be lower than the theoretical optimal. However, as also the total losses will at the same time be lower, there will be no impact on the thermal design.

On top of the cascaded configuration shown in the previous figure, the booster can be operated in *multi−phase mode* by combining more NCV78763 in the application. More details about the multiphase mode can be found in the dedicated section.

Booster Regulation Principles

The NCV78763 features a *current−mode* voltage controller, which regulates the V_{BOOST} line used by the buck converters. The regulation loop principle is shown in the following picture. The loop compares the reference voltage ($V_{BOOST_SETPOINT}$) with the actual measured voltage at the V_{BOOST} pin, thus generating an error signal which is treated internally by the error trans−conductance amplifier (block A1). This amplifier transforms the error voltage into current by means of the trans−conductance gain G_m. The amplifier’s output current is then fed into the external compensation network impedance (A2), so that it originates a voltage at the V_{COMP} pin, this last used as a reference by the current control block (B).

The current controller regulates the duty cycle as a consequence of the V_{COMP} reference, the sensed inductor peak current via the external resistor R_{SENSE} and the slope compensation used. The power converter (block C) represents the circuit formed by the boost converter externals (inductor, capacitors, MOSFET and forward diode). The load power (usually the LED power going via the buck converters) is applied to the converter.

The controlled variable is the boost voltage, measured directly at the device VBOOST pin with a unity gain feedback (block F). The picture highlights as block G all the elements contained inside the device. The regulation parameters are flexibly set by a series of SPI commands indicated in Tables 11 and 12. A detailed internal boost controller block diagram is presented in the next section.

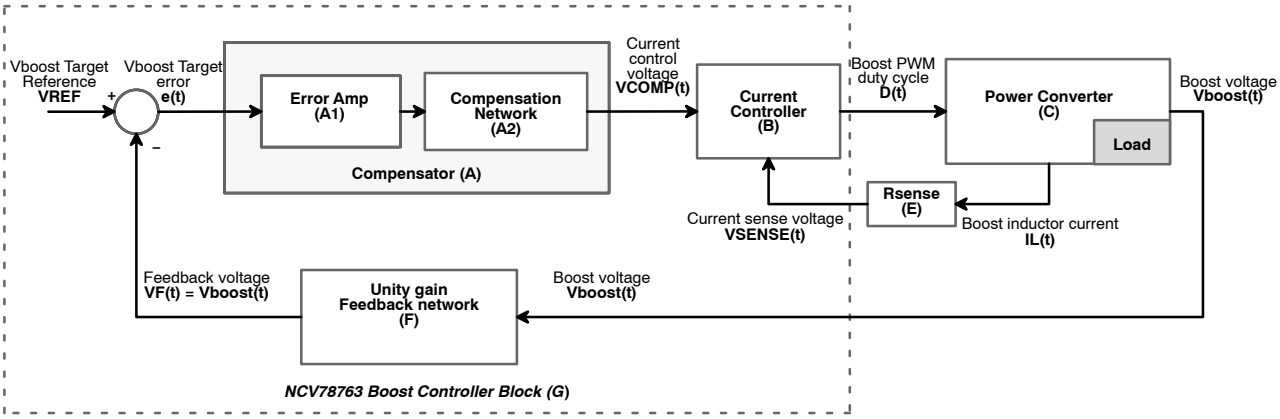


Figure 12. NCV78763 Boost Control Loop − Principle Block Diagram

Boost Controller Detailed Internal Block Diagram

A detailed NCV78763 boost controller block diagram is provided in this section. The main signals involved are indicated, with a particular highlight on the SPI programmable parameters.

The blocks referring to the principle block diagram are also indicated. In addition, the *protection specific* blocks can be found (see dedicated sections for details).

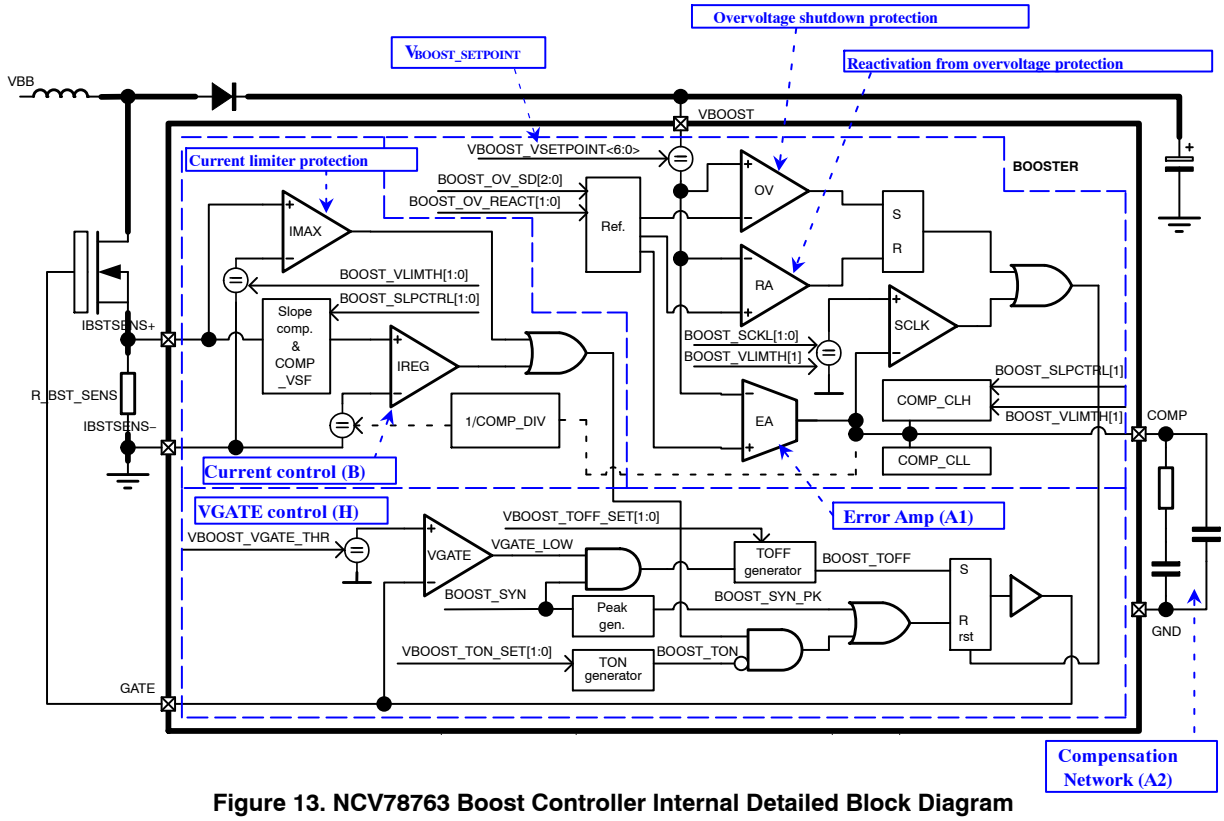


Figure 13. NCV78763 Boost Controller Internal Detailed Block Diagram

Booster Regulator Setpoint ($V_{BOOST_SETPOINT}$)

The booster voltage V_{BOOST} is regulated around the target programmable by the 7−bit SPI setting VBOOST_SETPOINT[6:0], ranging from a minimum of 11 V to a maximum of typical 64.1 V (please refer to Table 11 for details). Due to the step−up only characteristic of any boost converter, the boost voltage cannot obviously be lower than the supply battery voltage provided. Therefore a target of 11 V would be used only for systems that require the activation of the booster in case of battery drops below the nominal level.

At power−up, the booster is disabled and the setpoint is per default the minimum (all zeroes).

Booster Overvoltage Shutdown Protection

An integrated comparator monitors V_{BOOST} in order to protect the external booster components and the led driver device from overvoltage. When the voltage rises above the threshold defined by the sum of the $V_{BOOST_SETPOINT}$ (VBOOST_SETPOINT[6:0]) and the overvoltage shutdown value (BOOST_OV_SD[2:0]), the MOSFET gate is switched−off at least for the current PWM cycle and at the same time, the boost overvoltage flag in the status register will be set (BOOST_OV = 1), together with the BOOST_STATUS flag equals to zero. The PWM runs again as from the moment the V_{BOOST} will fall below the reactivation hysteresis defined by the BOOST_OV_REACT[1:0] SPI parameter. Therefore, depending on the voltage drop and the PWM frequency, it might be that more than one cycle will be skipped. A graphical interpretation of the protection levels is given in the figure below, followed by a summary table (Table 20).

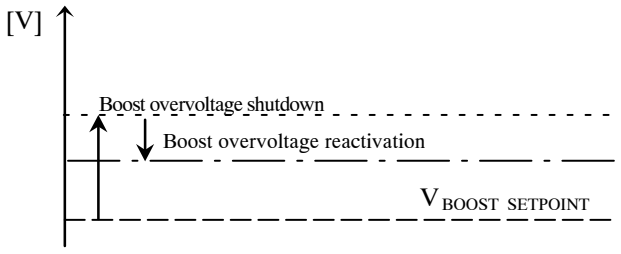


Figure 14. Booster Voltage Protection Levels with Respect to the Setpoint

Table 20. NCV78763 BOOSTER OVERVOLTAGE PROTECTION LEVELS AND RELATED SPI DIAGNOSTICS

ID	Description	PWM VGATE Condition	SPI FLAGS	
			BOOST_STATUS	BOOST_OV
A	$V_{BOOST} < V_{BOOST_SETPOINT}$	Normal (not disabled)	1	0
B	$V_{BOOST} > V_{BOOST_SETPOINT}$ + BOOST_OV_SD	Disabled until case “C”	0	1 (latched)
C	$V_{BOOST} < V_{BOOST_SETPOINT}$ + BOOST_OV_SD BOOST_OV_REACT	Re−enables the PWM, normal mode resumed if from case “B”	1	1
				(latched, if read in this condition it will go back to “0”)

After POR, the BOOST_OV flag may be set at first read out. Please note that the booster overvoltage detection is also active when Booster is OFF (booster disabled by SPI related bit). Please note that the tolerances of the booster setpoint level and the booster overvoltage and reactivation are given in Table 11. When too low voltage is detected on VBOOST pin on NV78763−9 device, overvoltage will be flagged and booster stopped. It is protection in situation when VBOOST feedback is lost and undetected overvoltage could happen.

Booster Current Regulation Loop

The peak−current level of the booster is set by the voltage of the compensation pin COMP (output of the trans−conductance error amplifier, “block B” of Figure 13). This reference voltage is fed to the current comparator through a divider by 7 and compared to the voltage V_{SENSE} on the external sense resistor R_{SENSE}, connected to the pins IBSTSENSE+ and IBSTSENSE−. The sense voltage is created by the booster inductor coil current when the MOSFET is switched on and is summed up to an additional offset of +0.5 V (see $COMP_V_{SF}$ in Table 11) and on top of that a slope compensation ramp voltage is added. The slope compensation is programmable by SPI via the setting (BOOST_SLP_CTRL[1:0]) and can also be disabled. Due to the offset, current can start to flow in the circuit as $V_{COMP} > COMP_V_{SF}$.

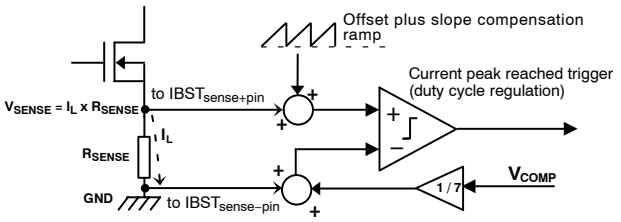


Figure 15. Booster Peak Current Regulator Involved in Current Control Loop

The maximum booster peak−current is limited by a dedicated comparator, presented in the next section.

Booster Current Limitation Protection

On top of the normal current regulation loop comparator, an additional comparator clamps the maximum physical current that can flow in the booster input circuit while the MOSFET is driven. The aim is to protect all the external components involved (boost inductor from saturation, boost diode and boost MOSFET from overcurrent, etc…). The protection is active PWM cycle−by−cycle and switches off the MOSFET GATE as V_{SENSE} reaches its maximum threshold V_{SENSE_MAX} defined by the BST_VLIMTH[1:0] register (see IMAX comparator in Figure 13 and Table 12 for more details). Therefore, the maximum allowed peak current will be defined by the ratio $I_{PEAK_MAX} = V_{SENSE_MAX} / R_{SENSE}$. The maximum current must be set in order to allow the total desired booster power for the lowest battery voltage. Warning: setting the current limit too low may generate unwanted system behavior as uncontrolled de−rating of the LED light due to insufficient power.

Booster PWM Frequency and Disable

The NCV78763 allows a flexible set of the booster PWM frequency. Two modes are available: internal generation or external drive, selectable by SPI bit setting BOOST_SRC[0]. In either case, the booster must be enabled via the dedicated SPI bit to allow PWM generation (BOOST_EN = 1). When BOOST_EN = 0, the peripheral is off and the GATE drive is disabled. Please note that the error amplifier is not shut off automatically and to avoid voltage generation on the VCOMP pin the G_m gain must be put to zero as well.

Booster PWM Internal Generation

This mode activated by BOOST_SRC = 0, creates the PWM frequency starting from the internal clock FOSC8M. A fine selection of frequencies is enabled by the register BOOST_FREQ[4:0], ranging from typical 210 kHz to typical 1 MHz (Table 11). The frequency generation is disabled by selecting the value “zero”; this is also the POR default value.

Booster PWM External Generation

When BOOST_SRC = 1, the booster PWM external generation mode is selected and the frequency is taken directly from the BOOST_SYNC device pin. There is no actual limitation in the resolution, apart from the system clock for the sampling and a debounce of two clock cycles on the signal edges. The gate PWM is synchronized with either the rising or falling edge of the external signal depending on the BOOST_SRCINV bit value. The default POR value is “0” and corresponds to synchronization to the rising flank. BOOST_SRCINV equals “1” selects falling edge synchronization.

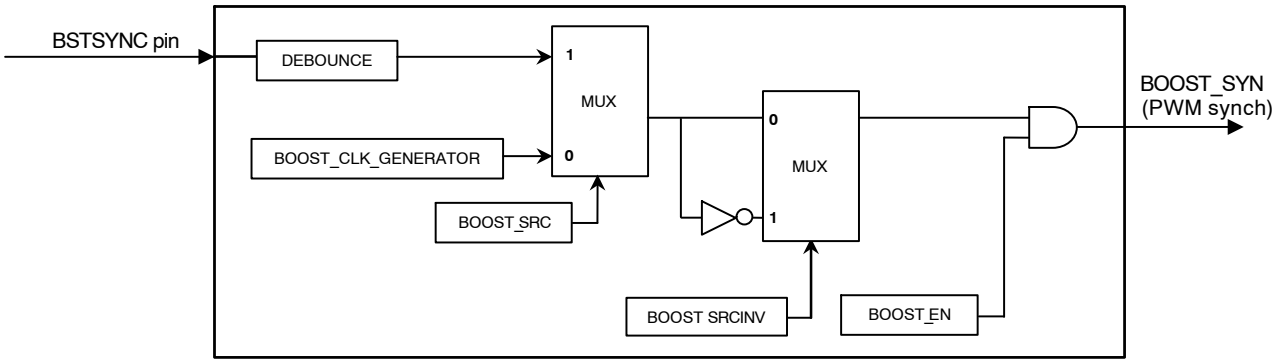


Figure 16. NCV78763 Booster Frequency Generation Block

Booster PWM Min TOFF and Min TON protection

As additional protection, the PWM duty cycle is constrained between a minimum and a maximum, defined per means of two parameters available in the device. The PWM *minimum on−time* is programmable via BOOST_TONMIN[1:0]: its purpose is to guarantee a minimum activation interval for the booster MOSFET GATE, to insure full drive of the component and avoiding switching in the linear region. Please note that this does not imply that the PWM is always running even when not required by the control loop, but means that whenever the MOSFET should be activated, then its on time would be at least the one specified. At the contrary When no duty cycle at all is required, then it will be zero.

The PWM *minimum off−time* is set via the parameter BOOST_TOFFMIN[1:0]: this parameter is limiting the maximum duty cycle that can be used in the regulation loop for a defined period T_{PWM}:

$$Duty_{MAX} = \frac{\left(T_{PWM} - T_{OFFMIN}\right)}{T_{PWM}}$$

The main aim of a maximum duty cycle is preventing MOSFET shoot−through in cases the (transient) duty cycle would get too close to 100% of the MOSFET real switch−off characteristics. In addition, as a secondary effect, a limit on the duty cycle may also be exploited to minimize the inrush current when the load is activated.

Warning: a wrong setting of the duty cycle constraints may result in unwanted system behavior. In particular, a too big T_{OFFMIN} may prevent the system to regulate the V_{BOOST} with low battery voltages (V_{BAT}). This can be explained by the simplified formula for booster *steady state continuous mode*:

$$V_{BOOST} \cong \frac{V_{BAT}}{(1 - Duty)} \Leftrightarrow Duty \cong \frac{V_{BOOST} - V_{BAT}}{V_{BOOST}}$$

So in order to reach a desired V_{BOOST} for a defined supply voltage, a certain duty cycle must be guaranteed.

Booster Compensator Model

A linear model of the booster controller compensator (block “A” Figure 13) is provided in this section. The protection mechanisms around are not taken into account. A type “2” network is taken into account at the VCOMP pin. The equivalent circuit is shown below:

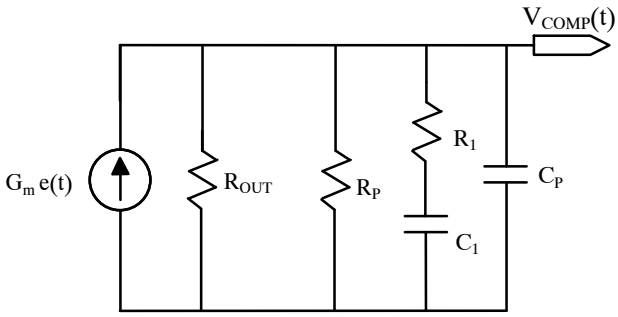


Figure 17. Booster Compensator Circuit with Type “2” Network

In the Figure, e(t) represents the control error, equals to the difference $V_{BOOST_SETPOINT}(t) - V_{BOOST}(t)$. “$G_m$” is the trans−conductance error amplifier gain, while “R_{OUT}” is the amplifier internal output resistance. The values of these two parameters can be found in Table 11 in this datasheet.

By solving the circuit in Laplace domain the following error to V_{COMP} transfer function is obtained:

$$H_{COMP}(s) = \frac{V_{COMP}(s)}{e(s)} = G_{COMP}\frac{\left(1 + \tau_1 s\right)}{\left(1 + \left(\tau_P + \tau_{1P}\right)s + \left(\tau_1 \times \tau_P\right)s^2\right)}$$

The explanation of the parameters stated in the equation above follows:

$$\begin{cases} G_{COMP} = G_m R_T \\ R_T = \dfrac{R_P \times R_{OUT}}{R_P + R_{OUT}} \\ \tau_1 = R_1 C_1 \\ \tau_P = R_T C_P \\ \tau_{1P} = \left(R_1 + R_T\right)C_1 \end{cases}$$

This transfer function model can be used for closed loop stability calculations.

Booster PWM skip cycles

In case of light booster load, it may be useful to reduce the number of effective PWM cycles in order to get a decrease of the input current inrush bursts and a less oscillating boost voltage. This can be obtained by using the “skip cycles” feature, programmable by SPI via BOOST_SKCL[1:0] (see Table 11 and SPI map). BOOST_SKCL[1:0] = ‘00’ means skip cycle disabled.

The selection defines the VCOMP voltage threshold below which the PWM is stopped, thus avoiding V_{BOOST} oscillations in a larger voltage window.

Booster Monophase or Multiphase Mode Principles

The NCV78763 booster can be operated in two main modes: *single phase* (N = 1), or “*multiphase*” (N ≥ 2).

In single phase mode, a unique NCV78763 booster is used, in the configuration shown in the standard application diagram (Figure 4).

In multiphase mode, more NCV78763 boosters can be connected together to the same V_{BOOST} node, sharing the boost capacitor block. Multiphase mode shows to be a cost effective solution in case of mid to high power systems, where bigger external BOM components would be required to bear the total power in one phase only with the same performances and total board size. In particular, the boost inductor could become a critical item for very high power levels, to guarantee the required minimum saturation current and RMS heating current.

Another advantage is the benefit from EMC point of view, due to the reduction in ripple current per phase and ripple voltage on the module input capacitor and boost capacitor. The picture below shows the (very) ideal case of 50% duty cycle, the ripple of the total module current (I_{Lmp_sum} = I_{L1mp} + I_{L2mp}) is reduced to zero. The equivalent single phase current (I_{Lsp}) is provided as a graphical comparison.

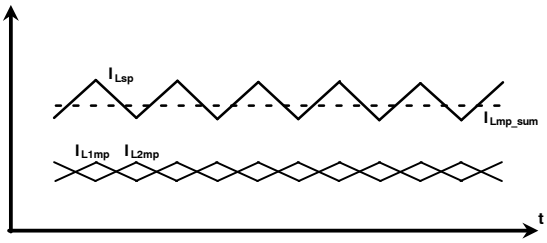


Figure 18. Booster Single Phase vs. Multiphase Example (N = 2)

Booster Multiphase Diagram and Programming

This section describes the steps both from hardware and SPI programming point of view to operate in multiphase mode. For hardware point of view, it is assumed that in multiphase mode (N boosters), each stage has the same external components. In particular, the values of the sense resistors have to match as much as possible to have a balanced current sharing. The following features have to be considered as well:

1. The compensation pin (COMP) of all boosters is connected together to the same compensation network, to equalize the power distribution of each booster. For the best noise rejection, the compensation network area has to be surrounded by the GND plane. Please refer to the PCB Layout recommendations section for more general advices.
2. To synchronize the MOSFET gate PWM clock and needed phase shifts, the boosters must use the external clock generation (BSTSYNC), generated by the board MCU or external logic, according to the user−defined control strategy. The generic number of lines needed is “N” equivalent to the number of stages. Please note that in case of a bi−phase system (N = 2) and an electrical phase shift of 180°, it is possible to use only one external clock line, exploiting the integrated NCV78763 features: the slave device shall have BOOST_SRCINV bit to “1” (clock polarity internal inversion active), whereas the master device will keep the BOOST_SRCINV bit to “0” (= no inversion, default).
3. Only the master booster error amplifier OTA must be active, while the other (slave) boosters must have all their own OTA block disabled (BOOST_OTA_GAIN[1:0] = ‘00’). For each of the devices in the chain, the register BOOST_MULTI_MD[1:0] must be kept to zero, default (‘00’)
4. In order to let the slave device(s) detect locally the boost over-voltage condition thus disabling the correspondent phase, the slave(s) must have the same (or higher) booster overvoltage shutdown level of the master device (see also section “Booster overvoltage shutdown protection” for more details on the protection mechanism and threshold). The MCU shall monitor the BOOST_OV flags to insure that all devices are properly operating in the application.

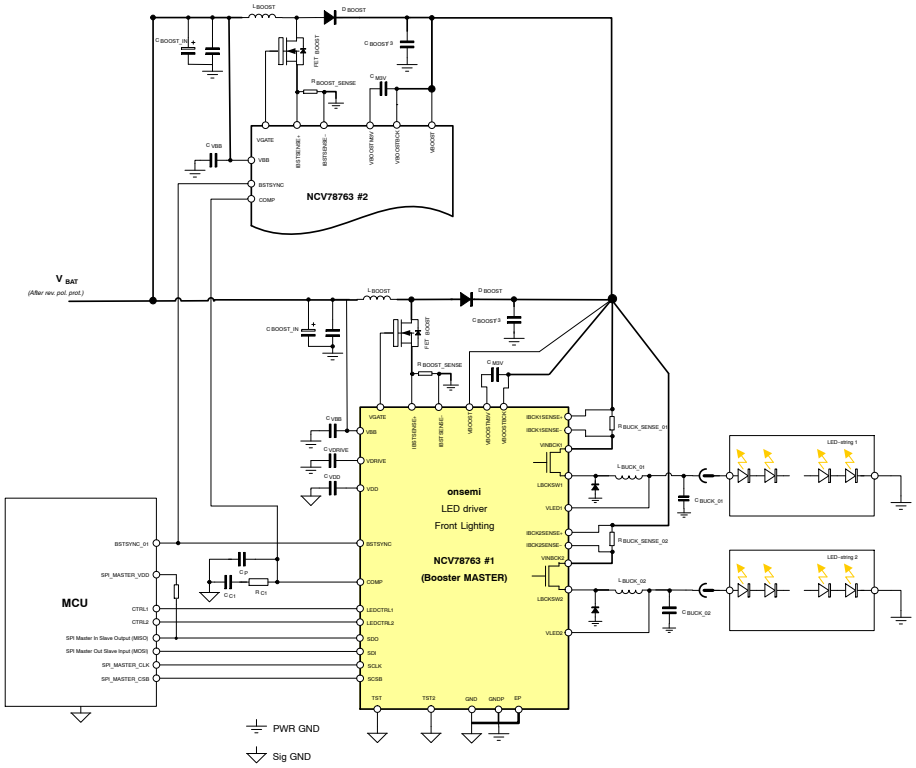


Figure 19. Booster Bi−phase Application Diagram (N = 2)

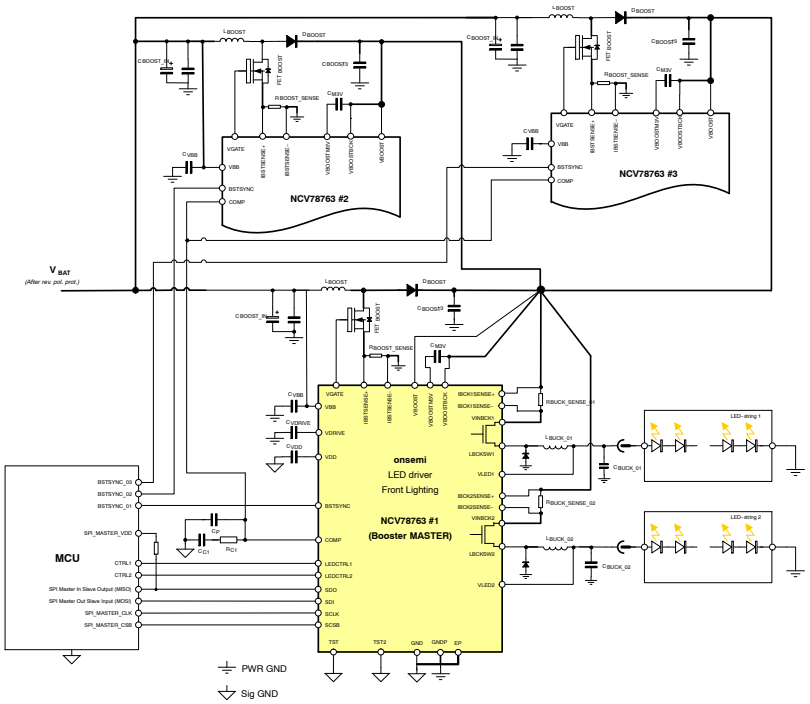


Figure 20. Booster Three−Phase Application Diagram (N = 3)

Booster Enable Control

The NCV78763 booster can be enabled/disabled directly by SPI via the bit BOOST_EN[0]. The enable signal is the transition from “0” to “1”; the disable function is vice−versa. The status of the physical activation is contained in the flag BOOST_STATUS: whenever the booster is running, the value of the flag is one, otherwise zero. It might in fact happen that despite the user *wanted* activation, the booster is stopped by the device in two main cases:

A Whenever the boost overvoltage detection triggers in the control loop. The booster is automatically activated when the voltage falls below the hysteresis (Figure 14).

B When a voltage setpoint level plus overvoltage protection higher than the maximum allowed by the max ratings is entered, to avoid electrical damage. In other notations, the following relation must be respected to avoid disabling the booster by wrong SPI setting:
{65 V − (127 − BOOST_VSETPOINT[6:0]) x 0.4 V + BOOST_OV_SD [V]} >
{67.8 V + (1 − 2 x VBOOST_OFF_COMP[3]) x 0.4 V x VBOOST_OFF_COMP[2:0]}

The value in register VBOOST_OFF_COMP[3:0] Is stored by factoring trimming by **onsemi**, individually per each device, to achieve maximum accuracy with respect to the maximum voltage setting allowed.

BUCK REGULATOR

General

The NCV78763 contains two high−current integrated buck current regulators, which are the sources for the LED strings. The bucks can be powered by the device own boost regulator, or by a booster regulator linked to another NCV78x63 device. Each buck controls the individual inductor peak current (I_{BUCK_peak}) and incorporates a constant ripple (ΔI_{BUCK_pkpk}) control circuit to ensure also stable average current through the LED string, independently from the string voltage. The buck average current is in fact described by the formula:

$$I_{BUCKAVG} = I_{BUCKpeak} - \frac{\Delta I_{BUCKpkpk}}{2}$$

This is graphically exemplified by Figure 21:

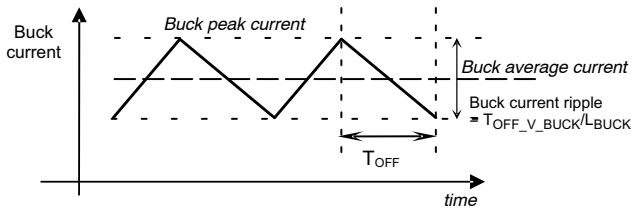


Figure 21. Buck Regulator Controlled Average Current

The parameter I_{BUCK_peak} is programmable through the device by means of the internal comparator threshold (V_{THR}, Table XX) over the external sense resistor R_{BUCK}:

$$I_{BUCKpeak} = \frac{V_{THR}}{R_{BUCK}}$$

The formula that defines the total ripple current over the buck inductor is also hereby reported:

$$\Delta I_{BUCKpkpk} = \frac{T_{OFF} \times (V_{LED} + V_{DIODE})}{L_{BUCK}}$$

$$\cong \frac{T_{OFF} \times V_{LED}}{L_{BUCK}} = \frac{T_{OFF_VLED_i}}{L_{BUCK}}$$

In the formula above, T_{OFF} represents the buck switch off time, V_{LED} is the LED voltage feedback sensed at the NCV78763 $VLED_X$ pin and L_{BUCK} is the buck inductance value. The parameter $T_{OFF_VLED_i}$ is programmable by SPI (BUCKx_TOFFVLED[3:0]), with values related to Table 15. In order to achieve a constant ripple current value, the device varies the T_{OFF} time inversely proportional to the V_{LED} sensed at the device pin, according to the selected factor $T_{OFF_VLED_i}$. On NV78763−9 device TOFF time is inversely proportional to voltage over the inductor (VLED + VDIODE) what will result in more accurate ripple for low VLED voltages. As a consequence to the constant ripple control and variable off time, the buck switching frequency is dependent on the boost voltage and LED voltage in the following way:

$$f_{BUCK} = \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \times \frac{1}{T_{OFF}}$$

$$= \frac{(V_{BOOST} - V_{LED})}{V_{BOOST}} \times \frac{V_{LED}}{T_{OFF_VLED_i}}$$

The LED average current in time (DC) is equal to the buck time average current. Therefore, to achieve a given LED current target, it is sufficient to know the buck peak current and the buck current ripple. A rule of thumb is to count a minimum of 50% ripple reduction by means of the capacitor C_{BUCK} and this is normally obtained with a low cost ceramic component ranging from 100 nF to 470 nF (such values are typically used at connector sides anyway, so this is included in a standard BOM). The following figure reports a typical example waveform:

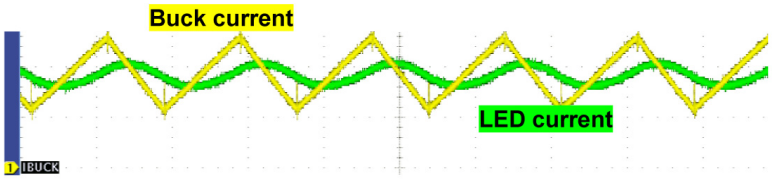


Figure 22. LED Current AC Components Filtered Out by the Output Impedance (oscilloscope snapshot)

The use of C_{BUCK} is a cost effective way to improve EMC performances without the need to increase the value of L_{BUCK}, which would be certainly a far more expensive solution.

The complete buck circuit diagram follows:

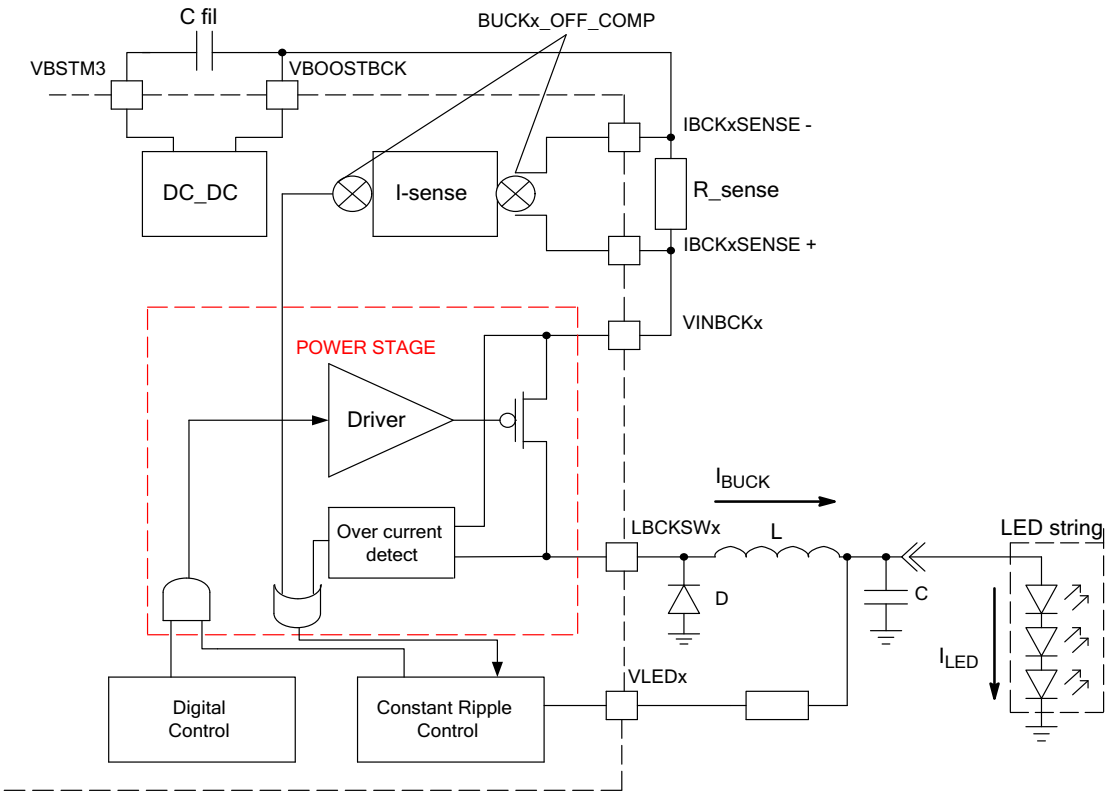


Figure 23. Buck Regulator Circuit Diagram

Different buck channels can be paralleled at the module output (after the buck inductors) for *higher current capability* on a unique channel, summing up together the individual DC currents. Please note that for each channel, the maximum buck allowed peak current is defined by the buck overcurrent detection circuit, see dedicated section for details.

In case of a *non−used* "x" channel, it is suggested to short circuit together the pins IBCKxSENSE+, IBCKxSENSE−, VINBCKx and VBOOST. The pins LBCKSWx and VLEDx can be left open.

Buck Offset Compensation

The NCV78763 buck features a peak current offset compensation that can be enabled by the SPI parameter BUCKx_OFF_CMP_EN[0]. When this bit is "1", the offset changes polarity each buck period, so that the average effect over time on the peak current is minimized (ideally zero). As a consequence of the polarity change, the peak current is toggling between two threshold values, one high value and one low, as shown in the picture below. The related sub−harmonic frequency (half the buck switching frequency) will appear in the spectrum. This has to be taken into account from EMC point of view. The use of the offset cancellation is very effective in case of high precision levels for low currents.

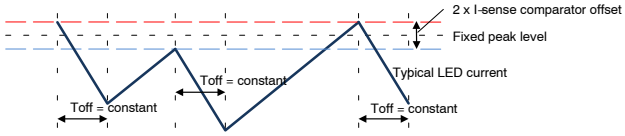


Figure 24. Buck Offset Compensation Feature

Buck Overcurrent Protection

Being a current regulator, the NCV78763 buck is by nature preventing overcurrent in all normal situations. However, in order to protect the system from overcurrent even in case of failures, two main mechanisms are available:

1. Internal sensing over the buck switch: when the peak current rises above the maximum limit (situated above 1.9 A, see Table 14), an internal counter starts to increment at each period, until the count written in BUCKx_OC_OCCMP_COUNT[2:0]+1 is attained. The count is reset if the buck channel is disabled and also at each dimming cycle. From the

moment the count is reached onwards, the buck is kept continuously off, until the SPI error flag OCLEDx is read. After reading the flag, the buck channel “x” is automatically re−enabled and will try to regulate the current again. The failure related to this protection mechanism is a short circuited sense resistor on the “x” channel. In these conditions in fact the voltage drop over the sensing element (short circuit) will be very low even in case of high currents.

2. Sensed voltage “I−sense” above the threshold: when the voltage produced over the sense resistor exceeds the desired threshold, another protection counter increases at each switching period, until the count defined by the SPI setting BUCKx_OC_ISENSCMP_COUNT[6:0]+1 is reached. As for the previous protection, the count is reset if the buck channel is disabled and also at each dimming cycle. The failure linked to this protection mechanism is a short circuit at the LED channel output and at the same time, a wrong feedback voltage at the VLEDx pin (or higher than the short circuit detection voltage typical 1.8 V, $VLED_{_LMT}$ in Table 15).

DIMMING

General

The NCV78763 supports both analog and digital dimming (or so called *PWM dimming*). Analog dimming is performed by controlling the LED amplitude current during operation. This can be done by means of changing the peak current level and/or the Toff_VLED_i constants by SPI commands (see Buck Regulator section).

In this section, we only describe PWM dimming as this is the preferred method to maintain the desired LED color temperature for a given current rating. In PWM dimming, the LED current waveform frequency is constant and the duty cycle is set according to the required light intensity. In order to avoid the *beats effect,* the dimming frequency should be set at “high enough” values, typically above 300 Hz.

The device handles two distinct PWM dimming modes: *external* and *internal*, depending on the SPI parameter DIM_SRC[1:0].

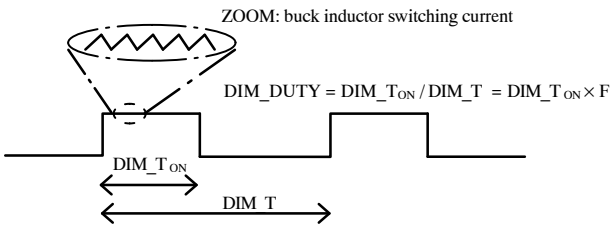


Figure 25. Buck Current Digital or PWM Dimming

External Dimming

The two independent control inputs LEDCTRLx handle the dimming signals for the related channel “x”. This mode is selected independently for buck channel ”1” by DIM_SRC[0] = 1 and for channel 2 by DIM_SRC[1] = 1. In external dimming, the buck activation is transparently linked to the logic status of the LEDCTRLx pins. The only difference is the controlled phase shift of typical 4 μs (Table 16) that allows synchronized measurements of the VLEDx pins via the ADC (see dedicated section for more details). As the phase shift is applied both to rising edges and falling edges, with a very limited jitter, the PWM duty cycle is not affected. Apart from the phase shift and the system clock OSC8M, there is no limitation to the PWM duty cycle values or resolutions at the bucks, which is a copy of the reference provided at the inputs.

Internal Dimming

This mode is selected independently for buck channel ”1” by DIM_SRC[0] = 0 and for channel “2” by DIM_SRC[1] = 0.

The register saturation value is per choice 1000 decimal, corresponding to 100% (register values between 1000 and 1023 will all provide a 100% duty cycle). Each least significant bit (lsb) change corresponds to a 0.1% duty cycle change.

The dimming PWM frequency is common between the channels and is programmable via the SPI parameter PWM_FREQ[1:0], as displayed in the table below. All frequencies are chosen sufficiently high to avoid the *beads effect* in the application. Please also note that the higher the frequency, the lower the voltage drop on the booster output due to the lower load power step.

Table 21. INTERNAL PWM DIMMING PROGRAMMABLE FREQUENCIES

PWM_FREQ[1:0]	PWM Frequency [Hz]
00	500
01	1000
10	2000
11	4000

SPI INTERFACE

General

The serial peripheral interface (SPI) allows the external microcontroller (MCU) to communicate with the device to read−out status information and to program operating parameters after power−up. The NCV78763 SPI transfer packet size is 16 bits. During an SPI transfer, the data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on

the two serial data lines: SDO and SDI. The SDO signal is the output from the Slave (LED Driver), and the SDI signal is the output from the Master.

A slave or chip select line (CSB) allows individual selection of a slave SPI device in a time multiplexed multiple−slave system.

The CSB line is active low. If an NCV78763 is not selected, SDO is in high impedance state and it does not interfere with SPI bus activities. Since the NCV78763 always clocks data out on the falling edge and samples data in on rising edge of clock, the MCU SPI port must be configured to match this operation.

The SPI CLK idles low between transferred frames. The diagram below is both a master and a slave timing diagram since CLK, SDO and SDI pins are directly connected between the Master and the Slave.

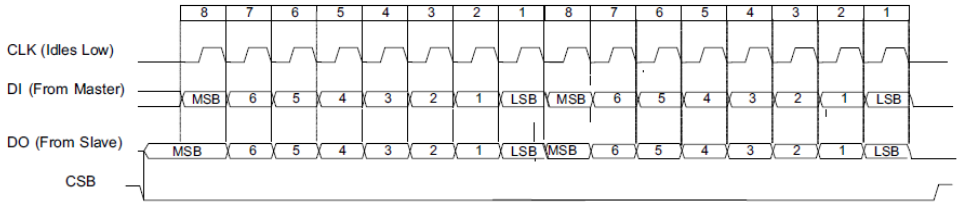


Figure 26. NCV78763 SPI Transfer Format

Note: The data transfer from the shift register into the locally used registers, interpretation of the data is only done at the rising edge of CSB.

The Data that is send over to the shift register to be transmitted to the external MCU is sampled at the falling edge of CSB, just at the moment the transmission starts.

The implemented SPI block allows interfacing with standard MCUs from several manufacturers. When interfaced, the NCV78763 acts always as a Slave and it cannot initiate any transmission. The MCU is instead the master, able to send read or write commands. The NCV78763 SPI allows connection to multiple slaves by means of both star connection (one individual CSB per Slave, while SDI, SDO, CLK are common) or by means of *daisy chain* (common CSB signal and clock, while the data lines are cascaded as in the figure). An SPI *star connection* requires a bus = (3 + N) total lines, where N is the number of Slaves used, the SPI frame length is 16 bits per communication. Regarding the SPI *daisy chain connection*, the bus width is always four lines independently on the number of slaves. However, the SPI transfer frame length will be a multiple of the base frame length so N x 16 bits per communication: the data will be interpreted and read in by the devices at the moment the CSB rises.

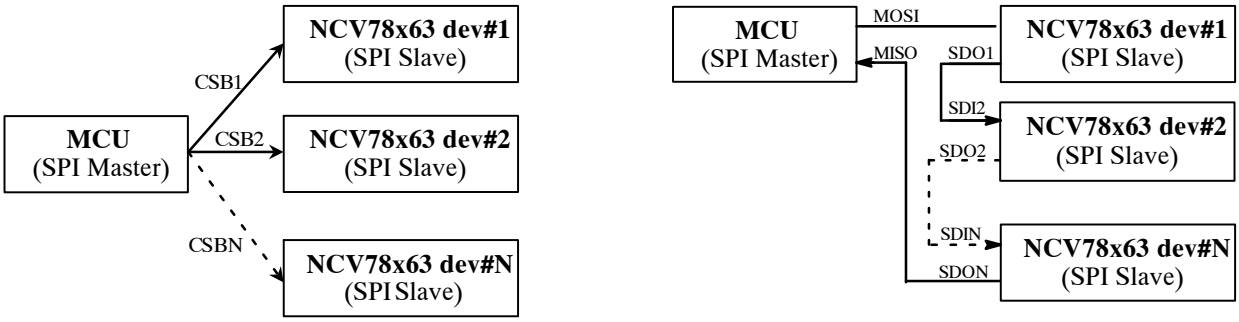


Figure 27. SPI Star vs. Daisy Chain Connection

A diagram showing the data transfer between devices in daisy chain connection is given on the right: CMDx represents the 16−bit command frame on the data input line transmitted by the Master, shifting via the chips' shift registers through the daisy chain. The chips interpret the command once the chip select line rises.

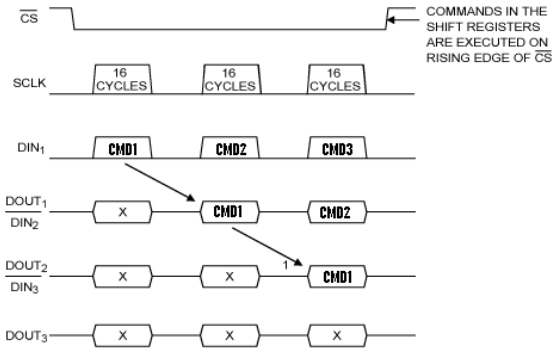


Figure 28. SPI Daisy Chain Data Shift Between Slaves. The symbol 'x' represents the previous content of the SPI shift register buffer.

The NCV78763 default power up communication mode is “star”. In order to enable daisy chain mode, a multiple of 16 bits clock cycles must be sent to the devices, while the SDI line is left to zero. Note: to come back to star mode the NOP register (address 0x0000) must be written with all ones, with the proper data parity bit and parity framing bit: see SPI protocol for details about parity and write operation.

SPI Protocol: Write / Read

Two main actions are performed by the NCV78763 SPI: *write to control register* and *read from register* (status or control). Control registers contain the parameters for the device operations to flexibly adapt to the application system requirements (control loop settings, voltage settings, dimming modes, etc…), while status registers bear the system information interpreted by the NCV78763 logic, such as diagnostics flags and ADC values. Each communication frame is protected by parity (ODD) for a more robust data transfer.

For the rest, the general transfer rules are:

- Commands and data are shifted; MSB first, LSB last.
- Each output data bit from the device into the SDO line are shifted out on the falling (detected) edge of the CLK signal;
- Each input bit on the SDI line is sampled in on the rising (detected) edge of CLK;
- Data transfer out from SDO starts with the (detected) falling edge of CSB; prior to that, the SDO open−drain transistor is High−Z (the voltage will be the one provided through the external pull−up);
- All SPI timing rules are defined by Table 19.

The frame protocol for the *write operation* is hereby provided:

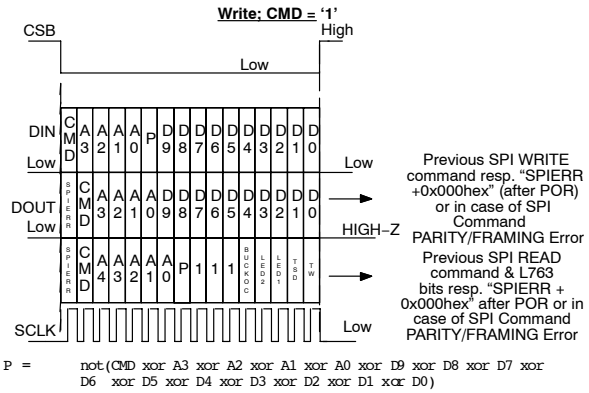


Figure 29. SPI Write Frame

Referring to the previous picture, the write frame coming from the master (into the chip SDI) is composed as follows:

- Bit [15] (msb): CMD bit = 1;
- Bits [14:11]: 4−bits WRITE ADDRESS field;
- Bit [10]: frame parity bit. It is ODD, formed by the negated XOR of all the other bits in the frame;
- Bits [9:0]: 10−bit data to write. The control register field is in fact 10 bits wide. See SPI Map for details.

Still referring to the picture, at the same time of the exchange, the device replies on the SDO line either with:

- If the previous command was a write and no SPI error had occurred, a copy of the address and data written; in case of previous SPI error, or at power−on−reset (POR), the response will be frame containing with only the msb equals to one;
- If the precedent command was a read, the response frame summarizes the address used and an overall diagnostic check (copy of the main detected errors, see diagnostic section for details).

The parity bit plays a fundamental role in each communication frame; would the parity be wrong, the NCV78763 will not store the data to the designated address and the SPIERR flag will be set.

The frame protocol for the *read operation* is:

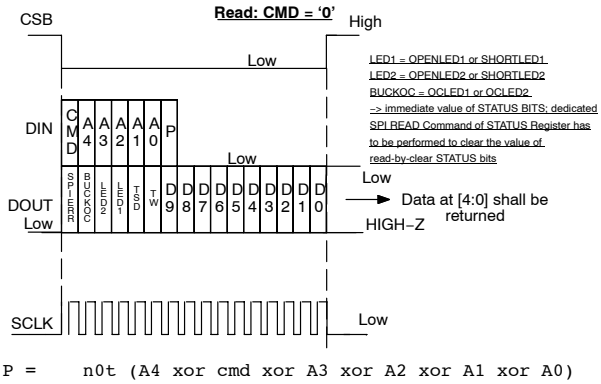


Figure 30. SPI Read Frame

Taking the figure above into account, the *read frame* coming from the master (into the chip SDI) is formed by:

- Bit [15] (msb): CMD bit = 0;
- Bits [14:10]: 5−bits READ ADDRESS field;
- Bit [9]: read frame parity bit. It is ODD, formed by the negated XOR of all the other bits in the frame;
- Bits [8:0]: 9−bits zeroes field.

The device answers immediately via the SDO in the same read frame with the register’s content thus achieving the lowest communication latency.

Note: all status registers that are ”cleared by read” (latched information) require a proper parity bit in order to execute the clearing out. Please be aware that the device will still send the information even if the parity is wrong. The MCU can still take action based on the value of the SPIERR bit. The SPIERR state can be reset only by reading the related status register. See SPI map and the next section for more details.

SPI Protocol: Framing and Parity Error

SPI communication framing error is detected by the NCV78763 in the following situations:

- Not an integer multiple of 16 CLK pulses are received during the active−low CSB signal;
- LSB bits (8..0) of a read command are not all zero;
- SPI parity errors, either on write or read operation.

Once an SPI error occurs, the SPI ERR flag can be reset only by reading the status register in which it is contained (using in the read frame the right communication parity bit).

SPI ADDRESS MAP

Starting from the left column, the table shows the address in (byte hexadecimal format), the access type (Read = R / Write = W) and the bits' indexes.

Details for the single registers are provided in the following section.

Table 22. NCV78763 SPI ADDRESS MAP

ADDR	R/W	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x00	NA	NOP register (read/write operation ignored)									
0x01	R/W	BOOST_OTA_GAIN[1:0]		BOOST_FREQ[4:0]					BOOST_SLPCTRL[1:0]		BOOST_SRC
0x02	R/W	BOOST_TOFF_MIN[1:0]		VBOOST_VGATE_THR	BOOST_SRCINV	BOOST_EN	BOOST_OV_REACT[1:0]		BOOST_OV_SD[2:0]		
0x03	R/W	VDRIVE_BST_EN	BOOST_VLIMTH[1:0]		BOOST_VSETPOINT[6:0]						
0x04	R/W	BUCK1_OFF_CMP_EN	BUCK2_OFF_CMP_EN	BUCK1_VTHR[7:0]							
0x05	R/W	BOOST_TON_MIN[1:0]		BUCK2_VTHR[7:0]							
0x06	R/W	BUCK1_TOFF_VLED[3:0]				BUCK2_TOFF_VLED[3:0]				BUCK1_EN	BUCK2_EN
0x07	R/W	BOOST_SKCL[1:0]		THERMAL_WARNING_THR[7:0]							
0x08	R/W	VDRIVE_VSETPOINT[3:0]				BOOST_MULTI_MD[1:0] / BUCK_ZCD_VLDEH_ENA[1:0]		DIM_SRC[1:0]		PWM_FREQ[1:0]	
0x09	R/W	PWM_DUTY1[9:0]									
0x0A	R/W	PWM_DUTY2[9:0]									
0x0B	R/W	BUCK1_OC_OCCMP_COUNT[2:0]			BUCK1_OC_ISENSCMP_COUNT[6:0]						
0x0C	R/W	BUCK2_OC_OCCMP_COUNT[2:0]			BUCK2_OC_ISENSCMP_COUNT[6:0]						
0x0D	R/W	0x0/BUCK_DRV_SLOW	LED_SEL_DUR[8:0]								
0x0E	R	0x0	ODD PARITY	VLED1ON[7:0]							
0x0F	R	0x0	ODD PARITY	VLED2ON[7:0]							
0x10	R	0x0	ODD PARITY	VLED1[7:0]							
0x11	R	0x0	ODD PARITY	VLED2[7:0]							
0x12	R	0x0	ODD PARITY	VTEMP[7:0]							
0x13	R	0x0	ODD PARITY	VBOOST[7:0]							
0x14	R	0x0	ODD PARITY	VBAT[7:0]							
0x15	R	0x0	ODD PARITY	BUCK1_TON_DUR[7:0]							
0x16	R	0x0	ODD PARITY	BUCK2_TON_DUR[7:0]							
0x17	R	0x0	ODD PARITY	BUCKACTIVE1	BUCKACTIVE2	OPENLED1	SHORTLED1	OCLED1	OPENLED2	SHORTLED2	OCLED2
0x18	R	0x0	ODD PARITY	BOOST_STATUS	BOOST_OV	TEST1_FAIL	LEDCTRL1VAL	LEDCTRL2VAL	SPIERR	TSD	TW
0x19	R	0x0	ODD PARITY	0x0		HWR	VBOOST_OFF_COMP[4:0]				
0x1A	R	0x0		REVID[7:0]							
OTHERS	R	0x0									

SPI REGISTERS DETAILS

ID: Register 0 /CR00: No Operation										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	NOP[9:0]									
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x00hex		**Access**: N.A. (Not Applicable)							
Bit	**Name**		**Description**							
9..0	NOP[9:0]		No Operation register. Always reads zero and cannot be written. When in daisy chain mode, trying to write all ones in the data field will force a change to SPI star mode.							

ID: Register 1 /CR01: Booster Settings 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	BOOST_OTA_GAIN[1:0]		BOOST_FREQ[4:0]					BOOST_SLPCTRL[1:0]		BOOST_SRC[0]
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x01hex		**Access**: Read/Write							
Bit	**Name**		**Description**							
9..0	BST_SET_01[9:0]		Booster Settings register, group 01: • Bit [0] – BOOST_SRC[0]: booster clock selection. When this bit equals one, external clock is selected. Otherwise, internal clock in combination with the register BOOST_FREQ[4:0]. • Bits [2:1] – BOOST_SLPCTRL[1:0]: booster slope compensation selection. • Bits [7:3] – BOOST_FREQ[4:0]: booster frequency programming with internal generation (BOOST_SRC[0] = 0) • Bits [9:8] – BOOST_OTA_GAIN[1:0]: booster error amplifier gain. Zero means output in high impedance.							

ID: Register 2 /CR02: Booster Settings 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	BOOST_MIN_TOFF[1:0]		BOOST_VGATE_THR[0]	BOOST_SRC_INV[0]	BOOST_EN[0]	BOOST_OV_REACT[1:0]		BOOST_OV_SD[2:0]		
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x02hex		**Access**: Read/Write							

Bit	Name	Description
9..0	BST_SET_02[9:0]	Booster Settings register, group 02: • Bits [2:0] – BOOST_OV_SD[2:0]: booster overvoltage shutdown. Controls the maximum allowed overshoot with respect to the regulation target. • Bits [4:3] – BOOST_OV_REACT[1:0]: booster overvoltage reactivation. Defines the hysteresis for the reactivation once the overvoltage shutdown is triggered. • Bit [5] – BOOST_EN[0]: booster enable. Controls the activation status of the booster (enabled when the bit is one). • Bit [6] – BOOST_SRC_INV[0]: booster clock inversion. Controls the polarity of the clock source (“1” = inverted). • Bit [7] – BOOST_VGATE_THR[0]: booster gate voltage threshold: defines the minimum voltage below which the MOSFET is considered off, allowing next start of the on time • Bit [9:8] – BOOST_MIN_TOFF[1:0]: booster minimum off–time setting.

ID: Register 3 /CR03: Booster Settings 03										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	VDRIVE_BST_EN[0]	BOOST_VLIMTH[1:0]		BOOST_VSETPOINT[6:0]						
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x03hex	**Access**: Read/Write								

Bit	Name	Description
9..0	BST_SET_03[9:0]	Booster Settings register, group 03: • Bits [6:0] – BOOST_VSETPOINT[6:0]: booster regulation setpoint voltage. • Bits [8:7] – BOOST_VLIMTH[1:0]: booster current limitation peak value. Defines the threshold for the current cycle by cycle peak comparator across the external sense resistor. • Bit [9] – VDRIVE_BST_EN[0]: controls the activation of the VBOOST_AUX_SUPPLY (VDRIVE powered via the booster for low battery voltages)

ID: Register 4 /CR04: Buck Settings 01											
Bit#	9	8	7	6	5	4	3	2	1	0	
Field	BUCK1_OFF_CMP_EN[0]	BUCK2_OFF_CMP_EN[0]	BUCK1_VTHR[7:0]								
Reset Value (POR)											
POR	0	0	0	0	0	0	0	0	0	0	
Address	0x04hex	**Access**: Read/Write									
Bit	**Name**	**Description**									
9..0	BCK_SET_01[9:0]	Buck Settings register, group 01: • Bits [7:0] – BUCK1_VTHR[7:0]: buck regulator channel 1 comparator threshold voltage setting. • Bit [8] – BUCK2_OFF_CMP_EN[0]: when programmed to one, the offset compensation for buck 2 is activated. • Bit [9] – BUCK1_OFF_CMP_EN[0]: when programmed to one, the offset compensation for buck 1 is activated.									

ID: Register 5 /CR05: Buck Settings 02											
Bit#	9	8	7	6	5	4	3	2	1	0	
Field	BOOST_TON_SET[1:0]		BUCK2_VTHR[7:0]								
Reset Value (POR)											
POR	0	0	0	0	0	0	0	0	0	0	
Address	0x05hex	**Access**: Read/Write									
Bit	**Name**	**Description**									
9..0	BCK_SET_02[9:0]	Buck Settings register, group 02: • Bits [7:0] – BUCK2_VTHR[7:0]: buck regulator channel 2 comparator threshold voltage setting. • Bit [9:8] – BOOST_TON_SET[1:0]: booster minimum on time setting.									

ID: Register 6 /CR06: Buck Settings 03									
Bit#	9	8	7	6	4	3	2	1	0
Field	BUCK1_TOFF_VLED[3:0]				BUCK2_TOFF_VLED[3:0]			BUCK_1_EN	BUCK_2_EN
Reset Value (POR)									
POR	0	0	0	0	0	0	0	0	0
Address	0x06hex	**Access**: Read/Write							

Bit	Name	Description
9..0	BCK_SET_03[9:0]	Buck Settings register, group 03: • Bit [0] – BUCK1_EN[0]: buck regulator channel 1 enable bit. • Bit [1] – BUCK2_EN[0]: buck regulator channel 2 enable bit. • Bits [5:2] – BUCK2_TOFF_SET[3:0]: tunes the Toff x VLED value for channel 2. • Bits [9:6] – BUCK1_TOFF_SET[3:0]: tunes the Toff x VLED value for channel 1.

ID: Register 7 /CR07: General Settings 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	BOOST_SKCL[1:0]		THERMAL_WARNING_THR[7:0]							
Reset Value (POR)										
POR	0	0	1	0	1	1	0	0	1	0
Address	0x07hex	**Access**: Read/Write								

Bit	Name	Description
9..0	GEN_SET_01[9:0]	General settings register, group 01: • Bits [7:0] – THERMAL_WARNING_THR[7:0]: thermal warning threshold setting. At POR, the register value equals the thermal shutdown value (factory trimmed) minus 10° Celsius. The formula between the SPI value and the temperature physical value is TEMP [°C] = SPI_VALUE (dec) – 20. • Bit [9:8] – BOOST_SKCL[1:0]: booster skip clock cycles setting.

ID: Register 8 /CR08: General Settings 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	VDRIVE_SETPOINT[3:0]				BOOST_MULTI_MD[1:0] / BUCK_ZCD_VLDEH_ENA[1:0]		DIM_SRC[1:0]		PWM_FREQ[1:0]	
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x08hex	**Access**: Read/Write								

Bit	Name	Description
9..0	GEN_SET_02[9:0]	General settings register, group 02: • Bits [1:0] – PWM_FREQ[1:0]: frequency selection for internal LED dimming generation. • Bits [3:2] – DIM_SRC[1:0]: dimming external vs. internal generation selection. • Bits [5:4] – BOOST_MULTI_MD[1:0]: reserved combination. Must be kept to zero. • Bits [5:4] on NV78763−9 device – BUCK_ZCD_VLDEH_ENA[1:0]: enables zero cross current comparator individually for each channel also above VLED_LMT threshold • Bits [9:6] – VDRIVE_SETPOINT[3:0]: setpoint voltage for VDRIVE regulator.

ID: Register 9 /CR09: PWM DUTY 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	PWM_DUTY_01[9:0]									
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x09hex	**Access**: Read/Write								

Bit	Name	Description
9..0	PWM_DUTY_01[9:0]	PWM duty cycle setting for channel 1: • Bits [9:0] – PWM_DUTY_01[9:0]: PWM duty cycle programming for channel 1 in case of internal dimming (1023dec = 100% duty cycle)

ID: Register 10 /CR10: PWM DUTY 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	PWM_DUTY_02[9:0]									
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x0Ahex	**Access**: Read/Write								

Bit	Name	Description
9..0	PWM_DUTY_02[9:0]	PWM duty cycle setting for channel 2: • Bits [9:0] – PWM_DUTY_02[9:0]: PWM duty cycle programming for channel21 in case of internal dimming (1023dec = 100% duty cycle)

ID: Register 11 /CR11: Overcurrent Settings 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	BUCK1_OC_OCCMP_COUNT[2:0]			BUCK1_OC_ISENSCMP_COUNT[6:0]						
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x0Bhex	**Access**: Read/Write								

Bit	Name	Description
9..0	OVC_SET_01[9:0]	Overcurrent settings register, group 01: • Bits [6:0] – BUCK1_OC_ISENSCMP_COUNT[6:0]: overcurrent via the ISENSE 1 comparator – counter settings. • Bits [9:7] – BUCK1_OC_OCCMP_COUNT[2:0]: overcurrent via internal switch 1 comparator – counter settings.

ID: Register 12 /CR12: Overcurrent Settings 02											
Bit#	9	8	7	6	5	4	3	2	1	0	
Field	BUCK2_OC_OCCMP_COUNT[2:0]			BUCK2_OC_ISENSCMP_COUNT[6:0]							
Reset Value (POR)											
POR	0	0	0	0	0	0	0	0	0	0	
Address	0x0Chex	**Access**: Read/Write									

Bit	Name	Description
9..0	OVC_SET_02[9:0]	Overcurrent settings register, group 02: • Bits [6:0] – BUCK2_OC_ISENSCMP_COUNT[6:0]: overcurrent via the ISENSE 2 comparator – counter settings. • Bits [9:7] – BUCK2_OC_OCCMP_COUNT[2:0]: overcurrent via internal switch 2 comparator – counter settings.

ID: Register 13 /CR13: LED channel sampling selection time										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0x0 / BUCK_DRV_SLOW	LED_SEL_DUR[8:0]								
Reset Value (POR)										
POR	0	0	0	0	0	0	0	0	0	0
Address	0x0Dhex	**Access**: Read/Write								

Bit	Name	Description
9..0	LED_SEL_DUR[8:0]	LED channel sampling duration • Bits [8:0] – LED_SEL_DUR[8:0]: LED sampling duration selection (linked to the ADC functioning, see details in ADC section). • Bit [9] – Not used (will be always read out as zero). • Bit [9] on NV78763−9 device – BUCK_DRV_SLOW: Slow Driver Slope Enable

ID: Register 14 / ADC 01: LED voltage ON measurement for channel 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VLED1ON[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x0Ehex	**Access**: Read only								

Bit	Name	Description
9..0	VLED1ON[8:0]	VLED channel 1 ON measurement • Bits [7:0] – VLED1ON[7:0]: LED channel 1 on measurement – byte value. • Bit [8] – VLED1ON[8]: LED channel 1 on measurement – parity bit (ODD). • Bit [9] – Not Used.

ID: Register 15 / ADC 02: LED voltage ON measurement for channel 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VLED2ON[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x0Fhex	**Access**: Read only								

Bit	Name	Description
9..0	VLED2ON[8:0]	VLED channel 2 ON measurement • Bits [7:0] – VLED2ON[7:0]: LED channel 2 on measurement – byte value. • Bit [8] – VLED2ON[8]: LED channel 2 on measurement – parity bit (ODD). • Bit [9] – Not Used.

ID: Register 16 / ADC 03: LED voltage measurement for channel 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VLED1[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x10hex	**Access**: Read only								

Bit	Name	Description
9..0	VLED1[8:0]	VLED channel 1 measurement • Bits [7:0] – VLED1[7:0]: LED channel 1 on measurement – byte value. • Bit [8] – VLED1[8]: LED channel 1 on measurement – parity bit (ODD). • Bit [9] – Not Used.

ID: Register 17 / ADC 04: LED voltage measurement for channel 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VLED2[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x11hex	**Access**: Read only								

Bit	Name	Description
9..0	VLED2[8:0]	VLED channel 2 measurement • Bits [7:0] – VLED2[7:0]: LED channel 2 on measurement – byte value. • Bit [8] – VLED2[8]: LED channel 2 on measurement – parity bit (ODD). • Bit [9] – Not Used.

ID: Register 18 / ADC 05: on−chip temperature measurement										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VTEMP[7:0]							
Reset Value (POR)										
POR	0	X	X	X	X	X	X	X	X	X
Address	0x12hex	**Access**: Read only								

Bit	Name	Description
9..0	VTEMP[8:0]	On−chip temperature measurement • Bits [7:0] − VTEMP[7:0]: on chip temperature measurement − byte value. • Bit [8] − VTEMP[8]: on chip temperature − parity bit (ODD). • Bit [9] − Not Used.

ID: Register 19 / ADC 06: boost voltage measurement										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VBOOST[7:0]							
Reset Value (POR)										
POR	0	X	X	X	X	X	X	X	X	X
Address	0x13hex	**Access**: Read only								

Bit	Name	Description
9..0	VBOOST[8:0]	Boost voltage measurement • Bits [7:0] − VBOOST[7:0]: boost voltage measurement − byte value. • Bit [8] − VBOOST[8]: boost voltage measurement − parity bit (ODD). • Bit [9] − Not Used.

ID: Register 20 / ADC 07: battery voltage measurement										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	VBB[7:0]							
Reset Value (POR)										
POR	X	X	X	X	X	X	X	X	X	X
Address	0x14hex	**Access**: Read only								

Bit	Name	Description
9..0	VBB[8:0]	Battery voltage measurement (on VBB pin) • Bits [7:0] − VBB[7:0]: battery voltage measurement − byte value. • Bit [8] − VBB[8]: battery voltage measurement − parity bit (ODD). • Bit [9] − Not Used.

ID: Register 21 / BUCK1_TON: buck 01 on−time measurements										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	BUCK1_TON_DUR[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x16hex	**Access**: Read only								

Bit	Name	Description
9..0	BUCK1_TON_DUR[8:0]	Buck 01 on−time duration measurement • Bits [7:0] − BUCK1_TON_DUR[7:0]: buck 01 on−time measurement − byte value (multiples of 250ns typ.) • Bit [8] − BUCK1_TON_DUR[8]: buck 01 on−time measurement − parity bit (ODD). • Bit [9] − Not Used.

ID: Register 22 / BUCK2_TON: buck 02 on−time measurements										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD Parity	BUCK2_TON_DUR[7:0]							
Reset Value (POR)										
POR	0	1	0	0	0	0	0	0	0	0
Address	0x16hex	**Access**: Read only								

Bit	Name	Description
9..0	BUCK2_TON_DUR[8:0]	Buck 02 on−time duration measurement • Bits [7:0] − BUCK2_TON_DUR[7:0]: buck 02 on−time measurement − byte value (multiples of 250ns typ.) • Bit [8] − BUCK2_TON_DUR[8]: buck 02 on−time measurement − parity bit (ODD). • Bit [9] − Not Used.

ID: Register 23 / Status Register 01										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD PARITY	BUCKACTIVE1	BUCKACTIVE2	OPENLED1	SHORTLED1	OCLED1	OPENLED2	SHORTLED2	OCLED2
Reset Value (POR)										
POR	0	X	0	0	0	X	0	0	X	0
Flags type (Latched = L; Non−latched = R; Not applicable = N.A.)										
Type	N.A.	R	R	R	L	L	L	L	L	L
Address	0x17hex	**Access**: R								

Bit	Name	Description
9..0	STATUS_REG_01[9:0]	Status register 01 • Bit [0] − OCLED2[0]: buck channel 02 overcurrent flag (1 = overcurrent detected) • Bit [1] − SHORTLED2[0]: buck channel 02 shorted LED string detection flag (1 = short detected) • Bit [2] − OPENLED2[0]: buck channel 02 open LED string detection flag (1 = open detected) • Bit [3] − OCLED1[0]: buck channel 01 overcurrent flag (1 = overcurrent detected) • Bit [4] − SHORTLED1[0]: buck channel 01 shorted LED string detection flag (1 = short detected) • Bit [5] − OPENLED1[0]: buck channel 01 open LED string detection flag (1 = open detected) • Bit [6] − BUCKACTIVE2[0]: buck 02 active channel flag (1 = active) • Bit [7] − BUCKACTIVE1[0]: buck 01 active channel flag (1 = active) • Bit [8] − Status 01 parity bit (ODD). • Bit [9] − Not Used.

ID: Register 24 / Status Register 02										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD PARITY	BOOST_STATUS	BOOST_OV	RESERVED	LEDCTRL1VAL	LEDCTRL2VAL	SPIERR	TSD	TW
Reset Value (POR)										
POR	0	X	0	X	X	X	X	X	X	X
Flags type (Latched = L ; Non latched = R; Not applicable = N.A.)										
Type	N.A.	R	R	L	N.A.	R	R	L	L	L
Address	0x18hex	**Access**: R								

Bit	Name	Description
9..0	STATUS_REG_02[9:0]	Status register 02 • Bit [0] − TW[0]: thermal warning flag (1 = thermal warning detected). • Bit [1] − TSD[0]: thermal shutdown flag (1 = thermal shutdown detected). • Bit [2] − SPIERR[0]: SPI error (1 = error detected). • Bit [3] − LEDCTRL2VAL[0]: LEDCTRL2 input pin logic value (1 = input high) • Bit [4] − LEDCTRL1VAL[0]: LEDCTRL1 input pin logic value (1 = input high) • Bit [5] − RESERVED[0]: reserved bit. Read as zero. • Bit [6] − BOOST_OV[0]: boost overvoltage flag (1 = overvoltage detected) • Bit [7] − BOOST_STATUS[0]: booster activation physical status (1 = active) • Bit [8] − Status 01 parity bit (ODD). • Bit [9] − Not Used.

ID: Register 25 / Status Register 03										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	ODD PARITY	0	0	HWR	VBOOST_OFF_COMP[4:0]				
Reset Value (POR)										
POR	0	X	0	0	1	X	X	X	X	X
Flags type (Latched = L ; Non latched = R; Not applicable = N.A.)										
Type	N.A.	R	N.A.	N.A.	L	R	R	R	R	R
Address	0x19hex	**Access**: R								

Bit	Name	Description
9..0	STATUS_REG_03[9:0]	Status register 02 • Bit [4:0] – VBOOST_OFF_COMP[4:0]: booster measurement compensation code (result of factory trimming) • Bit [5] – HWR: hardware reset flag (1 = device is out of reset / after power up). • Bit [7:6] – Not Used. Read as zero. • Bit [8] – Status 03 parity bit (ODD). • Bit [9] – Not Used. Read as zero.

ID: Register 26 / REVISION ID										
Bit#	9	8	7	6	5	4	3	2	1	0
Field	0	0	REVID[7:0]							
Reset Value (POR)										
POR	0	0	0	1	0	1	1	0	0	0
Flags type (Latched = L ; Non latched = R; Not applicable = N.A.)										
Type	N.A.	N.A.	R	R	R	R	R	R	R	R
Address	0x1Ahex	**Access**: R								

Bit	Name	Description
9..0	REV_ID[7:0]	Revision ID • Bit [7:0] – REV_ID[4:0]: revision ID information register. Reports the device revision number. Please note that this register is not protected by parity and it is read only. The REV ID can be exploited by the by the microcontroller to recognize the device and its revision, thus adapting the firmware parameters. • Bit [9:8] – Not Used. Read as zero.

NOTE: All other registers addresses are read only and report zeroes.
REVID[7:0] for NV78763−9 device is 0x6Ahex.

DIAGNOSTICS

The NCV78763 features a wide range of embedded diagnostic features. Their description follows. Please also refer to the previous SPI section for more details.

Diagnostics Description

- **Thermal Warning**: this mechanism detects a user−programmable junction temperature which is in principle close, but lower, to the chip maximum allowed, thus providing the information that some action (power de−rating) is required to prevent overheating that would cause Thermal Shutdown. A typical power de−rating technique consists in reducing the output dimming duty cycle in function of the temperature: the higher the temperature above the thermal warning, the lower the duty cycle. The thermal warning flag (TW) is given in STATUS register 02 and is latched. At power up the default thermal warning threshold is typically 159°C (SPI code 179).
- **Thermal Shutdown**: this safety mechanism intends to protect the device from damage caused by overheating, by disabling the booster and both buck channels, main sources of power dissipation. The diagnostic is displayed per means of the TSD bit in STATUS 02 (latched). Once occurred, the thermal shutdown condition is automatically exited when the temperature falls below the thermal warning level. The TSD flag is instead latched and cleared by SPI reading. The application thermal design should be made as such to avoid the thermal shutdown in the worst case conditions. The thermal shutdown level is not user programmable and factory trimmed (see ADC_TSD in Table 10).
- **SPI Error**: in case of SPI communication errors the SPIERR bit in STATUS 02 is set. The bit is latched. For more details, please refer to section “SPI protocol: framing and parity error”.
- **Open LEDx string**: individual open LED diagnostic flags indicate whether the “x” string is detected open. The detection is based on a counter overflow of typical 50µs when the related channel is activated. Both OPENLED1 and OPENLED2 flags (latched) are contained in STATUS 01. Please note that the open detection does not disable the buck channel(s).
- **Short LEDx string**: a short circuit detection is available independently for each LED channel per means of the flag SHORTLEDx (latched, STATUS 01). The detection is based on the voltage measured at the VLEDx pins via a dedicated internal comparator: when the voltage drops below the $VLED_{_LMT}$ minimum threshold (typical 1.8 V, see Table 15) the related flag is set. Together with the detection, a fixed TOFF is used. On NV78763−9 device, TOFF time is terminated immediately when the inductor current reaches zero. This improves the dimming behavior via external short switches (pixel control). Note that the detection is active also when the LEDx channel is off (in this case the fixed TOFF does not play any role).
- **Overcurrent on Channel x**: this diagnostics protects the LEDx and the buck channel x electronics from overcurrent. As the overcurrent is detected, the OCLEDx flag (latched, STATUS 01) is raised and the related buck channel is disabled. More details about the detection mechanisms and parameters are given in section “Buck Overcurrent Protection”.
- **Buck Active x**: these flags report the actual status of the buck channels (BUCKACTIVEx, non−latched, STATUS 01). The MCU can exploit this information in real time to check whether the channels responded to its activation commands, or at the contrary, they were for some reasons disabled.
- **Boost Status**: the physical activation of the booster is displayed by the BOOST_STATUS flag (non−latched, STATUS 01). Please note this is different from the BOOST_EN control bit, which reports instead the *willing* to activate the booster. See also section ”Booster Enable Control”.
- **Boost Overvoltage**: an overvoltage is detected by the booster control circuitry: BOOST_OV flag (latched, STATUS 01). When VBOOST feedback is lost and too low voltage is detected on VBOOST pin, overvoltage will be flagged on NV78763−9 device. More details can be found in the booster chapter.
- **LEDCTRLx pins Status**: the actual logic status read at the LEDCTRLx pin is reported by the flag LEDCTRLxVAL (non−latched, STATUS 02). Thanks to this diagnostic, the MCU can double−check the proper connection to the led driver at PCB level, or MCU pin stuck.
- **Hard Reset**: the out of reset condition is reported through the HWR bit (STATUS 03, latched). This bit is set only at each Power On Reset (POR) and indicates the device is ready to operate.

A short summary table of the main diagnostic bits related to the LED outputs follows.

Table 23. LED OUTPUTS DIAGNOSTIC TABLE SUMMARY

Diagnose		Detection Level	LED Output	Latched
Flag	**Description**			
TW	Thermal Warning	SPI register programmable	Not Disabled (if no TSD, otherwise disabled)	Yes
TSD	Thermal Shutdown	Factory trimmed	Disabled (automatically re−enabled when temp falls below TW)	Yes
OpenLEDx	LED string open circuit	BUCK ON time > BCK_TON_OPEN (50 μs typical)	Not Disabled	Yes
ShortLEDx	LED string short circuit	VLEDx < VLED_LMT	Not Disabled (buck fixed TOFF applied when output is on) (on NV78763−9 device buck fixed TOFF or Zero Cross TOFF applied when output is on)	Yes
OCLEDx	LED string overcurrent	I_Buckswitch > OCD	Disabled	Yes

PCB LAYOUT RECOMMENDATIONS

This section contains instructions for the NCV78763 PCB layout application design. Although this guide does not claim to be exhaustive, these directions can help the developer to reduce application noise impact and insuring the best system operation. All important areas are highlighted in the following picture:

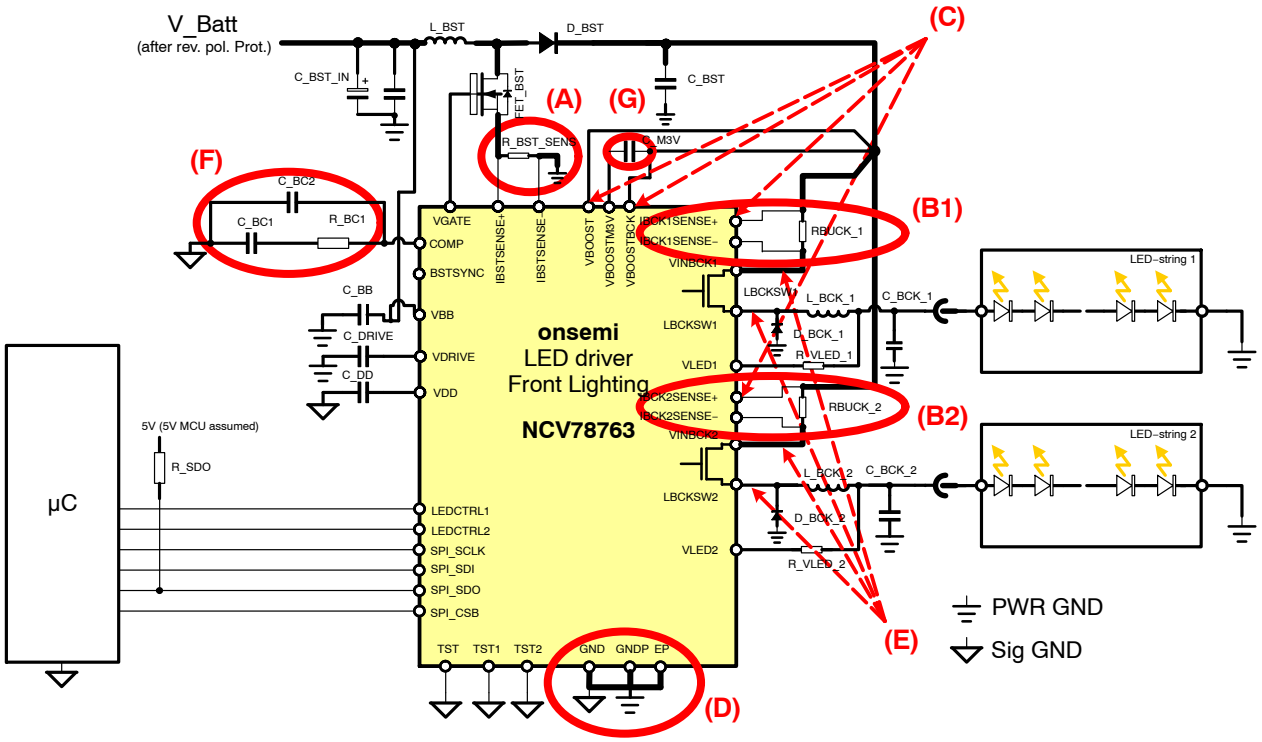


Figure 31. NCV78763 Application Critical PCB Areas

PCB Layout: Booster Current Sensing − Area (A)

The booster current sensing circuit used both by the loop regulation and the current limitation mechanism, relies on a low voltage comparator, which triggers with respect to the sense voltage across the external resistor R_BST_SENS. In order to maximize power efficiency (=minimum losses on the sense resistor), the threshold voltage is rather low, with a maximum setting of 100 mV typical. This area may be affected by the MOSFET switching noise if no specific care is taken. The following recommendations are given:

A Use a four terminals current sense method as depicted in the figure below. The measurement PCB tracks should run in parallel and as close as possible to each other, trying to have the same length. The number of vias along the measurement path should be minimized;

B Place R_BST_SENS sufficiently close to the MOSFET source terminal;
C The MOSFET's dissipation area should be stretched in a direction away from the sense resistor to minimize resistivity changes due to heating;
D If the current sense measurement tracks are interrupted by series resistors or jumpers (once as a maximum) their value should be matched and low ohmic (pair of 0 Ω to 47 Ω max) to avoid errors due to the comparator input bias currents. However, in case of high application noise, a PCB re−layout without RC filters is always recommended.
E Avoid using the board GND as one of the measurement terminals as this would also introduce errors.

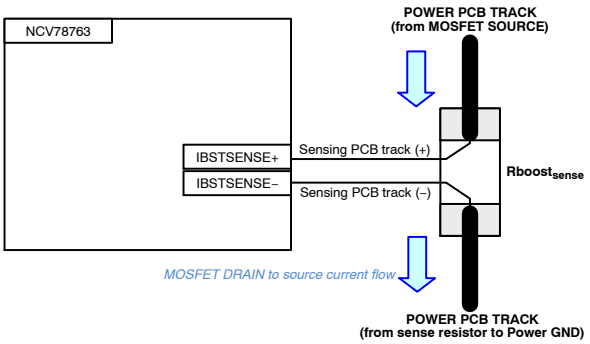


Figure 32. Four Wires Method for Booster Current Sensing Circuit

PCB Layout: Buck Current Sensing − Areas (B1) & (B2)

The blocks (B1) and (B2) control the buck peak currents by means, respectively, of the external sense resistors R_BCK1/2_SENS. As the regulation is performed with a comparator, the considerations explained in the previous section remain valid. In particular, the use of a four terminals current sense method is required, this time applied on (IBCKxSENSE+, IBCKxSENSE−). Sense resistors should be outside of the device PCB heating area in order to limit measurement errors produced by temperature drifts.

PCB Layout: Vboost related Tracks − Area (C)

The three NCV78763 device pins VBOOSTBCK, IBCK1SENSE+ and IBCK2SENSE+ must be at the same individual voltage potential to guarantee proper functioning of the internal buck current comparator (whose supply rails are VBOOSTBCK and VBOOSTM3V). In order to achieve this target, it is suggested to make a star connection between these three points, close to the device pins. The width of the tracks should be large enough (>40 mils) and as short as possible to limit the PCB parasitic parameters.

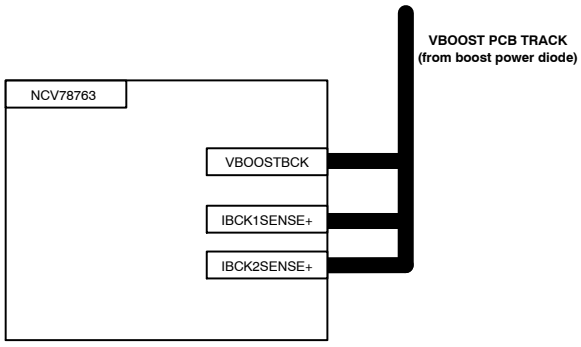


Figure 33. PCB Star Connection Between VBOOSTBCK, IBCK1SENSE+ and IBCK2SENSE+ (simplified drawing)

PCB Layout: GND Connections − Area (D)

The NCV78763 GND and GNDP pins must be connected together. It is suggested to perform this connection directly close to the device, behaving also as the cross−junction between the signal GND (all low power related functions) and the power GNDP (ground of VGATE driver). The device exposed pad should be connected to the GND plane for dissipation purposes.

It is recommended to place the VDD capacitor as close as possible to the device pins and connected with specific tracks, respectively to the VDD pin and to the GND pin (not connected to the general ground plane, to avoid ground shifts and application noise coupling directly into the chip).

PCB Layout: Buck Power Lines − Area (E)

To avoid power radiation and crosstalk between BUCK1 and BUCK2 regulators the VINBCKx and LBCKSWx tracks have to be as short as possible. They should also be symmetrical and the straightest. It is also recommended to insert a ground plate between them, especially between LBCKSW1 and LBCKSW2 track. See area "1" in the figure below.

PCB Layout: Booster Compensation Network − Area (F)

The compensation network must be placed very close to the chip and avoid noise capturing. It is recommended to connect its ground directly to the chip ground pin to avoid noise coming from other portions of the PCB ground. In addition a ground ring shall provide extra shielding ground around. See area "2" in the figure.

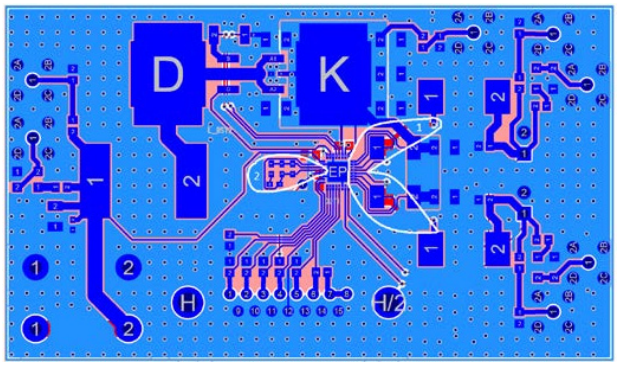


Figure 34. NCV78763 PCB Layout Example: areas (E) and (F)

PCB Layout: High Frequency Loop on Capacitors – Area (G)

All high frequency loops (with serial capacitor) have to be very short, with the capacitor as close as possible to the chip, to set the created loop antenna radiating frequency to the highest. In fact, would the tracks be too long, the loop antenna may capture a higher noise level, with the risk of downgrading the chip's performances.

PCB Layout: Additional EMC Recommendations on Loops

It is suggested in general to have a good metal connection to the ground and to keep it as continuous as possible, not interrupted by resistors or jumpers.

In additions, PCB loops for power lines should be minimized. A simplified application schematic is shown in the next figure to better focus on the theoretical explanation. When a DC voltage is applied to the VBB, at the left side of the boost inductor L_BST, a DC voltage also appears on the right side of L_BCK and on the C_BCK. However, due to the switching operation (boost and buck), the applied voltage generates AC currents flowing through the red area (1). These currents also create time variable voltages in the area marked in green (2). In order to minimize the radiation due to the AC currents in area 1, the tracks' length between L_BST and the pair L_BCK plus C_BCK must be kept low. At the contrary, if long tracks would be used, a bigger parasitic capacitance in area 2 would be created, thus increasing the coupled EMC noise level.

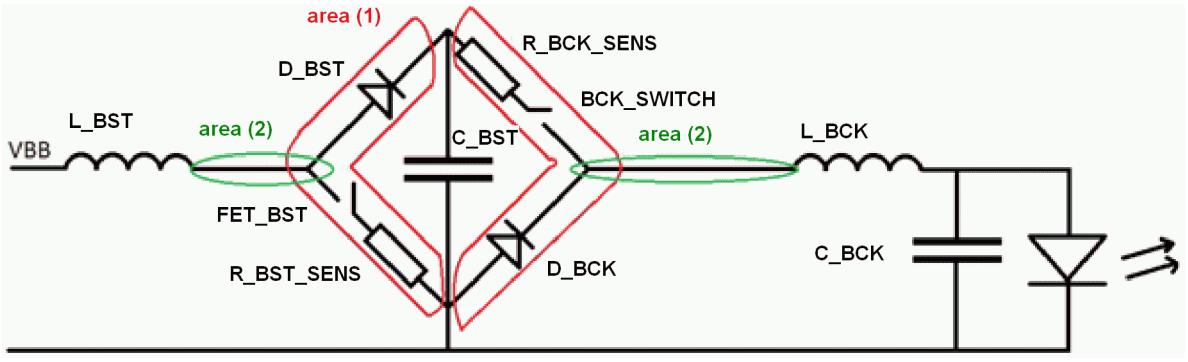


Figure 35. PCB AC Current Lines (Area 1) and AC Voltage Nodes (Area 2)

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV78763DQ9R2G (Note 34)	NV78763−9	SSOP36 EP (Pb−Free)	1500 / Tape & Reel
NCV78763DQ6AR2G (Notes 30 and 31)	NV78763−6		
NCV78763DQ6R2G (Note 30)			
NCV78763DQ0AR2G (Note 31)	NV78763−0		
NCV78763DQ0R2G			
NCV78763MW4AR2G (Notes 32 and 33)	N78763−4	QFNW32 5x5 with step−cut wettable flank (Pb−Free)	5000 / Tape & Reel
NCV78763MW0AR2G (Notes 32 and 33)	N78763−0		
NCV78763MW1AR2G (Note 33)	N78763−1	QFNW32 7x7 with step−cut wettable flank (Pb−Free)	2500 / Tape & Reel

DISCONTINUED (Note 29)

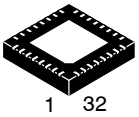
NCV78763MW4R2G (Note 32)	N78763−4	QFN32 5x5 (Pb−Free)	5000 / Tape & Reel
NCV78763MW0R2G (Note 32)	N78763−0	QFN32 5x5 (Pb−Free)	5000 / Tape & Reel
NCV78763MW1R2G	N78763−1	QFN32 7x7 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

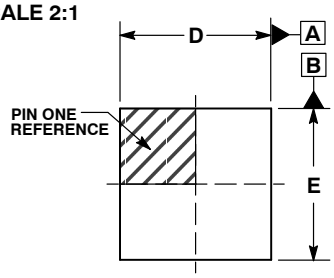
29. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.
30. Recommended for new design for improved conducted emissions in the low frequency range typically between 100 kHz and 200 kHz.
31. NCV78763DQ6AR2G & NCV78763DQ0AR2G are Dual Fab and Assembly OPNs. Please contact **onsemi** for technical details.
32. NCV78763MW4(A) & NCV78763MW0(A) have different package mold compound. Please contact **onsemi** for technical details.
33. NCV78763MW4AR2G & NCV78763MW0AR2G & NCV78763MW1AR2G are Dual Fab and Assembly OPNs. Please contact **onsemi** for technical details.
34. Recommended for new designs. Optimized for pixel/dynamic load. Improved conducted emissions around 32 kHz. NCV78763DQ9 has different package mold compound compared to NCV78763DQ0 & NCV788763DQ6. Please contact **onsemi** for technical details.

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ISSUE D

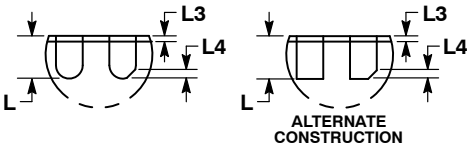
DATE 07 SEP 2018



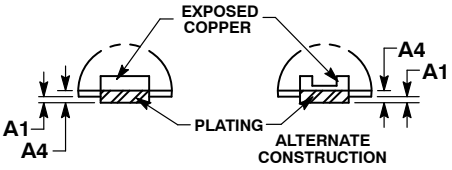
SCALE 2:1



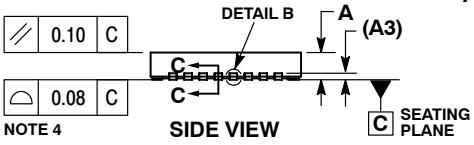
TOP VIEW



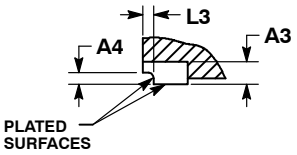
DETAIL A



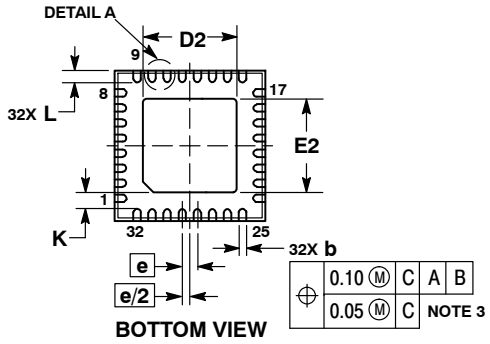
DETAIL B



SIDE VIEW



SECTION C–C

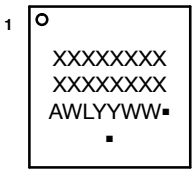


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.00	3.10	3.20
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e		0.50 BSC	
K	0.35	---	---
L	0.30	0.40	0.50
L3	---	---	0.10
L4		0.08 REF	

GENERIC MARKING DIAGRAM*

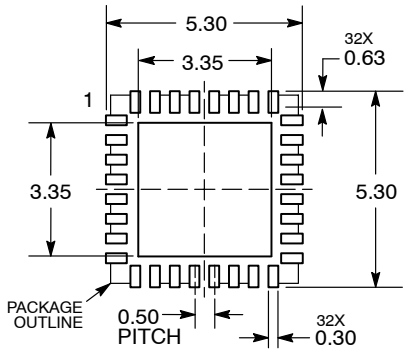


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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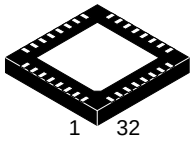
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

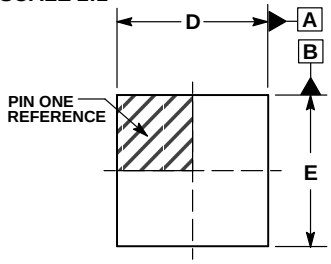
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CASE 484AG
ISSUE A

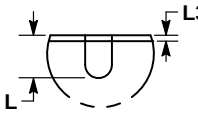
DATE 07 AUG 2018

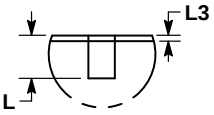


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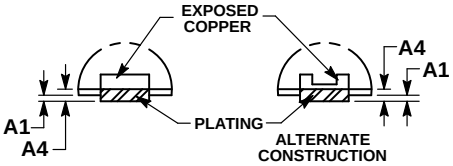


TOP VIEW

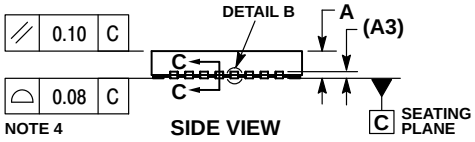




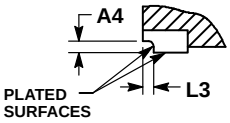
DETAIL A



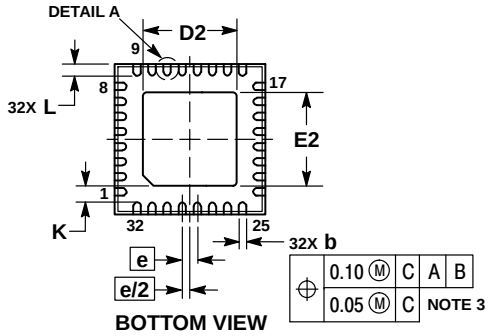
DETAIL B



SIDE VIEW



SECTION C−C

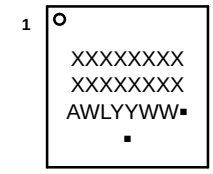


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	–––	–––	0.05
A3		0.20 REF	
A4	0.10	–––	–––
b	0.25	0.30	0.35
D	6.90	7.00	7.10
D2	4.60	4.70	4.80
E	6.90	7.00	7.10
E2	4.60	4.70	4.80
e		0.65 BSC	
K		0.60 REF	
L	0.50	0.55	0.60
L3		0.05 REF	

GENERIC MARKING DIAGRAM*

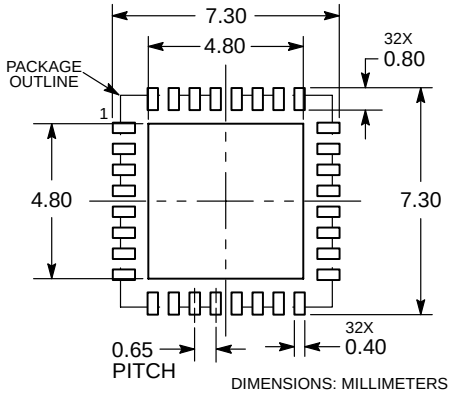


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

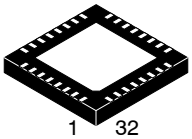
DOCUMENT NUMBER:	98AON64071G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	QFNW32 7x7, 0.65P		PAGE 1 OF 1

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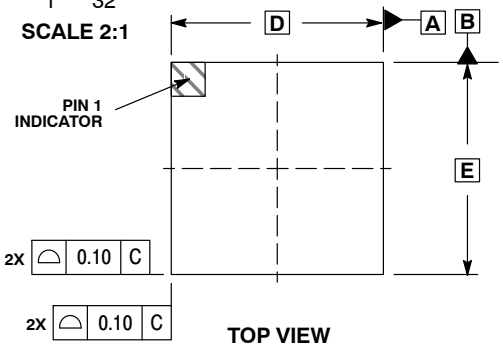
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QFN32 7x7, 0.65P
CASE 485ED
ISSUE A

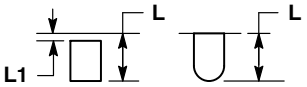
DATE 09 JUL 2015



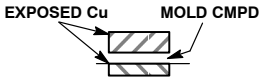
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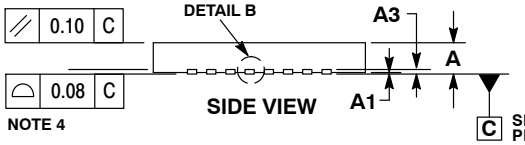
TOP VIEW

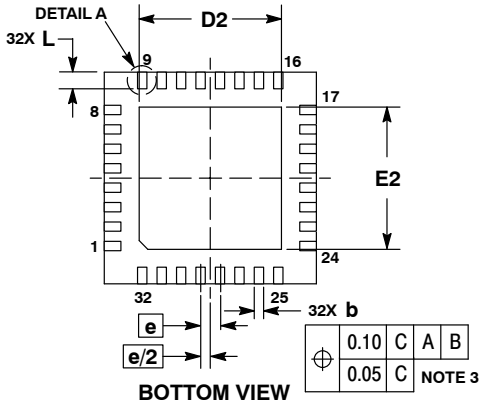


DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS



DETAIL B
ALTERNATE
CONSTRUCTION



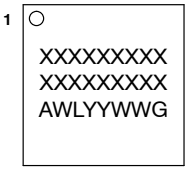


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	7.00 BSC	
D2	4.60	4.80
E	7.00 BSC	
E2	4.60	4.80
e	0.65 BSC	
L	0.45	0.65
L1	0.00	0.15

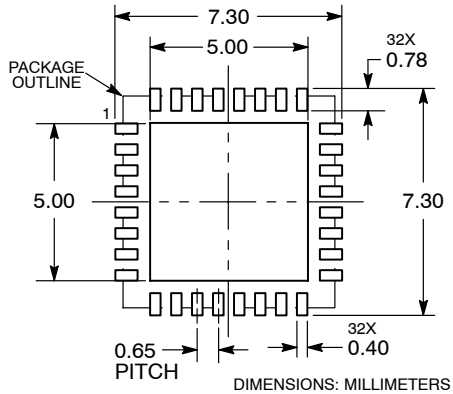
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT



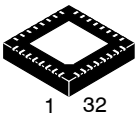
DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	**98AON23217F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN32 7X7, 0.65MM PITCH**	**PAGE 1 OF 1**

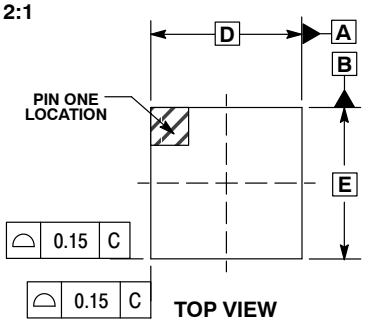
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QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

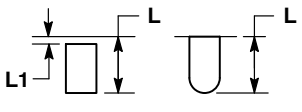
DATE 23 OCT 2013



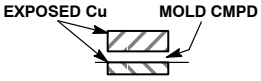
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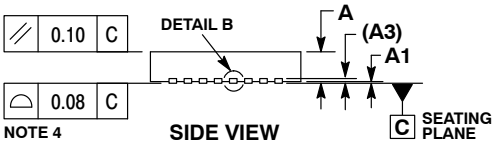
TOP VIEW



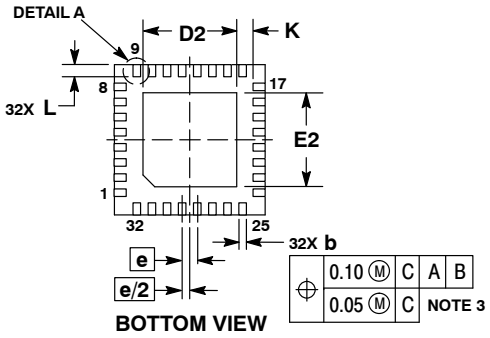
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SIDE VIEW

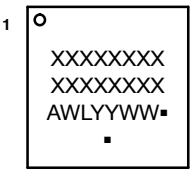


BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

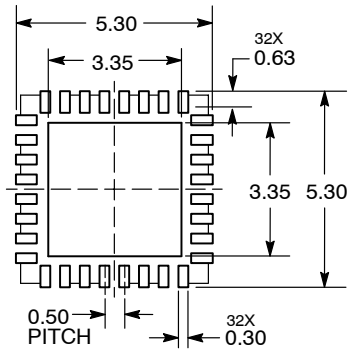


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



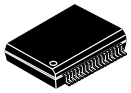
DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON20032D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN32 5x5 0.5P**	**PAGE 1 OF 1**

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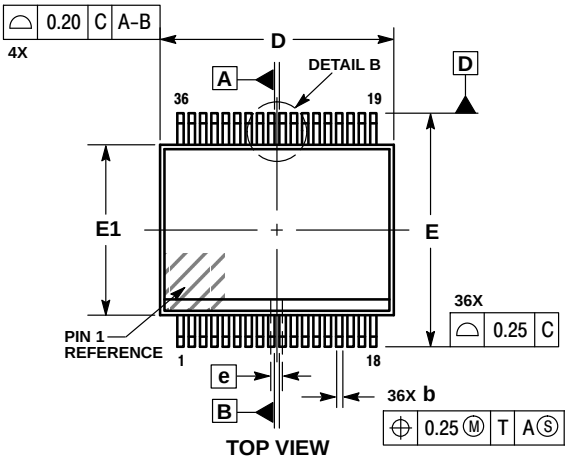
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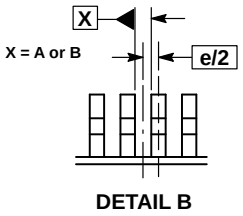


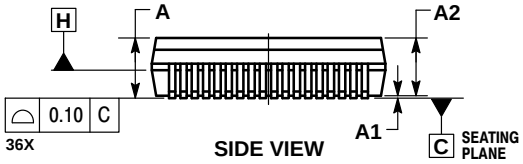
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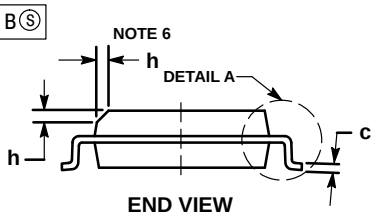
SSOP36 EP
CASE 940AB
ISSUE A

DATE 19 JAN 2016



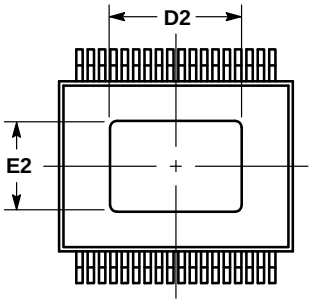


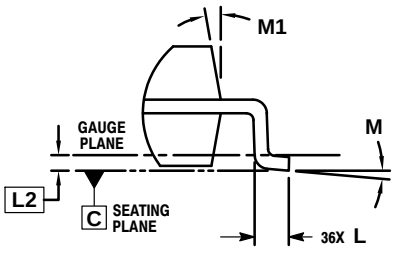




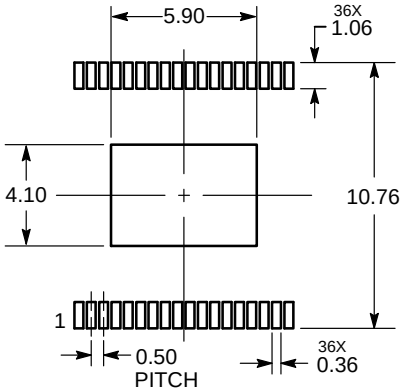
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICATED AREA.

	MILLIMETERS	
DIM	MIN	MAX
A	---	2.65
A1	---	0.10
A2	2.15	2.60
b	0.18	0.30
c	0.23	0.32
D	10.30 BSC	
D2	5.70	5.90
E	10.30 BSC	
E1	7.50 BSC	
E2	3.90	4.10
e	0.50 BSC	
h	0.25	0.75
L	0.50	0.90
L2	0.25 BSC	
M	0°	8°
M1	5°	15°



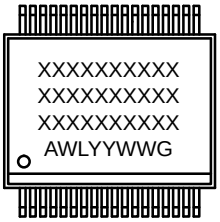


SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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