1.8 V Digital Temperature Sensor

CAT34TS00



TDFN8
VP2 SUFFIX
CASE 511AK

Description

CAT34TS00 is a low-voltage digital temperature sensor, which implements the JEDEC JC42.4 specification. CAT34TS00 measures temperature every 100 ms over a range of −20°C to +125°C, with a resolution of 12 bits.

The host communicates with the device via the serial I^2C / SMBus Interface, at either 100 kHz or 400 kHz. Temperature readings can be retrieved via serial interface. Internally, they are compared to high, low and critical trigger limits stored in device registers. Over or under limit conditions can be signaled on the open−drain EVENT pin. These limits, as well as other settings, can be configured via serial interface.

Features

- JEDEC JC42.4 Compliant Temperature Sensor
- Supply Range: 1.7 V to 1.9 V
- Temperature Range: −20°C to +125°C
- I^2C / SMBus Interface
- Temperature Sampling Rate: 100 ms max
- Temperature Reading Accuracy:
  ±0.5°C typ for Active Range (+75°C to +95°C)
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- 2 x 3 x 0.75 mm TDFN Package
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Solid State Drives
- Graphics Cards
- Portable Devices
- Process Control Equipment

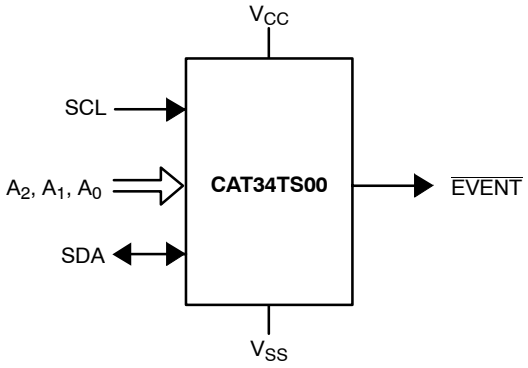
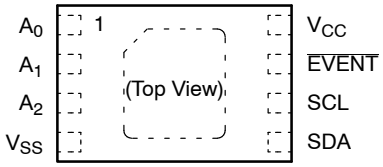


Figure 1. Functional Symbol

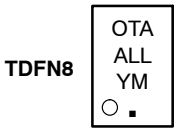
PIN CONFIGURATION



TDFN (VP2)

For the location of Pin 1, please consult the corresponding package drawing.

MARKING DIAGRAM



OTA	= Specific Device Code
A	= Assembly Location Code
LL	= Assembly Lot Number (Last Two Digits)
Y	= Production Year (Last Digit)
M	= Production Month (1 – 9, O, N, D)
▪	= Pb−Free Package
○	= Pin 1 Indicator

PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Inputs
V_{SS}	Ground
SDA	Serial Data Input / Output
SCL	Serial Clock Input
$\overline{EVENT}$	Open−drain Event Output
V_{CC}	Power Supply
DAP	Backside Exposed DAP at V_{SS}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Parameter	Rating	Unit
Voltage on any pin (except A_0) with respect to Ground (Note 3)	−0.5 to +6.5	V
Voltage on pin A_0 with respect to Ground	−0.5 to +10.5	V
Operating Temperature	−45 to +130	°C
Storage Temperature Range	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. SCL and SDA inputs can be raised to the maximum limit, irrespective of V_{CC}. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. TEMPERATURE CHARACTERISTICS

Parameter	Conditions	Typ	Max	Unit
Temperature Reading Error	+75°C ≤ T_A ≤ +95°C, active range	±0.5	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±1.0	±2.0	°C
	−20°C ≤ T_A ≤ +125°C, sensing range	±1.5	±3.0	°C
ADC Resolution			12	Bits
Temperature Resolution			0.0625	°C
Conversion Time			100	ms
Thermal Resistance (Note 4) θ_{JA}	Junction−to−Ambient (Still Air)		92	°C/W

4. Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2−layer PCB.

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.7 V to 1.9 V, T_A = −20°C to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
I_{CC}	Supply Current	TS active, Bus idle		500	μA
I_{SHDN}	Standby Current	TS shut−down; Bus idle		5	μA
I_{LKG}	I/O Pin Leakage Current	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage		−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA		0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. A.C. CHARACTERISTICS (V_{CC} = 1.7 V to 1.9 V, T_A = −20°C to +125°C)

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
F_{SCL} (Note 5)	Clock Frequency	10	100	10	400	kHz
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
$t_{TIMEOUT}$ (Note 6)	SMBus SCL Clock Low Timeout	25	35	25	35	ms
t_R (Note 7)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:DAT}$	Input Data Setup Time	250		100		ns
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		μs
$t_{HD:DAT}$	Input Data Hold Time	0		0		ns
t_{DH} (Note 7)	Output Data Hold Time	120	3450	120	900	ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50	ns
t_{PU} (Note 8)	Power-Up Delay to Valid Temperature Recording		100		100	ms

5. Timing reference points are set at 30%, respectively 70% of V_{CC}, as illustrated in Figure 5. Bus loading must be such as to allow meeting the V_{IL} and V_{OL} as well as all other timing requirements. The minimum clock frequency of 10 kHz is an SMBus recommendation; the minimum operating clock frequency is limited only by the SMBus time−out. The device also meets the Fast and Standard I^2C specifications, except that T_i and t_{DH} are shorter.
6. For the CAT34TS00, the interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count takes place when SCL is low in the time interval between START and STOP.
7. In a “Wired−OR” system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull−down device must be able to sink the (external) bus pull−up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} - t_{DH} - t_{SU:DAT}$, where t_{LOW} and t_{DH} are actual values (rather than spec limits). A shorter t_{DH} leaves more room for a longer SDA t_R, allowing for a more capacitive bus or a larger bus pull−up resistor.
8. The first valid temperature recording can be expected after t_{PU} at nominal supply voltage.

Table 5. PIN CAPACITANCE (T_A = 25°C, V_{CC} = 1.9 V, f = 400 kHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, $\overline{EVENT}$ Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (other pins)	V_{IN} = 0		6	pF

Table 6. INPUT IMPEDANCE

Symbol	Parameter	Test Conditions	Min	Max	Unit
Z_{EIL}	Input Impedance for A0, A1, A2 Pins	$V_{IN} < 0.3 * V_{CC}$	30		kΩ
Z_{EIH}	Input Impedance for A0, A1, A2 Pins	$V_{IN} > 0.7 * V_{CC}$	800		kΩ

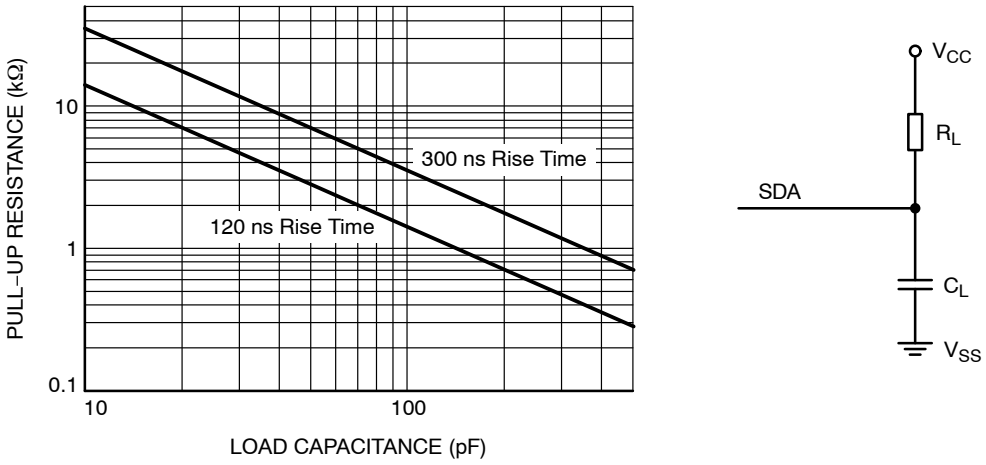

Figure 2. Pull−up Resistance vs. Load Capacitance

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the TS registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset (POR)

The CAT34TS00 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to an undetermined logic state. As V_{CC} exceeds the POR trigger level, the device will power up into conversion mode. When V_{CC} drops below the POR trigger level, the device will power down into Reset mode.

This bi−directional POR behavior protects CAT34TS00 against brown−out failure following a temporary loss of power. The POR trigger level is set below the minimum operating V_{CC} level.

Device Interface

The CAT34TS00 supports the Inter−Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34TS00 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34TS00 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2. The CAT34TS00 contains eight 16−bit internal registers which can be accessed for write and read using the I^2C/SMBus protocol.

I^2C/SMBus Protocol

The I^2C/SMBus uses two ‘wires’, one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address (the preamble) are fixed at binary 0011 (3hex). The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit, R/$\overline{\text{W}}$, specifies whether a Read (1) or Write (0) operation is being performed.

Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9th clock cycle (Figure 4). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9th clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 5.

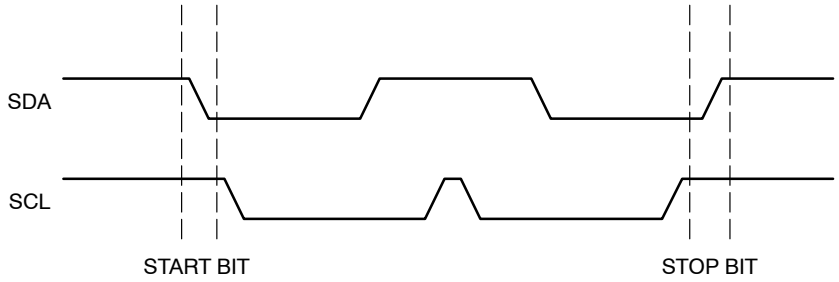

Figure 3. Start/Stop Timing

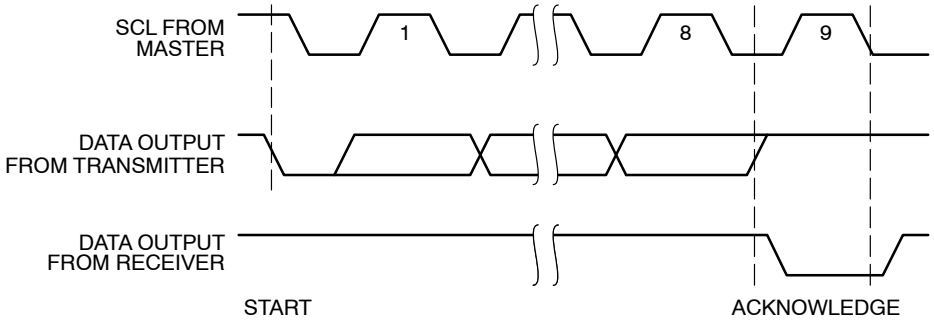

Figure 4. Acknowledge Timing

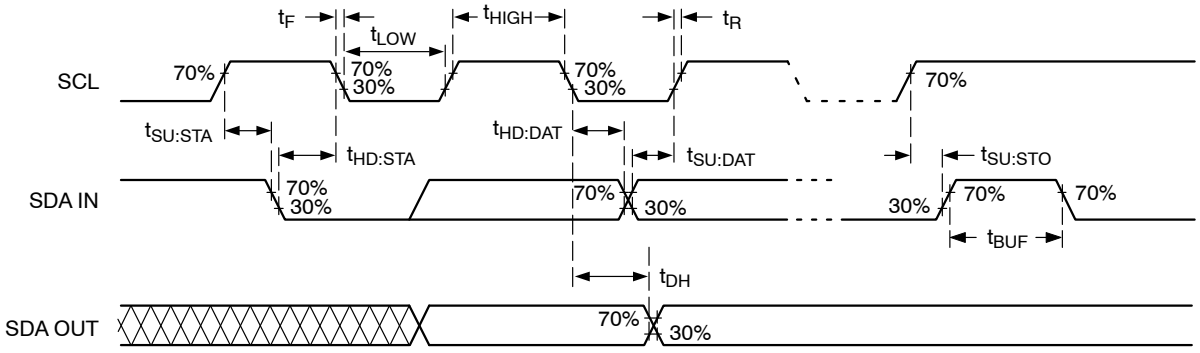

Figure 5. Bus Timing

Write Operations

To write data to one of the internal registers, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to '0'), followed by the register address, followed by two data bytes. The matching Slave will acknowledge the Slave address, register address and each data byte (Figure 6). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the register update.

Read Operations

Immediate Read

A CAT34TS00 presented with a Slave address containing a '1' in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting the content of the register at the current address pointer location. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 7).

Selective Read

The Read operation can be started from a specific address, by preceding the Immediate Read sequence with a 'data less' Write sequence. The Master sends out a START, Slave address and register address, but rather than following up with data (as in a Write operation), the Master then issues another START and continues with an Immediate Read sequence (Figure 8).

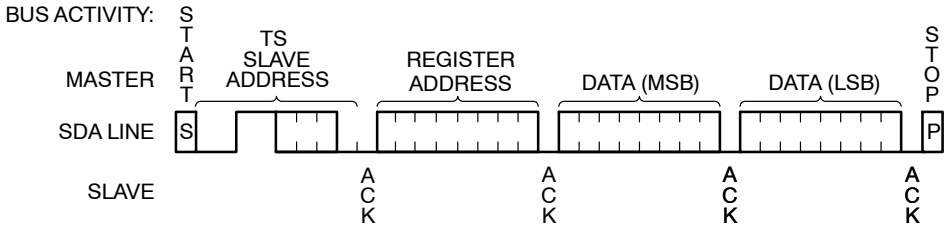

Figure 6. Temperature Sensor Register Write

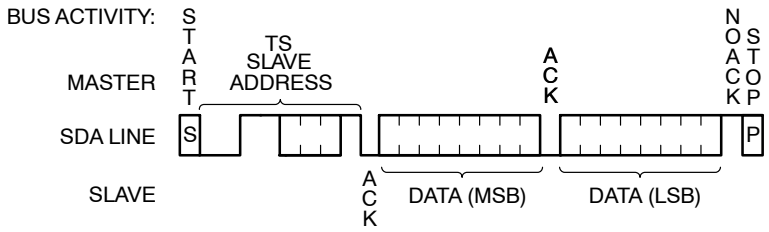

Figure 7. Temperature Sensor Immediate Read

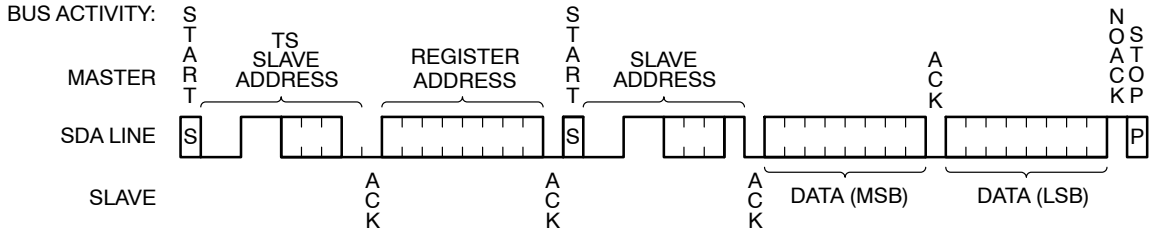

Figure 8. Temperature Sensor Selective Read

Temperature Sensor Operation

The TS component in the CAT34TS00 combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ−Δ modulator, yielding a 12 bit plus sign digital temperature representation. The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

Registers

The CAT34TS00 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 7. Upon power−up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The CAT34TS00 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the $\overline{\text{EVENT}}$ pin. To avoid undesirable $\overline{\text{EVENT}}$ pin activity, this pin is automatically disabled at power−up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two's complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

Temperature Data Register (User Read Only)

This register stores the measured temperature, as well as trip status information. B15, B14, and B13 are the trip status bits, representing the relationship between measured temperature and the 3 limit values; these bits are not affected by EVENT status or by Configuration register settings regarding $\overline{\text{EVENT}}$ pin. Measured temperature is represented by bits B12 to B0. Data format is two's complement, where B12 represents the sign, B11 represents 128°C, etc. and B0 represents 0.0625°C.

Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI−SIG trade organization to the CAT34TS00 device is fixed at 0x1B09.

Device ID and Revision Register (Read Only)

This register contains specific device ID and device revision information.

Table 7. THE TEMPERATURE SENSOR REGISTERS

Register Address	Register Name	Power−On Default	Read/Write
0x00	Capability Register	0x0077	Read
0x01	Configuration Register	0x0000	Read/Write
0x02	High Limit Register	0x0000	Read/Write
0x03	Low Limit Register	0x0000	Read/Write
0x04	Critical Limit Register	0x0000	Read/Write
0x05	Temperature Data Register	Undefined	Read
0x06	Manufacturer ID Register	0x1B09	Read
0x07	Device ID/Revision Register	0x2201	Read

Table 8. CAPABILITY REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU (Note 9)	RFU	RFU	RFU	RFU	RFU	RFU	RFU
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
EVSD	TMOUT	X	TRES [1:0]		RANGE	ACC	EVENT

9. RFU stands for Reserved for Future Use

Bit	Description
B15:B8	Reserved for future use; can not be written; should be ignored; will read as 0
B7 (Note 10)	0: Configuration Register bit 4 is frozen upon Configuration Register bit 8 being set (i.e. a TS shut−down freezes the $\overline{\text{EVENT}}$ output) 1: Configuration Register bit 4 is cleared upon Configuration Register bit 8 being set (i.e. a TS shut−down de−asserts the $\overline{\text{EVENT}}$ output)
B6	0: Not used 1: The TS implements SMBus time−out within the range 25 to 35 ms
B5	X: May be 0 or 1 (Default = 1)
B4:B3	00: LSB = 0.50°C (9 bit resolution) 01: LSB = 0.25°C (10 bit) 10: LSB = 0.125°C (11 bit) 11: LSB = 0.0625°C (12 bit)
B2	0: Not used 1: The temperature monitor can read temperatures below 0°C and sets the sign bit appropriately
B1	0: Not used 1: The temperature monitor has ±1°C accuracy over the active range (75°C to 95°C) and ±2°C accuracy over the monitoring range (40°C to 125°C)
B0	0: Not used 1: The device supports interrupt capabilities

10. Configuration Register bit 4 can be cleared (but not set) after Configuration Register bit 8 is set, by writing a “1” to Configuration Register bit 5 ($\overline{\text{EVENT}}$ output can be de−asserted during TS shut−down periods)

Table 9. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TCRIT_LOCK	ALARM_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Bit	Description
B15:B11	Reserved for future use; can not be written; should be ignored; will read as 0
B10:B9 (Note 11)	00: Disable hysteresis 01: Set hysteresis at 1.5°C 10: Set hysteresis at 3°C 11: Set hysteresis at 6°C
B8 (Note 15)	0: Thermal Sensor is enabled; temperature readings are updated at sampling rate 1: Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN
B7 (Note 14)	0: Critical trip register can be updated 1: Critical trip register cannot be modified; this bit can be cleared only at POR
B6 (Note 14)	0: Alarm trip registers can be updated 1: Alarm trip registers cannot be modified; this bit can be cleared only at POR
B5 (Note 13)	0: Always reads as 0 (self−clearing) 1: Writing a 1 to this position clears an event recording in interrupt mode only
B4 (Note 12)	0: EVENT output pin is not being asserted 1: EVENT output pin is being asserted
B3 (Note 11)	0: EVENT output disabled; *polarity dependent*: open−drain for **B1** = 0; grounded for **B1** = 1 1: EVENT output enabled
B2 (Note 17)	0: event condition triggered by alarm or critical temperature limit crossing 1: event condition triggered by critical temperature limit crossing only
B1 (Notes 11, 16)	0: EVENT output active low 1: EVENT output active high
B0 (Note 11)	0: Comparator mode 1: Interrupt mode

11. Cannot be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.
12. This bit is a *polarity independent* 'software' copy of the $\overline{\text{EVENT}}$ pin, i.e. it is under the control of B3. This bit is read−only.
13. Writing a '1' to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 9).
14. Cleared at power−on reset (POR). Once set, this bit can only be cleared by a POR condition.
15. The TS powers up into active mode, i.e. this bit is cleared at power−on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS cannot be shut down (B8 cannot be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.
16. The $\overline{\text{EVENT}}$ output is "open−drain" and requires an external pull−up resistor for either polarity. The "natural" polarity is "active low", as it allows "wired−or" operation on the EVENT bus.
17. Cannot be set as long as lock bit B6 is set.

Table 10. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 11. LOW LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 12. TCRIT LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 13. TEMPERATURE DATA REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C (Note 18)	0.125°C (Note 18)	0.0625°C (Note 18)

18. When supported – as defined by Capability Register bits TRES (1:0).

Bit	Description
B15	0: Temperature is below the TCRIT limit 1: Temperature is above the TCRIT limit
B14	0: Temperature is below the High limit 1: Temperature is above the High limit
B13	0: Temperature is above the Low limit 1: Temperature is below the Low limit
B12	0: Positive temperature 1: Negative temperature

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the "don't care" bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 14. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 9, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the (enabled) $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. Once the temperature exceeds the critical limit, the $\overline{\text{EVENT}}$ remains asserted as long as the temperature stays above the critical limit and cannot be cleared. A clear request sent to the CAT34TS00 while the temperature is above the critical limit will be acknowledged, but will be executed only after the temperature drops below the critical limit.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. Clear requests are ignored in this mode. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 10.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT34TS00 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.

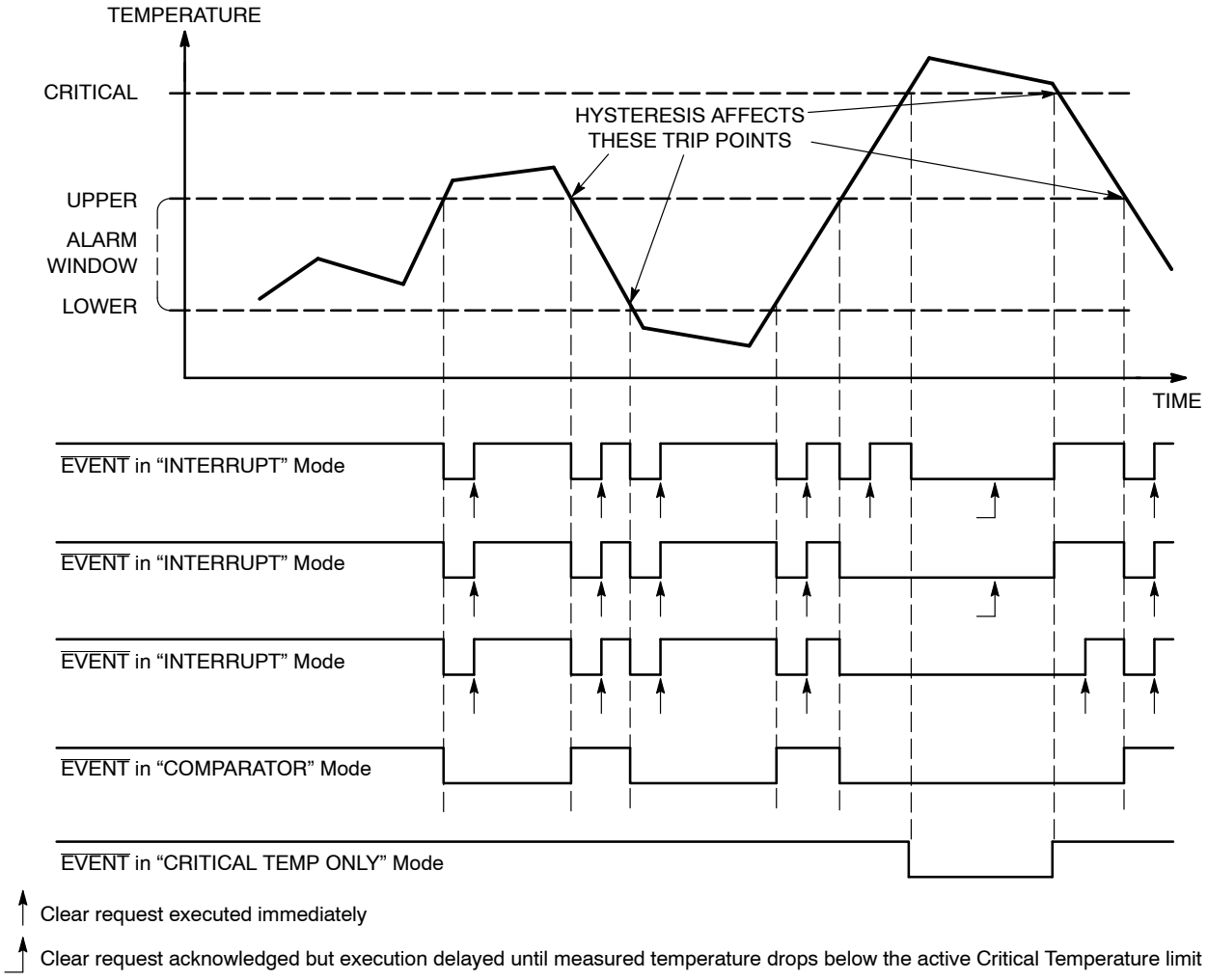

Figure 9. Event Detail

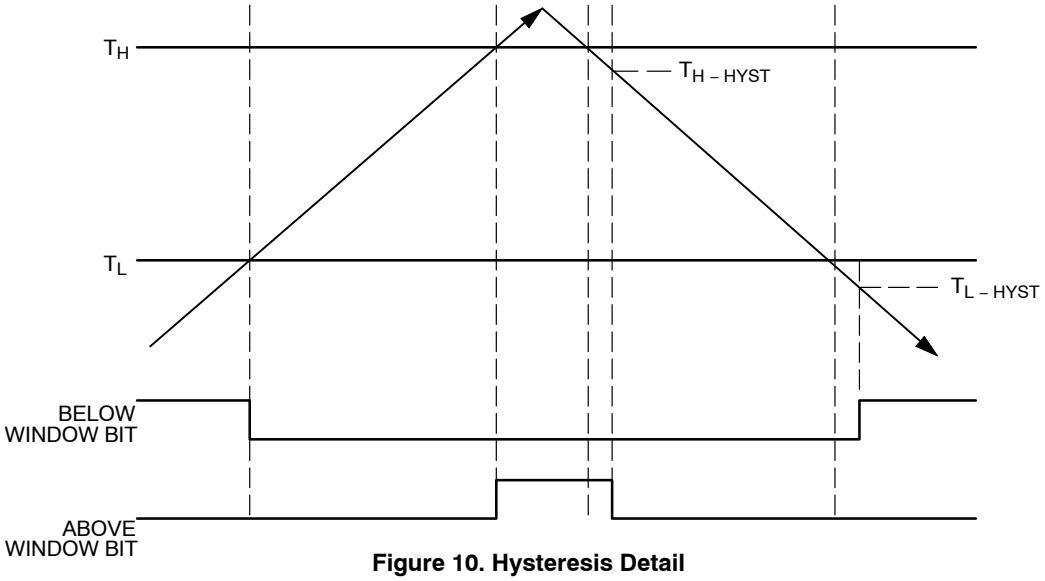

Figure 10. Hysteresis Detail

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Example of Ordering Information

Device Order Number	Specific Device Marking	Package Type	Shipping†
CAT34TS00VP2GT4A	OTA	TDFN8	Tape & Reel, 4,000 Units / Reel

19. All packages are RoHS−compliant (Lead−free, Halogen−free)
20. The standard lead finish is NiPdAu.

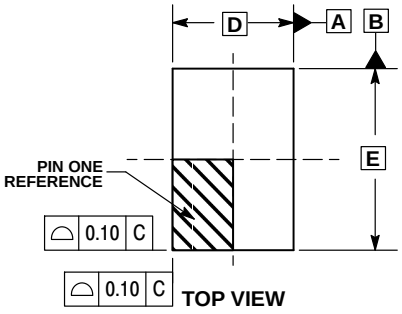
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

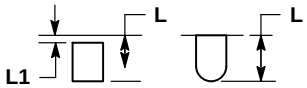


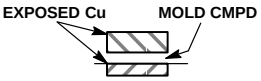
SCALE 2:1

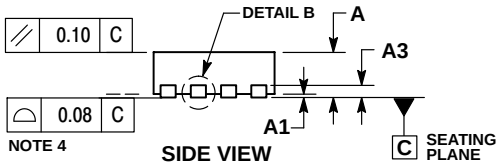
TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

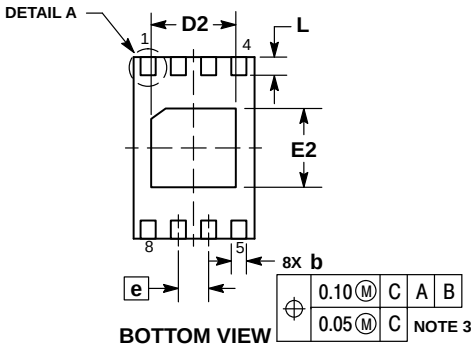
DATE 18 MAR 2015







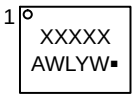




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.20	1.40
e	0.50 BSC	
L	0.20	0.40
L1	–––	0.15

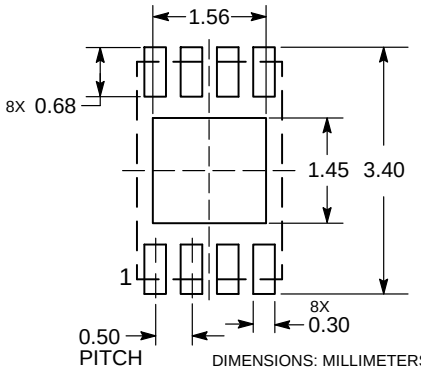
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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