Current Controller for Automotive LED Lamps

NCV7692

The NCV7692 is a device which uses an external NPN bipolar device combined with feedback resistor(s) to regulate a current for use in driving LEDs. The target application for this device is automotive rear combination lamps. A single driver gives the user flexibility to add single channels to multichannel systems. A dedicated dimming feature is included via the PWM input pin. The individual driver is turned off when an open load or short circuit is detected.

LED brightness levels are easily programmed using an external resistor in series with the bipolar transistor. The use of the resistor gives the user the flexibility to use the device over a wide range of currents. Multiple strings of LEDs can be operated with a single NCV7692 device. Set back power limit reduces the drive current during overvoltage conditions.

The device is available in a SOIC-8 package.

Features

- Constant Current Output for LED String Drive
- External Bipolar Device for Wide Current Range Flexibility
  - With BCP56 Transistor, Can Drive Multiple Strings Concurrently (ref. Datasheet Info)
- External Programming Current Resistor
- Pulse Width Modulation (PWM) Control
- Negative Temperature Coefficient Current Control Option
- Open LED String Diagnostic
- Short-Circuit LED String Diagnostic
- Multiple LED String Control
- Overvoltage Set Back Power Limitation
- SOIC-8 Package
- AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

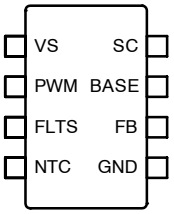
Applications

- Rear Combination Lamps (RCL)
- Daytime Running Lights (DRL)
- Fog Lights
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Turn Signal and Other Externally Modulated Applications
- General Automotive Linear Current LED Driver

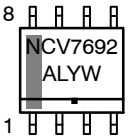


SOIC-8
CASE 751AZ

PINOUT DIAGRAM



MARKING DIAGRAM



IC (Pb−Free)

NCV7692	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7692D10R2G	SOIC-8 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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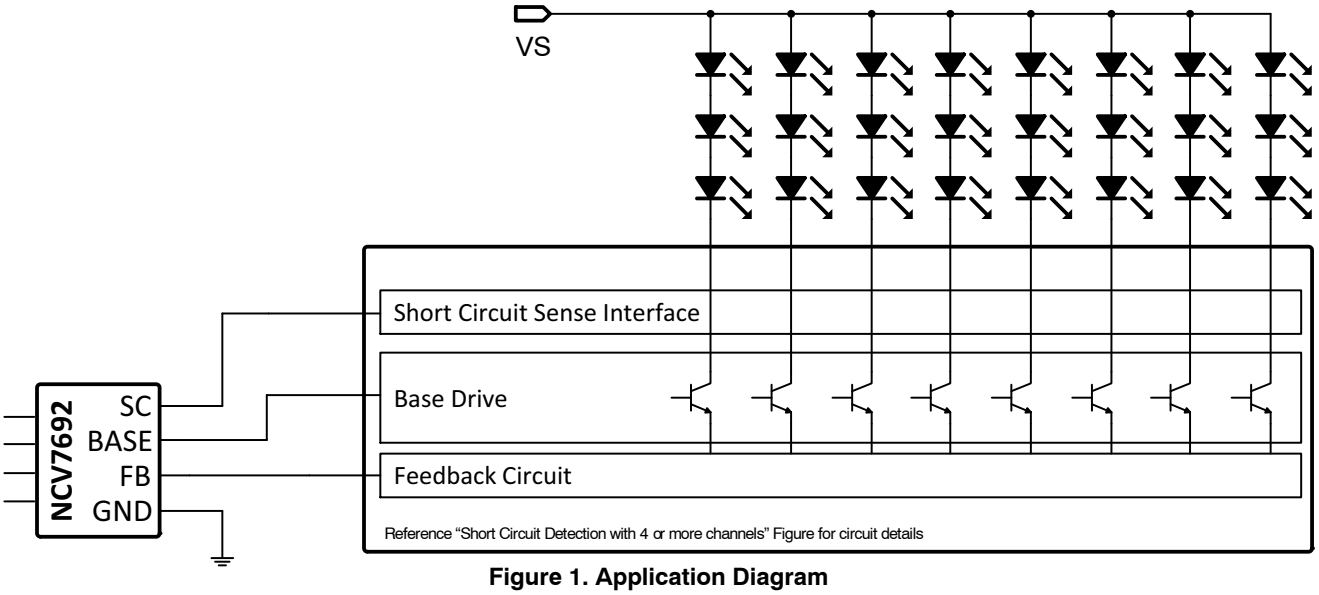


Figure 1. Application Diagram

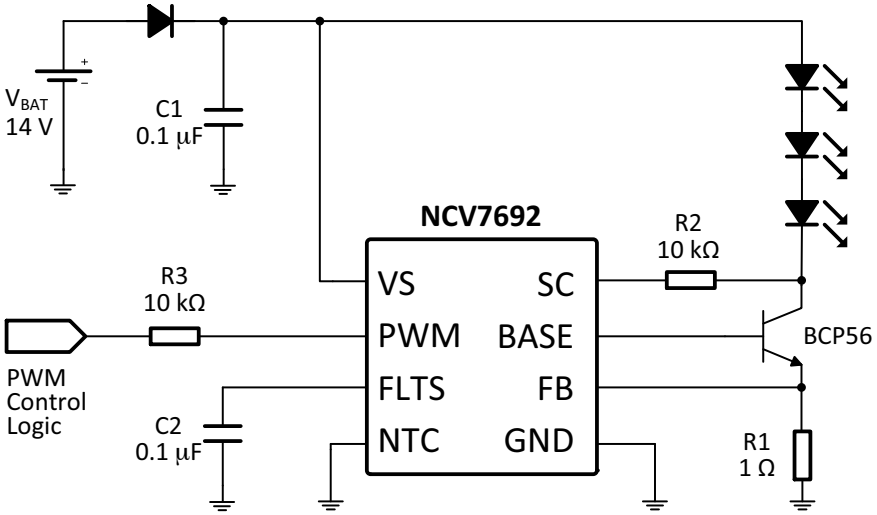


Figure 2. Microprocessor Controlled Application Diagram

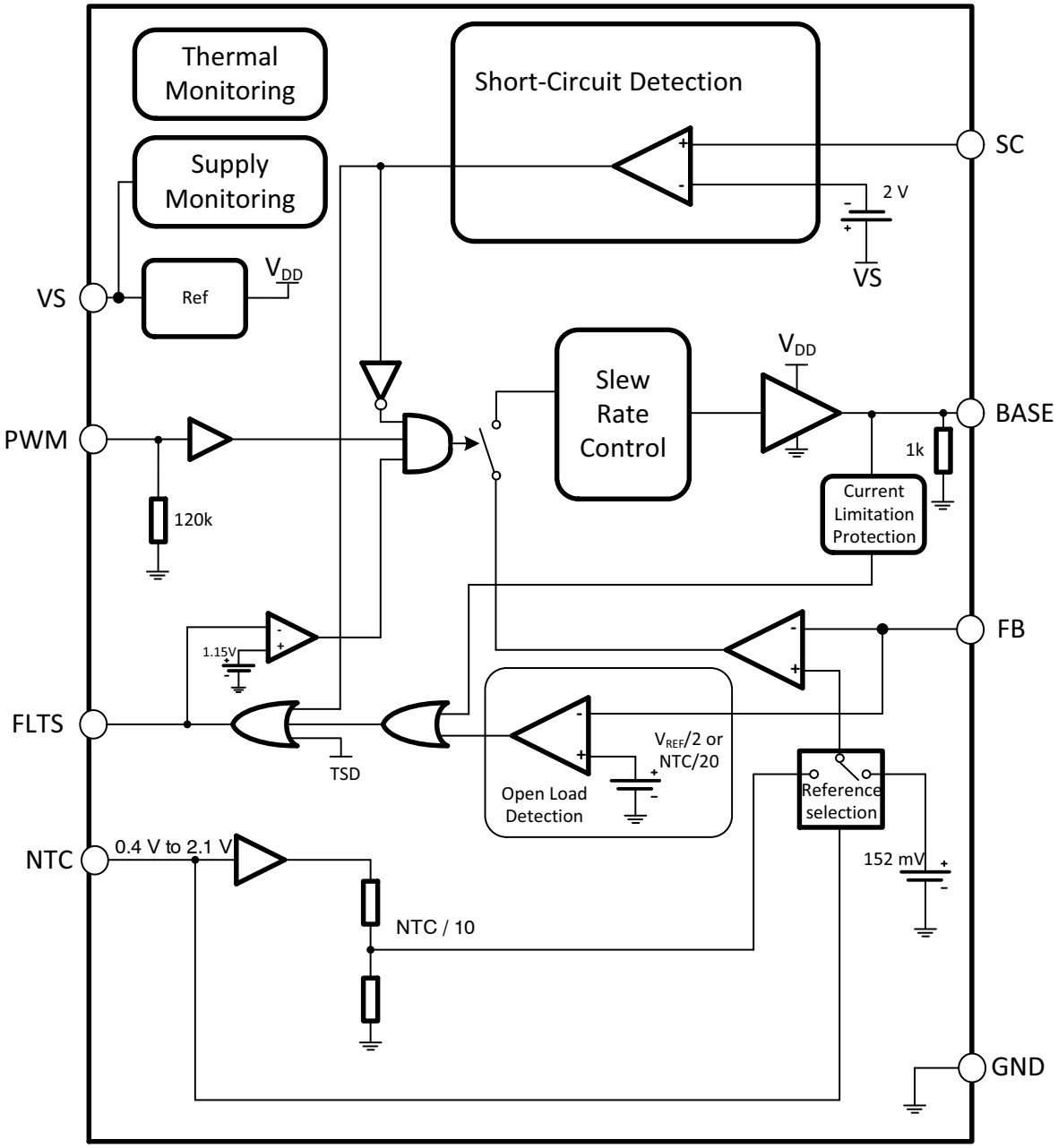


Figure 3. Block Diagram

PIN FUNCTION DESCRIPTION

Pin #	Symbol	Description
1	VS	Automotive Battery input voltage
2	PWM	Logic input for output on/off control. Pull high for output on.
3	FLTS	A capacitor to ground sets the time for open circuit, short circuit, and overtemperature detection.
4	NTC	Optional input for Negative Temperature Coefficient performance. Ground this pin if Negative Temperature Coefficient is not used.
5	GND	Ground
6	FB	Feedback pin for current regulation
7	BASE	Base Drive for external transistor (16 mA [min])
8	SC	LED Short Circuit Detection Input. Ground pin if not used.

MAXIMUM RATINGS

(Voltages are with respect to GND, unless otherwise specified)

Symbol	Rating	Value	Unit
V_S	Supply Voltage (VS) DC Peak Transient	 −0.3 to 50 50	V
V_{HV}	High Voltage Pins (PWM, SC)	−0.3 to (VS + 0.3)	V
V_{LV}	Low Voltage Pins (FB, NTC)	−0.3 to 3.6	V
V_{BASE}	Low Voltage Pin (BASE)	−0.3 to 3.6 or VS + 0.6, whichever is lower	V
V_{FLTS}	Fault Input / Output (FLTS)	−0.3 to (VS + 0.3) *Internally limited charge voltage	V
T_J	Junction Temperature, T_J	−40 to +150	°C
T_P	Peak Reflow Soldering Temperature: Pb-Free, 60 to 150 seconds at 217 °C (Note 1)	260 peak	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For additional information, please see or download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8003/D.

ATTRIBUTES

Symbol	Characteristic	Value	Value
	ESD Capability (Note 2)		
HBM	Human Body Model	≥ ±4.0	kV
MM	Machine Model	≥ ±150	V
CDM	Charge Device Model	≥ ±1.0	kV
MSL	Moisture Sensitivity	2	–
T_S	Storage Temperature	−55 to +150	°C
	Package Thermal Resistance – SOIC-8 (Note 3)		
$R_{\Psi JB}$	Junction−to−Board	129	°C/W
$R_{\theta JA}$	Junction−to−Ambient	179	°C/W
$R_{\Psi JL}$	Junction−to−Lead, R_{JL}	100	°C/W

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
   Latch up current maximum rating: ≥150 mA per JEDEC starndard: JESD78.
3. Values represent typical still air steady-state thermal performance on 1 oz. copper FR4 PCB with 650 mm^2 copper area.

ELECTRICAL CHARACTERISTICS

(4.5 V < VS < 18 V, C_{FLTS} = 0.1 μF, R1 = 1 Ω, Transistor NPN = BCP56, −40 °C ≤ T_J ≤ 150 °C, unless otherwise specified) (Note 4)

Characteristic	Conditions	Min	Typ	Max	Unit
General Parameters					
Supply Current in normal condition	VS = 14 V, PWM = High, Base Current subtracted	–	3.0	4.0	mA
	VS = 14 V, PWM = 0	–	1.6	2.5	mA
Supply Current in fault condition	VS = 14 V, PWM = High V_{FLTS} ≥ FLTS Clamp (5.0 V typ.)	–	1.8	2.8	mA
Under Voltage Lockout	VS rising	3.5	4.0	4.5	V
Under Voltage Lockout Hysteresis		–	200	–	mV
Thermal Shutdown	(Note 5)	150	170	190	°C
Thermal Hysteresis	(Note 5)	–	15	–	°C
Thermal Shutdown Delay	(Note 5)	10	23	36	μs
Base Current Drive					
Output Source Current	BASE = 1 V, FB = 0 V	16	25	30	mA
Output Pull-Down Resistance	PWM = 0 V, BASE = 1 V, FB = 0 V	0.5	1	2	kΩ
Unity Gain Bandwidth		–	100	–	kHz
Amplifier Trans-conductance		–	30	–	mA/m V
Programming					
FB Regulation Voltage	Under Voltage Lockout < VS < Over Voltage Fold Back Threshold 1 VS > Over Voltage Fold Back Threshold 1 VS > Over Voltage Fold Back Threshold 2	 142 54 25	 152 76 38	 162 100 50	mV
VS Overvoltage Fold Back Threshold 1	(Note 6)	18.5	19.5	20.5	V
VS Overvoltage Fold Back Threshold 1 Hysteresis		–	700	–	mV
VS Overvoltage Fold Back Threshold 2	(Note 6)	29.8	31.4	33.0	V
VS Overvoltage Fold Back Threshold 2 Hysteresis		–	700	–	mV
Open Load Timing					
VS Open Load Disable Threshold	VS rising VS falling	4.85 4.70	5.10 4.95	5.35 5.20	V V
FLTS Charge Current	PWM = 5 V, FB = 0 V, VS = 14 V	1	2	3	mA
FLTS Pull Down Resistor		400	600	800	kΩ
FLTS Threshold (Output Deactivation Threshold)		1.00	1.15	1.30	V
FLTS Clamp	VS = 18 V, (Note 7) PWM = 5 V, Charge Current activated (Above this clamp voltage Charge current rolls off to 0)	4	5	6	V
Short Circuit					
Short Circuit Detection Threshold		VS – 1.7	VS – 2	VS – 2.3	V
Short Circuit Output Current	Current out of the SC pin	–	8	16	μA
PWM					
Input High Threshold		–	–	2.2	V
Input Low Threshold		0.7	–	–	V
Hysteresis		–	0.35	–	V
Input Pull-down Resistor		50	120	190	kΩ

ELECTRICAL CHARACTERISTICS (continued)
(4.5 V < VS < 18 V, C_{FLTS} = 0.1 μF, R1 = 1 Ω, Transistor NPN = BCP56, −40 °C ≤ T_J ≤ 150 °C, unless otherwise specified) (Note 4)

Characteristic	Conditions	Min	Typ	Max	Unit
Temperature Compensation					
NTC Attenuation	0.4 V < NTC < 2.1 V	–	1/10	–	
Regulation Offset (referenced to FB)	NTC = 1.6 mV Typ, 0.4 V < NTC < 2.1 V, VS = 14 V	−2 −7	– –	+2 +7	% mV
NTC Input Pull-down Resistor	NTC = 150 mV (low impedance) NTC = 400 mV (high impedance) (Note 8)	15	22 1	31	kΩ MΩ
NTC Detection Level		170	220	300	mV
AC Characteristics					
LED Current rise time	10% / 90% criterion, PWM rising (Note 9)	0.25	1.0	1.5	μs
LED Current fall time	90% / 10% criterion, PWM falling (Note 9)	0.25	1.4	2.0	μs
Propagation Delay PWM rising to $Iout_{B/T}$	50% criterion (Note 9)	–	1.0	2.2	μs
Propagation Delay PWM falling to $Iout_{B/T}$	50% criterion (Note 9)	–	1.0	1.8	μs
PWM Propagation Delay Delta	|(Falling time) − (Rising time)| (Note 9)	–	0.3	1.0	μs
LED Current rise time	10% / 90% criterion, PWM rising (Note 10)	0.25	1.2	1.8	μs
LED Current fall time	90% / 10% criterion, PWM falling (Note 10)	0.25	2.0	3.2	μs
Propagation Delay PWM rising to $Iout_{B/T}$	50% criterion (Note 10)	–	1.5	4.2	μs
Propagation Delay PWM falling to $Iout_{B/T}$	50% criterion (Note 10)	–	1.0	3.4	μs
PWM Propagation Delay Delta	|(Falling time) − (Rising time)| (Note 10)	–	1.2	3.4	μs
Delay Time VS to BASE	VS rising through UVLO to BASE going high through 0.5 V C_{BASE} = 50 pF, R_{BASE} = 680 Ω PWM = VS, SC = floating, FB = GND, NTC = GND	–	4	9	μs
Open Load Blanking Delay	FLTS capacitor charge time not included	25	42	70	μs
Short Circuit Blanking Time		10	23	36	μs
Power-Up Blanking Time		10	23	36	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
5. Guaranteed by design.
6. VS can operate up to 45 V in fold back condition.
7. Device tested at 18 V. Upper limit of 6 V applies across the VS input supply range, but the maximum rating for FLTS (−0.3V to VS to −0.3V) must be considered for all system designs especially at the minimum extreme of VS = 4.5 V.
8. NTC = 400 mV is > NTC detection level and is a higher impedance than when operating within the detection level.
9. Evaluated at VS = 14V, NTC grounded or 1.6 V, 1 Ω sense resistor.
10. Evaluated at VS = 14V, 1.0 V ≤ NTC ≤ 2.1 V, 1 Ω sense resistor
    Guaranteed by design at VS = 14V, 0.4 V ≤ NTC ≤ 1.0 V, 1 Ω sense resistor.

APPLICATIONS INFORMATION

Detailed Operating Description

The NCV7692 device provides low-side current drive via an external bipolar transistor. The low voltage (152 mV) current sense threshold allows for maximum dropout voltage in the system. Dimming is performed using the dedicated PWM pin on the IC. Average output current is directly related to the intensity of the LED (or LED string).

Output Drive

Figure 4 shows the typical output drive configuration. A feedback loop regulates the current through the external LED. U1 monitors the voltage across the external sense resistor (R1). When the voltage exceeds the 152 mV reference, the output of U1 goes from high to low sending a signal the buffer (U2) decreasing the base drive to the external transistor (BCP56). For loads above 150 mA, a PZT651device (replacing the BCP56) is recommended for stable operation.

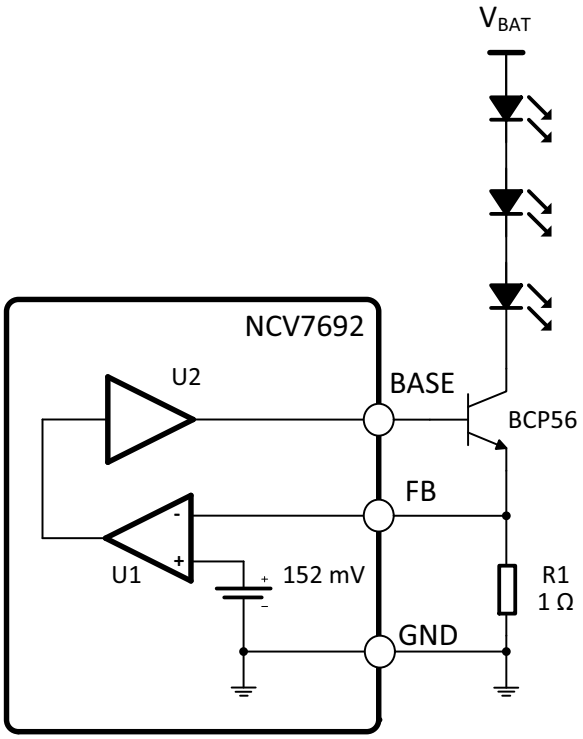


Figure 4. Output Drive Configuration

FLTS Reporting

FLTS reports three fault conditions (by going high) all of which force the output off.

- Open Circuit (latched)
- Thermal Shutdown (thermal hysteresis)
- Short Circuit (latched)

Latched off conditions can be reinitiated by a toggle of the PWM pin or a power down of the supply (VS).

Open Load Detection

Faulted output strings due to open load conditions sometimes require the complete shutdown of illumination within an automotive rear lighting system. The NCV7692 provides that feature option.

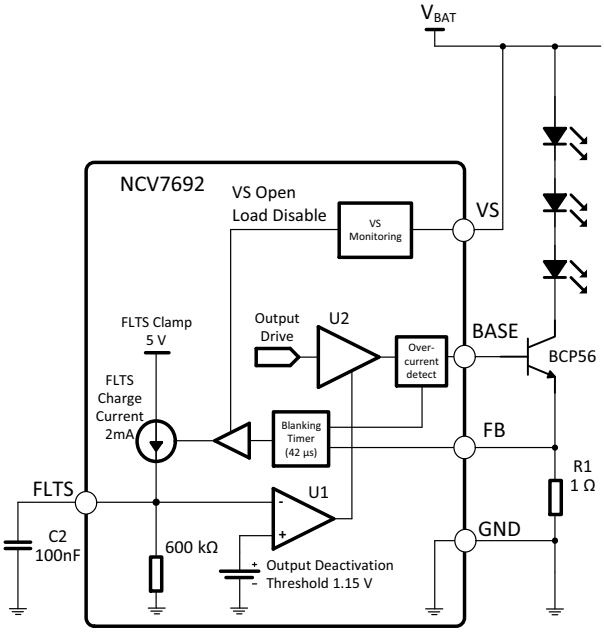
There are two open load detections schemes in the NCV7692. These are OR'd conditions.

1. In normal regulation, the IC monitors the FB voltage (typ 152 mV). When this voltage falls by 50% (to typ 76 mV), an open circuit is detected and a current starts to charge FLTS to flag open load, once FLTS voltage crosses the output deactivation threshold the driver is switched off resulting in a latched off-state. When regulating via the NTC pin, the open load detection threshold is V(NTC)/20.
2. During open load, the base current increases to try and satisfy the regulation loop. Internal circuitry monitors the base current. When the Base Current Drive reaches the Output Source Current (typ 25 mA) threshold, an open circuit is flagged and the driver is latched off.

   Two schemes are used should the rise in base current create a regulated voltage on the feedback pin (FB). If this occurs scheme #1 would not detect the open load.

When an open load is detected, the output turns off, and can be turned back on again by a toggle of the PWM pin or a power down of the supply (VS).

If the open load feature is not used, FLTS should be tied to GND. Grounding FLTS disables open load detection. Short circuit detection and thermal shutdown functions remain active but are not reported externally. The BASE pin is actively held low in this case.



Open load can be disabled by connecting FLTS to GND.

Figure 5. Open Load Detection Circuitry

Table 1. OPEN LOAD DETECTION

Open Load (VS > Open Load Disable Threshold)	**FLTS**	**BASE**
No Open Load	Normal Operation (with FLTS capacitor) (held low)	regulation
No Open Load	Grounded	regulation
FB ≤ 1/2 regulation	(with FLTS capacitor) FLTS starts charging	Held low via internal pull-down resistor after time-out.
BASE Current > 25 mA [typ]	(with FLTS capacitor) FLTS starts charging	Held low via internal pull-down resistor after time-out.
FB ≤ 1/2 regulation	Grounded	regulation
BASE Current > 25 mA [typ]	Grounded	regulation

Multiple String Open Load Consideration

In multi-string applications with high-beta transistors, the feedback voltage from individual strings is averaged, so one defective LED string does not always lead to the open load detection.

One of the ways to improve the open load detection capability is more precise external BASE current limitation. An example of the circuit with one extra resistor and PNP bipolar is shown in Figure 6.

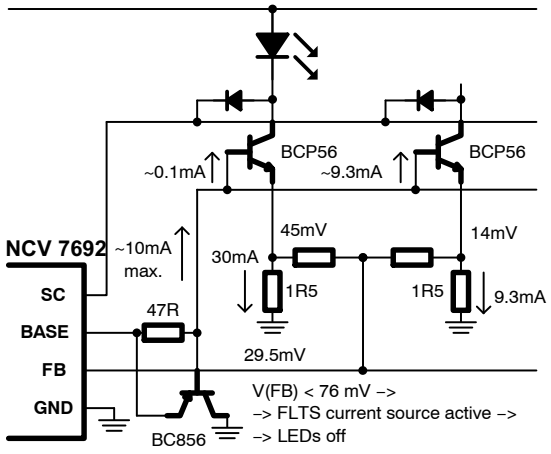


Figure 6. Improved Open Load Detection for Multiple Strings

System Voltage and Overvoltage Fold−back

Low voltage system operation is typically limited by head room in the LED string. Because of this limitation, detection of open loads is inactive below VS = typ 5.1 V (Open Load Disable voltage). There is also an upper limitation. The current roll off feature of the part resets the loop at a lower reference voltage and consequential lower current for VS above the Overvoltage Fold-back threshold on VS, (typ 19.5 V). The open load Detection circuitry is inactive for VS above this Overvoltage Fold-back threshold voltage.

Open Load Timing

The timing for open load detection is programmed using the FLTS pin. The NCV7692 device regulates a 152 mV reference point (Figure 5 on the feedback pin (FB)). When the voltage decreases (half of the FB Regulation Voltage) or the base current reaches the internal 25 mA (typ) limit for 42 μs the timer associated with the FLTS pin starts by charging the capacitor with a 2 mA current source. When the voltage on FLTS exceeds the output Deactivation Threshold (1.15 V (typ)), the BASE pin is pulled low and is held low by an internal pulldown resistor.

A 42 μs blanking time during power up ensures there is enough time for power-up to eliminate false open-load detections. The slow FLTS discharge (600 kΩ [typ]) load (and resultant long time to restart LED drive) eliminates flickering effects.

FLTS Interface

Figure 7 shows an open-drain logic level FET serving as a buffer to the microprocessor.

Figure 8 shows the proper wired “OR” connection for applications which require all channels to latch-off with an open load condition. An open load condition will be reported back to the microprocessor regardless of which channel it occurs on. Note the NCV7692 device uses a feature which allows any channel to charge the FLTS capacitor due to its definition at a charge current value much higher than the discharge value (2 mA versus 600 kΩ [typ]). Additional NCV7692 Single Current Controller devices device may share the same common FLTS capacitors in systems requiring multiple ICs.

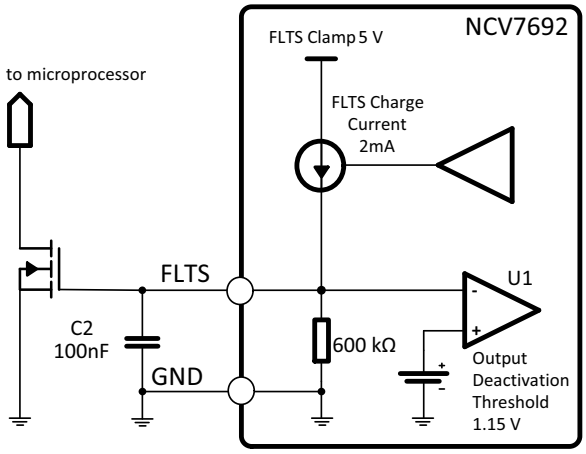
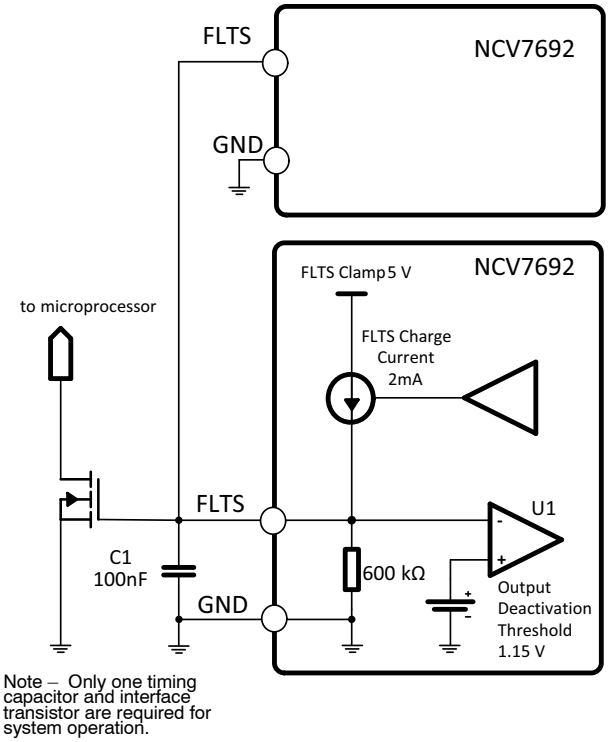


Figure 7. Open Drain Output Interface to Microprocessor



Note – Only one timing capacitor and interface transistor are required for system operation.

Figure 8. FLTS Wired OR to Microprocessor

Temperature Compensation

The NCV7692 device typically operates with a zero TC output current source. The NTC (Negative Temperature Coefficient) pin provides an alternative for an output current which degrades with temperature as defined by the designer's external components.

Zero TC operation is provided when the NTC pin is connected to GND. When a negative temperature coefficient output current is desired to compensate for effects of external LED illumination, the setup shown in Figure 9 will provide the function. On the NTC pin, a comparator detects when the voltage is higher than typ 220 mV, and this voltage is used to provide the feedback reference voltage for the current feedback regulation loop.

The zener provides a reference voltage for the negative temperature coefficient NTC device through an external divider. Be careful of your choice of the zener diode as the temperature coefficients of the devices have a wide variation with the low voltage zeners having a high negative temperature coefficient and the high voltage zeners having a positive temperature coefficient. The regulation loop voltage on NTC should be sufficiently higher than the 220 mV reference voltage to avoid interactions. A typical regulation voltage of 1.6 V is suggested.

The overall tolerance specification for the NTC functionality is broken down into two components.

1. Absolute error. A ±2% tolerance is attributed to the expected value as a result of internal circuitry (most predominantly the 1/10 resistor divider).
2. Reference error. A ± 7mV offset mismatch in the circuitry referenced to FB.

This provides a part capability of (V(NTC)/10) x 0.98 −7mV < V(FB) < (V(NTC)/10) x 1.02 + 7mV.

In addition to the temperature coefficient of the Zener diode (D1), a PTC resistor (R2) can be used to enhance the effect of the overall negative temperature coefficient. A positive temperature coefficient resistor at the top of the resistor divider creates a negative temperature coefficient at the resistor divider output. Alternatively, a negative temperature coefficient resistor for R3 would have the same effect.

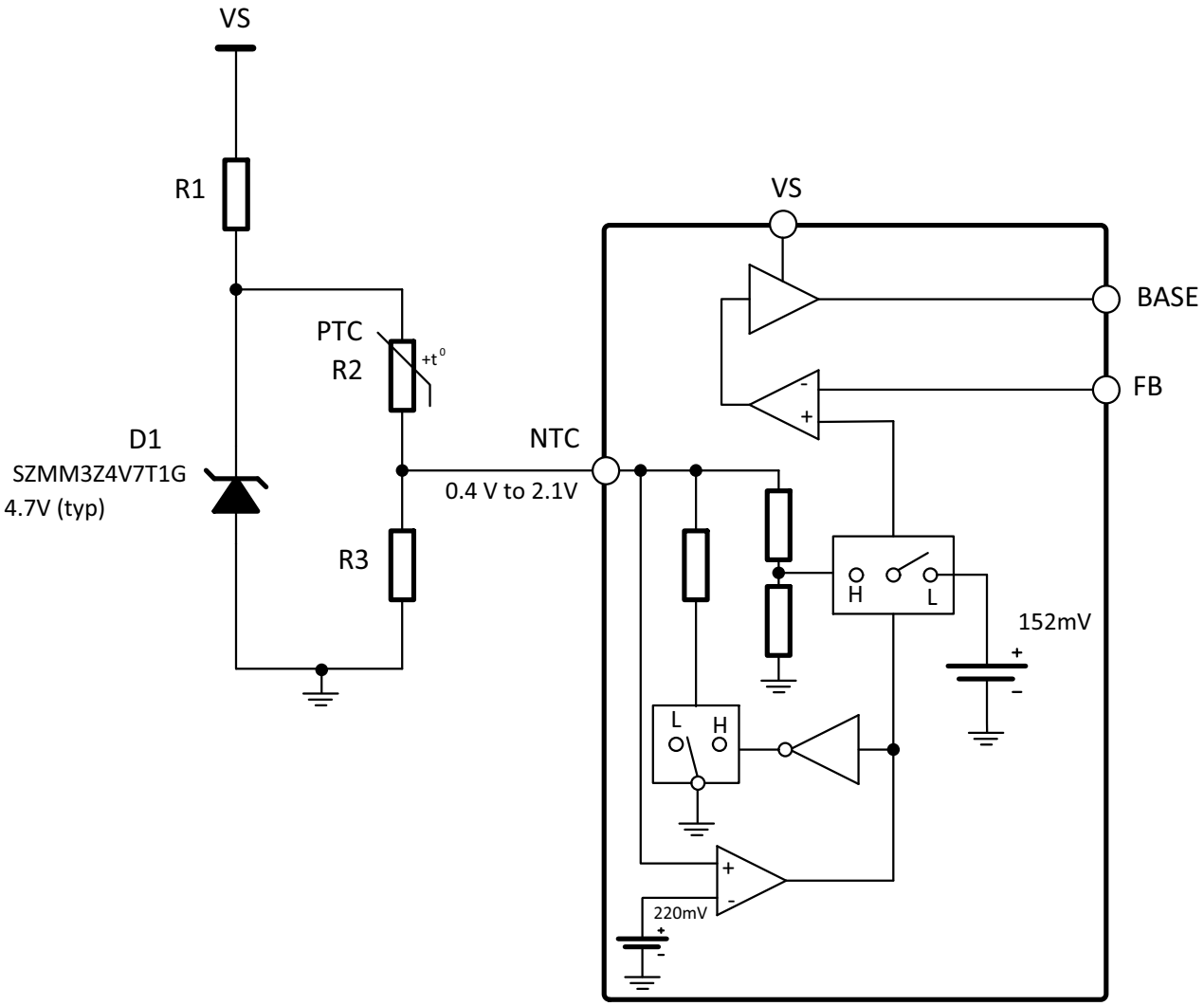


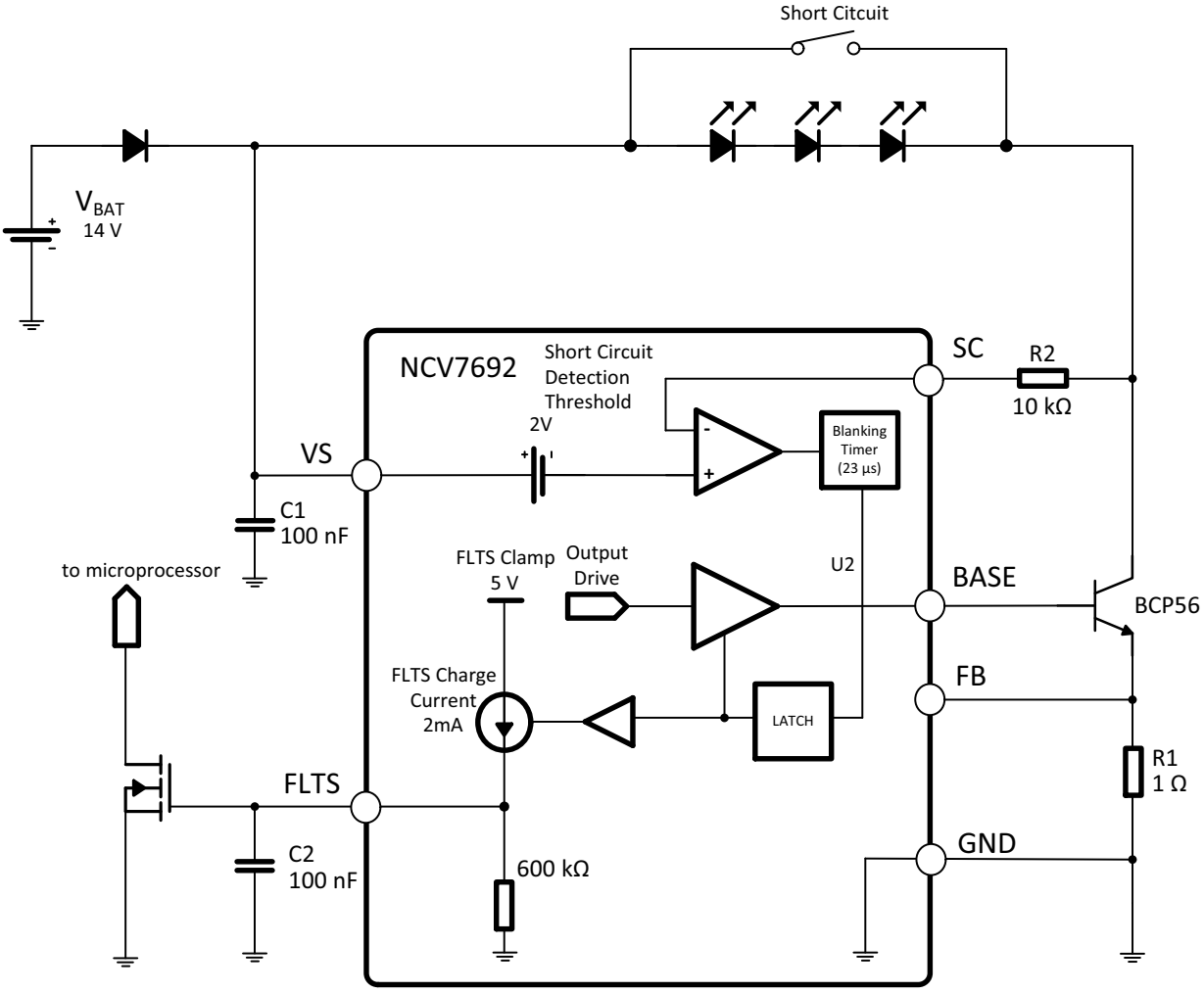
Figure 9. Negative Temperature Compensation Operation

Short Circuit Detection

The short circuit (SC) pin of the device is used as an input to detect a fault when the collector of the external bipolar transistor is shorted to the battery voltage. The threshold voltage detection is referenced 2.0 volts down from the VS pin. A voltage of less than 2.0 volts between VS and SC will latch the device off. The PWM pin must be toggled or UVLO event must occur to reinitiate a turn-on. The detection time for this event is swift to protect the external transistor. To maintain operation during transient events down to 4.5 V, the short circuit detection circuitry is inactive below VS = typ 5.1 V. (the same Open Load Disable voltage as used to disable Open load detection). Otherwise false short circuit events could be falsely triggered due to non-conduction of the external LEDs during transients. Figure 10 shows a short circuit event modeled as a switch (S1). The comparator connected between VS and SC is referenced to a voltage 2.0 V down from VS. A detection voltage less than 2.0 V will toggle a signal from the comparator to the output drive buffer turning off output drive (BASE) to the external bipolar transistor. An initial blanking time of 23 μs is used during turn-on of the device to ignore false detections. This is beneficial during normal operation and when the device is used without a microprocessor input (PWM) interface as in Figure 10.

Switching off the Base-driver in case of SC, will also make the FLTS charge active, indicating the error to the microprocessor.

When having multiple channels an isolation might be needed to provide the appropriate voltage back to the SC pin during short circuit. Figure 11 shows how external diodes can provide this feature.



Short Circuit Detection is disabled below 5.1 V (typ).

Figure 10. Short Circuit Detection

Short Circuit Detection with 4 or more Channels

Interfacing the short circuit detection for multiple channels with one NCV7692 driver system is done easily using diodes or a diode resistor combination depending on your system requirements.

Figure 11 shows the implementation using 4 individual diodes which will work for all applications.

Figure 12 shows an implementation which will work provided the drop across the loads is < 3.4 V. This limitation is due to the SC minimum specification of VS − 1.7 V. This setup saves the user 2 diodes.

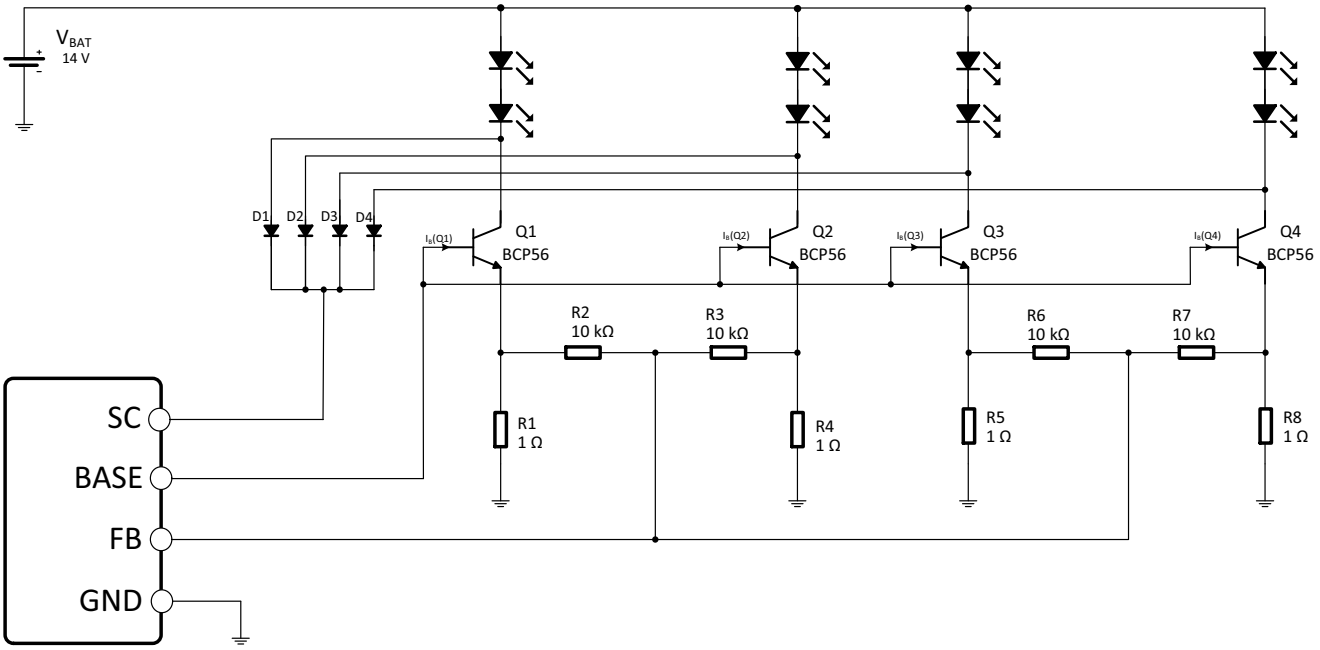


Figure 11. Short Circuit Detection with 4 or more Channels

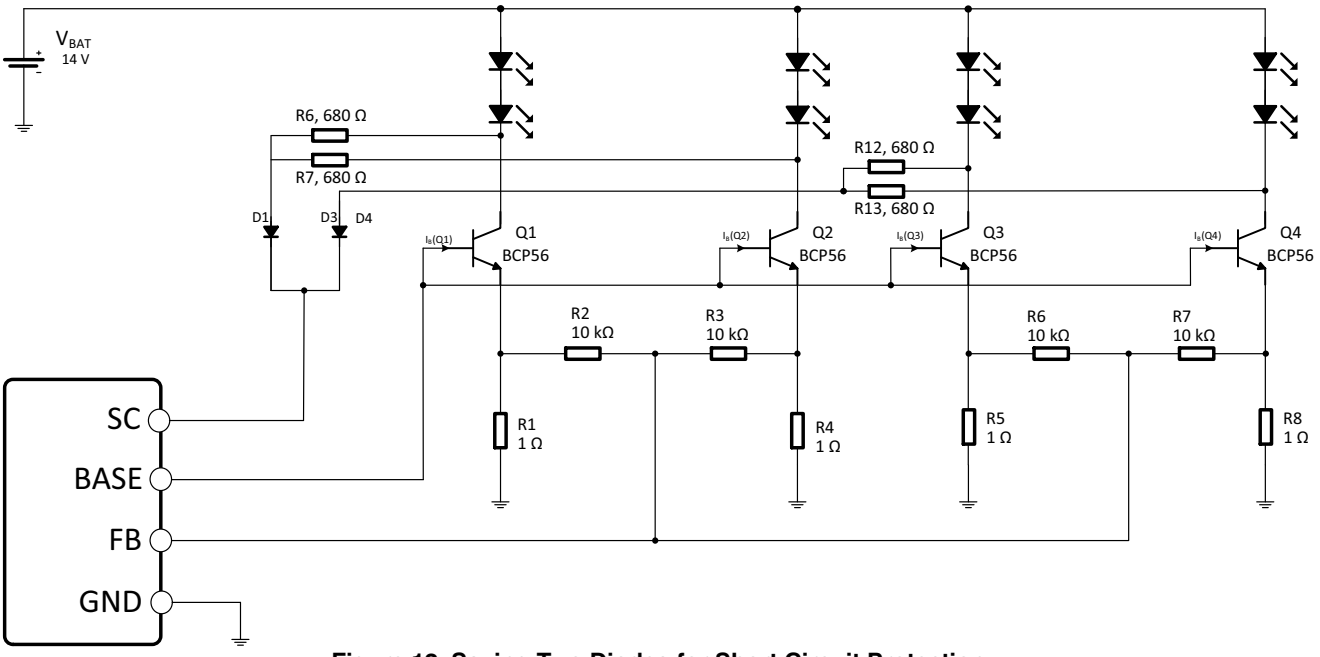


Figure 12. Saving Two Diodes for Short Circuit Protection

Thermal ShutDown

The thermal shut down circuit checks the internal junction temperature of the device. When the internal temperature rises above the Thermal shutdown threshold for greater than the thermal shutdown filter time (23 μs [typ]) the device is switched off. The filter is implemented to achieve a clean detection.

Switching off the Base-driver in case of TSD, will also make the FLTS charge active, indicating the error to the microprocessor.

Applications

Direct Drive without direct battery connection:

Some applications may not allow for a direct connection of VS to the battery voltage. These applications require a connection with a smart-FET. Figure 13 highlights this setup.

Stoplight / Tail Light Application

Automotive applications have a need to drive the RCL (Rear Combination Light). Combining the NCV7692 with the NCV1455B device accomplishes that task. Figure 14 shows the interface of the two ICs using an additional diode (D2). The STOP input signal provides a signal to the NCV7692 which will provide a 100% duty cycle output to the LED strings whenever STOP is high. When only TAIL is high, a modulated duty cycle input is provided to the PWM input and also provides power to the NCV7692 and the LED string. The NCV1455B can provide up to 200 mA (albeit with a 2.5 V drop at 200 mA) of output drive current.

If your application exceeds the current capability of the NCV1455B (200mA) two extra diodes will be required as shown in Figure 15. In this case, the current flow through the LEDs will come from STOP and/or TAIL eliminating the high current from the NCV1455B.

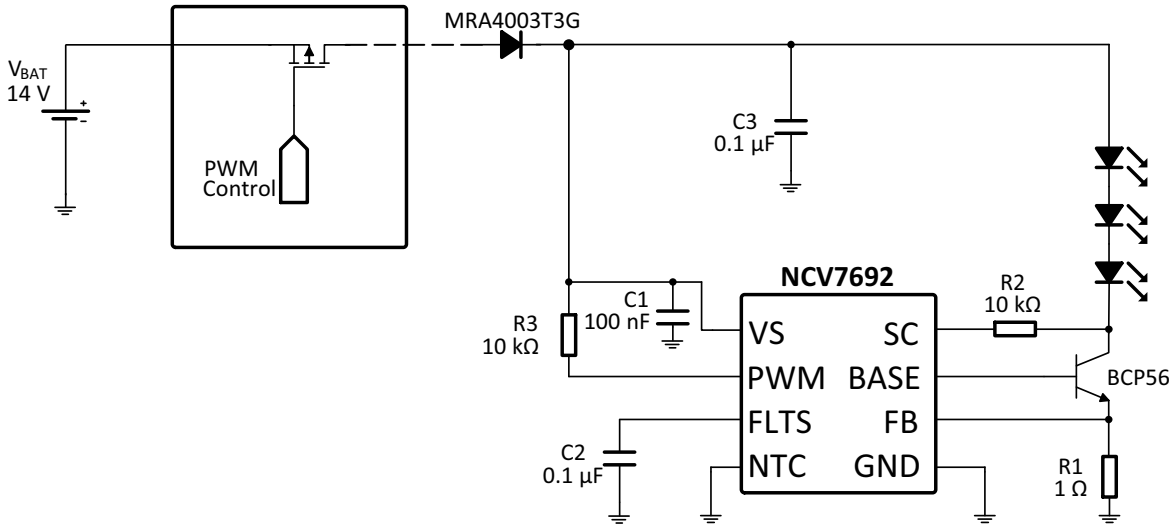


Figure 13. SmartFET Control

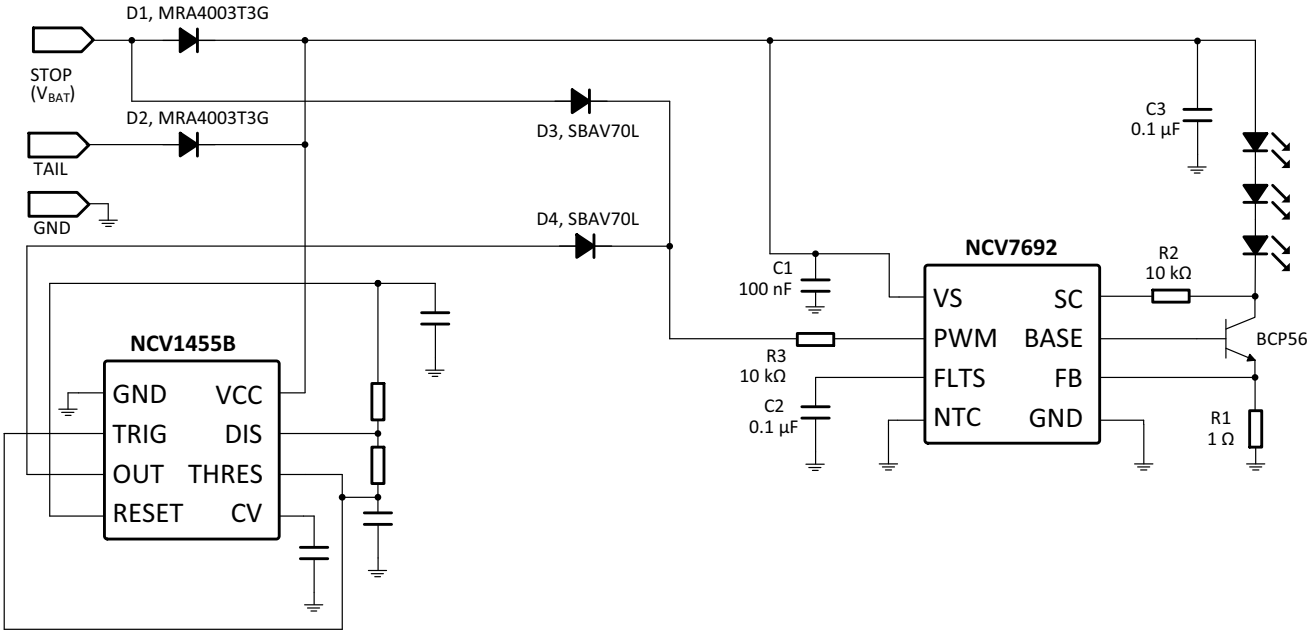


Figure 14. Stoplight / Taillight Application

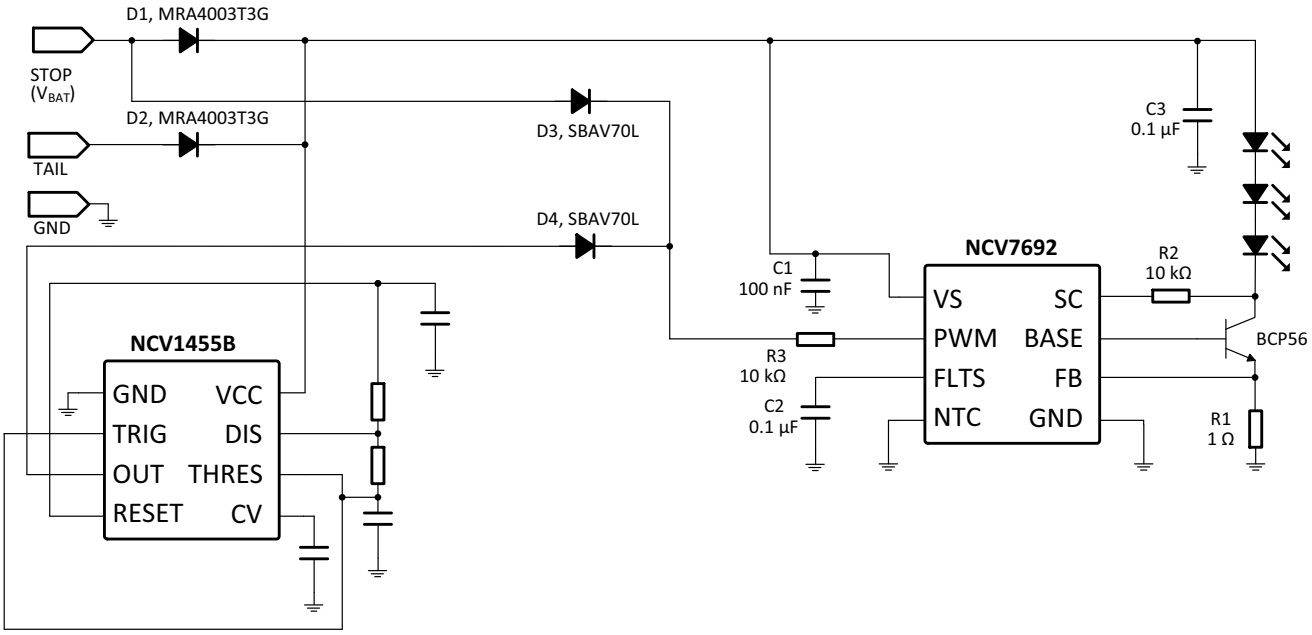


Figure 15. Stoplight / Taillight Application at higher currents

Figure 16: Application Diagram with no microprocessor.

A resistor pull-up from PWM to VS illustrates how the device can be used as a standalone LED driver without using a microprocessor to drive the PWM input.

Figure 17 along with Figure 18 and Figure 19 highlight the use of the NCV7692 device with multiple strings connected to a common drive BASE pin and using external resistors to tie additional strings to a common feedback point (FB). The FB pin will maintain regulation with the FB pin at 152 mV. R1 is used to limit current in the event of an open circuit on one of the strings.

Figure 18: Open Circuit.

It shows the change in BASE drive which occurs with an open circuit in one of the strings. The drive current out of BASE changes from (Ib(Q1)+ Ib(Q2)) to (Ib(Q1)+Ic(Q2)) as regulation will try to maintain in the loop to get 152 mV on FB. Figure 19 shows the equivalent circuit when an open load occurs.

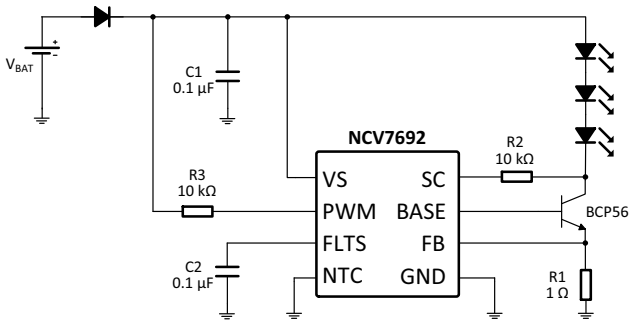
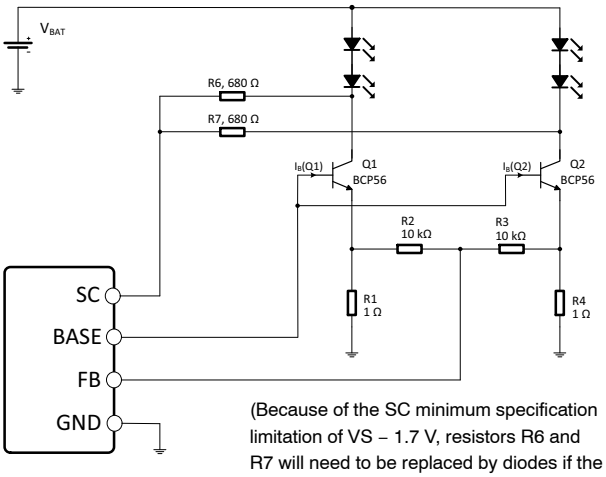
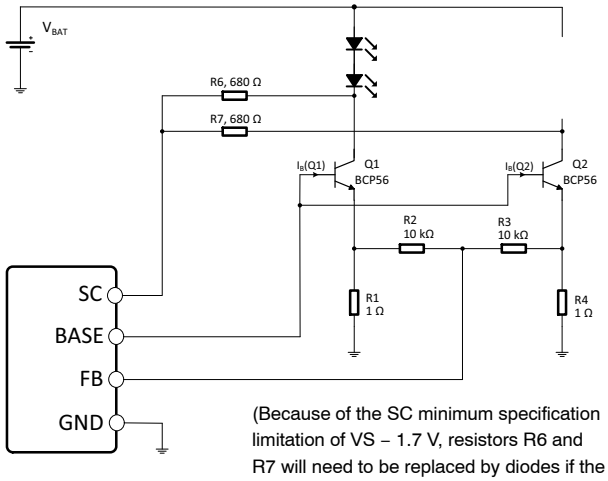


Figure 16. Application Diagram with No Microprocessor



(Because of the SC minimum specification limitation of VS − 1.7 V, resistors R6 and R7 will need to be replaced by diodes if the drop across the load is >3.4 V)

Figure 17. Driving Multiple Strings



(Because of the SC minimum specification limitation of VS − 1.7 V, resistors R6 and R7 will need to be replaced by diodes if the drop across the load is >3.4 V)

Figure 18. Open Circuit

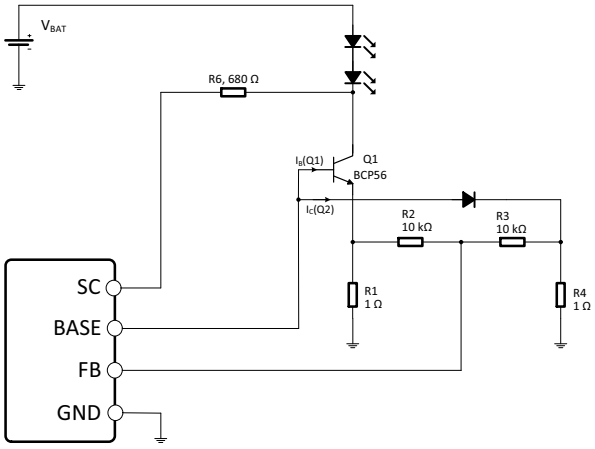


Figure 19. Open Circuit Equivalent

Table 2. FAULT HANDLING TABLE

Fault	Fault Memory	Sense Condition	Driver Condition During Fault	Driver Condition after Parameters Within Specified Limits	Output Fault Clear or Operation Restitution Requirement	Fault Reporting
Open Load (FLTS active)	Latched off.	42 μs w / FB < Vref/2 76 mV or I_{base} > 25 mA 5.1 V < VS < 19.5 V	Driver is latched Off.	Driver is latched Off.	Toggle PWM pin. VS power down below UVLO.	FLTS low to high
Open Load (FLTS = GND)	No effect.	n/a	No effect.	No effect.	n/a	n/a
Short Circuit to Vbat (FLTS active)	Latched off.	23 μs SC < VS − 2 V VS > 5.1 V	Driver is latched Off.	Driver is latched Off.	Toggle PWM pin. VS power down below UVLO.	FLTS low to high
Short Circuit to Vbat (FLTS = GND)	Latched off.	23 μs SC < VS − 2 V VS > 5.1 V	Driver is latched Off.	Driver is latched Off.	Toggle PWM pin. VS power down below UVLO.	FLTS low to high
Under Voltage Lockout	Driver Off	VS < 4 V	Driver Off	Driver back on.	VS > 4 V minus 200mV hysteresis.	n/a
Over Voltage	Output Current Reduced	Threshold 1 VS > 19.5 V Threshold 2 VS > 31.4 V	Reduced output current (FB Regulation Voltage)	Driver back to normal operation.	VS < threshold minus 700 mV hysteresis.	n/a
Thermal Shutdown (FLTS active)	Driver Off	23 μs T_J > 170 °C	Driver Off	Driver back on.	Die temperature below shutdown hysteresis	FLTS low to high
Thermal Shutdown (FLTS =GND)	Driver Off	23 μs T_J > 170 °C	Driver Off	Driver back on.	Die temperature below shutdown hysteresis	FLTS low to high

NOTE: All specified voltages, currents, and times refer to typical numbers.

REVISION HISTORY

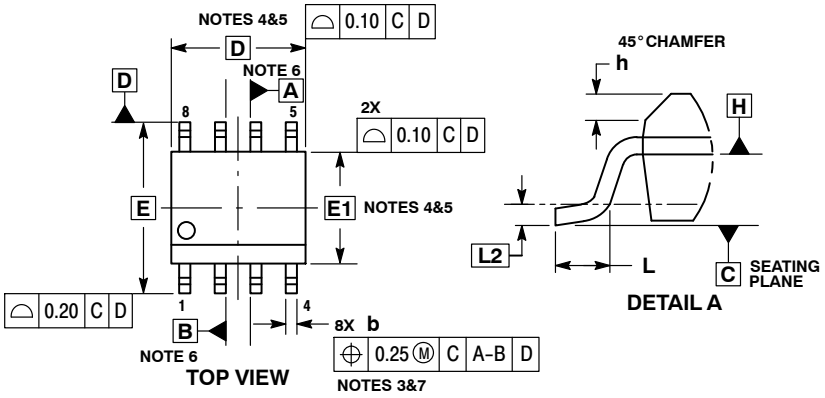
Revision	Description of Changes	Date
1	Rebranded the Data Sheet to **onsemi** format.	6/19/2025

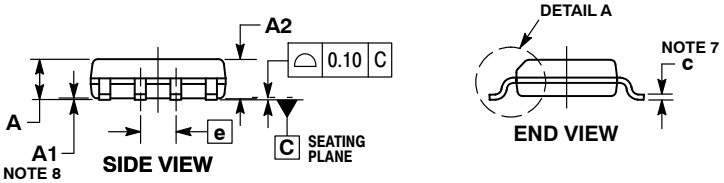


SCALE 1:1

SOIC−8
CASE 751AZ
ISSUE B

DATE 18 MAY 2015

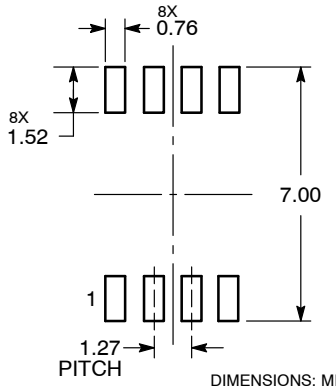




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

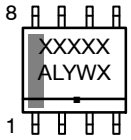
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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