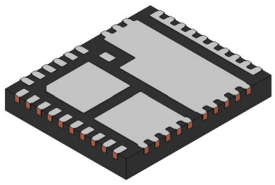
Integrated Driver and MOSFET with Integrated Current Monitor

NCP303150



PQFN39
MN SUFFIX
CASE 483BF

Description

The NCP303150 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP303150 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

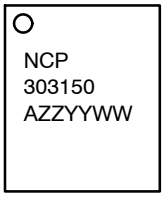
Features

- Capable of Average Currents up to 50 A
- 30 V / 30 V Breakdown Voltage MOSFETs for Higher Long Term Reliability
- High−Performance, Universal Footprint, Copper−Clip 5 mm x 6 mm PQFN Package
- Capable of Switching at Frequencies up to 1 MHz
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−level PWM Inputs
- Precise Current Monitoring
- Option for Zero Cross Detection with 3−level PWM
- Internal Bootstrap Diode
- Catastrophic Fault Detection
  - Thermal Flag (OTP) for Over−Temperature Condition
  - Over−Current Protection FAULT (OCP)
  - Under−Voltage Lockout (UVLO) on VCC and PVCC
- Supports Intel® Power State 4

Applications

- Desktop & Notebook Microprocessors
- Graphic Cards
- Routers and Switches

MARKING DIAGRAM



NCP303150	= Specific Device Code
A	= Assembly Location
ZZ	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NCP303150MNTWG	PQFN39 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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DIAGRAMS

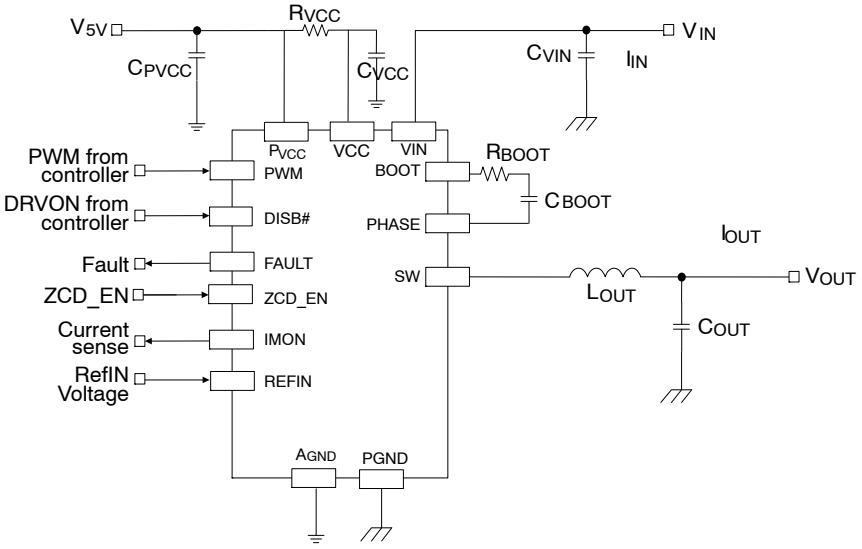


Figure 1. Application Diagram

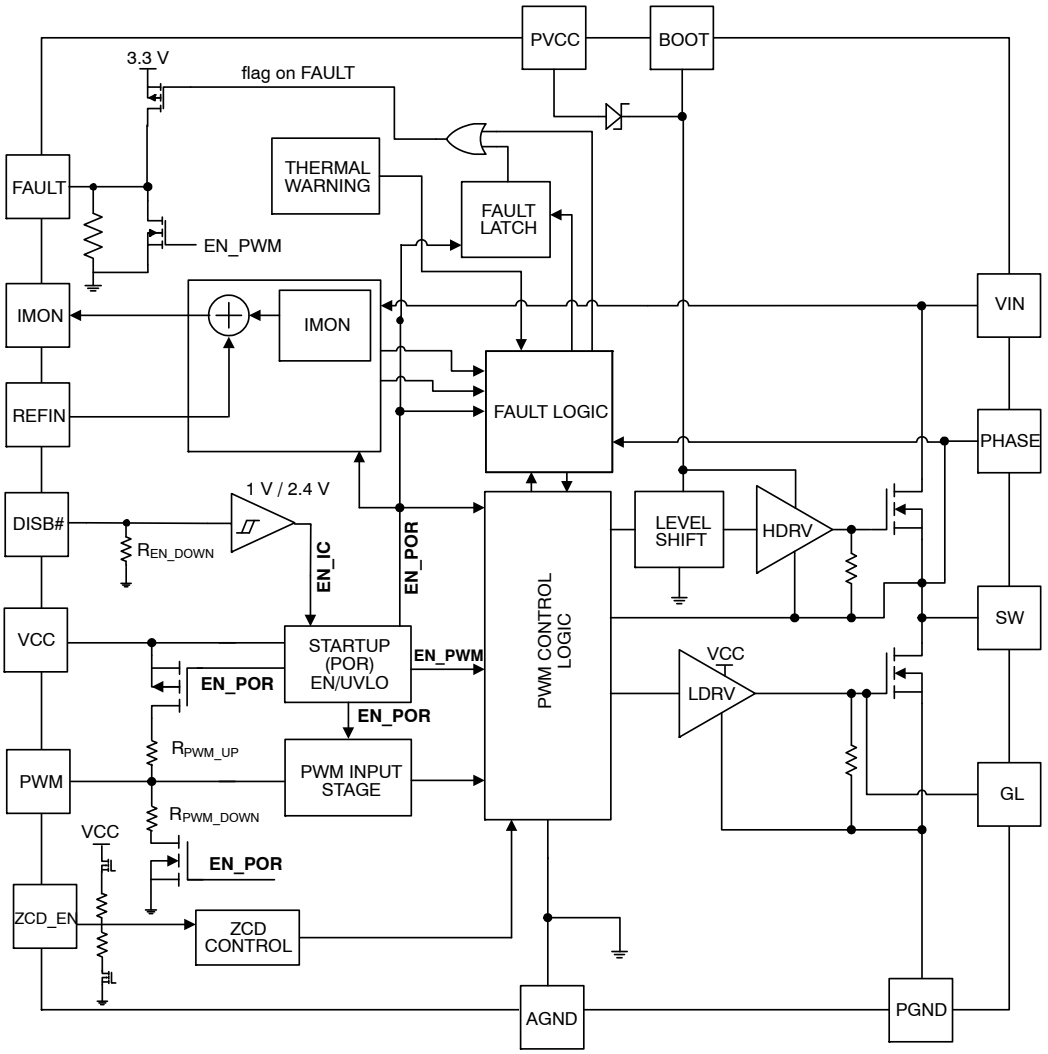


Figure 2. Block Diagram

PINOUT DIAGRAM

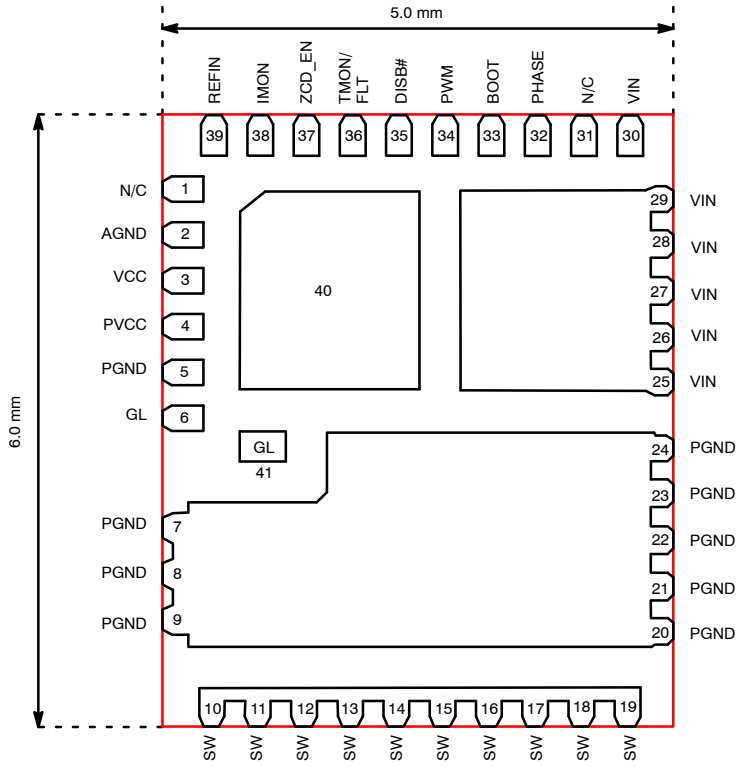


Figure 3. Top View

Table 1. PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	NC	No connect.
2	AGND	Analog Ground for the analog portions of the IC and for substrate.
3	VCC	Power Supply input for all analog control functions
4	PVCC	Power Supply input for LS Gate Driver and Boot Diode.
5, 40	PGND	Reserved for PVCC de−coupling capacitor return.
6, 41	GL	Low−Side Gate Monitor.
7−9, 20−24	PGND	Power ground connection for Power Stage high current path.
10−19	SW	Switching node junction between high−and low−side MOSFETs
25−30	VIN	Input Voltage to Power Stage.
31	NC	No connect.
32	PHASE	Return Connection for BOOT capacitor.
33	BOOT	Supply for high−side MOSFET gate driver. A capacitor from BOOT to PHASE supplies the charge to turn on the n−channel high side MOSFET. During the freewheeling interval (LS MOSFET on) the high side capacitor is recharged by an internal diode.
34	PWM	PWM input to gate driver IC.
35	DISB#	Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull−down resistor on this pin.
36	FAULT	FAULT Reporting Pin
37	ZCD_EN	Zero Current Detection Function Enable
38	IMON	Current Monitor Output (output is referenced to REFIN) − 5 μA/A
39	REFIN	Referenced voltage used for IMON feature. DC input voltage supplied by external source (not generated on SPS driver IC)

Table 2. ABSOLUTE MAXIMUM RATINGS (Electrical Information – all signals referenced to PGND unless noted otherwise)

Pin Name / Parameter		Min	Max	Unit
VCC, PVCC		−0.3	6	V
VIN		−0.3	30	V
BOOT (DC)		−0.3	32	V
BOOT to PHASE (DC)		−0.3	7	V
VSW, PHASE (DC)		−0.3	30	V
VSW, PHASE (< 5 ns)		−15	32	V
All Other Pins		−0.3	V_{VCC} + 0.3	V
ESD	Human Body Model, JESD22−A114	2000		V
	Charged Device Model, JESD22−C101	1000		V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance (under On Semi SPS Thermal Board)	θ_{JA}	12.4	°C/W
	θ_{J-PCB}	1.8	°C/W
Operating Junction Temperature Range (Note 1)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−55 to +150	°C
Moisture Sensitivity Level	MSL	1	

1. The maximum package power dissipation must be observed.
2. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
3. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, PVCC		4.5	5.0	5.5	V
Conversion Voltage	VIN		4.5	19	20	V
Continuous Output Current		F_{SW} = 1 MHz, V_{IN} = 19 V, V_{OUT} = 1.0 V, T_A = 25°C			45	A
		F_{SW} = 300 kHz, V_{IN} = 19 V, V_{OUT} = 1.0 V, T_A = 25°C			50	A
Peak Output Current		F_{SW} = 500 kHz, V_{IN} = 19 V, V_{OUT} = 1.0 V, Duration = 10 ms, Period = 1 s, T_A = 25°C			80	A
Junction Temperature			−40		125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = 5.0 V, V_{VIN} = 19 V, $V_{DISB\#}$ = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC SUPPLY CURRENT						
No switching		DISB# = 5 V, PWM = 0 V	–	8	–	mA
Disabled		DISB# = 0 V, SW = 0 V	–	120	–	μA
UVLO Threshold	V_{UVLO}	VCC rising	3.8	4.1	4.2	V
UVLO Hysteresis	$UVLO_{Hyst}$		–	0.17	–	V
POR Delay to Enable IC	T_{D_POR}	VCC UVLO rising to internal PWM enable			125	μs

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = 5.0 V, V_{VIN} = 19 V, $V_{DISB\#}$ = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DISB# INPUT						
Pull−Down Resistance			–	130	–	kΩ
High−Level Input Voltage	V_{UPPER}		2.7	–	–	V
Low−Level Input Voltage	V_{LOWER}		–	–	0.65	V
Enable Propagation Delay		PWM=GND, Delay Between EN from LOW to HIGH to GL from LOW to HIGH − Slow EN Setting	16	26	32	μs
Disable Propagation Delay		PWM=GND, Delay Between EN from HIGH to LOW to GL from HIGH to LOW − Fast EN setting	–	43	109	ns
PWM INPUT (T_A=25°C, V_{CC} / P_{VCC}=5 V, f_{SW}=1 MHz, I_{OUT}=10 A)						
Input High Voltage	V_{PWM_HI}		2.35	2.45	2.55	V
Mid−State Voltage Upper Threshold	V_{TRI_HI}		2.05	2.2	2.3	V
Mid−State Voltage Lower Threshold	V_{TRI_LO}		0.9	1.0	1.1	V
Input Low Voltage	V_{PWM_LO}		0.65	0.75	0.85	V
Pull−Up Impedance	R_{UP_PWM}		–	21	–	kΩ
Pull−Down Impedance	R_{DOWN_PWM}		–	10	–	kΩ
3−State Open Voltage	V_{PWM_HIZ}		1.4	1.65	1.85	V
Non−overlap Delay, Leading Edge	T_{DEADON}	GL <= 0.5 V to SW>1.2 V. PWM Transition 0→1		7		ns
Non−overlap Delay, Trailing Edge	$T_{DEADOFF}$	SW <= 1.2 V to GL>=0.5 V, PWM Transition 1→0		6		ns
PWM Propagation Delay, Rising	T_{PD_PHGLL}	PWM Going HIGH to GL Going LOW, V_{IH_PWM} to 90% GL	–	17	20	ns
PWM Propagation Delay, Falling	T_{PD_PLGHL}	PWM Going LOW to GH Going LOW, V_{IL_PWM} to 90% GH	–	26	30	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM_EXIT_L}$	PWM (from Tri−State) going LOW to GL going HIGH, VIL_PWM to 10% GL	–	20	30	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−High	$T_{PWM_EXIT_H}$	PWM (from Tri−State) going HIGH to SW going HIGH, VIH_PWM to 10% SW	–	27	30	ns
PWM High to 3−State hold Off Time	$T_{D_HOLDOFF1}$	PWM Going High to HS Going Off	20	43	50	ns
PWM Low to 3−State hold Off Time	$T_{D_HOLDOFF2}$	PWM Going Low to LS Going Off	20	36	50	ns
HS minimal turn on time	$T_{ON_MIN_HS}$	SW gate rising 10% to falling 10%		37		ns
LS minimal turn on time	$T_{ON_MIN_LS}$	LS gate rising 10% to falling 10%		33		ns
HS minimal turn off time	$T_{OFF_MIN_HS}$	SW gate falling 10% to rising 10%		31		ns
LS minimal turn off time	$T_{OFF_MIN_LS}$	LS gate falling 10% to rising 10%		51		ns
FAULT FLAG OUTPUT VOLTAGE/CURRENT						
FAULT Report Output Voltage	V_{FAULT}		2.85	–	–	V
Fault Report Delay time	T_{DFAULT}		–	100	–	ns
IMON						
HS off to LS On Blanking Stop Time	T_{BLANK_HSOFF}	IMON Blanking Time for PWM transition 1→0	–	90	–	ns
HS on to LS Off Blanking Stop Time	T_{BLANK_HSON}	IMON Blanking Time for PWM transition 0→1	–	70	–	ns
IMON Amplifier Gain BW	BW_{IMON}	L=150 nH, V_{IN}=19 V, V_{OUT}=1.0 V, f_{SW}=800 kHz	–	5	–	MHz

Table 5. ELECTRICAL CHARACTERISTICS
(V_{VCC} = 5.0 V, V_{VIN} = 19 V, $V_{DISB\#}$ = 2.0 V, C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
IMON						
IMON Propagation Delay Time	T_{DELAY}	L=150 nH, V_{IN}=19 V, V_{OUT}=1.0 V, f_{SW}=800 kHz, IMON Peak to IL Peak	–	60	75	ns
IMON OPERATING RANGE (T_A = T_J = −40°C to 125°C, V_{CC} = 4.5 V to 5.5 V, V_{IN} = 4.5 – 20 V)						
Dynamic range at IMON pin	V_{IMON}		0.6		2.3	V
IMON ACCURACY (T_A = 25°C to 125°C, V_{CC}/P_{VCC} = 5 V, V_{IN} = 19 V) (Note 4)						
I_{MON_SLOPE}	I_{MON_SLOPE}	I_{OUT}=−10 A to 40 A	4.75	5.00	5.25	μA/A
V_{IMON_10A}	R_{IMON}=1 kΩ resistor placed from IMON to REFIN. Current Monitor Voltage ($V_{IMON-REFIN}$)	I_{OUT}=10 A, Voltage is Referenced to REFIN Pin	46.5	50	53.5	mV
V_{IMON_20A}		I_{OUT} = 20 A, Voltage is Referenced to REFIN Pin	95	100	105	mV
V_{IMON_30A}		I_{OUT} = 30 A, Voltage is Referenced to REFIN Pin	142.5	150	157.5	mV
V_{IMON_40A}		I_{OUT} = 40 A, Voltage is Referenced to REFIN Pin	190	200	210	mV
BOOTSTRAP DIODE						
Forward Voltage	V_F	Forward Bias Current = 10 mA	–	350	–	mV
Breakdown Voltage	V_R		30			V
LOW−SIDE DRIVER						
Output Impedance, Sourcing	R_{SOURCE_GL}	Source Current=100 mA	–	0.64	–	Ω
Output Impedance, Sinking	R_{SINK_GH}	Sink Current=100 mA	–	0.29	–	Ω
OVER−TEMPERATURE WARNING FAULT						
Over−Temperature Warning Accuracy		Driver IC Temperature	136	140	143	°C
OTW Hysteresis		Driver IC Temperature		15		°C
HS CYCLE−BY−CYCLE POSITIVE I−LIMIT						
I−limit comparator input−output propagation delay.	$t_{D_ILimit-COMP}$	Input Signal = 380 mV, dv/dt = 0.2 mV/nsec.		60		ns
I−limit Blanking Time	t_{BLANK_ILimit}	De−glitch filter (blanking) time for I−limit comparator trip		33		ns
Over−Current Limit	I_{LIM}		74	80	86	A
OCP Hysteresis	I_{LIM_HYS}			8		A
NEGATIVE OVER−CURRENT (NOCP) FAULT						
NOCP Trip LOW Level	I_{NOCP_LOW}			−50		A
ZCD_EN INPUT						
Pull−Up Impedance	R_{UP_PWM}		–	21	–	kΩ
Pull−Down Impedance	R_{DOWN_PWM}		–	10	–	kΩ
ZCD_EN input Voltage High	V_{ZCD_HI}		2.25	2.4	2.55	V
ZCD_EN input Voltage Mid−state	V_{ZCD_MID}		1.4	–	2.0	V
ZCD_EN input Voltage Low	V_{ZCD_LO}		0.7	0.8	0.9	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Imon performance is guaranteed by independent ATE testing of High−side and Low−side slope and offset

TYPICAL CHARACTERISTICS

(Tests at T_A = 25°C, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

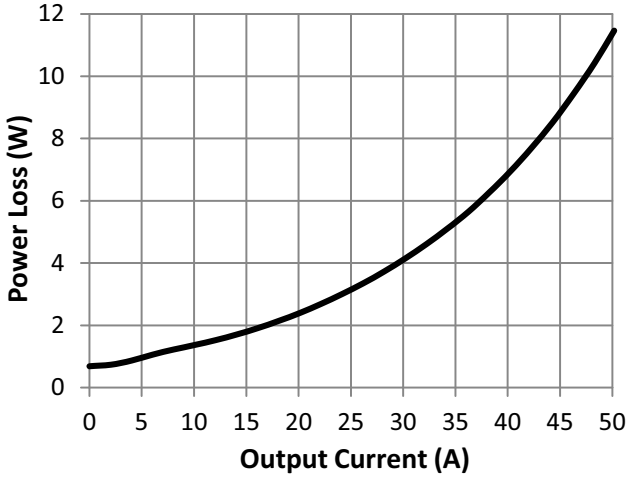


Figure 4. Power Loss vs. Output Current

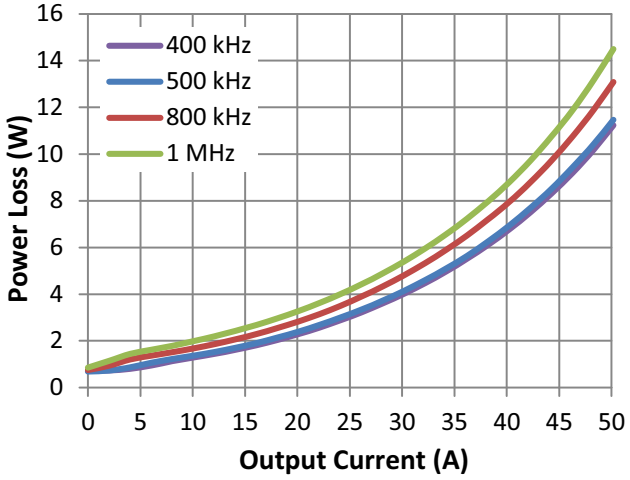


Figure 5. Power Loss vs. Switching Frequency

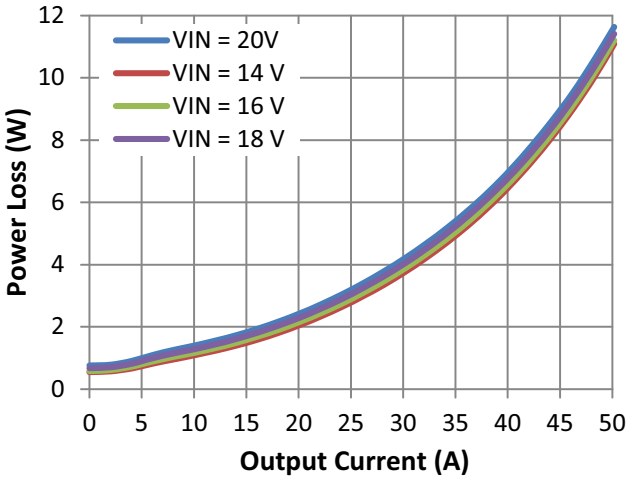


Figure 6. Power Loss vs. Input Voltage

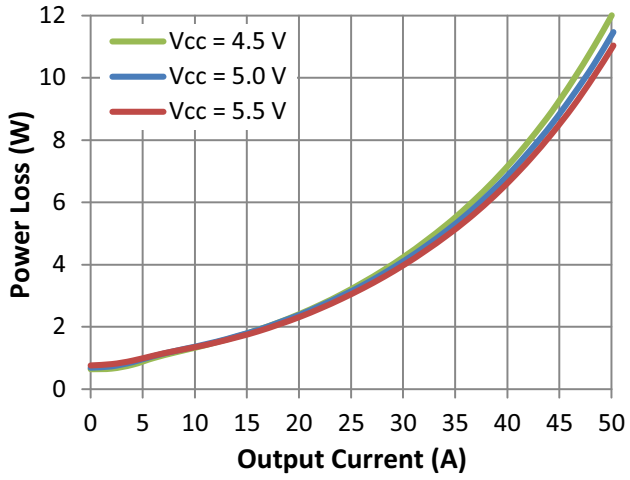


Figure 7. Power Loss vs. Driver Voltage

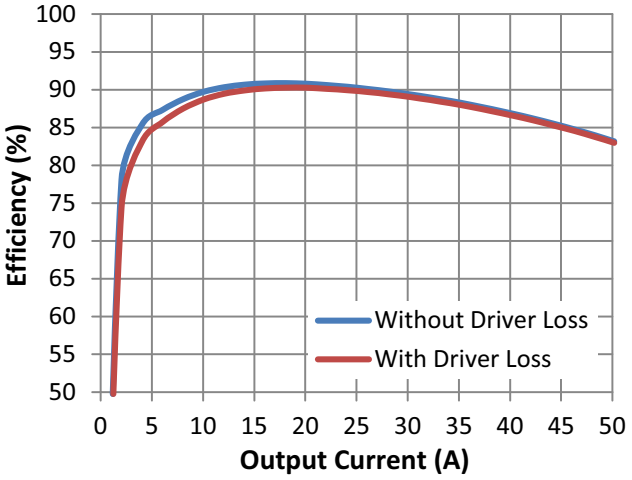


Figure 8. Efficiency vs. Output Load

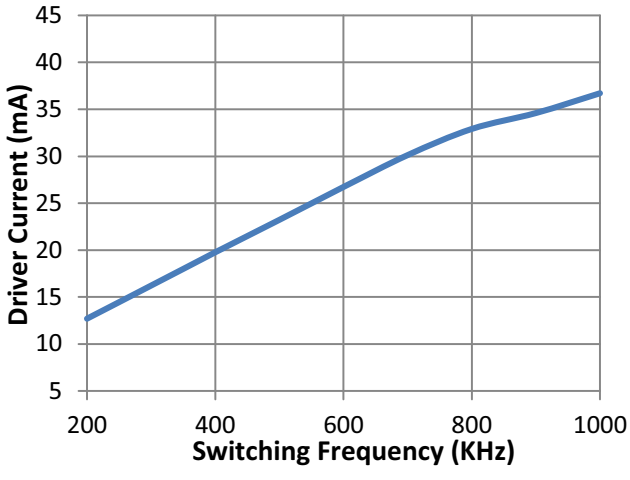


Figure 9. Driver Supply Current vs. Switching Frequency

TYPICAL CHARACTERISTICS

(Tests at T_A = 25°C, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

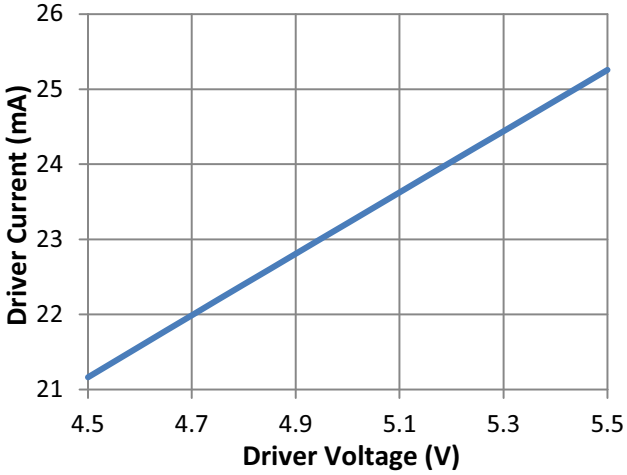


Figure 10. Driver Current vs. Driver Voltage

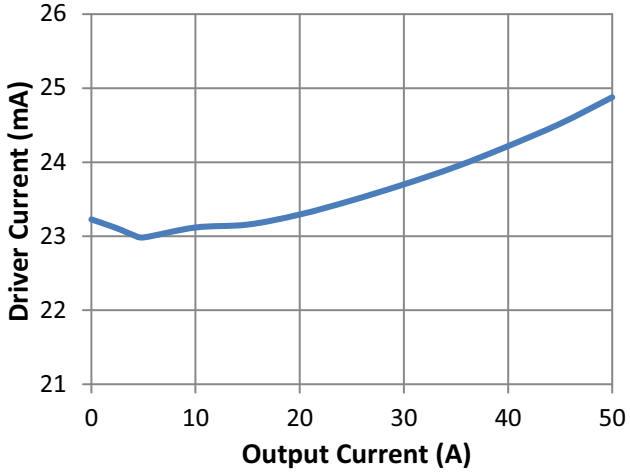


Figure 11. Driver Current vs. Output Current

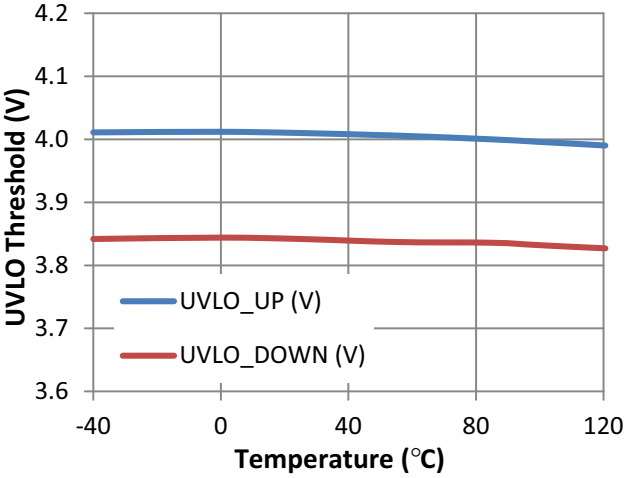


Figure 12. UVLO Threshold vs. Temperature

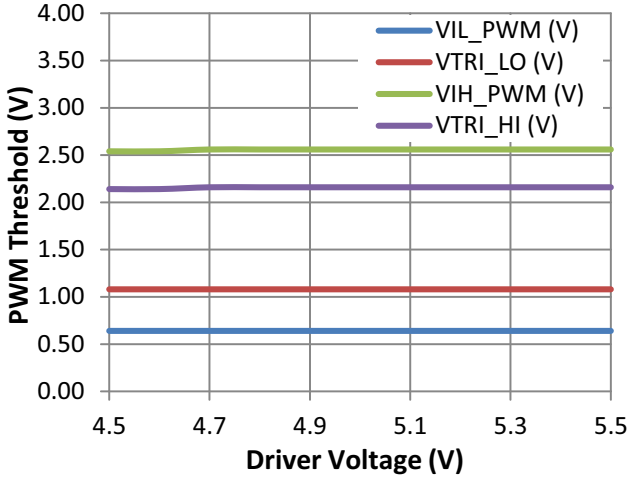


Figure 13. PWM Threshold vs. Driver Voltage

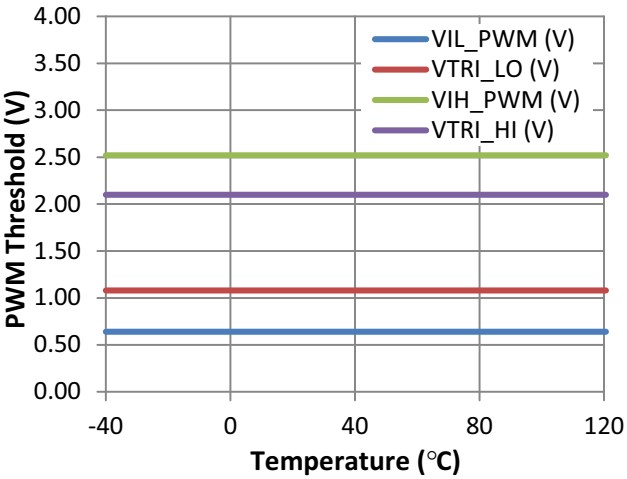


Figure 14. PWM Threshold vs. Temperature

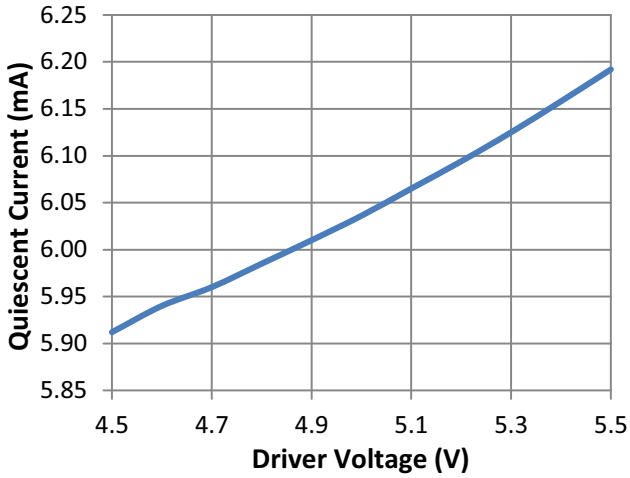


Figure 15. Quiescent Current vs. Driver Voltage

TYPICAL CHARACTERISTICS

(Tests at T_A = 25°C, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

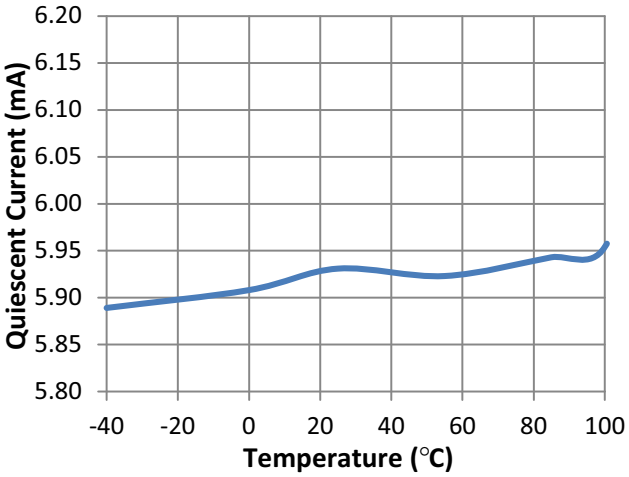


Figure 16. Quiescent Current vs. Temperature

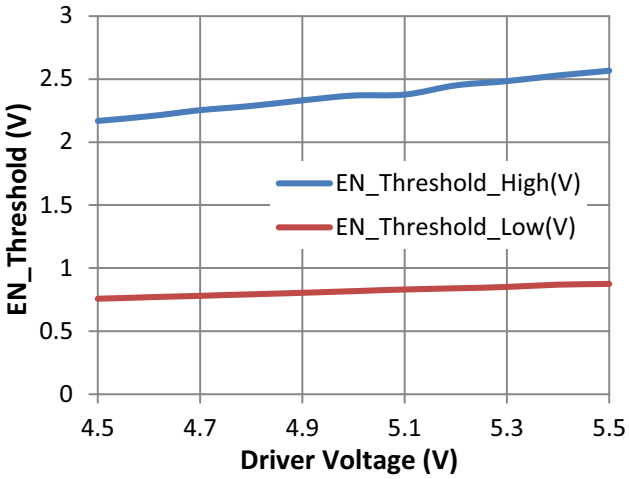


Figure 17. EN Threshold vs. Driver Voltage

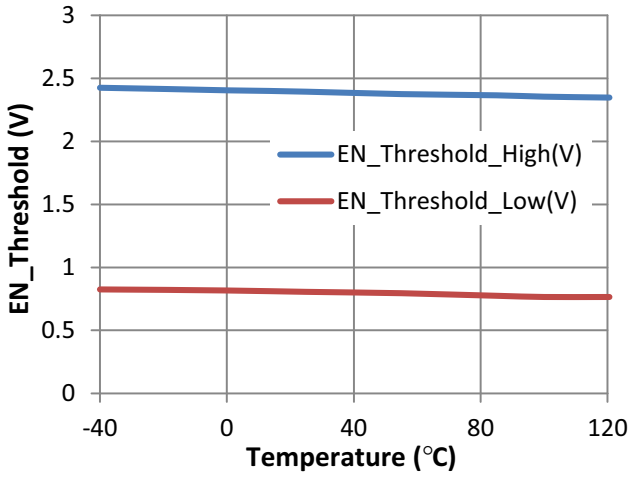


Figure 18. EN Threshold vs. Temperature

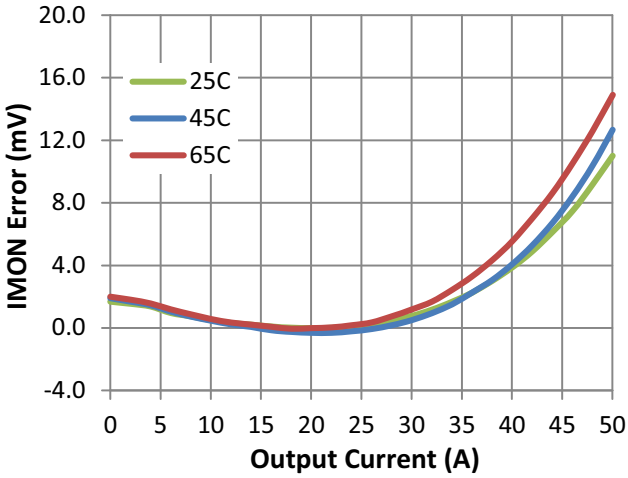


Figure 19. I_{MON} Accuracy vs. Temperature

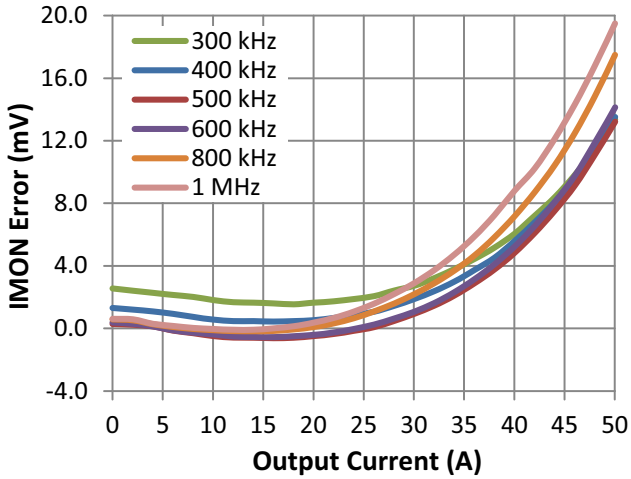


Figure 20. I_{MON} Accuracy vs. Switching Frequency

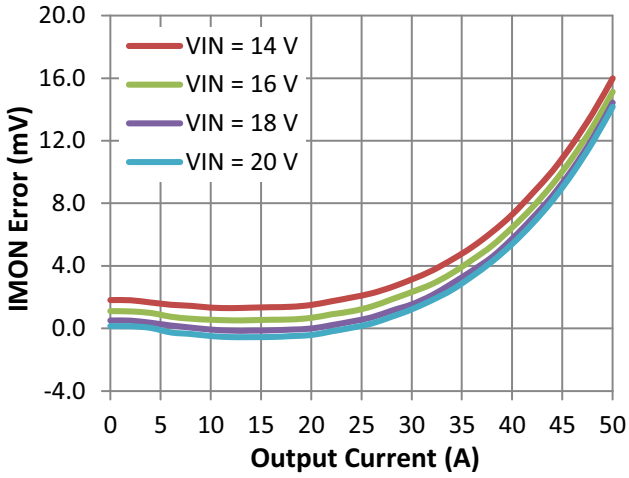


Figure 21. I_{MON} Accuracy vs. Input Voltage

TYPICAL CHARACTERISTICS

(Tests at T_A = 25°C, V_{CC} = 5 V, V_{IN} = 19 V, and V_O = 1 V unless otherwise specified)

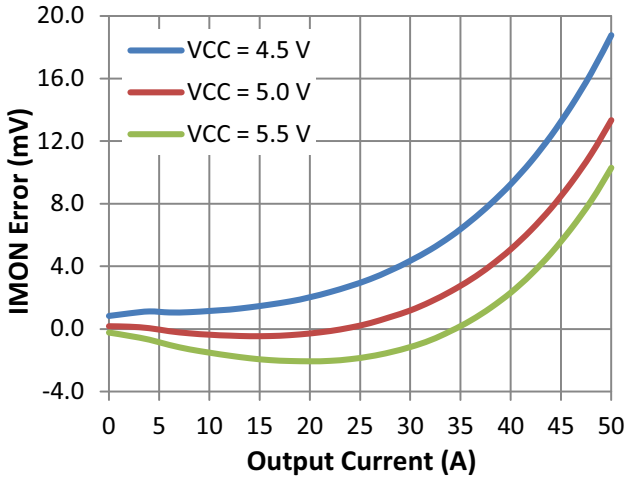


Figure 22. I_{MON} Accuracy vs. Driver Voltage

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FUNCTIONAL DESCRIPTION

The SPS NCP303150 is a driver plus MOSFET module optimized for the synchronous buck converter topology. A PWM input signal is required to properly drive the high−side and the low−side MOSFETs. The part is capable of driving speed up to 1 MHz.

DISB# and UVLO

The SPS NCP303150 is enabled by both DISB# pin input signal and V_{CC} UVLO. Table 6 summarizes the enable and disable logics. With DISB# low and VCC UVLO, SPS is fully shut down. If VCC is ready but DISB# is low, SPS goes into sleep mode with very low Quiescent current, where only critical circuitry are alive. The part should also read fuses/program itself during this state.

Table 6. UVLO AND DRIVER STATE

VCC UVLO	DISB#	Driver State
0	X	Full driver shutdown (GH, GL=0), requires 40 μs for start−up
1	0	Partial driver shutdown (GH, GL=0), requires 30 μs for startup
1	1	Enabled (GH/GL follow PWM)
X	Open/0	Disabled (GH, GL=0)

NCP303150 needs 40 μs time to go from fully shutdown mode to power ready mode. The time is 30 μs to go from partial shutdown mode to power ready mode. Before power is ready, FAULT pin is strongly pulled low with a 50 Ω resistor. As a result, FAULT pin can also be used as a power ready indicator.

Zero Current Detect Enable Input (ZCD_EN)

The ZCD_EN pin is a logic input pin with an internal voltage divider connected to VCC.

When ZCD_EN is set low, the NCP303150 will operate in synchronous rectifier (PWM) mode. This means that negative current can flow in the LS MOSFET if the load current is less than 1/2 delta current in the inductor. When ZCD_EN is set high, Zero Current Detect PWM (ZCD_PWM) mode will be enabled.

With ZCD_EN set high, if PWM falls to less than VPWM_HI, but stays above VPWM_LO, GL will go high after the non−overlap delay, and stay high for the duration of the ZCD Blanking time. Once this timer has elapsed, VSW will be monitored for zero current, and GL will be pulled low when zero current is detected.

With ZCD_EN set mid (open), if the PWM goes to low, GL will go high after the non−overlap delay, and stay high for the duration of the ZCD Blanking time. Once this timer has elapsed, VSW will be monitored for zero current, and GL will be pulled low when zero current is detected.

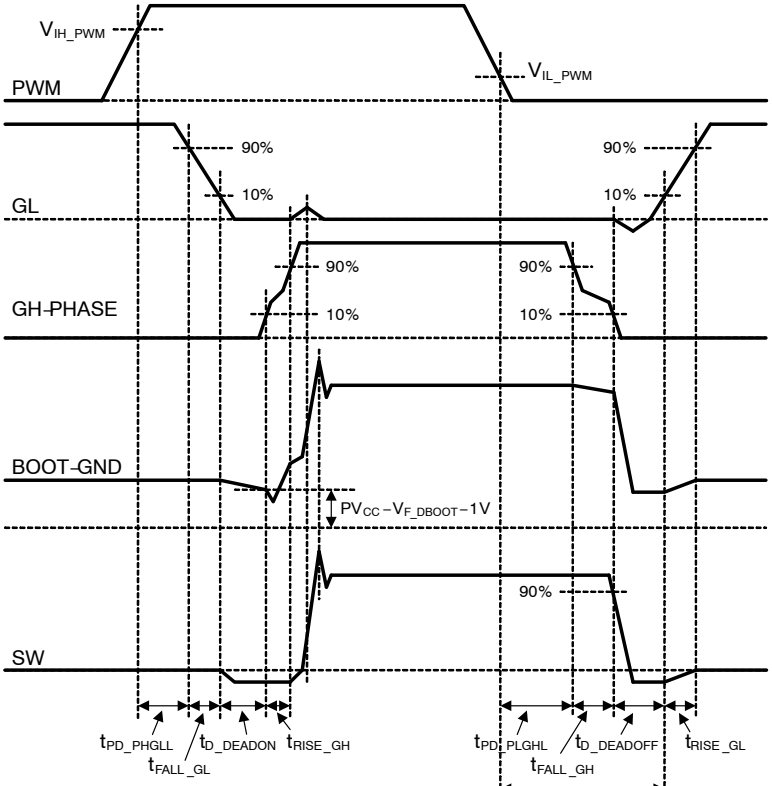
PWM

The PWM Input pin is a tri−state input used to control the HS MOSFET ON/OFF state. It also determines the state of the LS MOSFET. See Table 7 for logic operation with ZCD_EN.

There is a minimum PWM pulse width, typical at 37 ns (SW gate rising 10% to falling 10%), if the PWM input pulse width is shorter than that, the driver will extend the pulse width to 37 ns. If the PWM input is shorter than 5 ns, the driver will ignore it.

Table 7. LOGIC TABLE

INPUT TRUTH TABLE				
DISB#	ZCD_EN	PWM	GH	GL
L	X	X	L	L
H	H	H	H	L
H	H	L	L	H
H	H	MID	L	ZCD
H	L	H	H	L
H	L	L	L	H
H	L	MID	L	L
H	MID	H	H	L
H	MID	L	L	ZCD
H	MID	MID	L	L



t_{PD_PHGLL} = PWM HI to GL LO , V_{IH_PWM} to 90% GL
t_{FALL_GL} = 90% GL to 10% GL
t_{D_DEADON} = LS Off to HS On Dead Time , 10% GL to $V_{BOOT-GND}$ <= $PV_{CC} - V_{F_DBOOT} - 1V$ or BOOT -GND dip start point
t_{RISE_GH} = 10% GH to 90% GH, $V_{BOOT-GND}$ <= $PV_{CC} - V_{F_DBOOT} - 1V$ or BOOT -GND dip start point to GL bounce start point

t_{PD_PLGHL} = PWM LO to GH LO , V_{IL_PWM} to 90% GH or BOOT -GND decrease start point , $t_{PD_PLGLH} - t_{D_DEADOFF} - t_{FALL_GH}$
t_{FALL_GH} = 90% GH to 10% GH, BOOT -GND decrease start point to 90% V_{SW} or GL dip start point
$t_{D_DEADOFF}$ = HS Off to LS On Dead Time , 90% V_{SW} or GL dip start point to 10% GL
t_{RISE_GL} = 10% GL to 90% GL
t_{PD_PLGLH} = PWM LO to GL HI , V_{IL_PWM} to 10% GL

Figure 23. PWM Timing Diagram

For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP303150 to conduct zero current detection during discontinuous conduction mode (DCM).

The ZCD_EN pin needs to either be set to 5 V or left disconnected. The NCP303150 has an internal voltage divider connected to VCC that will set ZCD_EN to the logic mid state if this pin is left disconnected.

A. When ZCD_EN is set to high.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid−state. Whenever PWM transitions to mid−state, GH turns off and GL turns on. GL stays on for the duration of the ZCD blanking timers. Once this timer expires, the NCP303150 monitors the inductor current and turns GL off when the inductor current exceeds the ZCD threshold. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

There are three scenarios:

1. PWM from high to mid,
   Inductor current goes to zero before the ZCD blanking timer, GL is on and current goes to negative until the timer expires.
2. PWM from high to mid,
   ZCD blanking timer expires before inductor current goes to zero, GL is on until inductor current reaches zero.
3. PWM from mid to low to mid,
   ZCD blanking timer starts when PWM goes from mid to low, GL turns on. After PWM goes back to mid, driver will wait for the timer to expire to turn off GL.

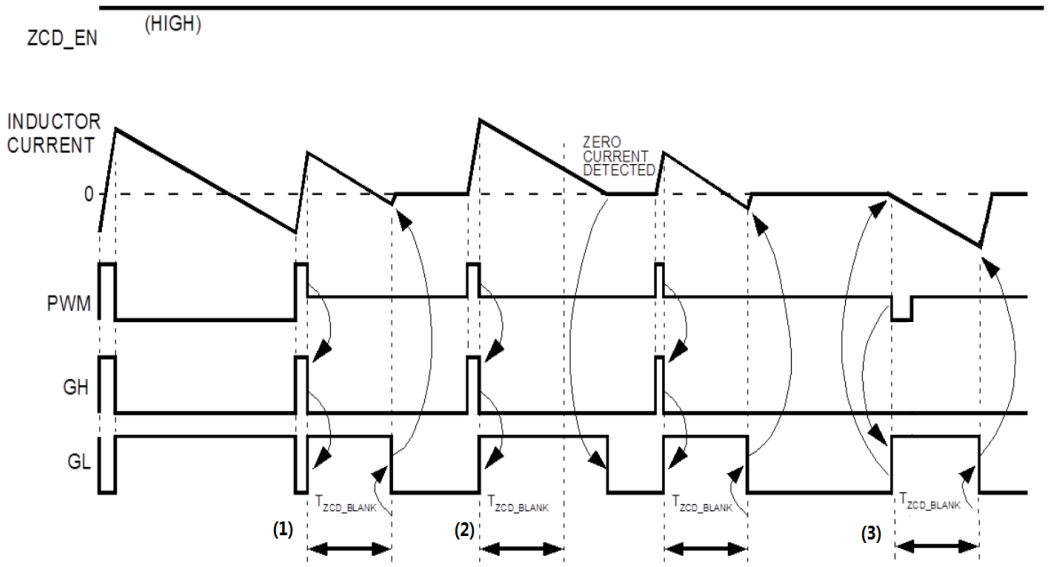


Figure 24. Timing Diagram − 3−state PWM Controller, No ZCD (a)

B. When ZCD_EN is set to mid (open).

With this setting, NCP303150 monitors the inductor current when PWM goes from high to low and turns off the GL when the inductor current exceeds the ZCD threshold.

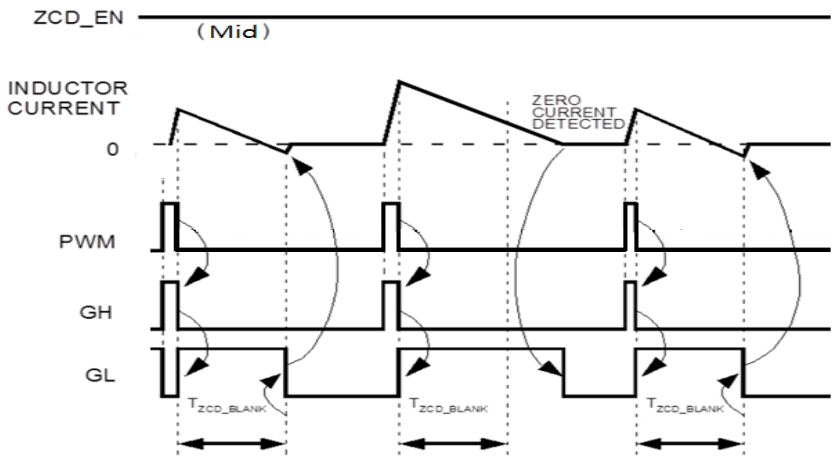


Figure 25. Timing Diagram – 3−state PWM Controller, No ZCD (b)

For Use with Controllers with 3−State PWM and Zero Current Detection Capability:

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM). The ZCD_EN pin needs to be pulled low.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP303150 to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid−state, which causes the NCP303150 to pull both GH and GL to their off states without delay.

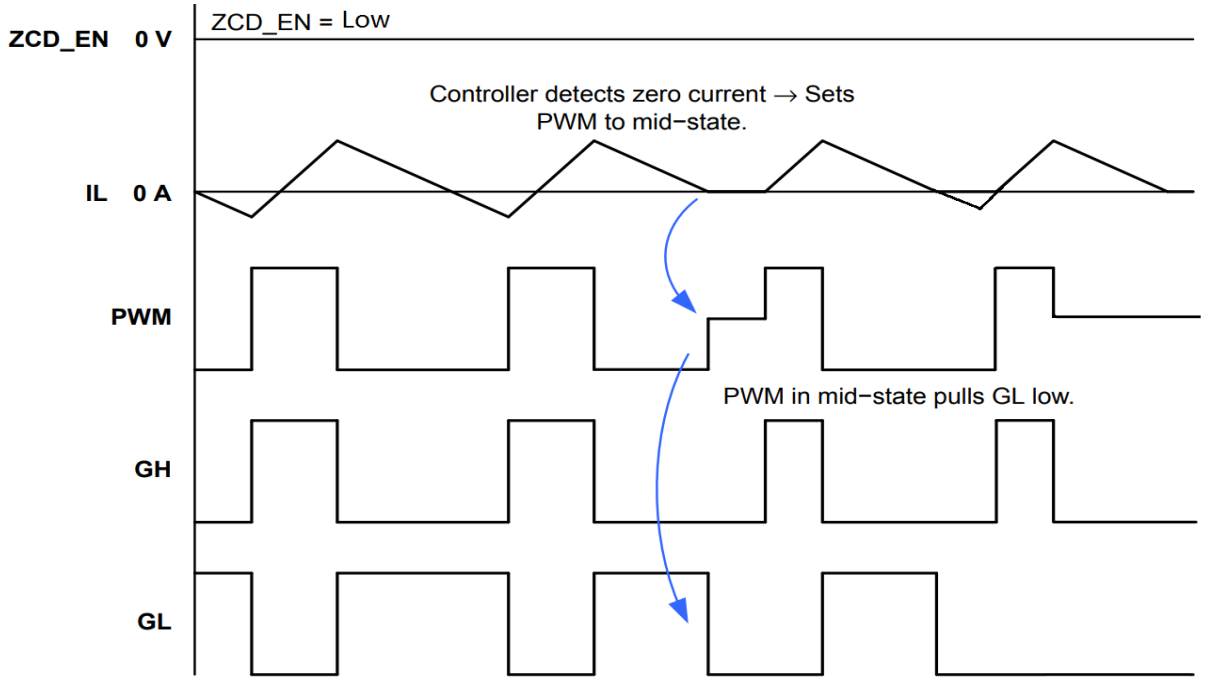


Figure 26. Timing Diagram – 3−state PWM Controller, with ZCD

Power Sequence

NCP303150 requires four (4) input signals to conduct normal switching operation: VIN, VCC, PWM, and DISB#. All combinations of power sequences are available. The below example of a power sequence is for a reference application design:

- From no input signals
  - –> VCC On: Typical 5 VDC
  - –> DISB# HIGH: Typical 5 VDC
  - –> VIN On: Typical 19 VDC
  - –> PWM Signaling: 3.3 V HIGH/ 0 V LOW

The VIN pins are tied to the system main DC power rail.

The DISB# pin can be tied to the VCC rail with an external pull−up resistor and it will maintain HIGH once the VCC rail turns on. Or the DISB# pin can be directly tied to the PWM controller for other purposes.

High−Side Driver

The high−side driver (HDRV) is designed to drive a floating N−channel MOSFET (Q1). The bias voltage for the high−side driver is developed by a bootstrap supply circuit, consisting of the internal Schottky diode and external bootstrap capacitor (C_{BOOT}). During startup, the SW node is held at PGND, allowing C_{BOOT} to charge to VCC through the internal bootstrap diode. When the PWM input goes HIGH, HDRV begins to charge the gate of the high−side MOSFET (internal GH pin). During this transition, the charge is removed from the CBOOT and delivered to the gate of Q1. As Q1 turns on, SW rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1. To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. C_{BOOT} is then recharged to VCC when the SW falls to PGND. HDRV output is in phase with the PWM input. The high−side gate is held LOW when the driver is disabled or the PWM signal is held within the 3−state window for longer than the 3−state hold−off time, $t_{D_HOLD-OFF}$.

Low−Side Driver

The low−side driver (LDRV) is designed to drive the gate−source of a ground referenced low $R_{DS(ON)}$ N−channel MOSFET (Q2). The bias for LDRV is internally connected between VCC and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the driver is disabled, LDRV is held LOW.

Dead−Times

The driver IC design ensures minimum MOSFET dead times, while eliminating potential shoot−through (cross−conduction) currents. To ensure optimal module efficiency, body diode conduction times must be reduced to the low nano−second range during CCM and DCM operation. Delay circuitry is added to prevent gate overlap during both the low−side MOSFET off to high−side MOSFET on transition and the high−side MOSFET off to low−side MOSFET on transition.

Boot Capacitor Refresh

NCP303150 monitors the low Boot−SW voltage. If DISB# and VCC are ready, but the voltage across the boot capacitor voltage is lower than 3.1 V, NCP303150 ignores the PWM input signal and starts the boot refresh circuit. The boot refresh circuit turns on the low side MOSFET with a 100 ns~200 ns narrow pulse in every 7~14 μs until Boot−SW voltage is above 3.6 V.

Current Monitor (IMON)

The SPS current monitor accurately senses high−side and low−side MOSFET currents. The currents are summed together to replicate the output filter inductor current. The signal is reported from the SPS module in the form of a 5 μA/A current signal ($I_{IMON-REFIN}$). The IMON signal will be referenced to an externally supplied signal (REFIN) and differentially sensed by an external analog/ digital PWM controller.

The motivation for the IMON feature is to replace the industry standard output filter DCR sensing, or output current sense using an external precision resistor. Both techniques are lossy and lead to reduced system efficiency. Inductor DCR sensing is also notoriously inaccurate for low value DCR inductors. Figure x shows a comparison between conventional inductor DCR sensing and the unique IMON feature.

The accuracy on IMON signal is ±5 % from 10 A to 40 A output current. For the SPS module, parameters that can affect IMON accuracy are tightly controlled and trimmed at the MOSFET/IC production stage. The user can easily incorporate the IMON feature and accuracy replacing the traditional current sensing methods in multi−phase applications.

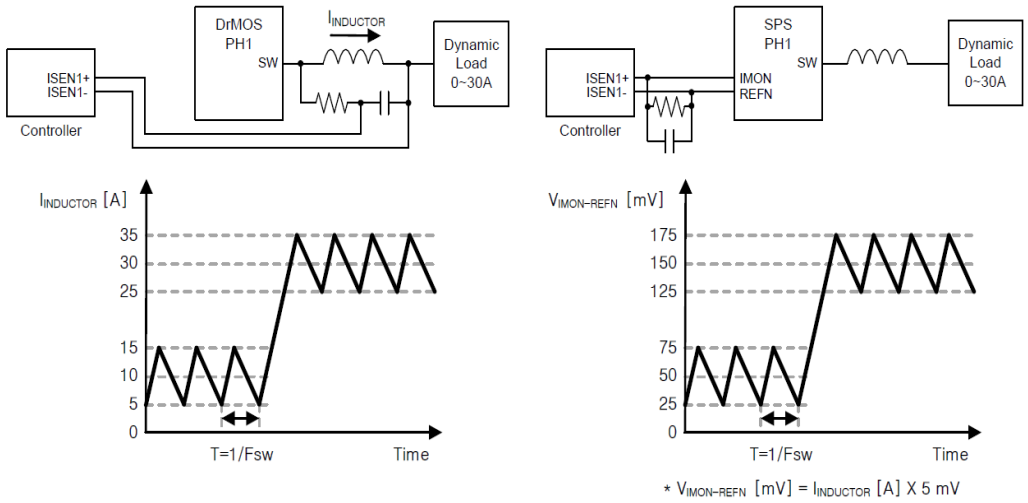


Figure 27. DrMOS with Inductor DCR Sensing vs. SPS with IMON

Fault Flag (FAULT)

Before power is ready, FAULT pin is strongly pulled low with a 50 Ω resistor. This pin is used as a module fault flag pin if there is OCP, OTW.

Over−Temperature Warning (OTW)

An over temperature event is considered catastrophic in nature. OTW raises fault flag HIGH once it exceeds 140°C temperature. Driver still responds to PWM commands. Once the IC falls below 125°C, fault flag is cleared internally by driver IC.

Over−Current Protection (OCP)

The NCP303150 has cycle−by−cycle over−current protection. If current exceeds the OCP threshold, HS FET is gated off regardless of PWM command. HS FET cannot be gated on again until the current is less than the OCP threshold with a hysteresis.

Fault flag will be pulled HIGH after 10 consecutive cycle−by−cycle OCPs are detected. Fault flag will clear once OCP is NOT detected. Module never shuts down nor does it disable HDRV/LDRV (but driver will still truncate HS on time when PWM=HIGH and ILIM is detected).

Negative−OCP

The NCP303150 can detect large negative inductor current and protect the low side MOSFET. Once this Negative current threshold is detected the driver module takes control and truncates LS on−time pulse (LS FET is gated off regardless of PWM command). The driver will stay in this state till one of two things happen 1) 200 ns expires in which case if the PWM pin is commanding the driver to turn on LS, the driver will respond and NOCP will again be monitored 2) PWM commands HS on in which case the driver will immediately turn on HS regardless of the 200 ns Timer.

APPLICATION INFORMATION

Decoupling Capacitor for VCC

For the supply input (VCC pin), local decoupling capacitor is required to supply the peak driving current and to reduce noise during switching operation. Use at least 0.68 ~ 2.2 μF/ 0402 ~ 0603/ X5R ~ X7R multi−layer ceramic capacitor for the power rail. Keep this capacitor close to the VCC pin and AGND copper planes. If it needs to be located on the bottom side of board, put through−hole vias on each pad of the decoupling capacitor to connect the capacitor pad on bottom with VCC pin on top.

The supply voltage range on VCC is 4.5 V ~ 5.5 V, typically 5 V for normal applications.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}). A bootstrap capacitor of 0.1 ~ 0.22 μF/ 0402 ~ 0603/ X5R ~ X7R is usually appropriate for most switching applications. A series bootstrap resistor may be needed for specific applications to lower high−side MOSFET switching speed. The boot resistor is required when the SPS is switching above 15 V V_{IN}; when it is effective at controlling V_{SW} overshoot. R_{BOOT} value from 2.2 to 6 Ω is typically recommended to reduce excessive voltage spike and ringing on the SW node. A higher R_{BOOT} value can cause lower efficiency due to high switching loss of high−side MOSFET.

Do not add a capacitor or resistor between the BOOT pin and GND.

It is recommended to add a PCB place holder for a small size 1 nF ~ 1 μF capacitor close to the REFIN pin and AGND to reduce switching noise injection.

It is also recommended to add a small 10 ~ 47 pF capacitor in parallel with the IMON resistor from IMON to REFIN. This capacitor can help reduce switching noise coupling onto the IMON signal. The place of the IMON resistor and cap should be close to the controller, not the SPS to improve the sensing accuracy.

PCB Layout Guideline

All of the high−current paths; such as VIN, SW, VOUT, and GND coppers; should be short and wide for low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

Input ceramic bypass capacitors must be close to the VIN and PGND pins. This reduces the high−current power loop inductance and the input current ripple induced by the power MOSFET switching operation.

An output inductor should be located close to the NCP303150 to minimize the power loss due to the SW copper trace. Care should also be taken so the inductor dissipation does not heat the SPS.

PowerTrench® MOSFETs are used in the output stage and are effective at minimizing ringing due to fast switching. In most cases, no RC snubber on SW node is required. If a snubber is used, it should be placed close to the SW and PGND pins. The resistor and capacitor of the snubber must be sized properly to not generate excessive heating due to high power dissipation.

Decoupling capacitor on VCC and BOOT capacitor should be placed as close as possible to the VCC ~ AGND and BOOT ~ PHASE pin pairs to ensure clean and stable power supply. Their routing traces should be wide and short to minimize parasitic PCB resistance and inductance.

The board layout should include a placeholder for small−value series boot resistor on BOOT ~ PHASE. The boot−loop size, including series R_{BOOT} and C_{BOOT}, should be as small as possible.

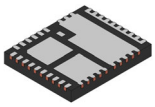
A boot resistor may be required and it is effective to control the high−side MOSFET turn−on slew rate and SW voltage overshoot. R_{BOOT} can improve noise operating margin in synchronous buck designs that may have noise issues due to ground bounce or high positive and negative VSW ringing. Inserting a boot resistance lowers the SPS module efficiency. Efficiency versus switching noise must be considered. R_{BOOT} values from 0.5 Ω to 6.0 Ω are typically effective in reducing VSW overshoot.

The VIN and PGND pins handle large current transients with frequency components greater than 100 MHz. If possible, these pins should be connected directly to the VIN and board GND planes. The use of thermal relief traces in series with these pins is not recommended since this adds extra parasitic inductance to the power path. This added inductance in series with either the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SW} ringing.

PGND pad and pins should be connected to the GND copper plane with multiple vias for stable grounding. Poor grounding can create a noisy and transient offset voltage level between PGND and AGND. This could lead to faulty operation of gate driver and MOSFETs.

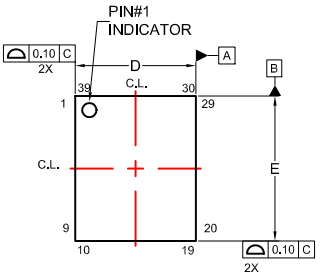
Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add any additional capacitors between BOOT to PGND. This may lead to excess current flow through the BOOT diode, causing high power dissipation.

Put multiple vias on the VIN and VOUT copper areas to interconnect top, inner, and bottom layers to evenly distribute current flow and heat conduction. Do not put too many vias on the SW copper to avoid extra parasitic inductance and noise on the switching waveform. As long as efficiency and thermal performance are acceptable, place only one SW node copper on the top layer and put no vias on the SW copper to minimize switch node parasitic noise. Vias should be relatively large and of reasonably low inductance. Critical high−frequency components; such as R_{BOOT}, C_{BOOT}, RC snubber, and bypass capacitors; should be located as close to the respective SPS module pins as possible on the top layer of the PCB. If this is not feasible, they can be placed on the board bottom side and their pins connected from bottom to top through a network of low−inductance vias.

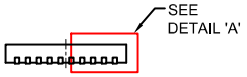


PQFN39 5X6, 0.45P
CASE 483BF
ISSUE B

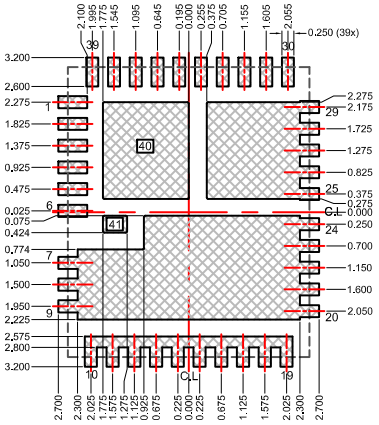
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TOP VIEW

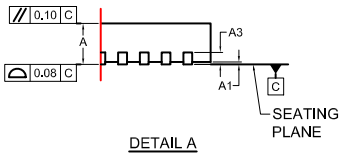


FRONT VIEW

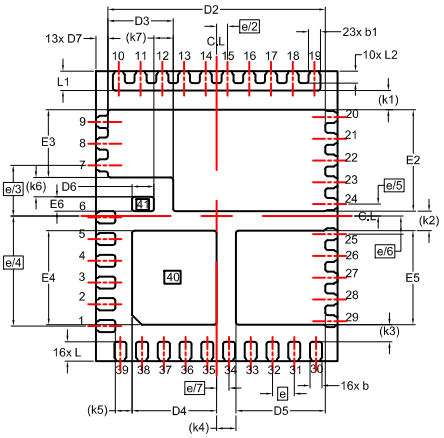


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DETAIL A
SCALE 2:1



BOTTOM VIEW
(SCALE: 2X)

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D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.20	0.25	0.30
b1	0.20	0.25	0.30
D	4.90	5.00	5.100
D2	4.40	4.50	4.60
D3	1.25	1.35	1.45
D4	1.65	1.75	1.85
D5	1.75	1.85	1.95
D6	0.35	0.45	0.55
D7	0.15	0.25	0.35
E	5.90	6.00	6.10
E2	2.00	2.10	2.20
E3	1.30	1.40	1.50
E4	1.85	1.95	2.05
E5	1.85	1.95	2.05
E6	0.20	0.30	0.40
e	0.450 BSC		
e/2	0.225 BSC		
e/3	1.050 BSC		
e/4	2.275 BSC		
e/5	0.250 BSC		
e/6	0.375 BSC		
e/7	0.255 BSC		
L	0.30	0.40	0.50
L1	0.30	0.40	0.50
L2	0.15	0.25	0.35
k1	0.40 REF		
k2	0.40 REF		
k3	0.35 REF		
k4	0.40 REF		
k5	0.35 REF		
k6	0.40 REF		
k7	0.40 REF		

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

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