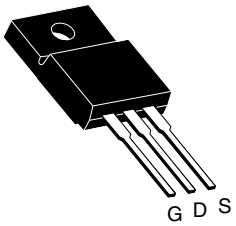
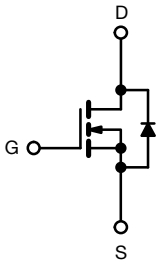
Power MOSFET

TO-220 FULLPAK





N-Channel MOSFET

FEATURES

- Low figure-of-merit R_{on} x Q_g
- 100 % avalanche tested
- Gate charge improved
- t_{rr}/Q_{rr} improved
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS* Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	560	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	1
Q_g max. (nC)	34	
Q_{gs} (nC)	7.8	
Q_{gd} (nC)	10.4	
Configuration	Single	

ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF8N50L-E3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current [a]	V_{GS} at 10 V	T_C = 25 °C	I_D	8	A
Pulsed Drain Current [b]			I_{DM}	22	
Linear Derating Factor				0.32	W/°C
Single Pulse Avalanche Energy [c]			E_{AS}	180	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	40	W
Peak Diode Recovery dV/dt [d]			dV/dt	24	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [e]	For 10 s			300	
Mounting Torque	M3 screw			0.6	Nm

Notes

a. Drain current limited by maximum junction temperature.
b. Repetitive rating; pulse width limited by maximum junction temperature.
c. V_{DD} = 50 V, starting T_J = 25 °C, L = 10 mH, R_g = 25 Ω, I_{AS} = 6 A.
d. $I_{SD} \leq 8$ A, dI/dt ≤ 460 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
e. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.5	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	50	µA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 4.0 A	-	0.85	1	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3 A	-	2	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz	-	873	-	pF
Output Capacitance	C_{oss}		-	105	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 6 A, V_{DS} = 400 V	-	22	34	nC
Gate-Source Charge	Q_{gs}		-	7.8	-	
Gate-Drain Charge	Q_{gd}		-	10.4	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250 V, I_D = 6 A, R_G = 14 Ω, V_{GS} = 10 V	-	17.3	-	ns
Rise Time	t_r		-	35	-	
Turn-Off Delay Time	$t_{d(off)}$		-	23.6	-	
Fall Time	t_f		-	17	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	0.7	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8	A
Pulsed Diode Forward Current	I_{SM}		-	-	22	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8 A, V_{GS} = 0 V	-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S, dI/dt = 100 A/µs, V_R = 15 V	-	63	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	114	-	nC
Body Diode Reverse Recovery Current	I_{RRM}		-	3.3	-	A

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

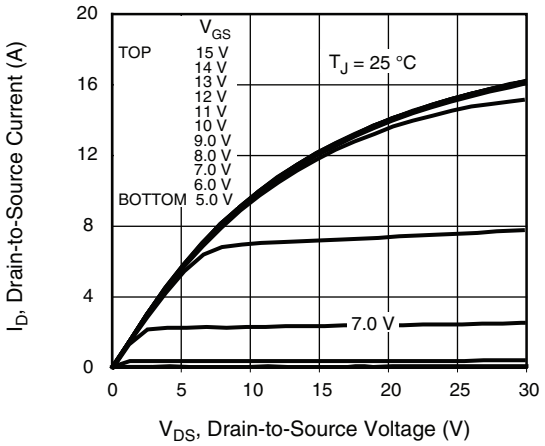


Fig. 1 - Typical Output Characteristics

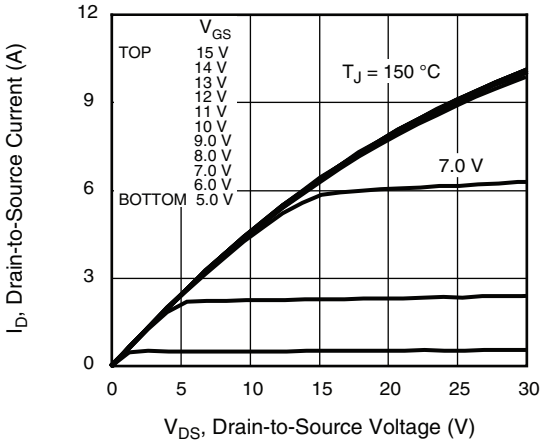


Fig. 2 - Typical Output Characteristics

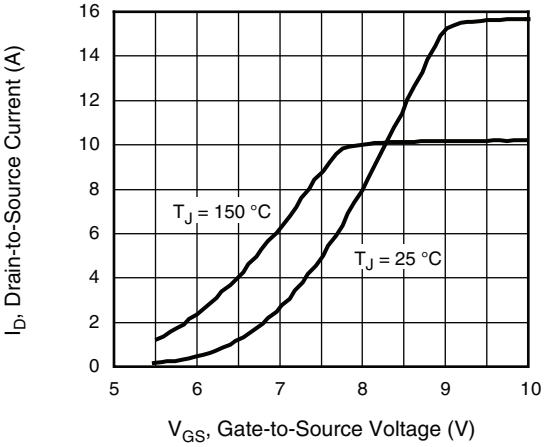


Fig. 3 - Typical Transfer Characteristics

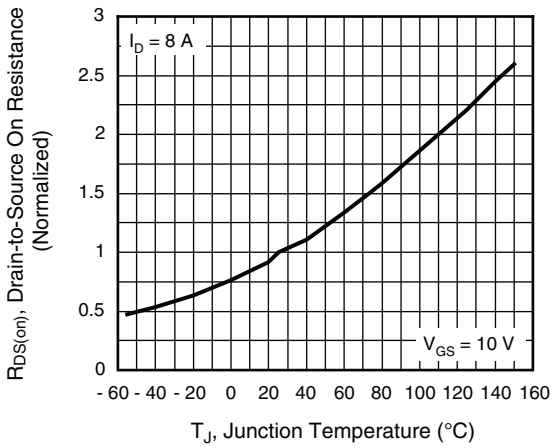


Fig. 4 - Normalized On-Resistance vs. Temperature

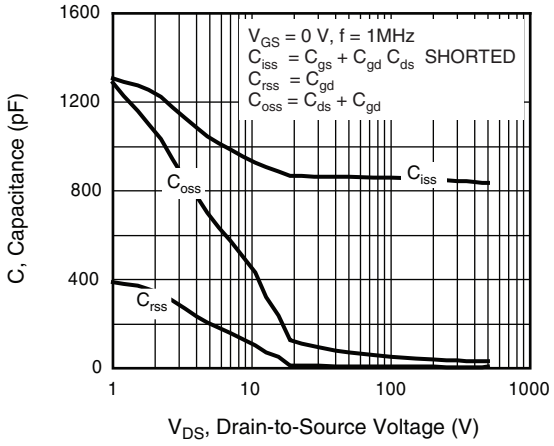


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

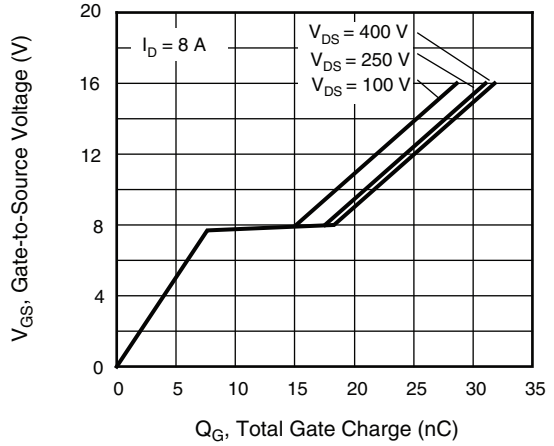


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

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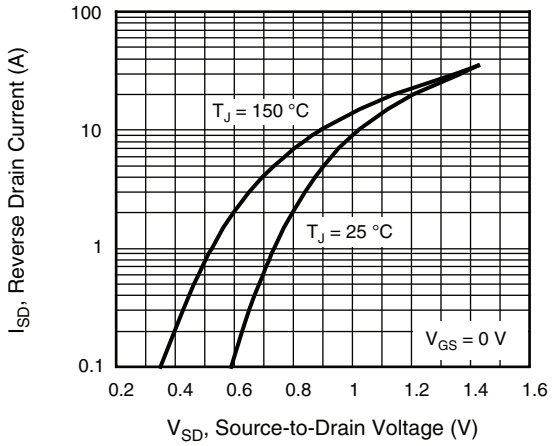


Fig. 7 - Typical Source-Drain Diode Forward Voltage

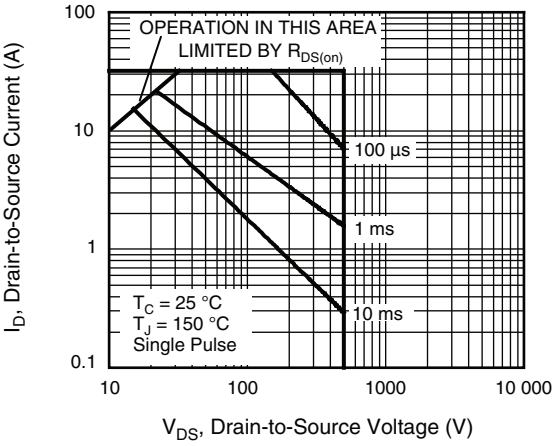


Fig. 8 - Maximum Safe Operating Area

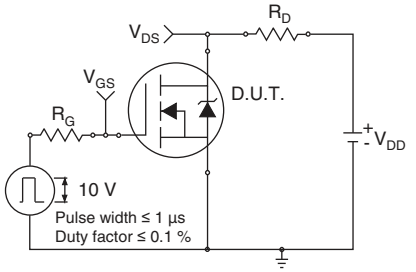


Fig. 9a - Switching Time Test Circuit

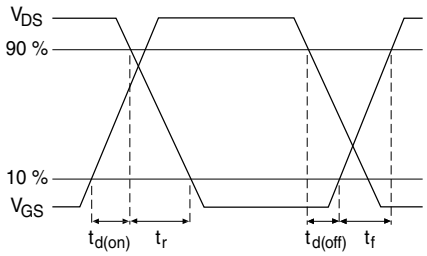


Fig. 9b - Switching Time Waveforms

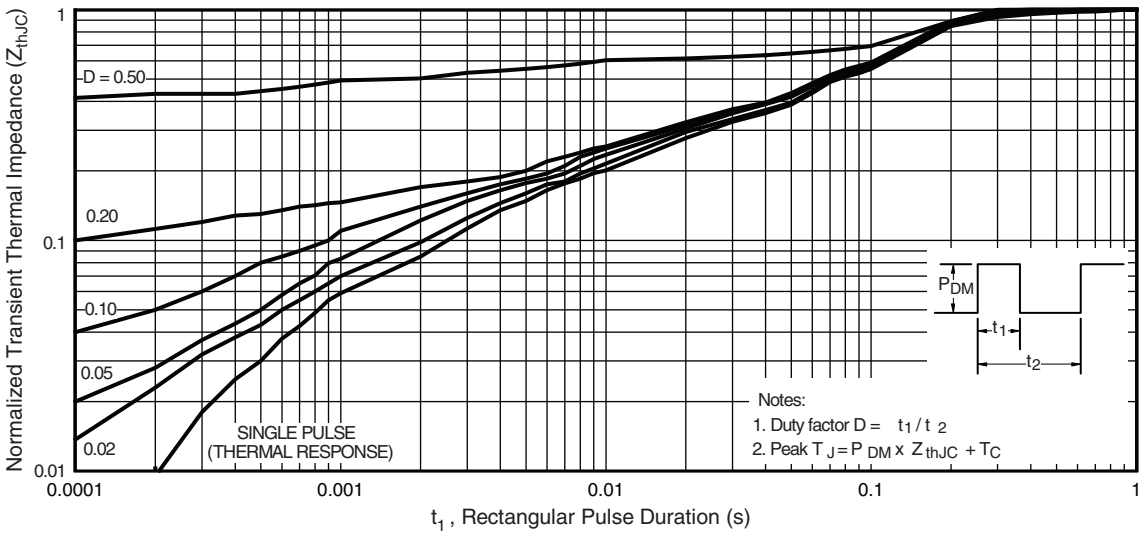


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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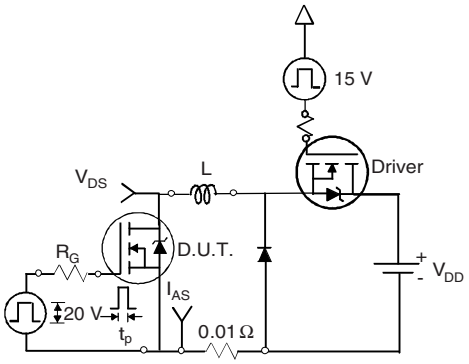


Fig. 11a - Unclamped Inductive Test Circuit

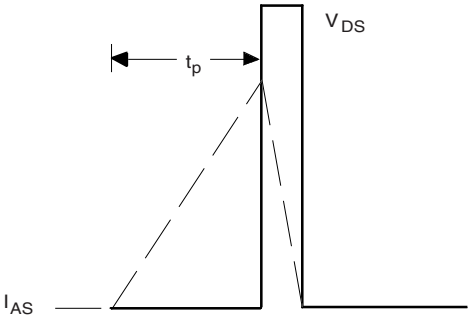


Fig. 11b - Unclamped Inductive Waveforms

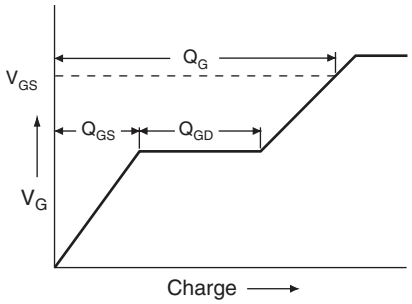


Fig. 12a - Basic Gate Charge Waveform

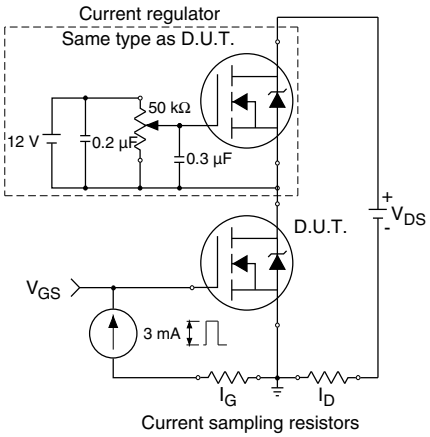
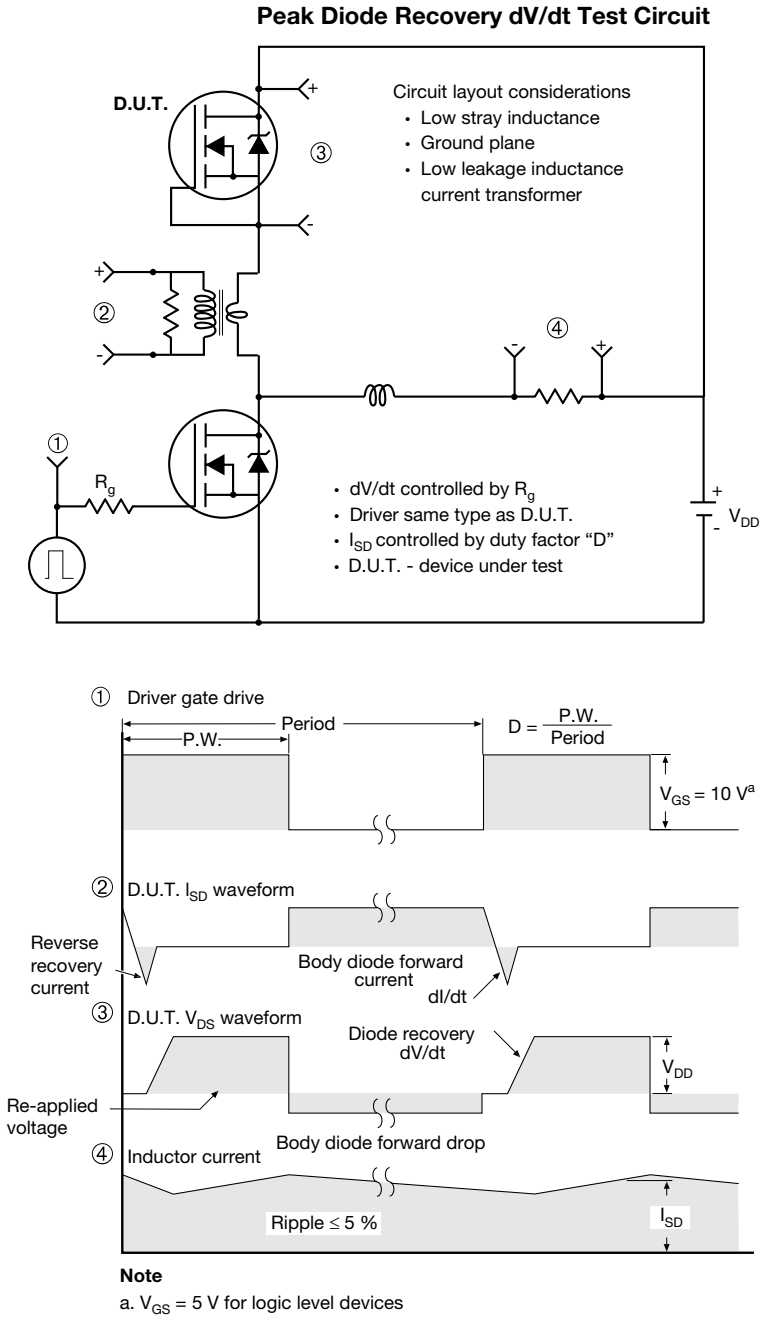


Fig. 12b - Gate Charge Test Circuit

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Note

a. V_{GS} = 5 V for logic level devices

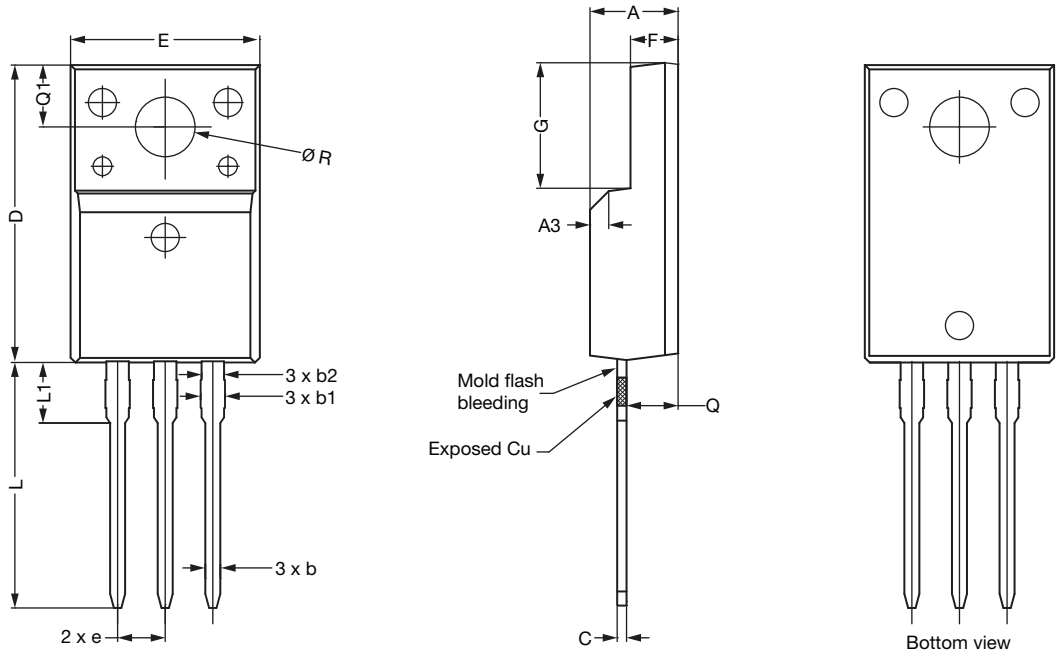
Fig. 13 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



	MILLIMETERS		
DIM.	**MIN.**	**NOM.**	**MAX.**
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e		2.54 BSC	
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

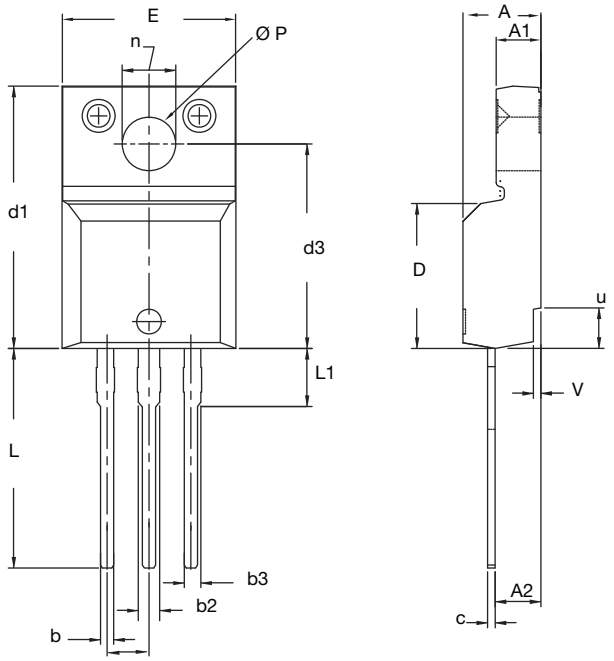
Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking

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OPTION 2: FACILITY CODE = Y



	MILLIMETERS		INCHES	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020
ECN: E19-0180-Rev. D, 08-Apr-2019 DWG: 5972				

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
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