MPQ1922

100V, 3A, Half-Bridge Pre-Driver IC, AEC-Q100 Qualified

DESCRIPTION

The MPQ1922 is a 100V, single-channel, integrated circuit (IC) gate driver designed for motor driver applications and other power control applications. The two N-channel power MOSFETs are set up in a half H-bridge configuration, and operate on power supplies up to 100V. The device is qualified to AEC-Q100 for automotive use.

The MPQ1922 combines a bootstrap (BST) capacitor and an internal charge pump to generate a supply voltage of the high-side MOSFET (HS-FET) driver. The device's HS-FET driver generates a voltage above the power supply, which in many cases indefinitely maintains a high output at 100% duty cycle operation.

The half-bridge pre-driver features configurable slew rate control, FET desaturation protection, adjustable dead-time control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ1922 is available in a QFN-22 (4mmx5mm) package with an exposed thermal pad.

FEATURES

- Supports 100V Supply Operation
- 3A Source, 4A Sink Gate Drive Current
- Internal Charge Pump and Auto-Refresh for High-Side (HS) Gate Drive
- Integrated Current-Sense Amplifier
- Low-Power Sleep Mode
- Programmable Controlled Slew Rate
- Desaturation Protection of External MOSFETs
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package
- Available in a QFN-22 (4mmx5mm) Package with Wettable Flank
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Brushless DC (BLDC) Motor and Permanent Magnet Synchronous Motor (PMSM) Drives
- High-Current Brushed DC Motor Drives
- Automotive Pumps, Fans, Superchargers, and Actuators
- Power Drills
- E-Bikes

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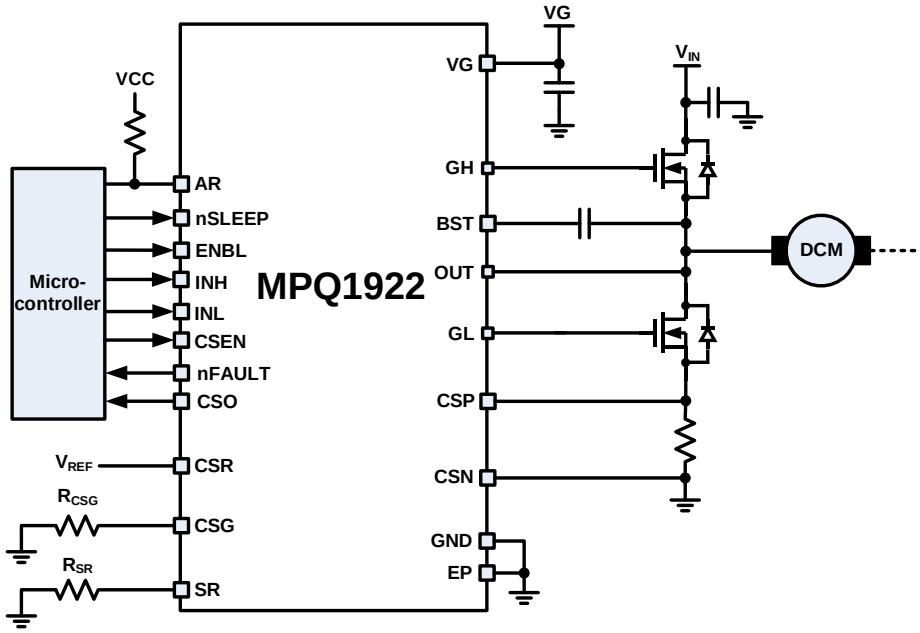
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ1922GV-AEC1*	QFN-22 (4mmx5mm)	*See Below*	*2*
MPQ1922GVE-AEC1**	QFN-22 (4mmx5mm)	*See Below*	*2*

* For Tape & Reel, add suffix -Z (e.g. MPQ1922GV-AEC1-Z).
** Wettable Flank

TOP MARKING (MPQ1922GV-AEC1)

MPSYWW
MP1922
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP1922: Part number
LLLLLL: Lot number

TOP MARKING (MPQ1922GVE-AEC1)

MPSYWW
MP1922
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP1922: Part number
LLLLLL: Lot number
E: Wettable flank

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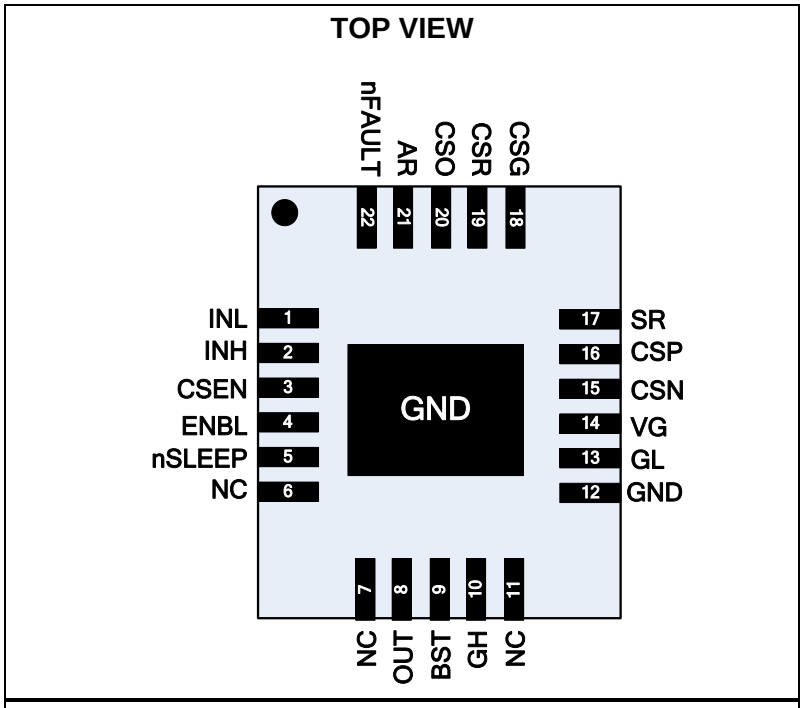
PACKAGE REFERENCE



QFN-22 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	INL	**Low-side (LS) control input.** Pull this pin logic high to turn on the low-side MOSFET (LS-FET). This pin has an internal pull-down resistor.
2	INH	**High-side (HS) control input.** Pull this pin logic high to turn on the high-side MOSFET (HS-FET). This pin has an internal pull-down resistor.
3	CSEN	**Current-sense output enable pin.** Pull this pin logic high to enable current-sense output. This pin has an internal pull-down resistor.
4	ENBL	**Enable input.** Pull this pin high to enable the part; pull it low to turn off the external FETs.
5	nSLEEP	**Sleep input.** Pull this pin logic low to enter sleep mode; pull it high for normal operation. This pin has an internal pull-down resistor.
6	NC	**Not connected.**
7	NC	**Not connected.**
8	OUT	**Half-bridge output (HS source/LS drain).**
9	BST	**Bootstrap (BST) capacitor.** Connect a ceramic capacitor between BST and OUT.
10	GH	**HS gate drive output.**
11	NC	**Not connected.**
12, exposed pad	GND	**Ground.**
13	GL	**LS gate drive output.**
14	VG	**Gate drive supply voltage.**
15	CSN	**Current-sense amplifier negative input.**
16	CSP	**Current-sense amplifier positive input.**
17	SR	**Slew rate adjustment pin.** Connect a resistor to ground to set the output slew rate.
18	CSG	**Current-sense amplifier gain adjustment pin.** Connect a resistor to ground to set the current-sense amplifier gain.
19	CSR	**Current-sense amplifier reference input.** Connect CSR to the reference voltage for a zero-current output.
20	CSO	**Current-sense output.**
21	AR	**Auto-refresh programming and status pin.**
22	nFAULT	**Fault output.** Open-drain output, active low. This pin requires an external pull-up resistor.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_G).....-0.3V to +16V
BST capacitor .....-0.3V to +115V
GH (DC).....-5V to +115V
GH (<2µs transient) .....-25V to +115V
GL (DC) .....-0.3V to +16V
GL (<2µs transient).....-2V to +16V
OUT (DC).....-5V to +100V
OUT (<2µs transient). .....-25V to +100V
nSLEEP .....-0.3V to +5.5V
All other pins to GND .....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-22 (4mmx5mm)……...3.1W
Storage temperature..... -55°C to +175°C
Junction temperature .....175°C
Lead temperature (solder) .....260°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 0V to 100V
Input voltage (V_G) ..... 5V to 15V
Operating junction temp (T_J).....-40°C to +165°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN-22 (4mmx5mm)…….…….	40	9°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_G = 12V, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Gate drive supply voltage	V_G		5		15	V
VG quiescent current	I_{GQ}	nSLEEP = 1, not switching		800		µA
	I_{G_SLEEP}	nSLEEP = 0		0.1		µA
Control Logic						
Low input logic threshold	V_{IL}	INH, INL, CSEN, nSLEEP			0.8	V
High input logic threshold	V_{IH}	INH, INL, CSEN, nSLEEP	2.2			V
ENBL rising threshold	$V_{ENBL(H)}$			1.2		V
ENBL falling threshold	$V_{ENBL(L)}$			1.0		V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		+20	µA
Internal pull-down resistance	R_{PD}	All logic inputs		350		kΩ
nFAULT Output (Open-Drain Output)						
Low output voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
High output leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
VG UVLO rising threshold	V_{UVLO}			3.1		V
VG UVLO hysteresis	ΔV_{UVLO}			250		mV
V_{BST} UVLO threshold	V_{BSTUV}	To initiate auto-refresh		V_G x 0.65		V
Low-side (LS) desaturation threshold voltage	V_{DSTHL}			1.9		V
High-side (HS) desaturation threshold voltage	V_{DSTHH}			V_G - 1.2		V
Desaturation deglitch time	t_{DSDEG}			2		µs
SLEEP wakeup time	t_{WAKE}			0.8		ms
Thermal shutdown	T_{TSD}			190		°C
Gate Drive Outputs						
Gate drive pull-up resistance	R_{PU}	R_{SR} = 0Ω, V_G = 12V		1.8		Ω
		R_{SR} = 10kΩ, V_G = 12V		8		
		R_{SR} = 30kΩ, V_G = 12V		25		
		R_{SR} = 100kΩ, V_G = 12V		100		
Gate drive pull-down resistance	R_{PD}	R_{SR} = 0Ω, V_G = 12V		1.4		Ω
		R_{SR} = 10kΩ, V_G = 12V		3.7		
		R_{SR} = 30kΩ, V_G = 12V		14		
		R_{SR} = 100kΩ, V_G = 12V		42		
Propagation delay	t_{PD-LH} (5)			100		ns
	t_{PD-HL} (5)			300		

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ELECTRICAL CHARACTERISTICS *(continued)*

V_G = 12V, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current-Sense Amplifier						
Amplifier gain	A_{CS}	R_{CSG} = 0Ω	158	210	265	V/V
		R_{CSG} = 10kΩ	81	105	131	
		R_{CSG} = 30kΩ	39	52.5	65	
		R_{CSG} = 100kΩ	18	21	24	
Amplifier input offset	V_{OFS}	V_{CSP} = V_{CSN} = 0V, V_{CSR} = 2V, R_{CSG} = 10kΩ	-2.2	0	+2.8	mV
Input voltage range	V_{CSP}, V_{CSN}		-0.6		+2	V
Input common mode rejection	CMRR (5)	V_{CSP} = V_{CSN} = 0V, f = DC		135		dB
Settling time	BW	A_{CS} = 20, 50pF load on the CSO pin, 50mV step		2		µs

Notes:

5) Not tested in production.

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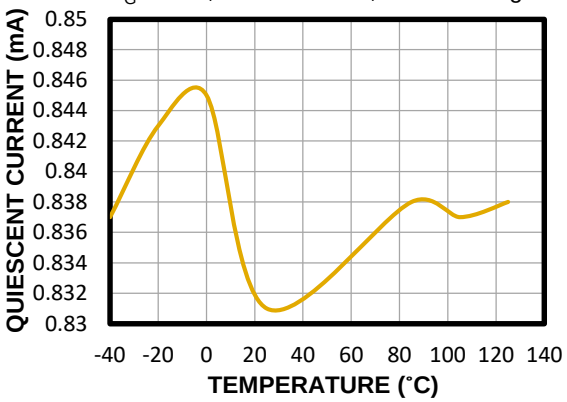
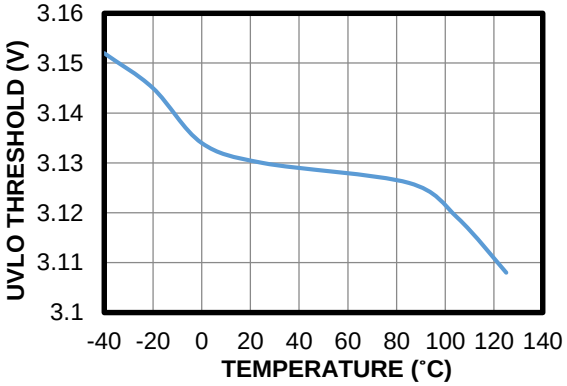
TYPICAL CHARACTERISTICS

VG Quiescent Current vs. Temperature

V_G = 12V, nSLEEP = 5V, not switching

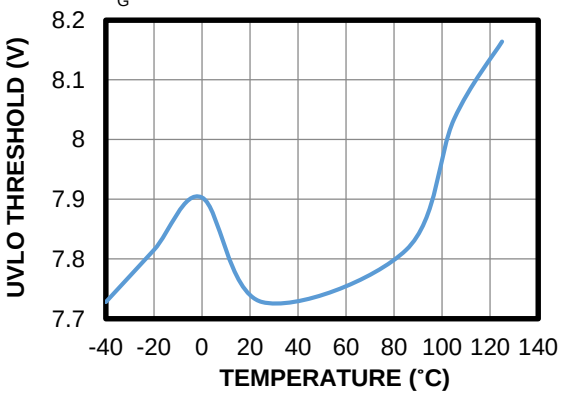


VG UVLO Threshold vs. Temperature



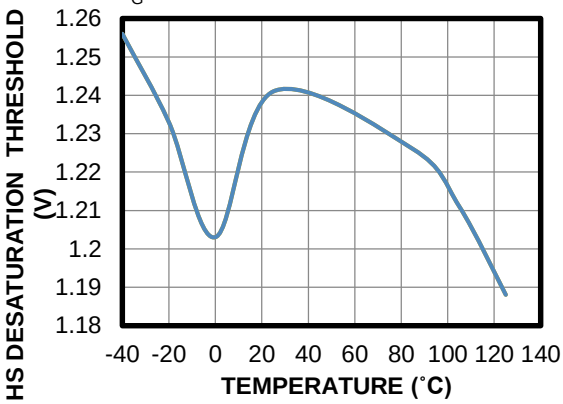
V_{BST} UVLO Threshold vs. Temperature

V_G = 12V

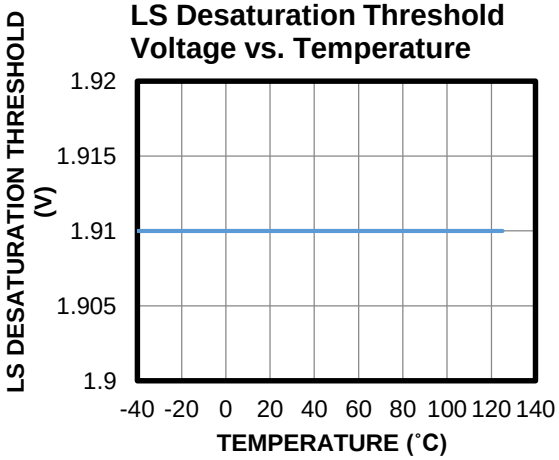


HS Desaturation Threshold Voltage vs. Temperature

V_G = 12V

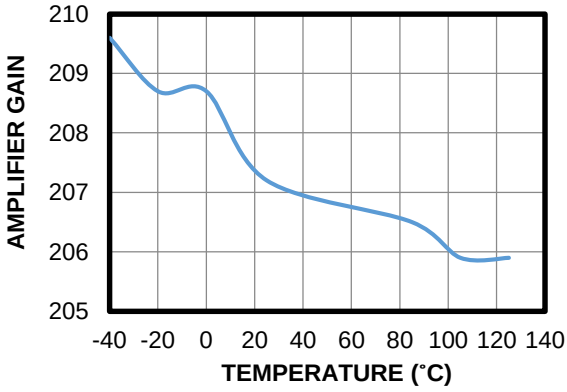


LS Desaturation Threshold Voltage vs. Temperature



Amplifier Gain vs. Temperature

R_{CSG} = 0Ω



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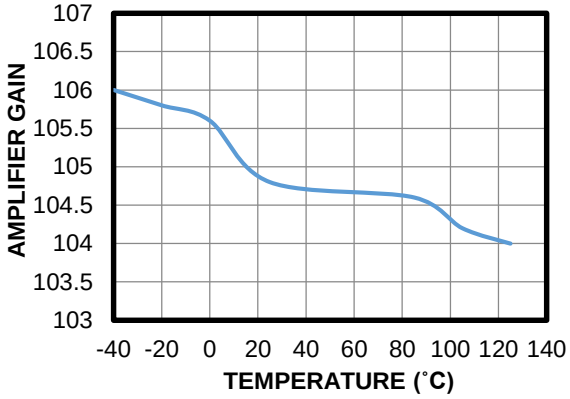
TYPICAL CHARACTERISTICS *(continued)*

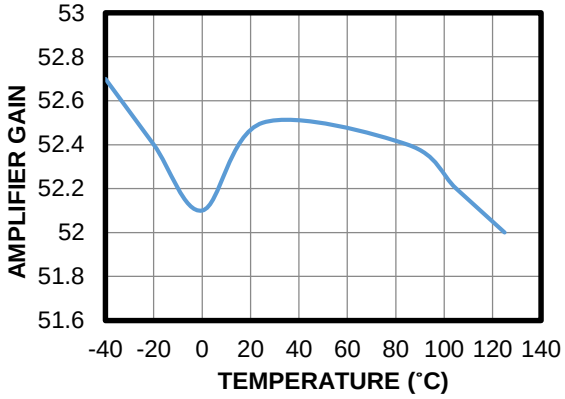
Amplifier Gain vs. Temperature

RCSG = 10kΩ



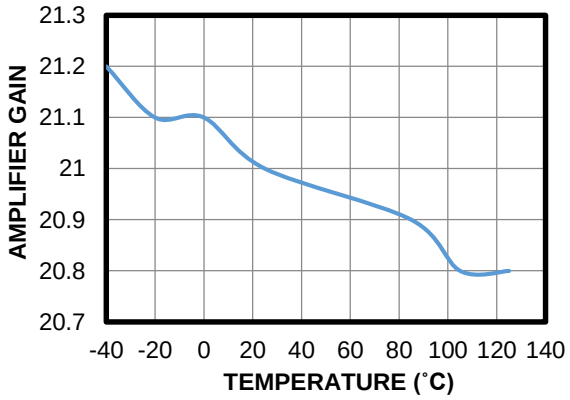
Amplifier Gain vs. Temperature

RCSG = 30kΩ



Amplifier Gain vs. Temperature

RCSG = 100kΩ



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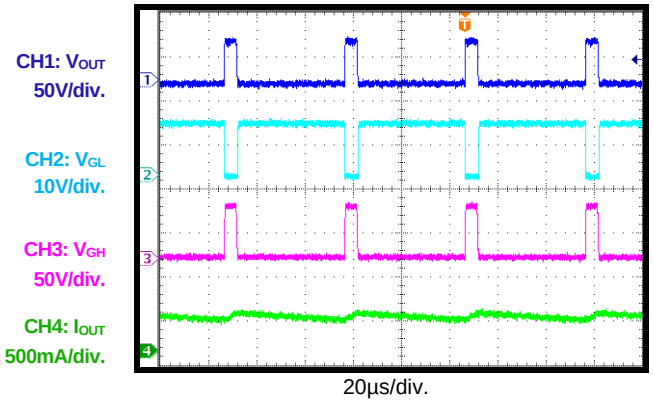
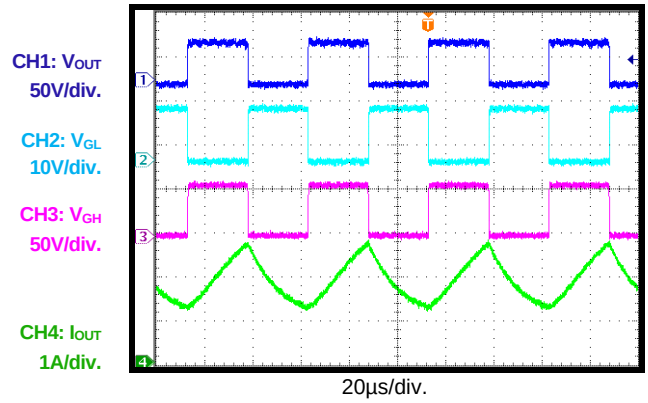
TYPICAL PERFORMANCE CHARACTERISTICS

V_G = 12V, V_{IN} = 48V, SR = CSG = 10kΩ, PWM = 20kHz, T_A = 25°C, resistor + inductor load: 10Ω + 2mH to GND, unless otherwise noted.

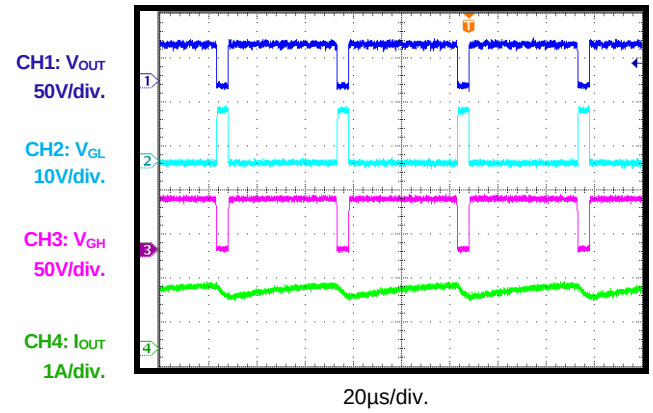
Steady State
Duty = 10%



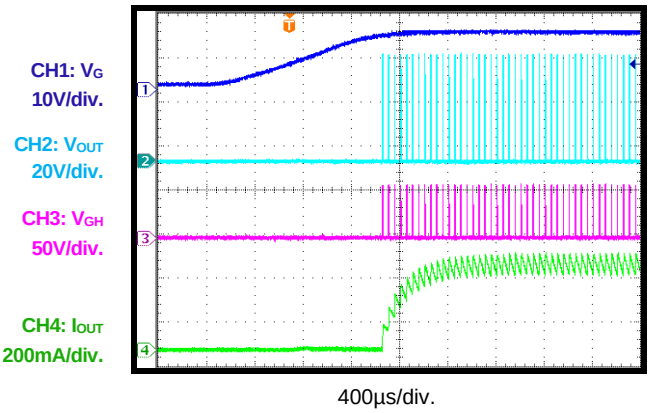
Steady State
Duty = 50%



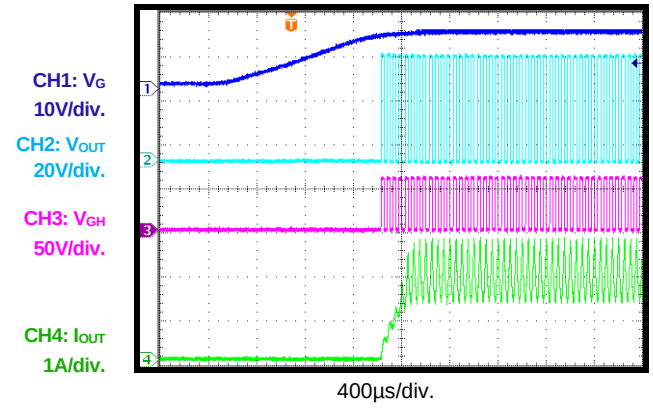
Steady State
Duty = 90%, 30Ω + 2mH load



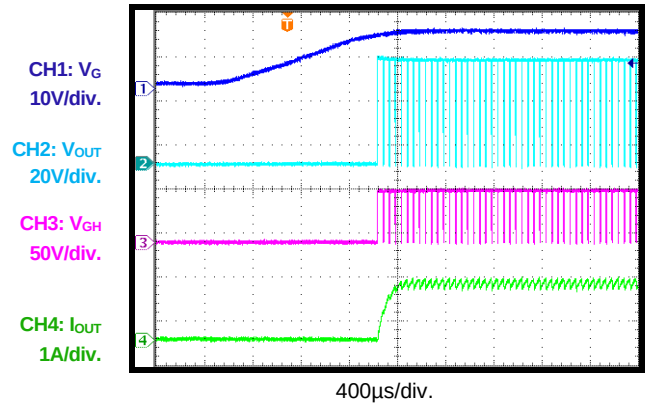
VG Power Ramping Up
Duty = 10%



VG Power Ramping Up
Duty = 50%



VG Power Ramping Up
Duty = 90%, 30Ω + 2mH load



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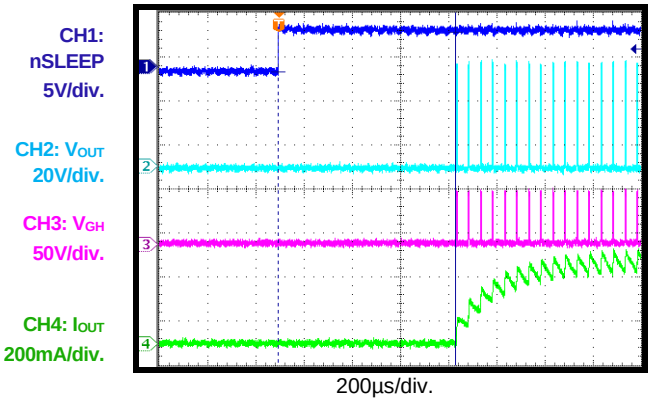
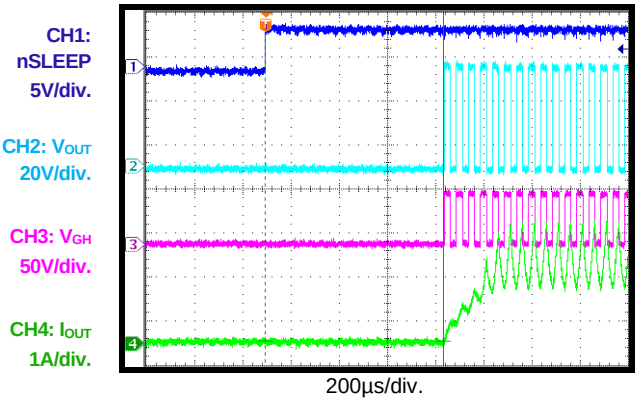
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_G = 12V, V_{IN} = 48V, SR = CSG = 10kΩ, PWM = 20kHz, T_A = 25°C, resistor + inductor load: 10Ω + 2mH to GND, unless otherwise noted.

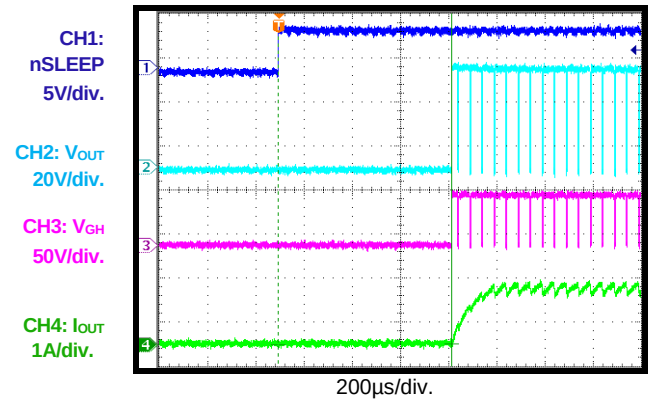
Sleep Mode Recovery
Duty = 10%



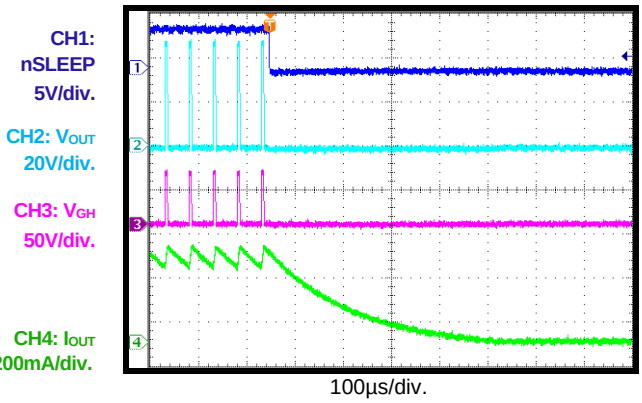
Sleep Mode Recovery
Duty = 50%



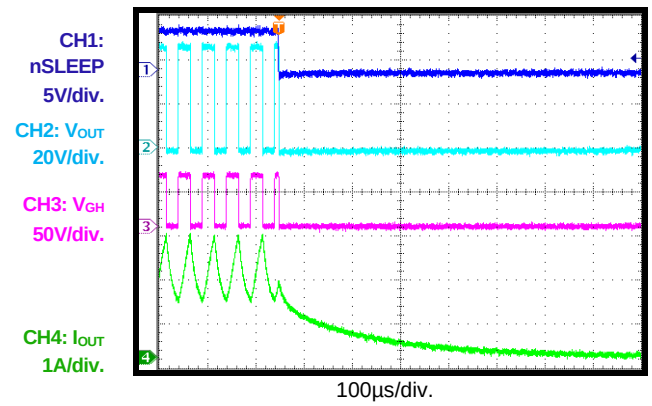
Sleep Mode Recovery
Duty = 90%, 30Ω + 2mH load



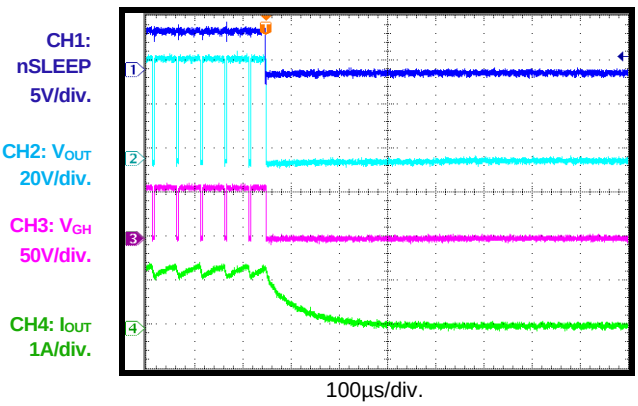
Sleep Mode Entry
Duty = 10%



Sleep Mode Entry
Duty = 50%



Sleep Mode Entry
Duty = 90%, 30Ω + 2mH load



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FUNCTIONAL BLOCK DIAGRAM

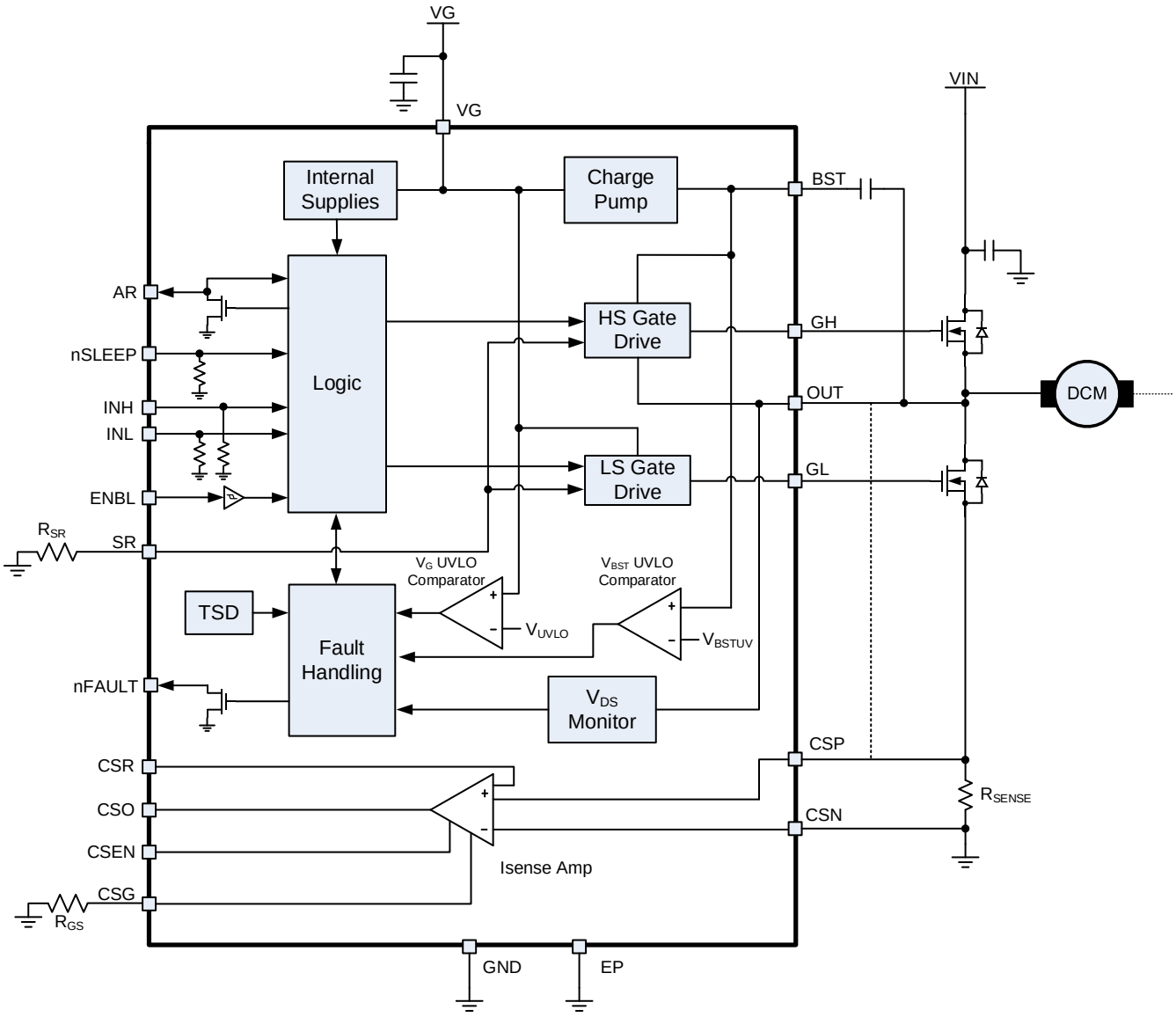

Figure 1: Functional Block Diagram

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OPERATION

The MPQ1922 is a 100V, single-channel integrated circuit (IC) half-bridge pre-driver for driving two N-channel power MOSFETs with up to 3A source and 4A sink current capability. The device also supports output supply voltages up to 100V.

The MPQ1922 features low-power sleep mode, which disables the device and draws a very low supply current. It also provides flexible functions such as configurable output slew rate, adjustable dead-time control, and output desaturation detection, which allow the device to be used in many applications.

Start-Up

Start-up is initiated by the application of voltage to the VG pin.

To initiate start-up, the VG voltage (V_G), which is the power supply voltage for the MPQ1922, must exceed the V_{UVLO} threshold (about 3.1V). After V_G exceeds this threshold, the MPQ1922 turns on the internal circuitry, including the high-side gate drive charge pump.

If auto-refresh is enabled at start-up and the AR pin is grounded, then the MPQ1922 initiates a bootstrap (BST) charge cycle by briefly turning off the high-side MOSFET (HS-FET) and turning on the low-side MOSFET (LS-FET) during start-up.

If the output is commanded high (INH = H, INL = L) before the BST charge process is complete, then a fault may be triggered due to insufficient gate drive voltage for fully turning on the HS-FET. If auto-refresh is not enabled, then the LS-FET should be turned on for at least a few microseconds to quickly charge the BST capacitor (C_{BST}). Relying on the internal charge pump to initially charge C_{BST} is not recommended due to limited current capability and the time required to provide sufficient charge to the capacitor.

The start-up process takes between 1ms and 2ms.

Sleep Operation

By driving nSLEEP low, the device enters a low-power sleep state, in which all internal circuits are disabled and all inputs are ignored. To wake up from sleep mode, about 1ms must pass for circuits to initialize and for the gate drive charge pump to start up before the device drives the FETs.

Input Logic

The INH input pin is used to control the HS-FET gate drive. The INL pin controls the LS-FET gate drive. Positive dead time is enforced by the device. If both INH and INL are driven high, then neither FET is driven (see Table 1).

Table 1: Input Logic

INL	INH	OUT
H	H	High impedance
H	L	GND
L	H	VIN
L	L	High impedance

The ENBL pin enables the outputs. When ENBL is low, both high-side (HS) and low-side (LS) gate drive outputs are pulled to ground, disabling both output FETs. The ENBL input can be used for fast protection circuits.

nFAULT

The nFAULT pin reports to the system when a fault condition, such as output FET desaturation or over-temperature (OT) is detected. nFAULT is an open-drain output, and is pulled low when a fault occurs. If the fault condition is reset by de-asserting ENBL, removing V_G, or activating nSLEEP, then the nFAULT pin is pulled high by the external pull-up resistor.

The nFAULT pin can be connected to the ENBL input pin and a pull-up resistor to make the MPQ1922 automatically restart after a fault. When a fault occurs, the nFAULT pin pulls the ENBL pin low, which resets the fault condition. After this reset, the pull-up resistor pulls ENBL high again.

Adding a capacitor in parallel with the pull-up resistor introduces a delay in re-enabling the MPQ1922 and extends the retry cycle. The RC time constant sets the retry delay.

The state of the nFAULT pin is sampled at start-up. If nFAULT is low, then the desaturation detection feature is disabled.

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Current-Sense Amplifier

An integrated current-sense amplifier magnifies the voltage difference between the CSP input pin and CSN input pin, which is outputted to the CSO pin.

The current-sense amplifier gain is programmed to one of four settings by an external resistor connected between the CSG pin and ground. Table 2 shows the current-sense gain.

Table 2: Current-Sense Gain

R_{CSG}	Gain
0Ω	210
10kΩ	105
30kΩ	52.5
100kΩ	21

The CSR pin creates a bias in the output toward a positive reference voltage corresponding to zero current. With this method, current can be measured in both positive and negative directions.

The current-sense amplifier is typically used to measure the voltage drop across an LS shunt resistor. In some special applications, the amplifier also measures the voltage drop across the LS-FET by connecting the CSP input to the drain of the LS-FET and connecting CSN to ground through blocking diodes (see Figure 2).

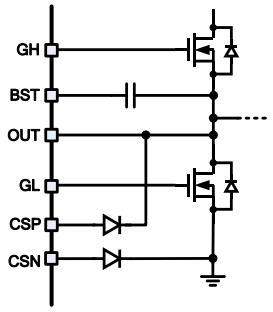

Figure 2: Measure LS-FET Voltage Drop

CSEN is an output enable pin that disables the current-sense amplifier's output. The CSEN pin therefore allows multiple MPQ1922 devices to be connected to a single analog-to-digital converter (ADC) input, with one CSO output enabled at a time to perform measurements.

To guarantee stability, the CSO pin should not be loaded with capacitance above 100pF. The CSO pin can drive about 500μA of output current (I_{OUT}).

Desaturation Detection

The voltage across both the HS-FET and LS-FET is monitored by a circuit that compares the voltage drop across the FET when it turns on to a reference voltage.

Whenever a FET is turned on, there is a blanking period, and then the voltage across the FET is compared to the reference voltage. If the FET voltage drop exceeds the reference, then the outputs are disabled and the nFAULT pin is driven active low.

The outputs remain disabled until the device is disabled by de-asserting ENBL, removing V_G, or activating nSLEEP.

High-Side (HS) Gate Drive Generation

The HS gate drive voltage is typically generated from C_{BST} (connected between the OUT pin and BST pin). Each time the LS-FET is turned on, C_{BST} is charged.

If the output is held high for a long period of time (typically several seconds), then C_{BST} slowly discharges. This discharge eventually results in the loss of the HS-FET gate drive.

To offset this leakage, an internal charge pump generates a small current to maintain the C_{BST} charge. In some cases, especially at high temperatures, this trickle current is not sufficient to maintain the voltage on C_{BST}.

The BST voltage (V_{BST}) is monitored by an under-voltage detection circuit. If the bootstrap voltage falls below the V_{BST} under-voltage lockout (UVLO) threshold, then the MPQ1922 initiates a BST refresh cycle by briefly turning off the HS-FET and turning on the LS-FET.

The auto-refresh behavior is controlled and reported by the AR pin. The state of the AR pin is sampled during start-up. If AR is connected directly to ground, auto-refresh is enabled. If AR is pulled up to a logic supply, then when V_{BST} falls below its UVLO threshold, the HS-FET is disabled and the AR pin is pulled low. The system must consequently take action to charge C_{BST} by turning on the LS-FET or initiating a new start-up cycle.

Thermal Shutdown

If the die temperature exceeds safe limits, the MPQ1922 latches off and the nFAULT pin is pulled low. The device remains disabled until it is

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reset, either through nSLEEP or removal of V_G, and re-enabled.

Slew Rate Control

To quickly reduce electromagnetic interference (EMI) generated by the output switching action, configurable slew rate control is integrated into the MPQ1922. Slew rate control eliminates the need for series resistors or resistor/diode networks between the IC gate driver and MOSFET gates.

The slew rate is controlled by changing the pull-up and pull-down resistance of the MOSFET gates, which is set by the resistance between the SR pin and ground (see Table 3).

Table 3: Slew Rate Adjustment

R_{SR}	Pull-Up Resistance	Pull-Down Resistance	Adaptive Dead Time
0Ω	1.8Ω	1.4Ω	No
10kΩ	8Ω	3.7Ω	Yes
30kΩ	25Ω	14Ω	Yes
100kΩ	100Ω	42Ω	Yes

Note that the slew rate can only be set to the four selections shown in Table 3.

During one FET's on period, a strong Miller clamp is applied to the other FET's gate to prevent accidental turn-on due to the parasitics.

Shoot-Through Protection

The MPQ1922 does not allow both the HS-FET and the LS-FET to be on at the same time due to the risk of shoot-through. Shoot-through occurs when any overlap in conduction between the MOSFETs causes a short circuit between the power supply and ground, which creates large transient currents and can destroy the MOSFETs.

To prevent shoot-through in the output FETs, a dead time (t_{DEAD}) is inserted between the HS-FET turning off and LS-FET turning on, and vice versa.

When set to limit the output slew rate (R_{SR} = 10kΩ to 100kΩ), the MPQ1922 generates an adaptive dead time by monitoring the gate drive output voltage to ensure that a MOSFET gate has been fully discharged before turning on the other MOSFET. Longer dead times can be generated by adding a delay between the INH and INL input signals.

If external series gate resistance is added, then the adaptive shoot-through function may not work correctly, unless a diode parallel to the resistor is added to discharge the gate capacitance.

When the slew rate adjustment is set to full drive strength (R_{SR} = 0Ω), adaptive dead time is disabled. While the simultaneous start-up of the HS-FET and the LS-FET is prevented, no additional dead time is generated. In this case, inserting some delay between the INH and INL input signals is recommended to enforce the dead time requirements and ensure safe operation.

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APPLICATION INFORMATION

Selecting the MOSFETs

Selecting the correct power MOSFETs to drive a motor is crucial to designing a successful motor drive.

The MOSFET's VDS breakdown voltage must exceed the supply voltage (V_{IN}). Adding a considerable margin of at least 10V to 15V is recommended to prevent MOSFET damage from transient voltages caused by parasitic inductances in the PCB layout and wiring. For example, in 24V power supply applications, MOSFETs with a minimum breakdown voltage of 40V to 60V are recommended. A larger margin is ideal in high-current applications, as the transients caused by parasitic inductances may be larger. Conditions such as regenerative braking inject current back into the power supply. Care must be taken to ensure such conditions do not cause a large enough increase in the power supply voltage to damage components.

The MOSFETs must be able to safely pass the current required to run the motor. The highest current condition, which is typically when the motor is first started or stalled (called the stall current of the motor), must be supported.

The MOSFET's on resistance ($R_{DS(ON)}$) is related to its current capability. The MOSFET dissipates power proportional to $R_{DS(ON)}$ and the motor current: $P = I^2R$. $R_{DS(ON)}$ must be able to safely dissipate heat generated in the desired motor current. In some cases, $R_{DS(ON)}$ selection may require special PCB design considerations or external heatsinks for the MOSFETs.

Some consideration should be made for the safe operating area of the MOSFETs in the event of fault conditions, such as a short circuit. The IC responds quickly in the event of a short, but there is still a brief period of time (about 1µs to 2µs) during which large currents can flow in the MOSFETs while the protection circuits recognize the fault and disable the outputs.

Selecting the External Capacitor

The MPQ1922 has an internal charge pump to keep the HS gate drive supply charged. However, the primary source of the HS gate drive voltage is provided by C_{BST}.

C_{BST} supplies the large peak currents required to turn on the HS-FET. When the output is driven low, C_{BST} is charged and is then used to enable the MOSFET at high outputs.

The value of C_{BST} is selected based on the HS-FET's total gate charge. When the MOSFET is on, the charge stored in C_{BST} is transferred to the MOSFET gate. Estimate the minimum BST capacitance with Equation (1):

$$C_{BOOT} > 8 \times Q_G \quad (1)$$

Where Q_G is the total gate charge of the MOSFET (in nC), and C_{BOOT} is the boot capacitance (in nF).

C_{BST} should not exceed 1µF or it may lead to improper operation at start-up.

For most applications, a C_{BST} between 100nF and 1µF, rated for 25V minimum is recommended. Capacitors should be X5R or X7R ceramic.

The VG power supply input pin requires a bypass capacitor to ground. The peak current flowing in VG can be as high as several amps for a short period of time. For an X7R or X5R ceramic capacitor with a 25V minimum rating, a minimum 100nF bypass capacitor placed immediately adjacent to the VG pin is recommended. More capacitance may be required depending on the distance from the power source and any bulk capacitors present on the power rail.

Dead Time

Since motors are inductive by nature, once current is flowing in the motor, it cannot stop immediately, even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field decays.

When the MOSFETs are turned off, this current flows through the body diode in the MOSFET device.

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MOSFET body diodes have a much larger voltage drop than the MOSFET during conduction, so there is more power dissipated during body diode conduction than when the MOSFET is on. Because of this, it is desirable to minimize the dead time. However, the dead time must be made large enough to guarantee that the HS-FET and the LS-FET are never on at the same time.

Dead time is typically inserted by the microcontroller. The MPQ1922 prevents shoot-through by prohibiting the HS-FET and LS-FET from being turned on at the same time, but no additional dead time is inserted. If slew rate control is used though, then an adaptive dead time function monitors the gate voltage to ensure that there is no shoot-through, regardless of whether a very slow slew rate is selected, or no dead time is inserted by the microcontroller.

Setting the Slew Rate

The MPQ1922 has four drive strength settings to control the output MOSFETs' slew rate.

The selected MOSFETs' gate characteristics affect how fast they are switched on and off. At slower slew rate settings, a higher source resistance drives the MOSFET gates, which results in slower turn-on and turn-off transitions on the output.

Setting the ideal slew rate is a compromise. For minimum switching losses, the slew rate must be as fast as possible. High slew rates, however, result in increased radiated and conducted EMI.

The pulse-width modulation (PWM) frequency (f_{PWM}) also impacts the slew rate selection. For very low PWM frequencies (e.g. 8kHz), the slew rate can be very low, as it would still be a small fraction of the overall PWM cycle. For high PWM frequencies (above 50kHz to 75kHz), the slew rate must be fast to prevent it from occupying an inordinate amount of the PWM cycle.

For most applications, it is not necessary to add any external components between the MPQ1922 and the MOSFET gates. However, in some cases, adding external components (e.g. resistors and diodes) to modify the MOSFET turn-on and turn-off characteristics may be advantageous.

If external components such as resistors and diodes are used in the gate signals, the slew rate must be set to the fastest setting, with the SR pin grounded. For slower slew rate settings, the MPQ1922's adaptive dead time function monitors the voltage to ensure a MOSFET is fully turned off before the other MOSFET is enabled. Placing external components in the gate leads prevents the IC from seeing the real gate voltage, so there is a risk of shoot-through.

If external components are used to slow the transition times, an appropriate dead time must be inserted by the microcontroller to prevent shoot-through.

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PCB Layout Guidelines

Proper PCB layout is critical to the performance of MOSFET gate drivers. The MPQ1922 is designed to accommodate negative undershoot. However, if the undershoot is excessive, then unpredictable operation or damage to the IC may result. For the best results, refer to Figure 3 and follow the guidelines below:

1. Make the connection between the HS source and the LS drain as direct as possible to avoid negative undershoot on the phase node due to parasitic inductances.
2. Use the surface-mount N-channel MOSFETs to make very short connections between the MOSFETs.
3. Use wide copper areas to connect the LS sense resistor, which is composed of three parallel resistors (R9, R10, and R11), to both the input supply ground and the LS-FET source terminals. All of the high-current paths also utilize wide copper areas.
4. Place the C_{BST} (C5) and supply bypass capacitor (C4) as close as possible to the IC.
5. Place an additional bulk capacitor (C3) on the V_G line.
6. Use four vias to connect the ground side of these capacitors (which is connected to a solid ground plane) to both the MPQ1922's ground pin and exposed pad.
7. Keep the high-current ground path between the input supply, input bulk capacitor (C2), and MOSFETs away from the IC.

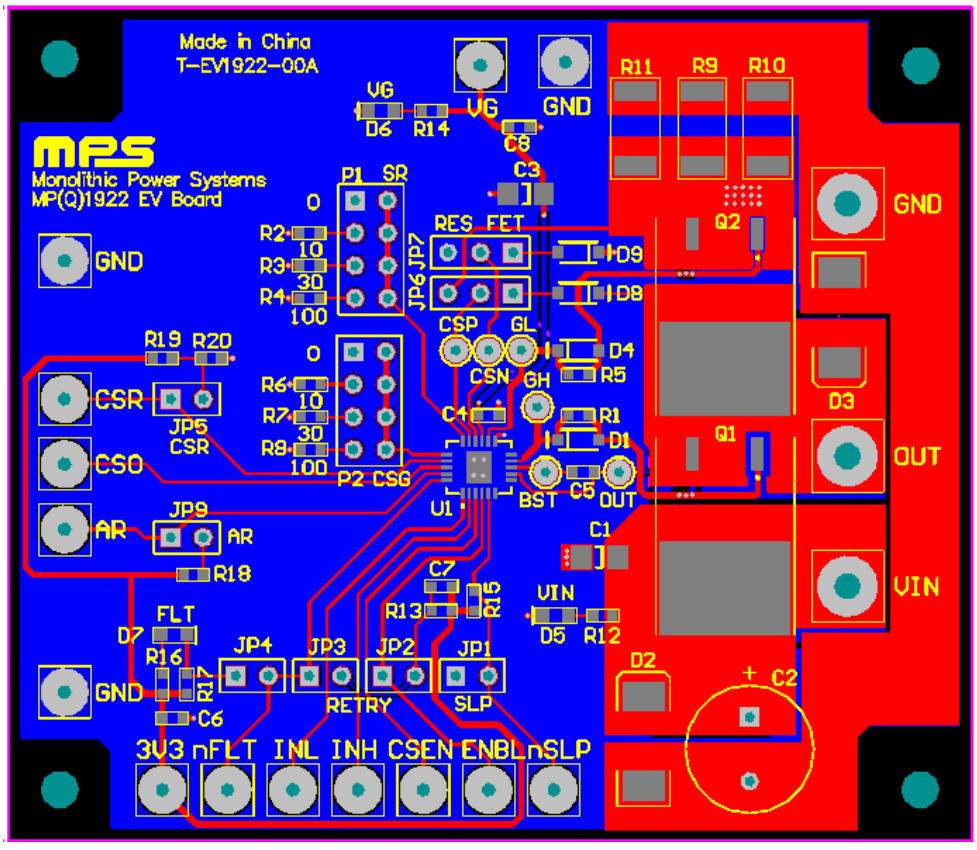

Figure 3: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

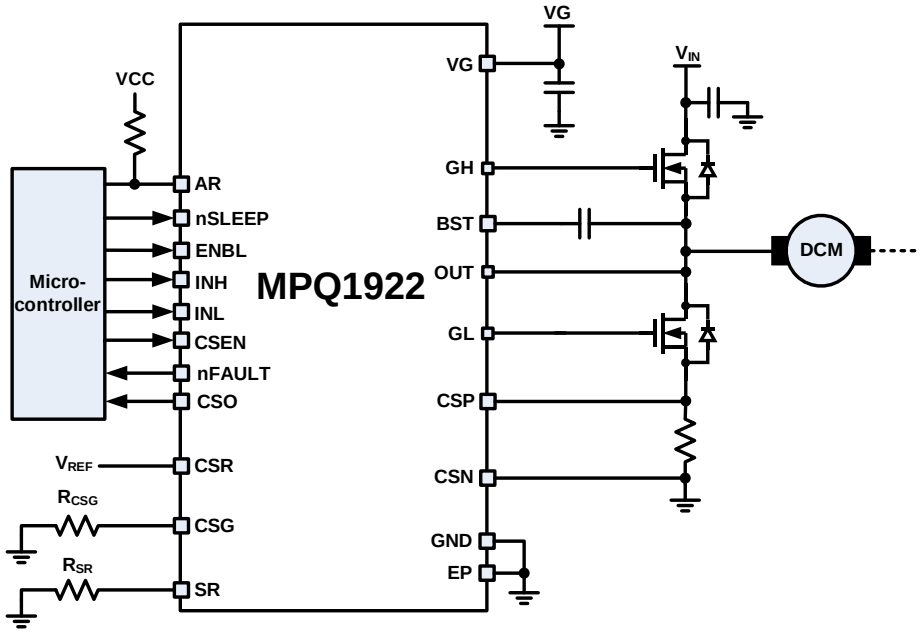

Figure 4: Typical Application Circuit

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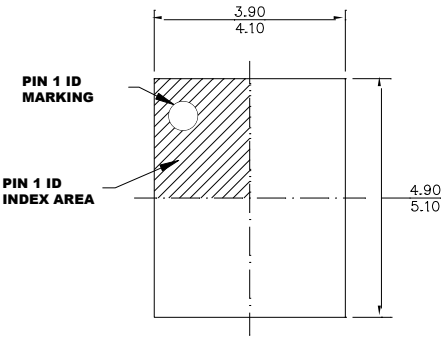
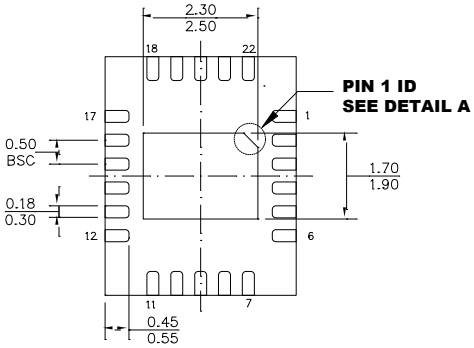
PACKAGE INFORMATION

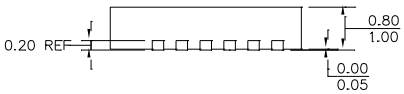
QFN-22 (4mmx5mm)
Non-Wettable Flank



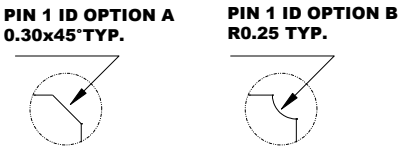
TOP VIEW



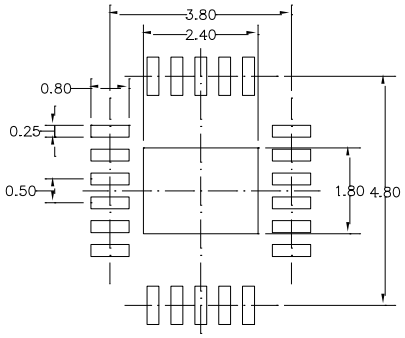
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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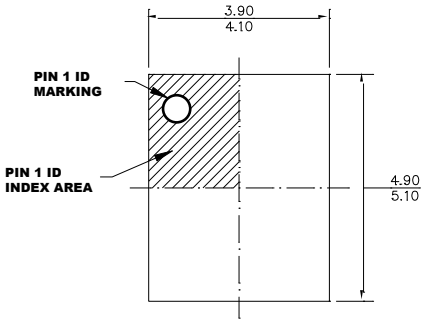
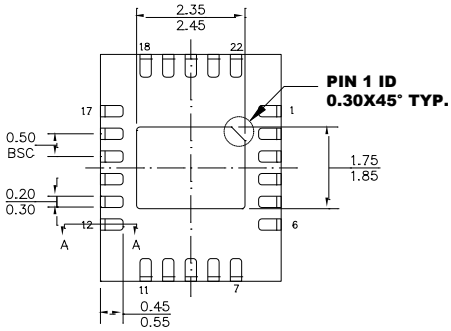
PACKAGE INFORMATION

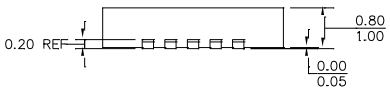
QFN-22 (4mmx5mm)
Wettable Flank



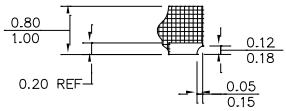
TOP VIEW



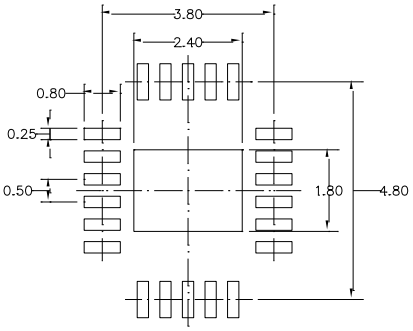
BOTTOM VIEW



SIDE VIEW



SECTION A-A



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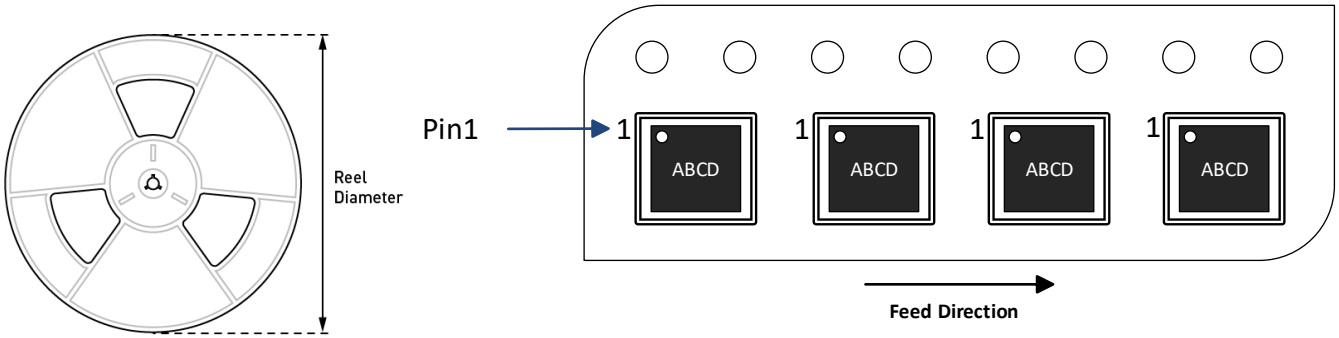
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ1922GV-AEC1-Z MPQ1922GVE-AEC1-Z	QFN-22 (4mmx5mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/10/2021	Initial Release	-

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