MP5042

2A, 28V E-Fuse with Adjustable Current Limit

DESCRIPTION

The MP5042 is a protection device designed to protect circuitry on the output from transients on the input. The MP5042 also protects the input from undesired shorts and transients coming from the output.

During start-up, the inrush current is limited by limiting the slew rate at the output. The slew rate is controlled by setting the DV/DT pin.

The maximum load at the output is current-limited. The current limit (I_{LIMIT}) magnitude is controlled by an external resistor connected between ILIMIT and GND. The I_{LIMIT} threshold can be set between 25mA and 2A. When the ILIMIT pin is floating, I_{LIMIT} is fixed at 260mA.

The MP5042 is available in a TSOT23-6 package.

FEATURES

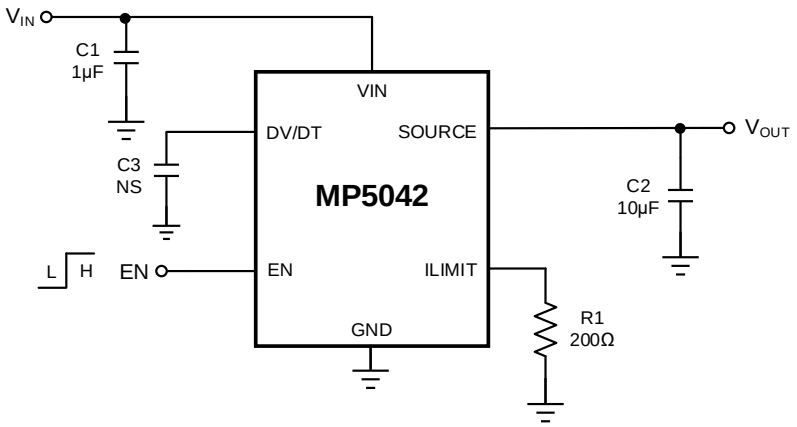
- Wide 4.2V to 28V Operating Input Voltage (V_{IN}) Range
- Low 175µA Quiescent Current (I_Q)
- Integrated 115mΩ MOSFET
- Adjustable 25mA to 2A Current Limit (I_{LIMIT}) or Fixed 260mA I_{LIMIT} when the ILIMIT Pin Is Floating
- Configurable Soft-Start Time (t_{SS}) via the DV/DT Pin
- ±10% I_{LIMIT} Accuracy at 260mA
- ±7% I_{LIMIT} Accuracy at 800mA
- Fast Response for Hard Short Protection
- Over-Current Protection (OCP) with Hiccup Mode and Latch-Off Protection
- Thermal Shutdown and Automatic Retry
- Available in a TSOT23-6 Package

APPLICATIONS

- Hard Disk Drives (HDDs) and Solid-State Drives (SSDs)
- Hot-Swap Devices
- Wireless Modem Data Cards
- Power Meters

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5042GJ	TSOT23-6	*See Below*	1

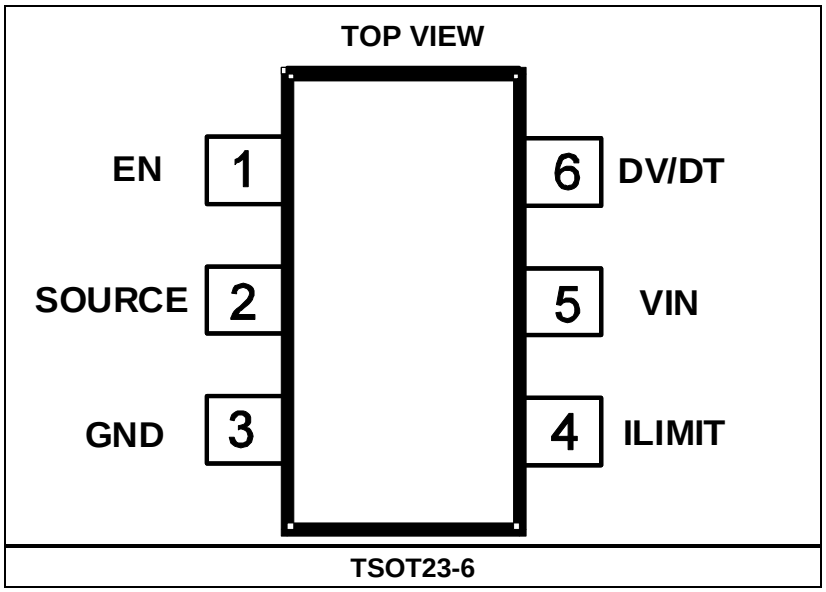
* For Tape & Reel, add suffix -Z (e.g. MP5042GJ-Z).

TOP MARKING

| BQGY

BQG: Product code of MP5042GJ
Y: Year code

PACKAGE REFERENCE



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable.** Force the EN pin high to enable the MP5042. Float or pull EN to GND to disable the IC.
2	SOURCE	**Source of the internal power MOSFET and output terminal of the IC.**
3	GND	**System ground.**
4	ILIMIT	**Current limit setting.** Place a resistor between the ILIMIT pin and ground to set the current limit (I_{LIMIT}). Float ILIMIT to achieve a fixed I_{LIMIT} at 260mA. Do not short this pin to GND.
5	VIN	**Supply voltage.** The MP5042 operates across a 4.2V to 28V input rail. A ceramic capacitor is required to decouple the input rail. Connect the VIN pin to the ceramic capacitor using a wide PCB trace.
6	DV/DT	**DV/DT.** Connect a capacitor between the DV/DT pin and ground to set the DV/DT slew rate. The default slew rate is 0.9V/ms when DV/DT is floating.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}), source .....-0.3V to +32V
All other pins .....-0.3V to +5.5V
Junction temperature (T_J) ..... -40°C to +150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C
Continuous power dissipation (T_A = 25°C) (2)
TSOT23-6 ..... 1.89W

ESD Ratings

Human body model (HBM) ..... ±2000V (3)
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4.2V to 28V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***
TSOT23-6		
EV5042-J-00A (5)	66	23...°C/W
JESD51-7 (6)	100	55...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation may generate an excessive die temperature, which can cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The ILIMIT pin passes +2000V/-1000V. All the other pins pass ±2000V.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the EV5042-J-00A, 2-layer PCB (50mmx50mm).
6) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, R_{LIMIT} = 200Ω, C_{OUT} = 10μF, T_J = -40°C to +125°C [7], typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Quiescent supply current	I_Q	EN = high		175	300	μA
Shutdown supply current	I_{SHDN}	EN = GND			2	μA
Power MOSFET						
On resistance	$R_{DS(ON)}$	I_{OUT} = 1A		115	200	mΩ
Turn-on delay	t_{DELAY}	Enable to 10% of V_{OUT}, float DVDT		2000		μs
Off-state leakage current	I_{OFF}	V_{IN} = 12V, V_{EN} = 0V		0.1	1	μA
Under-Voltage Protection (UVP)						
Under-voltage lockout (UVLO) rising threshold	V_{UVLO}		3.85	3.95	4.05	V
UVLO hysteresis	V_{UVLO_HYS}			350		mV
DV/DT						
DV/DT slew rate	dV/dt	Float DV/DT	0.7	0.9	1.1	V/ms
DV/DT current	$I_{DV/DT}$	$V_{DV/DT}$ = 0.5V	4.5	6.5	8.5	μA
Current Limit						
Current limit at normal operation	I_{LIMIT_NOR}	Float the ILIMIT pin, T_J = 25°C	10%	260	10%	mA
		R_{LIMIT} = 200Ω, T_J = 25°C	-7%	2	+7%	A
		R_{LIMIT} = 604Ω, T_J = 25°C	-7%	800	+7%	mA
Enable (EN)						
EN rising threshold	V_{EN_RISING}		1.15	1.25	1.35	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN_DOWN}			0.8		MΩ
Over-Temperature Protection (OTP)						
Thermal shutdown [8]	T_{SD}			175		°C
Thermal hysteresis [8]	T_{SD_HYS}			50		°C

Notes:

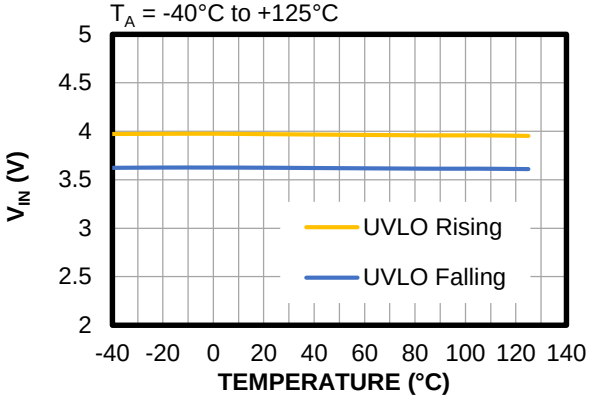
7) Not tested in production. Derived by over-temperature correlation.
8) Derived by sample characterization. Not tested in production.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

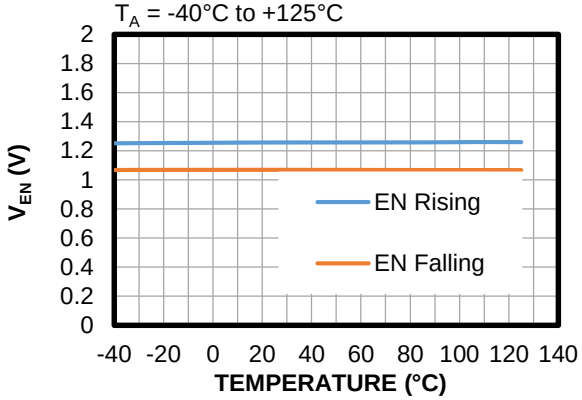
TYPICAL CHARACTERISTICS

V_{IN} = 12V, R_{LIMIT} = 200Ω, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

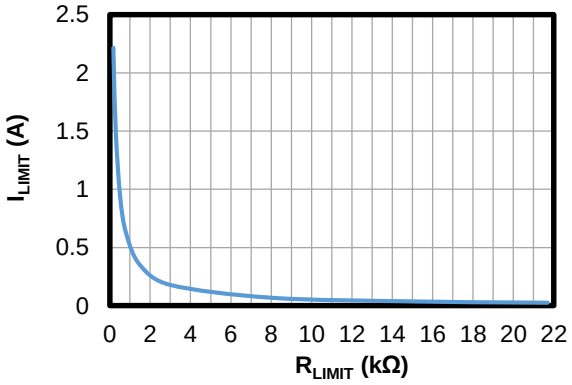
V_{IN} UVLO Rising/Falling Threshold vs. Temperature



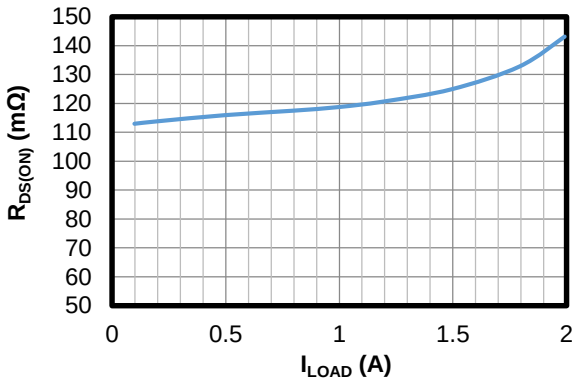
EN Rising/Falling Threshold vs. Temperature



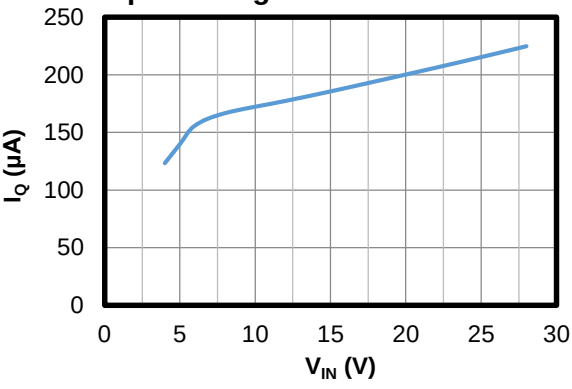
Current Limit vs. R_{LIMIT}



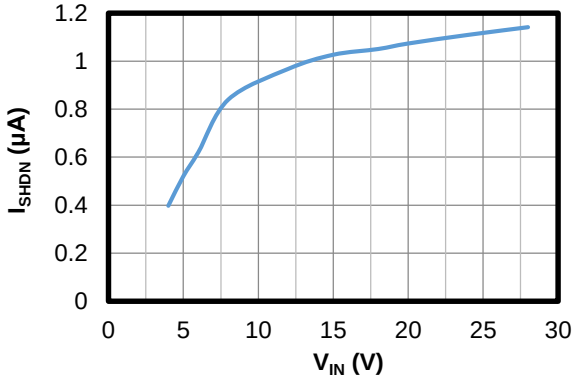
On Resistance vs. Load Current



Quiescent Current vs. Input Voltage



Shutdown Current vs. Input Voltage



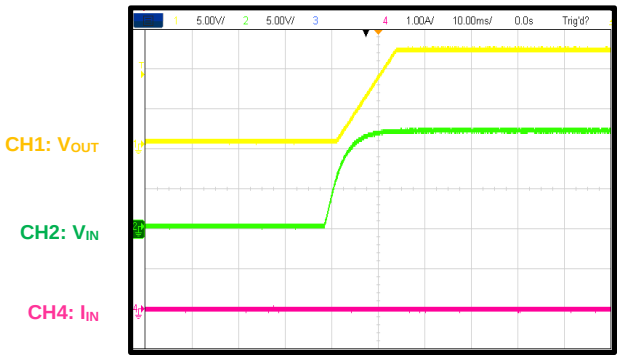
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, R_{LIMIT} = 200Ω, C_{OUT} = 10μF, T_A = 25°C, unless otherwise noted.

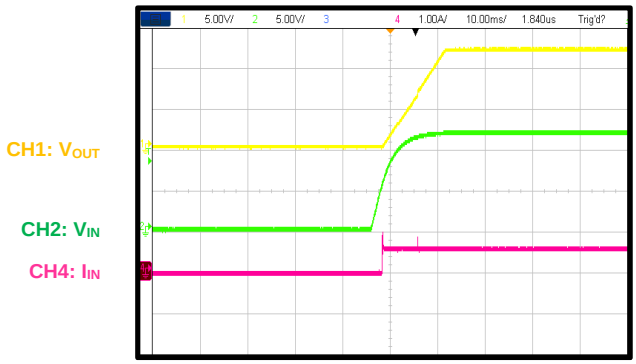
Start-Up through VIN

I_{OUT} = 0A



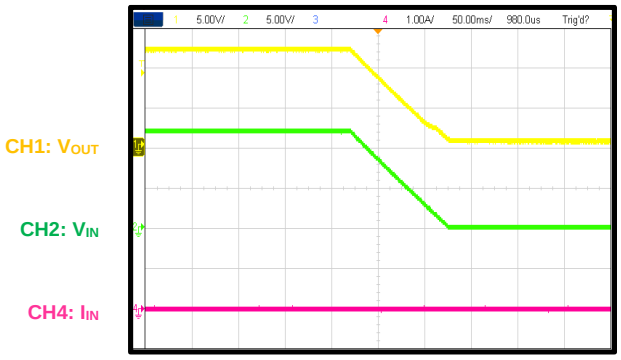
Start-Up through VIN

I_{OUT} = 0.6A



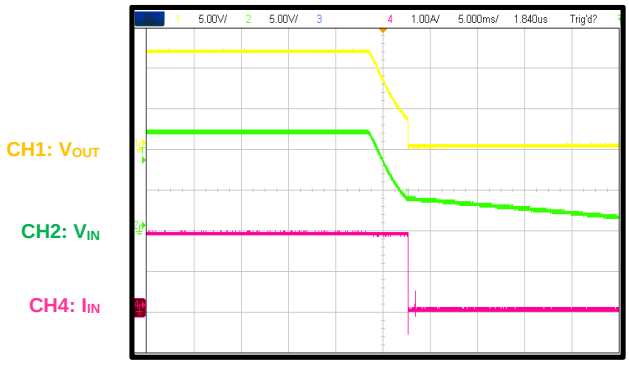
Shutdown through VIN

I_{OUT} = 0A



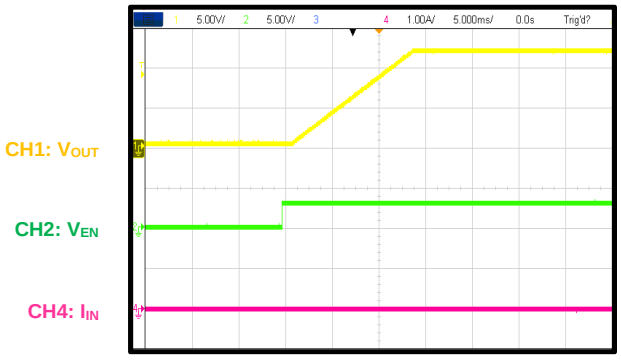
Shutdown through VIN

I_{OUT} = 2A



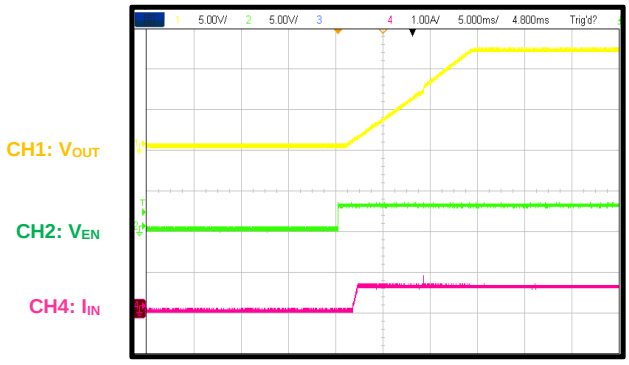
Start-Up through EN

I_{OUT} = 0A



Start-Up through EN

I_{OUT} = 0.6A



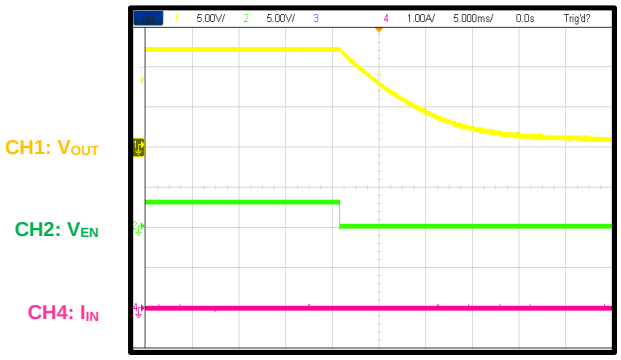
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{LIMIT} = 200Ω, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

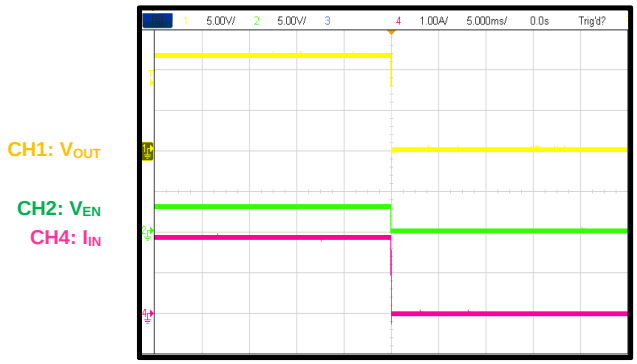
Shutdown through EN

I_{OUT} = 0A



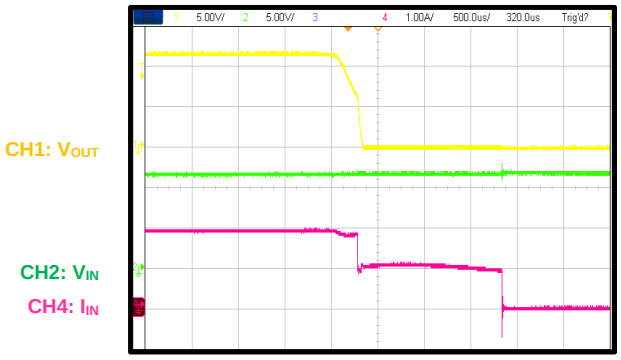
Shutdown through EN

I_{OUT} = 2A



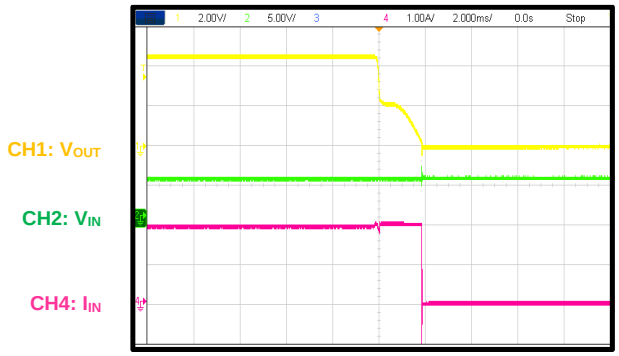
Current Limit

Increase I_{OUT} slowly, V_{IN} = 12V



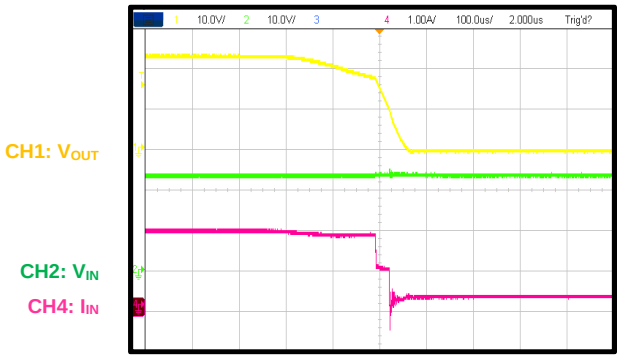
Current Limit

Increase I_{OUT} slowly, V_{IN} = 5V



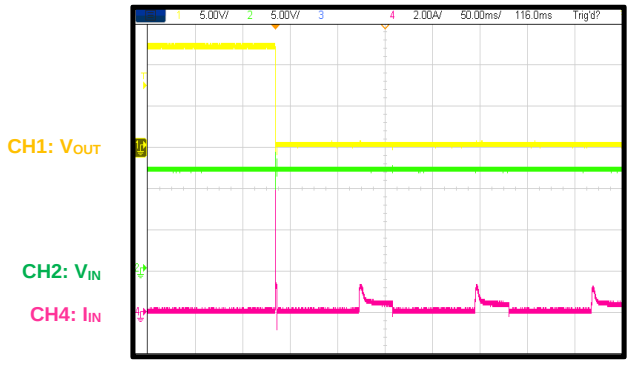
Current Limit

Increase I_{OUT} slowly, V_{IN} = 24V



Short-Circuit Protection Entry

I_{OUT} = 0A



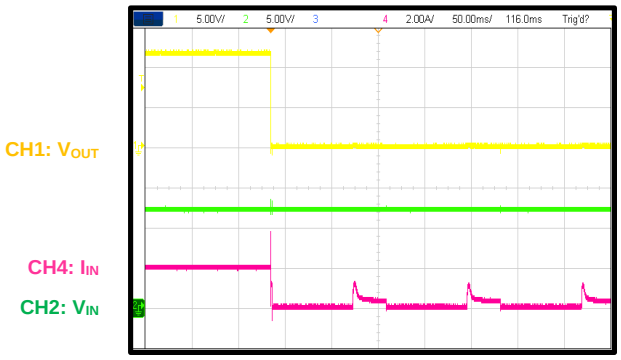
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, R_{LIMIT} = 200Ω, C_{OUT} = 10µF, T_A = 25°C, unless otherwise noted.

Short-Circuit Protection Entry

I_{OUT} = 2A



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

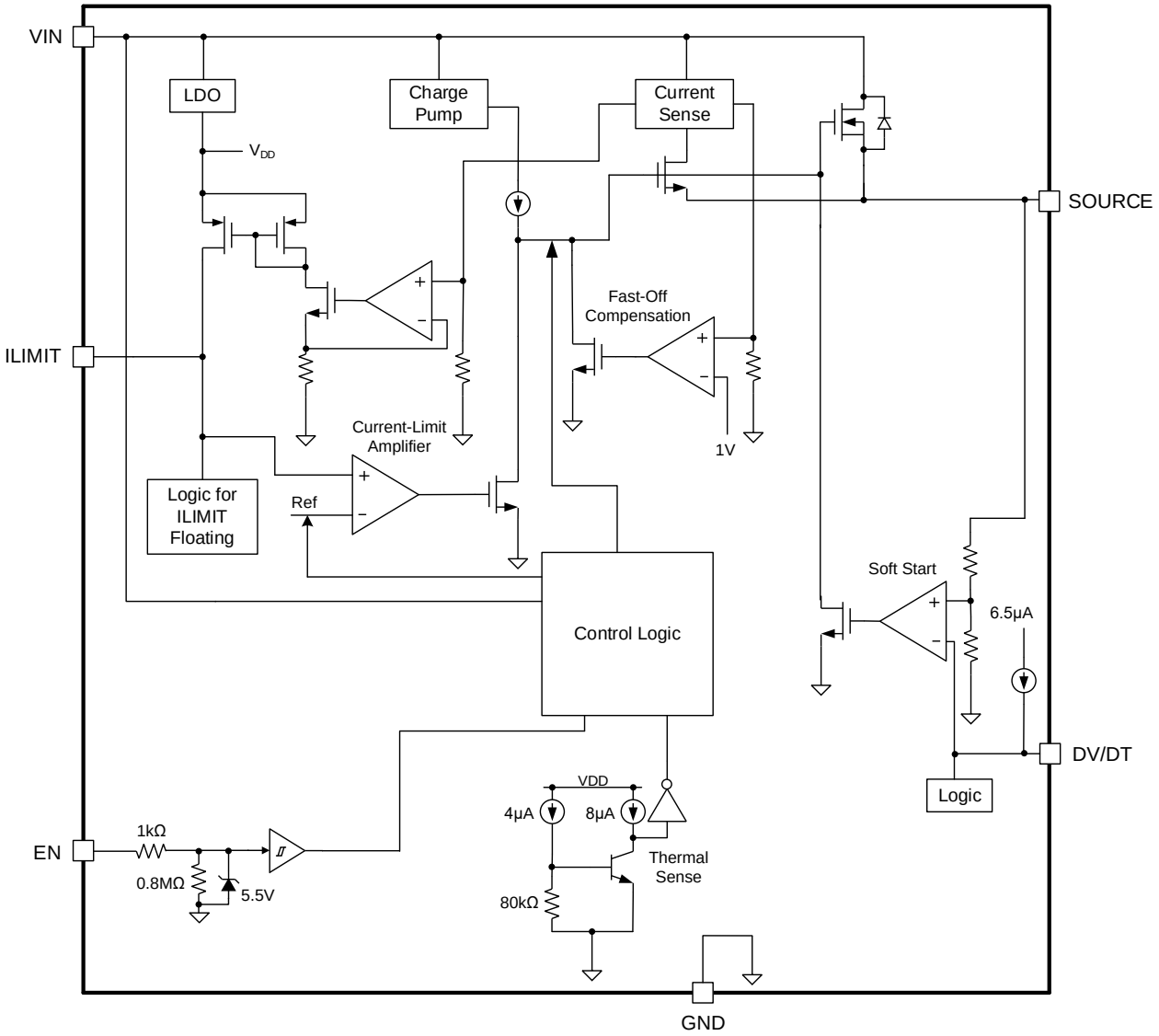


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

The MP5042 is designed to limit the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop and the dV/dt of the voltage to the load. The device offers an integrated solution for monitoring the input voltage (V_{IN}), output voltage (V_{OUT}), output current (I_{OUT}), and die temperature to eliminate the need for an external current-sense power resistor, power MOSFET, and temperature-sense device.

Under-Voltage Lockout (UVLO)

The MP5042 operates across a 4.2V to 28V V_{IN} range. There are high energy transients during normal operation or hot swap that depend on the parasitic inductance, resistance of the wire, and a capacitor at the VIN node. If a power-clamped transient-voltage-suppression (TVS) diode is not used, then the e-fuse must be able to withstand this transient voltage. The MP5042 integrates a high-voltage MOSFET with up to 28V of continuous V_{IN}. In addition, the MP5042 uses a high-voltage circuit for the VIN node to guarantee safe operation.

Soft Start (SS)

The soft-start (SS) time (t_{SS}) is related to the DV/DT slew rate and V_{IN}. t_{SS} can be calculated with Equation (1):

$$t_{SS}\ (ms) = \frac{V_{IN}\ (V)}{dV/dt\ (V/ms)} \quad (1)$$

The DV/DT slew rate is controlled by setting the DV/DT pin. For more details, see the Application Information section on page 12.

Current Limit

The MP5042 provides a constant current limit, (I_{LIMIT}) that can be configured by an external resistor connected between the ILIMIT and GND pins.

The desired I_{LIMIT} is a function of the external current-limit resistor and can be calculated with Equation (2):

$$I_{LIMIT}\ (A) = \frac{545}{R_{LIMIT}\ (\Omega) + 72} \quad (2)$$

Once the current limit threshold is reached, the internal circuit regulates the gate voltage (V_G) to hold the current in the power MOSFET constant. To limit the current, the gate-to-source voltage (V_{GS}) must be regulated to decrease from 5V to about 1V. The typical response time is about 15µs. During this period, I_{OUT} may have a small overshoot. The hold current folds back according to the voltage drop on the power MOSFET. Three different scenarios for the hold current are described below:

1. When V_{IN} - V_{OUT} < 7V, the hold current is clamped at 100% of I_{LIMIT}.
2. When 7V < V_{IN} - V_{OUT} < 14V, if the set I_{LIMIT} exceeds 260mA, then the hold current is clamped at 50% of I_{LIMIT}. If the set I_{LIMIT} is below 260mA, the hold current is clamped at 100% of I_{LIMIT}.
3. When V_{IN} - V_{OUT} > 14V, if the set I_{LIMIT} exceeds 260mA, then the hold current is clamped at 260mA. If the set I_{LIMIT} is below 260mA, the hold current is clamped at 100% of I_{LIMIT}.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Figure 2 shows over-current protection (OCP) at a 12V input.

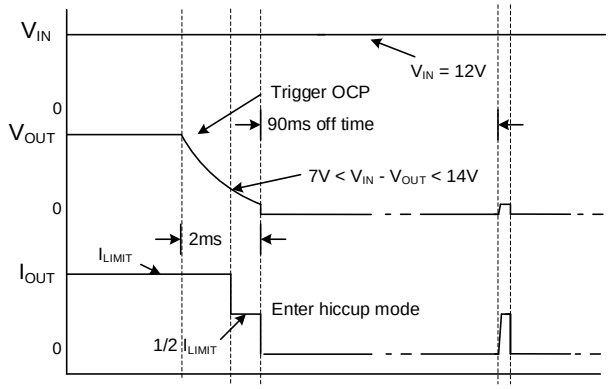


Figure 2: Over-Current Protection (12V Input)

Figure 3 shows OCP at a 24V input.

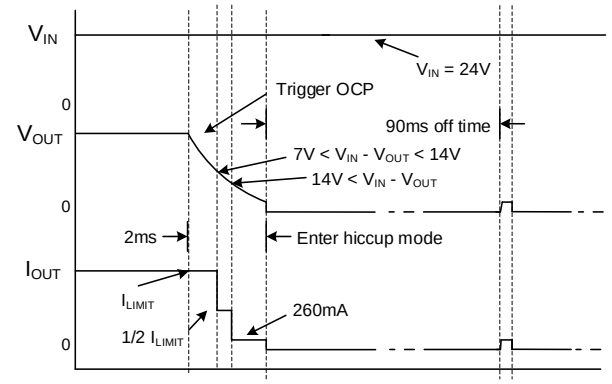


Figure 3: Over-Current Protection (24V Input)

If the overload condition lasts longer than 2ms, the IC enters hiccup mode with an off time of 90ms. Hiccup protection mode can be trimmed to latch-off mode. Due to the current limit foldback mechanism, the MP5042 has limited load capability during start-up.

The MP5042 allows the ILIMIT pin to be floated during operation. If ILIMIT is floating, I_{LIMIT} is fixed at 260mA internally.

Short-Circuit Protection (SCP)

If the load current (I_{LOAD}) increases rapidly due to a short-circuit event, then the current may exceed I_{LIMIT} before the control loop can respond. If the current reaches the secondary I_{LIMIT} at 5A, then a fast turn-off circuit activates to turn the power MOSFET off. This limits the peak current through the switch, preventing a significant V_{IN} drop. The total short-circuit response time is about 300ns. The MP5042 restarts after the MOSFET switches off.

During the restart process, if the short still exists, the MP5042 regulates V_G to hold the current at a different level according to the voltage drop on the power MOSFET. The IC enters hiccup mode for an off time of 90ms. Hiccup protection mode can be trimmed to latch-off mode. To prevent damage to the safe operating area (SOA) during a high V_{IN} short-circuit protection (SCP) condition, the IC's I_{LIMIT} folds back when the junction temperature (T_J) exceeds 110°C.

Enable (EN)

The MP5042 is enabled when the EN pin is high; it is disabled when EN is low. Floating EN shuts down the MP5042 due to the internal 0.8MΩ resistor pulling EN down to ground.

EN is clamped internally using a 5.5V Zener diode (see Figure 4).

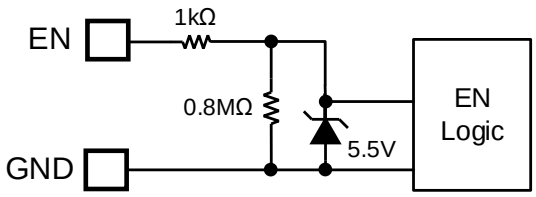


Figure 4: Zener Diode between EN and GND

Connect the EN input to VIN via a pull-up resistor to limit the EN input current below 100μA, which prevents damage to the Zener diode.

For example, when connecting a 300kΩ pull-up resistor to 12V VCC, the Zener current (I_{ZENER}) is (12V - 5.5V) / 300kΩ - 5.5V / 0.8MΩ = 14.8μA.

When using a pull-up resistor to set the power-on threshold, avoid using a pull-up resistor that is too small to increase the operating quiescent current (I_Q).

Thermal Shutdown and Automatic Retry

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the silicon die temperature exceeds 175°C, then the entire chip shuts down, and EN reports a fail mode. Once the temperature drops below its lower threshold (typically 125°C), the chip is enabled again after a 90ms delay typically.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Current Limit

The MP5042's I_{LIMIT} should exceed the normal maximum I_{LOAD}, allowing for tolerances in the current sense. I_{LIMIT} is a function of the external current-limit resistor. Table 1 shows examples of the typical I_{LIMIT} as a function of the current-limit resistance (R_{LIMIT}).

Table 1: Typical Current Limit vs. R_{LIMIT} (9)

I_{LIMIT} (A)	R_{LIMIT} (Ω)
0.025	21700
0.26	Float
0.8	604
2	200

Note:

9) I_{LIMIT} is a typical value for the reference design.

Figure 5 shows the relationship between I_{LIMIT} and R_{LIMIT}.

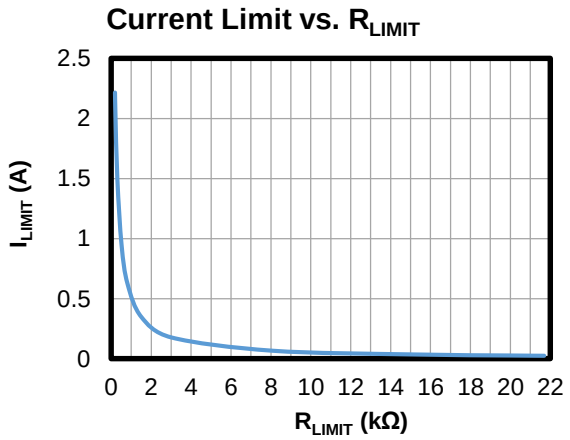


Figure 5: Current Limit vs. R_{LIMIT}

Connect the proper R_{LIMIT} to configure the MP5042's I_{LIMIT} between 25mA and 2A.

Setting the Soft-Start Time

t_{SS} is related to the DV/DT slew rate and V_{IN}, and can be calculated with Equation (3):

$$t_{SS}(ms) = \frac{V_{IN}(V)}{dv/dt\ (V/ms)} \quad (3)$$

The DV/DT slew rate is controlled by setting the external DV/DT capacitor ($C_{DV/DT}$). When DV/DT is floating, the DV/DT slew rate is 0.9V/ms.

If there is an external $C_{DV/DT}$, the DV/DT slew rate can be calculated with Equation (4):

$$dV/dt\ (V/ms) = \frac{6.5\mu A \times 15}{C_{DV/DT}(nF)} \quad (4)$$

For example, when the external $C_{DV/DT}$ is 47nF, the DV/DT slew rate is 2.1V/ms.

Design Example

Table 2 shows a design example following the application guidelines for the given specifications.

Table 2: Design Example

V_{IN} (V)	Current Limit (A)	DV/DT Slew Rate (V/ms)
12	2	0.9V/ms

Figure 7 on page 14 shows the detailed application circuit. See the Typical Performance Characteristics section on page 6 for the typical performance and circuit waveforms. For more detailed device applications, refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for stable performance. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the high-current paths (VIN and SOURCE) close to the device using short, direct, and wide traces.
2. Place the input capacitors close to the VIN and GND pins.
3. Connect the VIN and SOURCE pads to the large VIN and SOURCE planes, respectively, to achieve improved thermal performance.
4. Place R_{LIMIT} close to the ILIMIT pin.
5. Place $C_{DV/DT}$ close to the DV/DT pin.

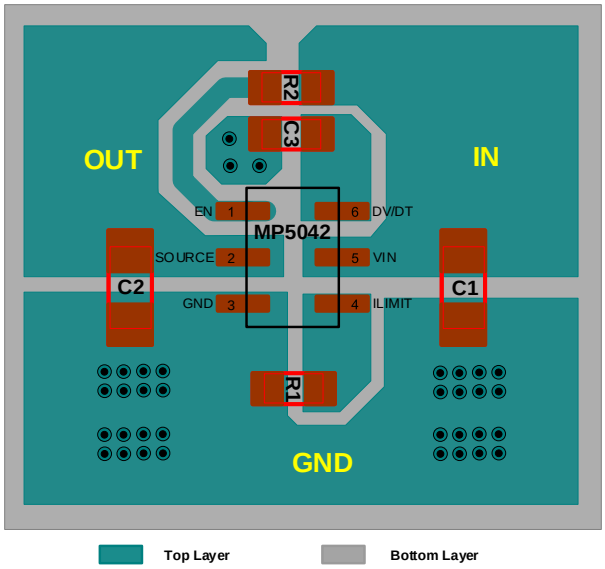


Figure 6: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

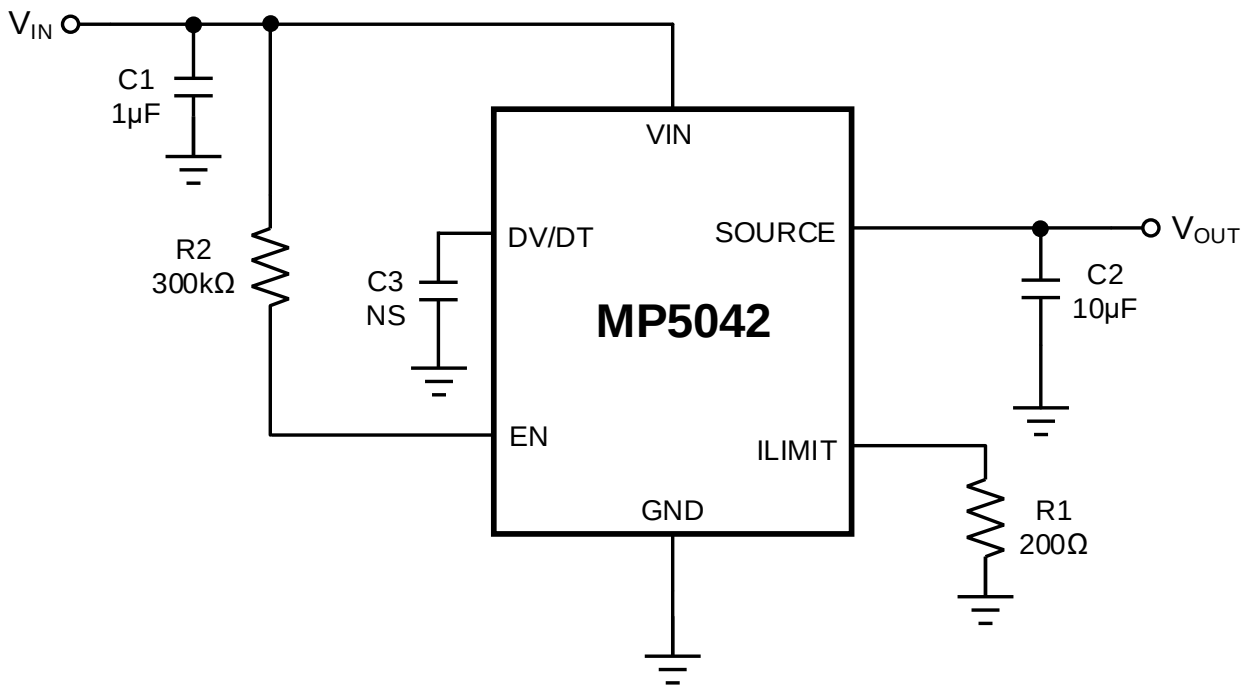
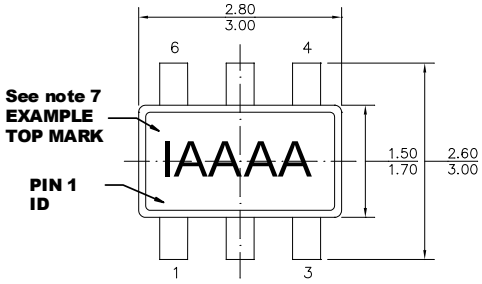


Figure 7: Typical Application Circuit (Current Limit Output = 2A)

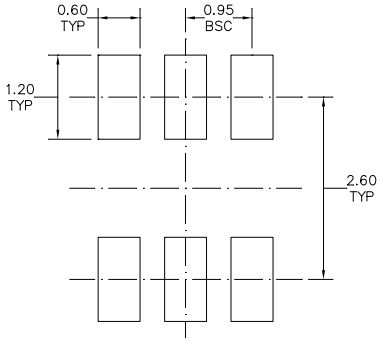
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

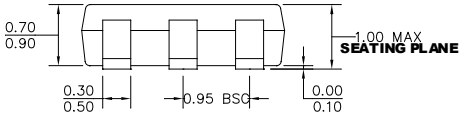
TSOT23-6



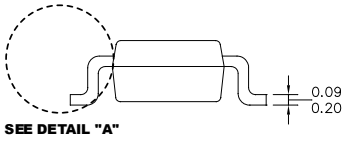
TOP VIEW



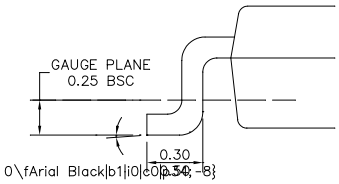
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



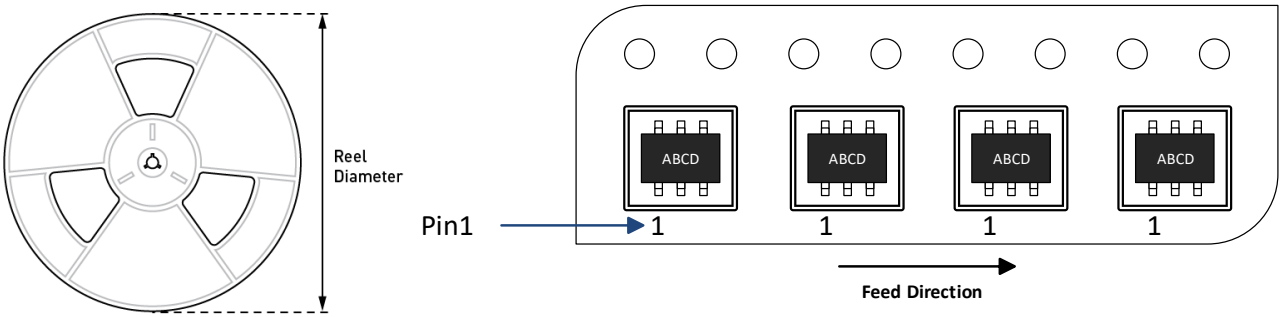
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5042GJ-Z	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/22/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.