NCP345

Overvoltage Protection IC

The NCP345 overvoltage protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients and power supply faults when used in conjunction with an external P−channel FET. The device is designed to sense an overvoltage condition and quickly disconnect the input voltage supply from the load before any damage can occur. The OVP consists of a precise voltage reference, a comparator with hysteresis, control logic, and a MOSFET gate driver. The OVP is designed on a robust BiCMOS process and is intended to withstand voltage transients up to 30 V.

The device is optimized for applications that have an external AC/DC adapter or car accessory charger to power the product and/or recharge the internal batteries. The nominal overvoltage threshold is 6.85 V so it is suitable for single cell Li−Ion applications as well as 3/4 cell NiCD/NiMH applications.

Features

- Overvoltage Turn−Off Time of less than 1.0 μsec
- Accurate Voltage Threshold of 6.85 V (nominal)
- Undervoltage Lockout Protection
- CNTRL Input Compatible with 1.8 V Logic Levels
- Pb−Free Package is Available

Typical Applications

- Cellular Phones
- Digital Cameras
- Portable Computers and PDAs
- Portable CD and other Consumer Electronics

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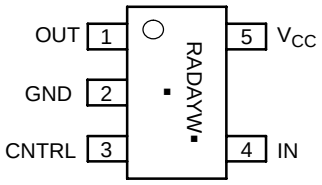
THIN SOT−23−5
SN SUFFIX
CASE 483

PIN CONNECTIONS & MARKING DIAGRAM



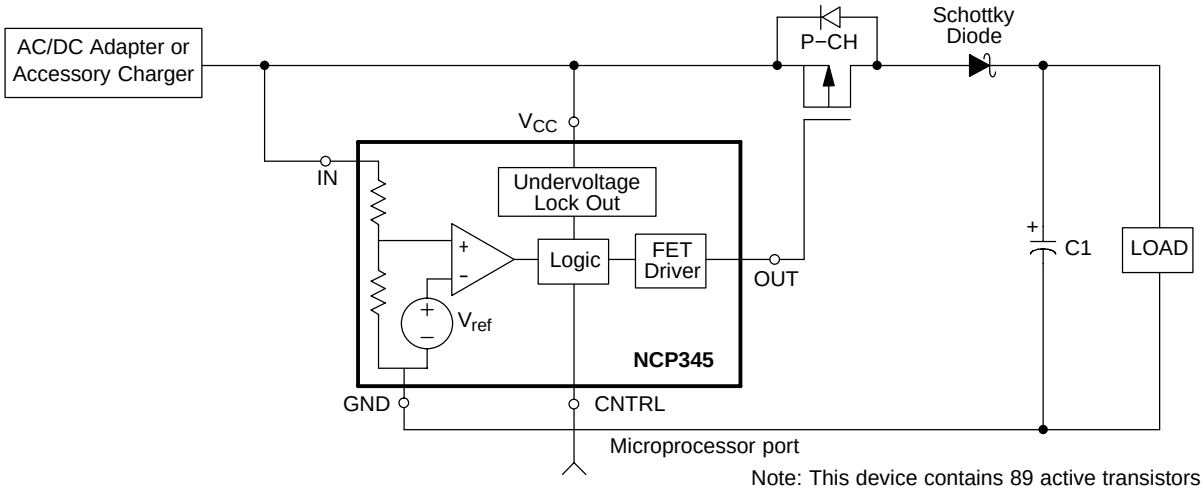
(Top View)

RAD = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP345SNT1	SOT−23−5	3000 / Tape & Reel (7 inch Reel)
NCP345SNT1G	SOT−23−5 (Pb−Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Note: This device contains 89 active transistors

Figure 1. Simplified Application Diagram

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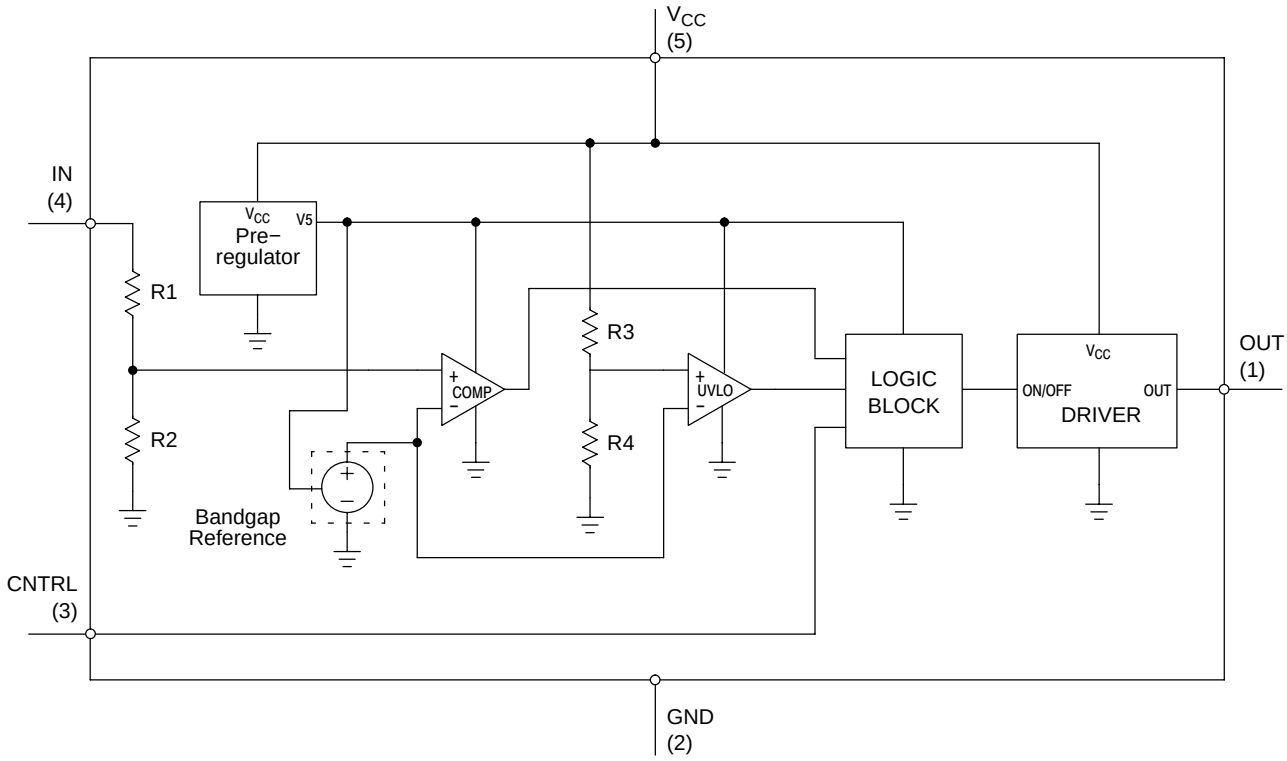


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	OUT	This signal drives the gate of a P−channel MOSFET. It is controlled by the voltage level on IN or the logic state of the CNTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{CC} in less than 1.0 μsec provided that gate and stray capacitance is less than 12 nF.
2	GND	Circuit Ground
3	CNTRL	This logic signal is used to control the state of OUT and turn−on/off the P−channel MOSFET. A logic High results in the OUT signal being driven to within 1.0 V of V_{CC} which disconnects the FET. If this pin is not used, the input should be connected to ground.
4	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (VTH), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the FET. The nominal threshold level is 6.85 V and this threshold level can be increased with the addition of an external resistor between IN and V_{CC}.
5	V_{CC}	Positive Voltage supply. If V_{CC} falls below 2.8 V (nom), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the P−channel FET.

TRUTH TABLE

IN	CNTRL	OUT
$<V_{th}$	L	GND
$<V_{th}$	H	V_{CC}
$>V_{th}$	L	V_{CC}
$>V_{th}$	H	V_{CC}

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Pin	Symbol	Min	Max	Unit
OUT voltage to GND	1	V_O	−0.3	30	V
Input and CNTRL pin voltage to GND	4 3	V_{input} V_{CNTRL}	−0.3 −0.3	30 13	V
V_{CC} Maximum Range	5	$V_{CC(max)}$	−0.3	30	V
Maximum Power Dissipation at T_A = 85°C	−	P_D	−	0.216	W
Thermal Resistance Junction to Air	−	$R_{\theta JA}$	−	300	°C/W
Junction Temperature	−	T_J	−	150	°C
Operating Ambient Temperature	−	T_A	−40	85	°C
V_{CNTRL} Operating Voltage	3	−	0	5.0	V
Storage Temperature Range	−	T_{stg}	−65	150	°C
ESD performance (HBM)†	all	−	2.5	−	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

† Human body model (HBM): MIL STD 883C Method 3015−7, (R = 1500 ohms, C = 100 pf, F = 3 pulses delay 1 s).

ELECTRICAL CHARACTERISTICS

(For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C, V_{CC} = 6.0 V, unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
V_{CC} Operating Voltage Range	$V_{CC(opt)}$	5	3.0	4.8	25	V
Supply Current (I_{CC} + I_{Input}; V_{CC} = 6.0 V Steady State)	−	4,5	−	0.75	1.0	mA
Input Threshold (V_{Input} connected to V_{CC}; V_{Input} increasing)	V_{Th}	4	 6.65	 6.85	 7.08	V
Input Hysteresis (V_{Input} connected to V_{CC}; V_{Input} decreasing)	V_{Hyst}	4	50	100	200	mV
Input Impedance (Input = V_{Th})	R_{in}	4	70	150	−	kΩ
CNTRL Voltage High	V_{ih}	3	1.5	−	−	V
CNTRL Voltage Low	V_{il}	3	−	−	0.5	V
CNTRL Current High (V_{ih} = 5.0 V)	I_{ih}	3	−	95	200	μA
CNTRL Current Low (V_{il} = 0.5 V)	I_{il}	3	−	10	20	μA
Undervoltage Lockout (V_{CC} decreasing)	V_{Lock}	3	2.5	2.8	3.0	V
Output Sink Current (V_{CC} < V_{Th}, V_{OUT} = 1.0 V)	I_{Sink}	1	10	33	50	μA
Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 10 mA) Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 0.25 mA) Output Voltage High (V_{CC} = V_{in} = 8.0 V; I_{Source} = 0 mA)	V_{oh}	1	V_{CC}−1.0 V_{CC}−0.25 V_{CC}−0.1	− − 	− − 	V
Output Voltage Low (Input < 6.5 V; I_{Sink} = 0 mA; V_{CC} = 6.0 V, CNTRL = 0 V)	V_{ol}	1	−	−	0.1	V
Turn ON Delay − Input (V_{Input} connected to V_{CC}; V_{Input} step down signal from 8.0 to 6.0 V; measured to 50% point of OUT)*	$T_{ON\ IN}$	1	−	−	10	μsec
Turn OFF Delay − Input (V_{Input} connected to V_{CC}; V_{Input} step up signal from 6.0 to 8.0 V; C_L = 12 nF Output > V_{CC}−1.0 V)	$T_{OFF\ IN}$	1	−	0.5	1.0	μsec
Turn ON Delay − CNTRL (CNTRL step down signal from 2.0 to 0.5 V; measured to 50% point of OUT)*	$T_{ON\ CT}$	1	−	−	10	μsec
Turn OFF Delay − CNTRL (CNTRL step up signal from 0.5 to 2.0 V; C_L = 12 nF Output > V_{CC}−1.0 V)	$T_{OFF\ CT}$	1	−	1.0	2.0	μsec

*Turn ON Delay is guaranteed by design.

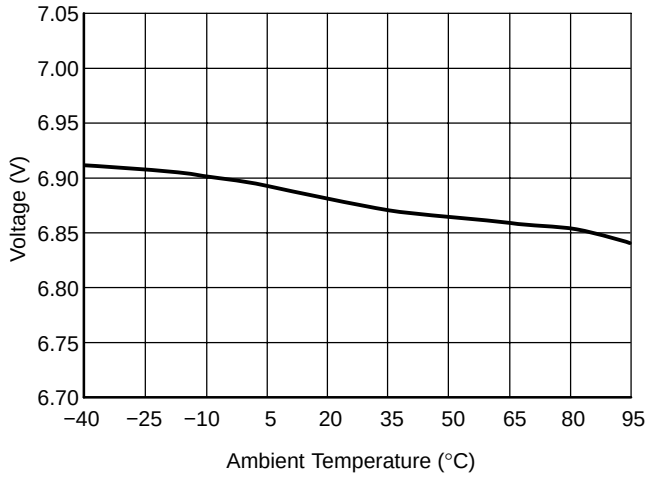


Figure 3. Typical V_{th} Threshold Variation vs. Temperature

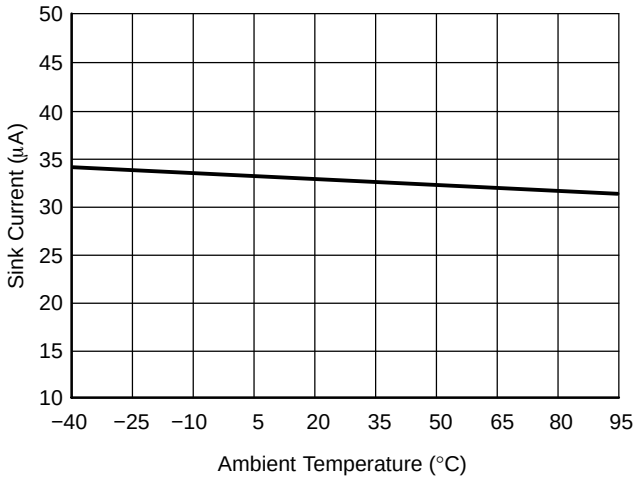


Figure 4. Typical OUT Sink Current vs. Temperature $V_{in} < V_{th}$, $V_{out} = 1$ V

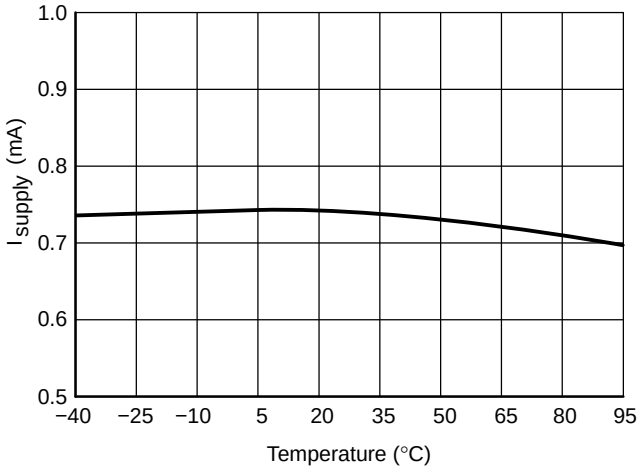


Figure 5. Typical Supply Current vs. Temperature $I_{cc} + I_{in}$, $V_{CC} = 6$ V

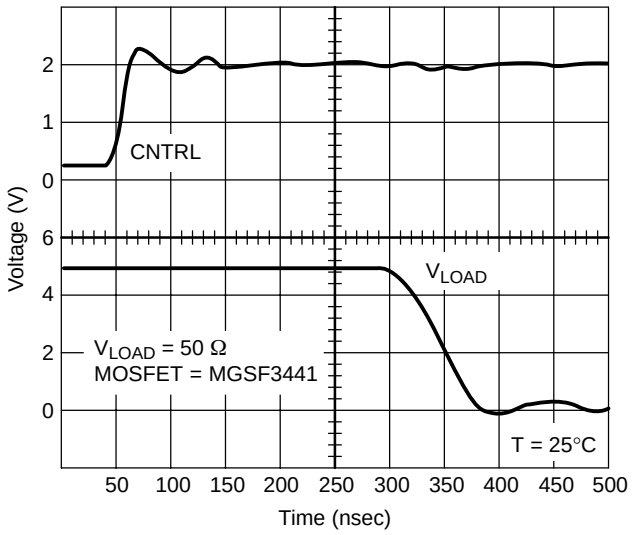


Figure 6. Typical Turn−off Time CNTRL to V_{LOAD}

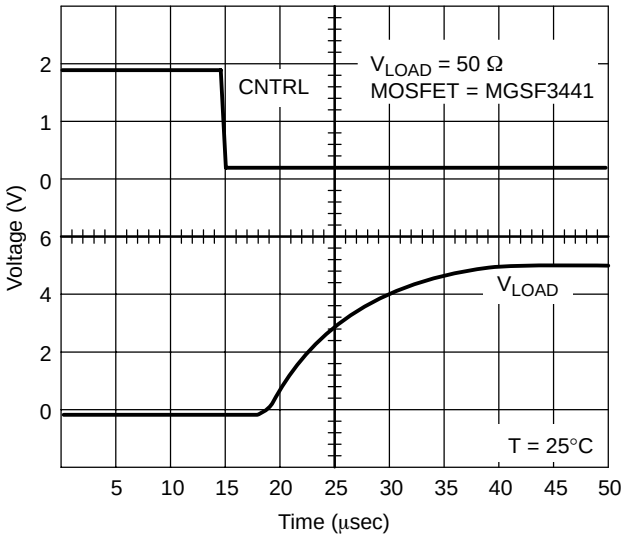


Figure 7. Typical Turn−on Time CNTRL to V_{LOAD}

APPLICATION INFORMATION

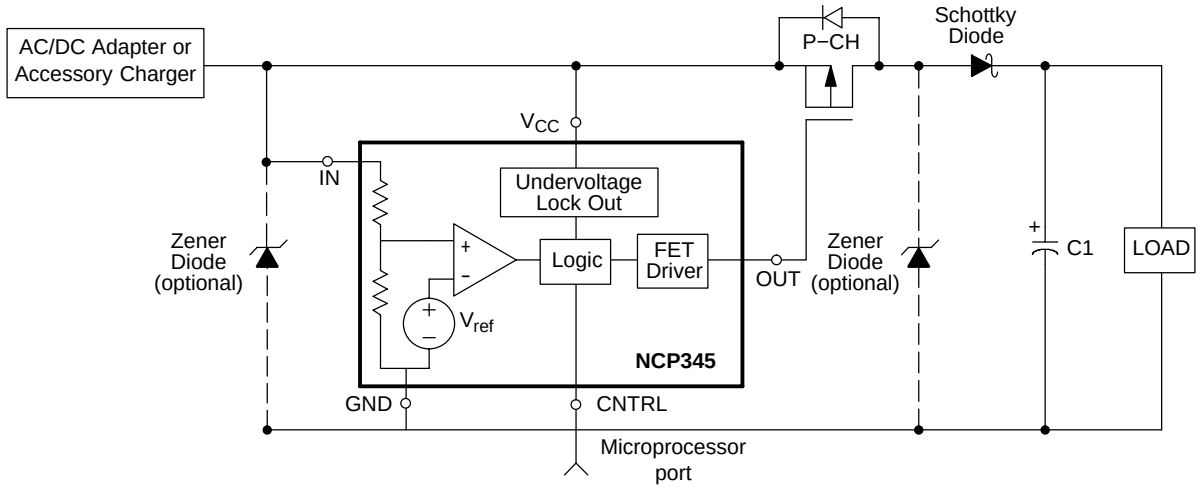


Figure 8.

Introduction

In many electronic products, an external AC/DC wall adapter is used to convert the AC line voltage into a regulated DC voltage or a current limited source. Line surges or faults in the adapter may result in overvoltage events that can damage sensitive electronic components within the product. This is becoming more critical as the operating voltages of many integrated circuits have been lowered due to advances in sub−micron silicon lithography. In addition, portable products with removable battery packs pose special problems since the pack can be removed at any time. If the user removes a pack in the middle of charging, a large transient voltage spike can occur which can damage the product. Finally, damage can result if the user plugs in the wrong adapter into the charging jack. The challenge of the product designer is to improve the robustness of the design and avoid situations where the product can be damaged due to un−expected, but unfortunately, likely events that will occur as the product is used.

Circuit Overview

To address these problems, the protection system above has been developed consisting of the NCP345 Over Voltage Protection IC and a P−channel MOSFET switch such as the MGSF3441. The NCP345 monitors the input voltage and will not turn on the MOSFET unless the input voltage is within a safe operating window that has an upper limit of 7.05 V. A zener diode can be placed in parallel to the load to provide for secondary protection during the brief time that it takes for the NCP345 to detect the overvoltage fault and disconnect the MOSFET. The decision to use this secondary diode is a function of the charging currents expected, load capacitance across the battery, and the desired protection voltage by analyzing the dV/dT rise that occurs during the brief time it takes to turn−off the MOSFET. For battery powered applications, a low−forward voltage Schottky diode such as the MBRM120LT3 can be placed in series with the MOSFET to block the body diode of the MOSFET and prevent shorting the battery out if the input is accidentally shorted to ground. This provides additional voltage margin at the load since there is a small forward drop across this diode that reduces the voltage at the load.

When the protection circuit turns off the MOSFET, there can be a sudden rise in the input voltage of the device. This transient can be quite large depending on the impedance of the supply and the current being drawn from the supply at the time of an overvoltage event. This inductive spike can be clamped with a zener diode from IN to ground. This diode breakdown voltage should be well above the worst case supply voltage provided from the AC/DC adapter or Cigarette Lighter Adapter (CLA), since the zener is only intended to clamp the transient. The NCP345 is designed so that the IN and V_{CC} pin can safely protect up to 25 V and withstand transients to 30 V. Since these spikes can be very narrow in duration, it is important to use a high bandwidth probe and oscilloscope when prototyping the product to verify the operation of the circuit under all the transient conditions. A similar problem can result due to contact bounce as the DC source is plugged into the product.

For portable products it is normal to have a capacitor to ground in parallel with the battery. If the product has a battery pack that is easily removable during charging, this scenario should be analyzed. Under that situation, the charging current will go into the capacitor and the voltage may rise rapidly depending on the capacitor value, the charging current and the power supply response time.

Normal Operation

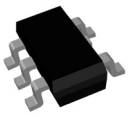
Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The OVP monitors the voltage from the charger and if the voltage exceeds a nominal voltage of 6.85 V, the OUT signal drives the gate of the MOSFET to within 1.0 V of V_{CC}, thus turning off the FET and disconnecting the source from the load. The nominal time it takes to drive the gate to this state is 400 nsec (1.0 usec maximum for gate capacitance of < 12 nF). Typical turn off performance using the CNTRL input can be seen in Figure 6. The CNTRL input can also be used to interrupt charging and allow the microcontroller to measure the cell voltage under a normal condition to get a more accurate measure of the battery voltage. Once the over voltage is removed, the NCP345 will turn on the MOSFET. The turn on circuitry is designed to turn on the MOSFET more gradually to limit the in−rush current. Typical turn−on performance is illustrated using the MGSF3441 in Figure 7. This characteristic is a function of the threshold of the MOSFET and will vary depending on the device characteristics such as the gate capacitance.

The OVP has an under voltage lockout (UVLO) circuit which disables the gate driver circuit until the UVLO senses that the V_{CC} voltage is above 2.6 V. Once the UVLO has released the gate driver circuit, the OUT signal will stay high until the voltage on the IN is sensed. If the input voltage to IN is less than 6.85 V nominal, then the OUT signal will be driven LOW and the FET will be turned on so the source can be connected to the load.

There are three events that will cause the OVP to drive the gate of the FET to a HIGH state.

- Voltage on V_{CC} falls below the UVLO threshold
- Voltage on IN rises above 6.85 V (nominal)
- CNTRL input is driven to a logic High

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

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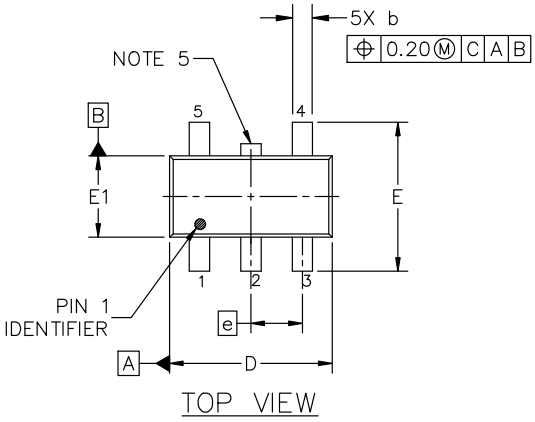
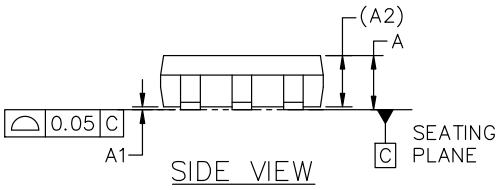
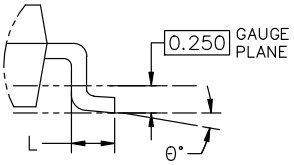


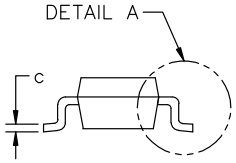
TOP VIEW



SIDE VIEW



DETAIL "A"
SCALE 2:1

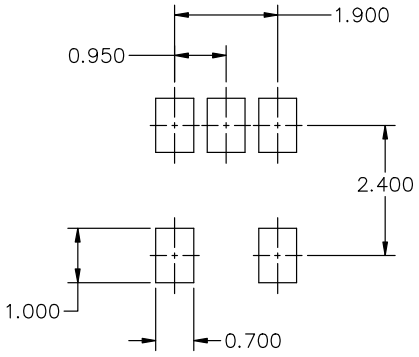


END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

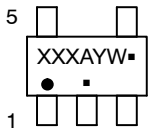
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

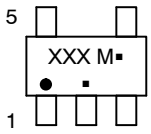
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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