Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

CY91460P Series

FR60 32-bit Microcontroller

CY91460P series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 141 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously
  - 2 transfer sources (internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  - 10-bit resolution: maximum 41 channels *
  - Conversion time: minimum 1 µs
- External interrupt inputs : 16 channels *
  - 9 channels shared with CAN RX or I^2C pins
- Bit search module (for REALOS)
  - Function to search the first bit position of “1”, “0”, “changed” from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 12 channels, 4 channels with FIFO *
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I^2C bus interface (supports 400 kbps): 4 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): up to 4 channels
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- 16-bit PPG timer : 32 channels *
- 16-bit PFM timer : 1 channel
- 16-bit reload timer: 16 channels
  - 8 reload timers can be used as up to 4 32-bit reload timers (by cascading 2 reload timers each).
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 8 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 4 channels (4*8-bit or 2*16-bit) *
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock supervisor
  - Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

Note: * The maximum channel count is given; the real number depends on port multiplexing.

- Clock modulator
- Clock monitor
- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Package and technology

- Package : QFP-176
- CMOS 0.18 µm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40°C and + 125°C

Contents

Product Lineup 4
Pin Assignment 7
CY91F465PA 7
CY91F467PA 8
Pin Description 9
CY91F465PA, CY91F467PA 9
I/O Circuit Types 23
Port Multiplexing 29
PPMUX Register 29
PPMUX2 Register (CY91F467PA) 29
Multiplex Pinout CY91F465PA 30
Multiplex Pinout CY91F467PA 31
Reload Timer / New Features 32
Overview 32
Features 32
Registers 33
Cascading Operation 35
Additional PPGs 36
Register 36
A/D Converter / New Features (CY91F467PA) 38
A/D Converter Features 38
Analog Input Connections 38
A/D Converter / Range Comparator (CY91F467PA) 40
Overview of A/D Converter and A/D Range Comparator 40
A/D Converter Input Impedance 41
Block Diagram of A/D Converter 42
Registers of the A/D Converter 43
Range Comparator 53
Operation of A/D Converter 60
ADC Interrupt Generation and DMA Access 63
Handling Devices 64
Preventing Latch-up 64
Handling of unused input pins 64
Power supply pins 64
Crystal oscillator circuit 64
Notes on using external clock 64
Mode pins (MD_x) 65
Notes on operating in PLL clock mode 65
Pull-up control 65
Notes on Debugger 66
Execution of the RETI Command 66
Break function 66
Operand break 66
Notes on PS register 66
Block Diagram 67
CY91F465PA, CY91F467PA 67
CPU and Control Unit 68
Features 68
Internal architecture 68
Programming model 69
Registers 70
Embedded Program/Data Memory (Flash) 73
Flash features 73
Operation modes: 73
Flash access in CPU mode 74
Parallel Flash programming mode 78
Poweron Sequence in parallel programming mode 79
Flash Security 80
Notes About Flash Memory CRC Calculation 82
Embedded Data Flash (CY91F467PA) 83
Data Flash Features 83
Data Flash Block Diagram 83
Data Flash Operation Modes 84
Data Flash access in CPU mode 85
Data Flash Registers 88
Data Flash Interrupts and DMA Access 94
Data Flash parallel programming mode 95
Data Flash Security 97
Memory Space 101
Memory Maps 102
CY91F465PA, CY91F467PA 102
I/O Map 103
CY91F465PA, CY91F467PA 103
Flash Memory, Data Flash and External Bus Area 138
Data Flash memory sector organisation 140
Interrupt Vector Table 141
Recommended Settings 146
PLL and Clockgear settings 146
Clock Modulator settings 147
Electrical Characteristics 152
Absolute maximum ratings 152
Recommended operating conditions 155
DC characteristics 156
A/D converter characteristics 160
FLASH memory program/erase characteristics 164
AC characteristics 166
Ordering Information 188
Package Dimension 189
Revision History 190
Major Changes 191
Document History 192

1. Product Lineup

Feature	Emulation Devices		CY91F465PA	CY91F467PA
	CY91V460A	CY91FV460B		
Max. core frequency (CLKB)	80 MHz	100 MHz	100 MHz	100 MHz
Max. resource frequency (CLKP)	40 MHz	50 MHz	50 MHz	50 MHz
Max. external bus frequency (CLKT)	40 MHz	50 MHz	50 MHz	50 MHz
Max. CAN frequency (CLKCAN)	20 MHz	50 MHz	50 MHz	50 MHz
Max. FlexRay frequency (SCLK)	-	-	-	-
Technology	0.35µm	0.18µm	0.18µm	0.18µm
Watchdog timer	yes	yes	yes	yes
Watchdog timer (RC osc. based)	yes (disengageable)	yes	yes	yes
Bit Search	yes	yes	yes	yes
Reset input (INITX)	yes	yes	yes	yes
Hardware standby input (HSTX)	yes	no	no	no
Clock Modulator	yes	yes	yes	yes
Clock Monitor	yes	yes	yes	yes
Low Power Mode	yes	yes	yes	yes
DMA	5 ch	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)*1	MPU (16 ch)*1	MPU (8 ch)*1	MPU (8 ch)*1
Flash memory	Emulation SRAM 32bit read data	Internal Flash memory 2112KB + external emulation SRAM with 64bit read data	544 KByte	1088 KByte
Satellite Flash memory	-	Data Flash 64 KByte	-	Data Flash 64 KByte
Flash Protection	-	yes	yes	yes
D-RAM	64 KByte	64 KByte	24 KByte	48 KByte
ID-RAM	64 KByte	64 KByte	16 KByte	32 KByte
Flash-Cache (Instruction cache)	16 KByte	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	16 KByte Boot Flash	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch	1 ch
Free Running Timer	8 ch	12 ch	8 ch*2	8 ch*2
ICU	8 ch	10 ch	8 ch*2	8 ch*2
OCU	8 ch	8 ch	8 ch*2	8 ch*2
Reload Timer	8 ch	16 ch	16 ch	16 ch
PPG 16-bit	16 ch	32 ch	32 ch*2	32 ch*2
PFM 16-bit	1 ch	1 ch	1 ch	1 ch
Sound Generator	1 ch	1 ch	1 ch	1 ch

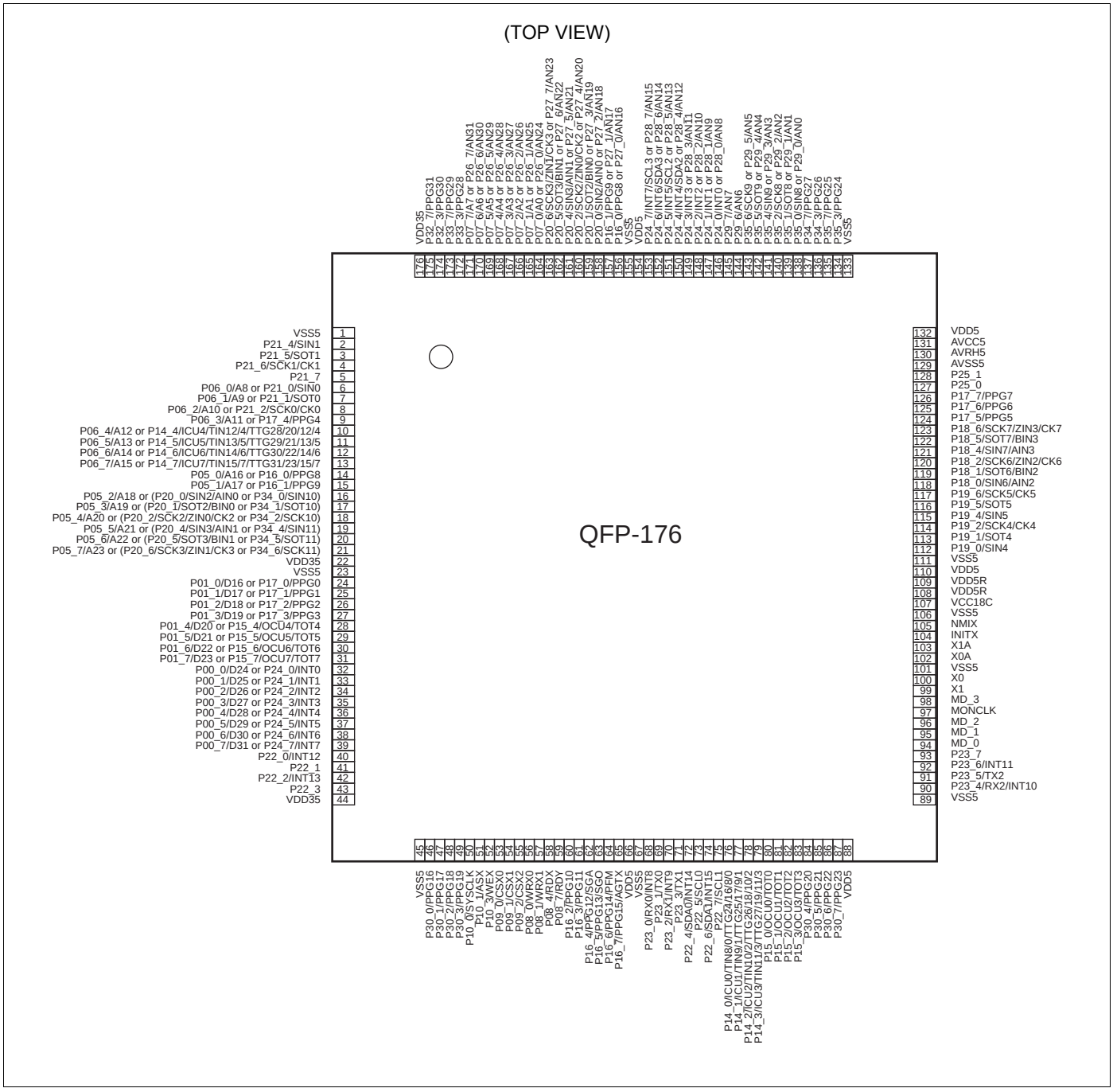
Feature	Emulation Devices		CY91F465PA	CY91F467PA
	CY91V460A	CY91FV460B		
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	4 ch (8-bit) / 2 ch (16-bit)	4 ch (8-bit) / 2 ch (16-bit)*2	4 ch (8-bit) / 2 ch (16-bit)*2
C_CAN	6 ch (128msg)	6 ch (128msg)	3 ch (32msg)	4 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	16 ch FIFO	8 ch + 4 ch FIFO*2	8 ch + 4 ch FIFO*2 (2 more pin relocations)
I^2C (400K)	4 ch	8 ch	4 ch*2	4 ch*2
FR external bus	yes (32bit addr, 32bit data)	yes (32bit addr, 32bit data)	yes (24bit addr, 16bit data)	yes (24bit addr, 16bit data)
External Interrupts	16 ch	16 ch	16 ch*2	16 ch*2
NMI Interrupts	1 ch	1 ch	1 ch	1 ch
General I/O ports	288	328 (24 non-multi-plexed)	141	141
SMC	6 ch	328 (24 non-multi-plexed)	-	-
LCD controller (40x4)	1 ch	1 ch	-	-
ADC (10-bit)	32 ch	32 ch + 22 ch (2 ADC macros)	32 ch*2	32 ch *2 + 9 ch (2 ADC macros)
Alarm Comparator	2 ch	2 ch	-	-
Supply Supervisor (low voltage detection)	yes	yes	yes	yes
Clock Supervisor	yes	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32kHz	32kHz	32kHz	32kHz
RC oscillator	100kHz	100kHz / 2MHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 20	x 25	x 25	x 25
DSU4	yes	yes	no	no
EDSU	yes (32 BP)*1	yes (32 BP)*1	yes (16 BP)*1	yes (16 BP)*1
Supply voltage	3V/5V	3V/5V	3V/5V	3V/5V
Regulator	yes	yes	yes	yes
Power consumption	n.a.	n.a.	< 1.4 W	< 1.4 W
Temperature Range (Ta)	0..70 C	0..70 C	-40..125 C	-40..125 C

Feature	Emulation Devices		CY91F465PA	CY91F467PA
	CY91V460A	CY91FV460B		
Package	BGA660	BGA896	LQFP-176	LQFP-176
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 8 sec. typical	< 5 sec. typical	< 6 sec. typical

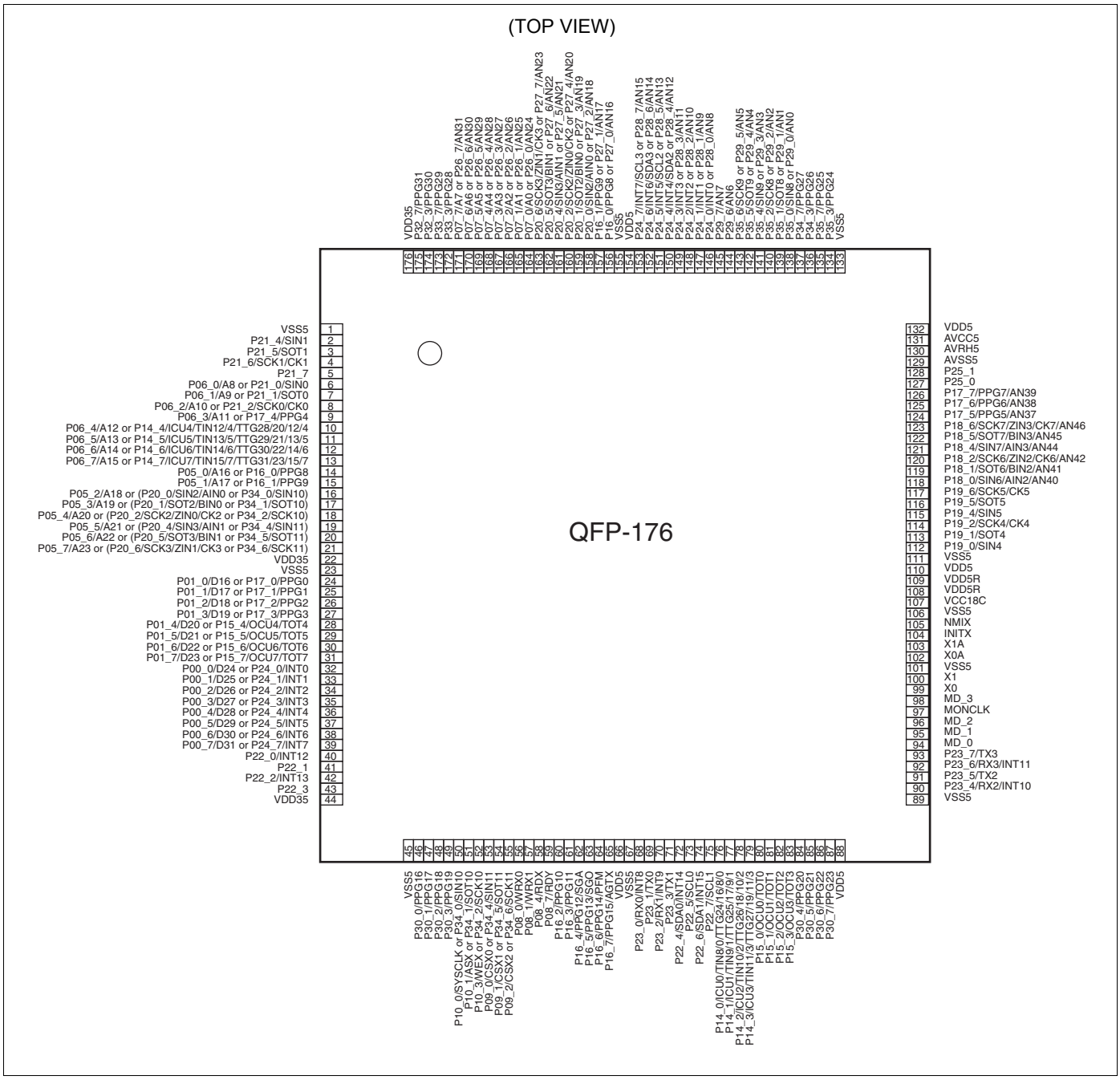
*1: MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).
*2: Maximum channel count is shown; function is multiplexed with external bus addresses.

2. Pin Assignment

2.1 CY91F465PA



2.2 CY91F467PA



The pinout of CY91F467PA differs versus CY91F465PA at the following pins:

- Pins 50-55: Added re-located LIN-USART10/11
- Pins 92-93: Added CAN3 RX3,TX3
- Pins 118-126: Added ADC channels AN37-42, AN44-46
- Pins 99-100: X0/X1 are mirrored

3. Pin Description

3.1 CY91F465PA, CY91F467PA

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
2	P21_4	I/O	A	—	General-purpose input/output port
	SIN1				Data input pin of USART1
3	P21_5	I/O	A	—	General-purpose input/output port
	SOT1				Data output pin of USART1
4	P21_6	I/O	A	—	General-purpose input/output port
	SCK1				Clock input/output pin of USART1
	CK1				External clock input pin of free-run timer 1
5	P21_7	I/O	A	—	General-purpose input/output port
6	P06_0	I/O	A	PPMUX.PS4=0	General-purpose input/output port
	A8				Signal pin of external address bus (bit8)
	OR				
	P21_0	I/O	A	PPMUX.PS4=1	General-purpose input/output port
	SIN0				Data input pin of USART0
7	P06_1	I/O	A	PPMUX.PS4=0	General-purpose input/output port
	A9				Signal pin of external address bus (bit9)
	OR				
	P21_1	I/O	A	PPMUX.PS4=1	General-purpose input/output port
	SOT0				Data output pin of USART0
8	P06_2	I/O	A	PPMUX.PS4=0	General-purpose input/output port
	A10				Signal pin of external address bus (bit10)
	OR				
	P21_2	I/O	A	PPMUX.PS4=1	General-purpose input/output port
	SCK0				Clock input/output pin of USART0
	CK0				External clock input pin of free-run timer 0
9	P06_3	I/O	A	PPMUX.PS4=0	General-purpose input/output port
	A11				Signal pin of external address bus (bit11)
	OR				
	P17_4	I/O	A	PPMUX.PS4=1	General-purpose input/output port
	PPG4				Output pin of PPG timer

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
10 to 13	P06_4 to P06_7	I/O	A	PPMUX.PS4=0	General-purpose input/output ports
	A12 to A15				Signal pins of external address bus (bit12 to bit15)
	OR				
	P14_4 to P14_7	I/O	A	PPMUX.PS4=1	General-purpose input/output ports
	ICU4 to ICU7				Input capture input pins
	TIN12/4 to TIN15/7				External trigger input pins of reload timer
	TTG28/20/12/4 to TTG31/23/15/7				External trigger input pins of PPG timer
14	P05_0	I/O	A	PPMUX.PR10=0	General-purpose input/output port
	A16				Signal pin of external address bus (bit16 to bit17)
	OR				
	P16_0	I/O	A	PPMUX.PR10=1	General-purpose input/output port
	PPG8				Output pin of PPG timer
15	P05_1	I/O	A	PPMUX.PR11=0	General-purpose input/output port
	A17				Signal pin of external address bus (bit16 to bit17)
	OR				
	P16_1	I/O	A	PPMUX.PR11=1	General-purpose input/output port
	PPG9				Output pin of PPG timer
16	P05_2	I/O	A	PPMUX.PR12=0	General-purpose input/output port
	A18				Signal pin of external address bus (bit18)
	OR				
	P20_0	I/O	A	PPMUX.PR12=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SIN2				Data input pin of USART2
	AIN0				Up/down counter input pin
	OR				
	P34_0	I/O	A	PPMUX.PR12=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SIN10				Data input pin of USART10
17	P05_3	I/O	A	PPMUX.PR13=0	General-purpose input/output port
	A19				Signal pin of external address bus (bit19)
	OR				
	P20_1	I/O	A	PPMUX.PR13=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SOT2				Data output pin of USART2
	BIN0				Up/down counter input pin
	OR				
	P34_1	I/O	A	PPMUX.PR13=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SOT10				Data output pin of USART10

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
18	P05_4	I/O	A	PPMUX.PR14=0	General-purpose input/output port
	A20				Signal pin of external address bus (bit20)
	OR				
	P20_2	I/O	A	PPMUX.PR14=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SCK2				Clock input/output pin of USART2
	ZIN0				Up/down counter input pin
	CK2				External clock input pin of free-run timer 2
	OR				
	P34_2	I/O	A	PPMUX.PR14=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SCK10				Clock input/output pin of USART10
19	P05_5	I/O	A	PPMUX.PR15=0	General-purpose input/output port
	A21				Signal pin of external address bus (bit21)
	OR				
	P20_4	I/O	A	PPMUX.PR15=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SIN3				Data input pin of USART3
	AIN1				Up/down counter input pin
	OR				
	P34_4	I/O	A	PPMUX.PR15=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SIN11				Data input pin of USART11
20	P05_6	I/O	A	PPMUX.PR16=0	General-purpose input/output port
	A22				Signal pin of external address bus (bit22)
	OR				
	P20_5	I/O	A	PPMUX.PR16=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SOT3				Data output pin of USART3
	BIN1				Up/down counter input pin
	OR				
	P34_5	I/O	A	PPMUX.PR16=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SOT11				Data output pin of USART11
21	P05_7	I/O	A	PPMUX.PR17=0	General-purpose input/output port
	A23				Signal pin of external address bus (bit23)
	OR				
	P20_6	I/O	A	PPMUX.PR17=1 and PPMUX.PRPS0=1	General-purpose input/output port
	SCK3				Clock input/output pin of USART3
	ZIN1				Up/down counter input pin
	CK3				External clock input pin of free-run timer 3
	OR				
	P34_6	I/O	A	PPMUX.PR17=1 and PPMUX.PRPS0=0	General-purpose input/output port
	SCK11				Clock input/output pin of USART11

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
24 to 27	P01_0 to P01_3	I/O	A	PPMUX.PS3=0	General-purpose input/output ports
	D16 to D19				Signal pins of external data bus (bit16 to bit19)
	OR				
	P17_0 to P17_3	I/O	A	PPMUX.PS3=1	General-purpose input/output ports
	PPG0 to PPG3				Output pins of PPG timer
28 to 31	P01_4 to P01_7	I/O	A	PPMUX.PS3=0	General-purpose input/output ports
	D20 to D23				Signal pins of external data bus (bit20 to bit23)
	OR				
	P15_4 to P15_7	I/O	A	PPMUX.PS3=1	General-purpose input/output ports
	OCU4 to OCU7				Output compare output pins
	TOT4 to TOT7				Reload timer output pins
32 to 39	P00_0 to P00_7	I/O	A	PPMUX.PR0=0	General-purpose input/output ports
	D24 to D31				Signal pins of external data bus (bit24 to bit31)
	OR				
	P24_0 to P24_7	I/O	A	PPMUX.PR0=1	General-purpose input/output ports
	INT0 to INT7				External interrupt input pins
40	P22_0	I/O	A	—	General-purpose input/output port
	INT12				External interrupt input pin
41	P22_1	I/O	A	—	General-purpose input/output port
42	P22_2	I/O	A	—	General-purpose input/output port
	INT13				External interrupt input pin
43	P22_3	I/O	A	—	General-purpose input/output port
46 to 49	P30_0 to P30_3	I/O	A	—	General-purpose input/output ports
	PPG16 to PPG19				Output pins of PPG timer
50	P10_0	I/O	A	—	General-purpose input/output port
	SYSCLK				External bus clock output pin
	OR (CY91F467PA only)				
	P34_0	I/O	A	PPMUX2.PR0=1	General-purpose input/output port
	SIN10				Data input pin of USART10
51	P10_1	I/O	A	—	General-purpose input/output port
	ASX				Address strobe output pin
	OR (CY91F467PA only)				
	P34_1	I/O	A	PPMUX2.PR1=1	General-purpose input/output port
	SOT10				Data output pin of USART10
52	P10_3	I/O	A	—	General-purpose input/output port
	WEX				Write enable output pin
	OR (CY91F467PA only)				
	P34_2	I/O	A	PPMUX2.PR2=1	General-purpose input/output port
	SCK10				Clock input/output pin of USART10

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
53	P09_0	I/O	A	—	General-purpose input/output port
	CSX0				Chip select output pin
	OR (CY91F467PA only)				
	P34_4	I/O	A	PPMUX2.PR3=1	General-purpose input/output port
	SIN11				Data input pin of USART11
54	P09_1	I/O	A	—	General-purpose input/output port
	CSX1				Chip select output pin
	OR (CY91F467PA only)				
	P34_5	I/O	A	PPMUX2.PR4=1	General-purpose input/output port
	SOT11				Data output pin of USART11
55	P09_2	I/O	A	—	General-purpose input/output port
	CSX2				Chip select output pin
	OR (CY91F467PA only)				
	P34_6	I/O	A	PPMUX2.PR5=1	General-purpose input/output port
	SCK11				Clock input/output pin of USART11
56, 57	P08_0, P08_1	I/O	A	—	General-purpose input/output ports
	WRX0, WRX1				External write strobe output pins
58	P08_4	I/O	A	—	General-purpose input/output port
	RDX				External read strobe output pin
59	P08_7	I/O	A	—	General-purpose input/output port
	RDY				External ready input pin
60, 61	P16_2, P16_3	I/O	A	—	General-purpose input/output ports
	PPG10, PPG11				Output pins of PPG timer
62	P16_4	I/O	A	—	General-purpose input/output port
	PPG12				Output pin of PPG timer
	SGA				SGA output pin of sound generator
63	P16_5	I/O	A	—	General-purpose input/output port
	PPG13				Output pin of PPG timer
	SGO				SGO output pin of sound generator
64	P16_6	I/O	A	—	General-purpose input/output port
	PPG14				Output pin of PPG timer
	PFM				Pulse frequency modulator output pin
65	P16_7	I/O	A	—	General-purpose input/output port
	PPG15				Output pin of PPG timer
	ATGX				A/D converter external trigger input pin
68	P23_0	I/O	A	—	General-purpose input/output port
	RX0				RX input pin of CAN0
	INT8				External interrupt input pin
69	P23_1	I/O	A	—	General-purpose input/output port
	TX0				TX output pin of CAN0

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
70	P23_2	I/O	A	—	General-purpose input/output port
	RX1				RX input pin of CAN1
	INT9				External interrupt input pin
71	P23_3	I/O	A	—	General-purpose input/output port
	TX1				TX output pin of CAN1
72	P22_4	I/O	C	—	General-purpose input/output port
	SDA0				I^2C bus DATA input/output pin (open drain)
	INT14				External interrupt input pin
73	P22_5	I/O	C	—	General-purpose input/output port
	SCL0				I^2C bus clock input/output pin (open drain)
74	P22_6	I/O	C	—	General-purpose input/output port
	SDA1				I^2C bus DATA input/output pin (open drain)
	INT15				External interrupt input pin
75	P22_7	I/O	C	—	General-purpose input/output port
	SCL1				I^2C bus clock input/output pin (open drain)
76 to 79	P14_0 to P14_3	I/O	A	—	General-purpose input/output ports
	ICU0 to ICU3				Input capture input pins
	TIN8/0 to TIN11/3				External trigger input pins of reload timer
	TTG24/16/8/0 to TTG27/19/11/3				External trigger input pins of PPG timer
80 to 83	P15_0 to P15_3	I/O	A	—	General-purpose input/output ports
	OCU0 to OCU3				Output compare output pins
	TOT0 to TOT3				Reload timer output pins
84 to 87	P30_4 to P30_7	I/O	A	—	General-purpose input/output ports
	PPG20 to PPG23				Output pins of PPG timer
90	P23_4	I/O	A	—	General-purpose input/output port
	RX2				RX input pin of CAN2
	INT10				External interrupt input pin
91	P23_5	I/O	A	—	General-purpose input/output port
	TX2				TX output pin of CAN2
92	P23_6	I/O	A	—	General-purpose input/output ports
	RX3				RX input pin of CAN3 *4
	INT11				External interrupt input pin
93	P23_7	I/O	A	—	General-purpose input/output port
	TX3				TX output pin of CAN3 *4
94	MD_0	I	G	—	Mode setting pin
95	MD_1	I	G	—	Mode setting pin
96	MD_2	I	G	—	Mode setting pin
97	MONCLK	O	M	—	Clock Monitor pin
98	MD_3	I	G	—	Fast clock input pin

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
99	X1	—	J1	—	Clock (oscillation) output, F465PA
	X0				Clock (oscillation) input, F467PA
100	X0	—	J1	—	Clock (oscillation) input, F465PA
	X1				Clock (oscillation) output, F467PA
102	X0A	—	J2	—	Sub clock (oscillation) input
103	X1A	—	J2	—	Sub clock (oscillation) output
104	INITX	I	H	—	External reset input pin
105	NMIX	I	H	—	Non-maskable interrupt input pin
112	P19_0	I/O	A	—	General-purpose input/output port
	SIN4				Data input pin of USART4
113	P19_1	I/O	A	—	General-purpose input/output port
	SOT4				Data output pin of USART4
114	P19_2	I/O	A	—	General-purpose input/output port
	SCK4				Clock input/output pin of USART4
	CK4				External clock input pin of free-run timer 4
115	P19_4	I/O	A	—	General-purpose input/output port
	SIN5				Data input pin of USART5
116	P19_5	I/O	A	—	General-purpose input/output port
	SOT5				Data output pin of USART5
117	P19_6	I/O	A	—	General-purpose input/output port
	SCK5				Clock input/output pin of USART5
	CK5				External clock input pin of free-run timer 5
118	P18_0	I/O	A or B *2	—	General-purpose input/output port
	SIN6				Data input pin of USART6
	AIN2				Up/down counter input pin
	AN40				Analog input pin of A/D converter 2 *3
119	P18_1	I/O	A or B *2	—	General-purpose input/output port
	SOT6				Data output pin of USART6
	BIN2				Up/down counter input pin
	AN41				Analog input pin of A/D converter 2 *3
120	P18_2	I/O	A or B *2	—	General-purpose input/output port
	SCK6				Clock input/output pin of USART6
	ZIN2				Up/down counter input pin
	CK6				External clock input pin of free-run timer 6
	AN42				Analog input pin of A/D converter 2 *3
121	P18_4	I/O	A or B *2	—	General-purpose input/output port
	SIN7				Data input pin of USART7
	AIN3				Up/down counter input pin
	AN44				Analog input pin of A/D converter 2 *3

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
122	P18_5	I/O	A or B *2	—	General-purpose input/output port
	SOT7				Data output pin of USART7
	BIN3				Up/down counter input pin
	AN45				Analog input pin of A/D converter 2 *3
123	P18_6	I/O	A or B *2	—	General-purpose input/output port
	SCK7				Clock input/output pin of USART7
	ZIN3				Up/down counter input pin
	CK7				External clock input pin of free-run timer 7
	AN46				Analog input pin of A/D converter 2 *3
124 to 126	P17_5 to P17_7	I/O	A or B *2	—	General-purpose input/output ports
	PPG5 to PPG7				Output pin of PPG timer
	AN37 to AN39				Analog input pins of A/D converter 2 *3
127, 128	P25_0, P25_1	I/O	A	—	General-purpose input/output ports
134	P35_3	I/O	A	—	General-purpose input/output port
	PPG24				Output pin of PPG timer
135	P35_7	I/O	A	—	General-purpose input/output port
	PPG25				Output pin of PPG timer
136	P34_3	I/O	A	—	General-purpose input/output port
	PPG26				Output pin of PPG timer
137	P34_7	I/O	A	—	General-purpose input/output port
	PPG27				Output pin of PPG timer
138	P35_0	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SIN8				Data input pin of USART8
	OR				
	P29_0	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN0				Analog input pin of A/D converter
139	P35_1	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SOT8				Data output pin of USART8
	OR				
	P29_1	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN1				Analog input pin of A/D converter
140	P35_2	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SCK8				Clock input/output pin of USART8
	OR				
	P29_2	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN2				Analog input pin of A/D converter

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
141	P35_4	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SIN9				Data input pin of USART9
	OR				
	P29_3	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN3				Analog input pin of A/D converter
142	P35_5	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SOT9				Data output pin of USART9
	OR				
	P29_4	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN4				Analog input pin of A/D converter
143	P35_6	I/O	B	PPMUX.PS5=0	General-purpose input/output port
	SCK9				Clock input/output pin of USART9
	OR				
	P29_5	I/O	B	PPMUX.PS5=1	General-purpose input/output port
	AN5				Analog input pin of A/D converter
144, 145	P29_6, P29_7	I/O	B	—	General-purpose input/output ports
	AN6, AN7				Analog input pins of A/D converter
146 to 149	P24_0 to P24_3	I/O	B	PPMUX.PS2=0 and PPMUX.PR0=0	General-purpose input/output ports
	INT0 to INT3				External interrupt input pins
	OR				
	P28_0 to P28_3	I/O	B	PPMUX.PS2=1 or PPMUX.PR0=1	General-purpose input/output ports
	AN8 to AN11				Analog input pins of A/D converter
150	P24_4	I/O	D	PPMUX.PS2=0 and PPMUX.PR0=0	General-purpose input/output port
	INT4				External interrupt input pin
	SDA2	I/O	D		I^2C bus DATA input/output pin (open drain)
	OR				
	P28_4	I/O	D	PPMUX.PS2=1 or PPMUX.PR0=1	General-purpose input/output port
	AN12				Analog input pin of A/D converter
151	P24_5	I/O	D	PPMUX.PS2=0 and PPMUX.PR0=0	General-purpose input/output port
	INT5				External interrupt input pin
	SCL2	I/O	D		I^2C bus clock input/output pin (open drain)
	OR				
	P28_5	I/O	D	PPMUX.PS2=1 or PPMUX.PR0=1	General-purpose input/output port
	AN13				Analog input pin of A/D converter
152	P24_6	I/O	D	PPMUX.PS2=0 and PPMUX.PR0=0	General-purpose input/output port
	INT6				External interrupt input pin
	SDA3				I^2C bus DATA input/output pin (open drain)
	OR				
	P28_6	I/O	D	PPMUX.PS2=1 or PPMUX.PR0=1	General-purpose input/output port
	AN14				Analog input pin of A/D converter

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
153	P24_7	I/O	C	PPMUX.PS2=0 and PPMUX.PR0=0	General-purpose input/output port
	INT7				External interrupt input pin
	SCL3				I^2C bus clock input/output pin (open drain)
	OR				
	P28_7	I/O	B	PPMUX.PS2=1 or PPMUX.PR0=1	General-purpose input/output port
	AN15				Analog input pin of A/D converter
156	P16_0	I/O	A	PPMUX.PS1=0 and PPMUX.PR10=0	General-purpose input/output port
	PPG8				Output pin of PPG timer
	OR				
	P27_0	I/O	A	PPMUX.PS1=1 or PPMUX.PR10=1	General-purpose input/output port
	AN16				Analog input pin of A/D converter
157	P16_1	I/O	A	PPMUX.PS1=0 and PPMUX.PR11=0	General-purpose input/output port
	PPG9				Output pin of PPG timer
	OR				
	P27_1	I/O	A	PPMUX.PS1=1 or PPMUX.PR11=1	General-purpose input/output port
	AN17				Analog input pin of A/D converter
158	P20_0	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR12=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SIN2				Data input pin of USART2
	AIN0				Up/down counter input pin
	OR				
	P27_2	I/O	A	PPMUX.PS1=1 or (PPMUX.PR12=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN18				Analog input pin of A/D converter
159	P20_1	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR13=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SOT2				Data output pin of USART2
	BIN0				Up/down counter input pin
	OR				
	P27_3	I/O	A	PPMUX.PS1=1 or (PPMUX.PR13=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN19				Analog input pin of A/D converter

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
160	P20_2	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR14=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SCK2				Clock input/output pin of USART2
	ZIN0				Up/down counter input pin
	CK2				External clock input pin of free-run timer 2
	OR				
	P27_4	I/O	A	PPMUX.PS1=1 or (PPMUX.PR14=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN20				Analog input pin of A/D converter
161	P20_4	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR15=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SIN3				Data input pin of USART3
	AIN1				Up/down counter input pin
	OR				
	P27_5	I/O	A	PPMUX.PS1=1 or (PPMUX.PR15=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN21				Analog input pin of A/D converter
162	P20_5	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR16=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SOT3				Data output pin of USART3
	BIN1				Up/down counter input pin
	OR				
	P27_6	I/O	A	PPMUX.PS1=1 or (PPMUX.PR16=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN22				Analog input pin of A/D converter
163	P20_6	I/O	A	PPMUX.PS1=0 and_not (PPMUX.PR17=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	SCK3				Clock input/output pin of USART3
	ZIN1				Up/down counter input pin
	CK3				External clock input pin of free-run timer 3
	OR				
	P27_7	I/O	A	PPMUX.PS1=1 or (PPMUX.PR17=1 and PPMUX.PRPS0=1)	General-purpose input/output port
	AN23				Analog input pin of A/D converter
164	P07_0	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A0				Signal pin of external address bus (bit0)
	OR				
	P26_0	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN24				Analog input pin of A/D converter

Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
165	P07_1	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A1				Signal pin of external address bus (bit1)
	OR				
	P26_1	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN25				Analog input pin of A/D converter
166	P07_2	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A2				Signal pin of external address bus (bit2)
	OR				
	P26_2	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN26				Analog input pin of A/D converter
167	P07_3	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A3				Signal pin of external address bus (bit3)
	OR				
	P26_3	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN27				Analog input pin of A/D converter
168	P07_4	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A4				Signal pin of external address bus (bit4)
	OR				
	P26_4	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN28				Analog input pin of A/D converter
169	P07_5	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A5				Signal pin of external address bus (bit5)
	OR				
	P26_5	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN29				Analog input pin of A/D converter
170	P07_6	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A6				Signal pin of external address bus (bit6)
	OR				
	P26_6	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN30				Analog input pin of A/D converter
171	P07_7	I/O	A	PPMUX.PS0=0	General-purpose input/output port
	A7				Signal pin of external address bus (bit7)
	OR				
	P26_7	I/O	A	PPMUX.PS0=1	General-purpose input/output port
	AN31				Analog input pin of A/D converter
172	P33_3	I/O	A	—	General-purpose input/output port
	PPG28				Output pin of PPG timer
173	P33_7	I/O	A	—	General-purpose input/output port
	PPG29				Output pin of PPG timer

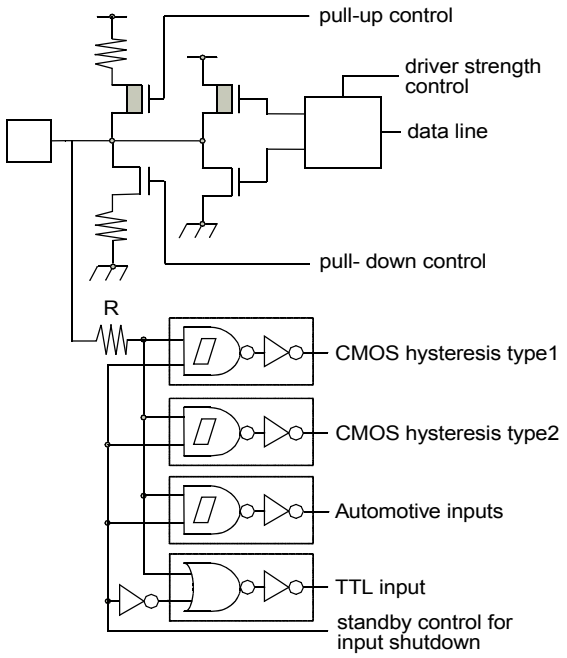
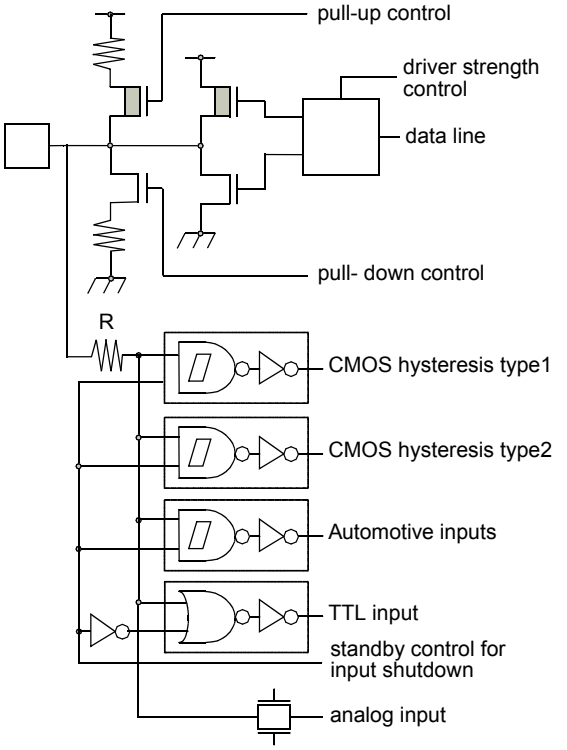
Pin no.	Pin name	I/O	I/O circuit type*1	Mux	Function
174	P32_3	I/O	A	—	General-purpose input/output port
	PPG30				Output pin of PPG timer
175	P32_7	I/O	A	—	General-purpose input/output port
	PPG31				Output pin of PPG timer

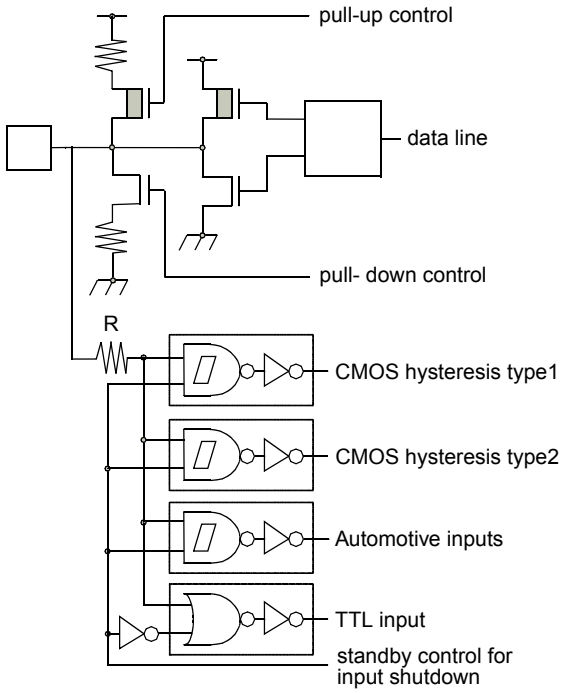
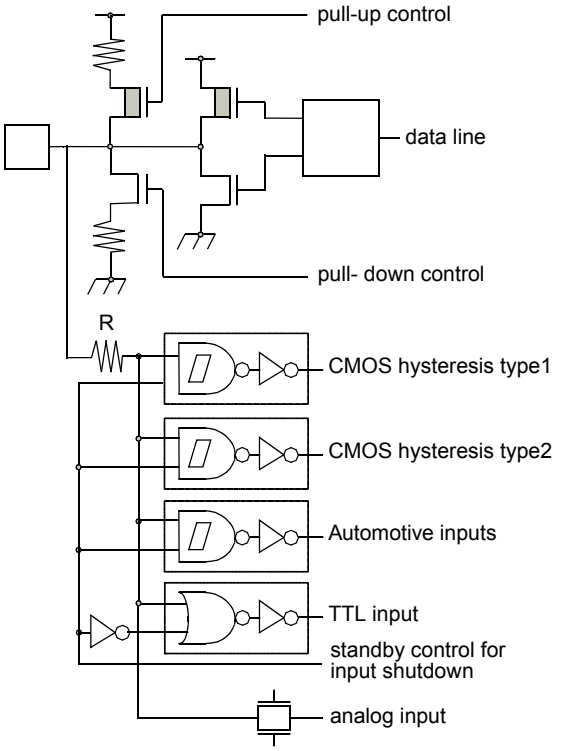
*1: For information about the I/O circuit type, refer to “4. I/O Circuit Types”.
*2: CY91F465PA has type A, CY91F467PA has type B
*3: A/D converter channels 37-42, 44-46 only available on CY91F467PA.
*4: CAN3 only available on CY91F467PA.

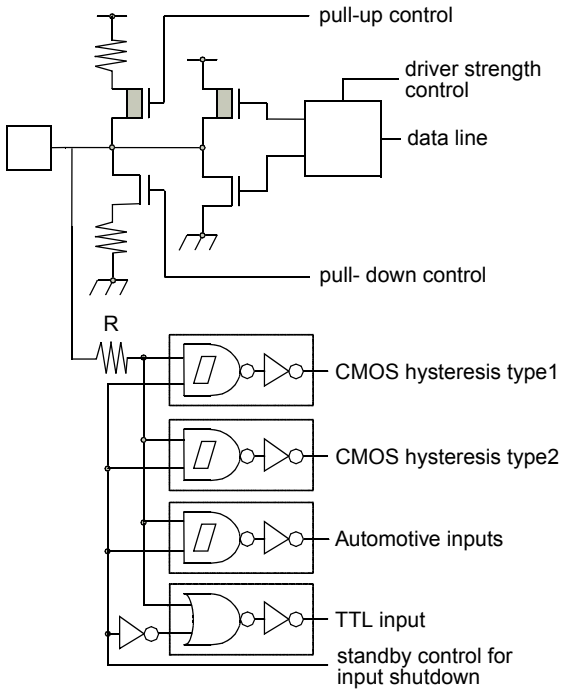
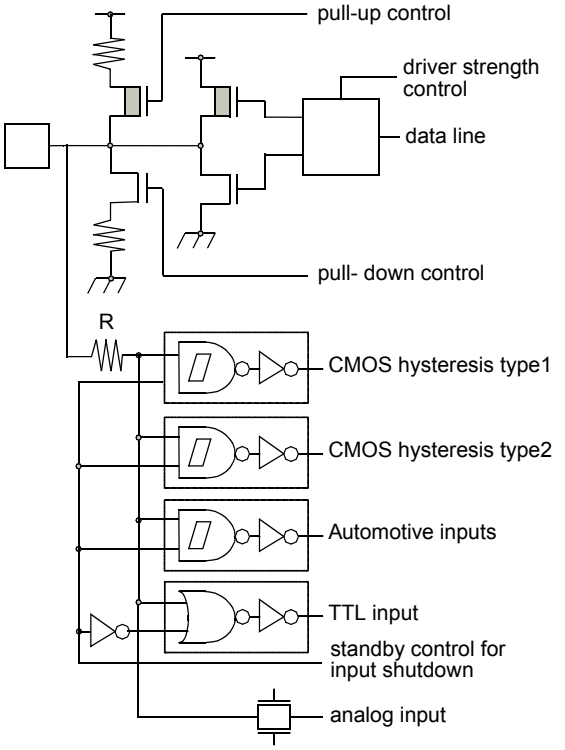
[Power supply/Ground pins]

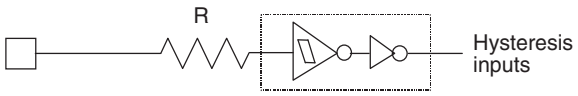
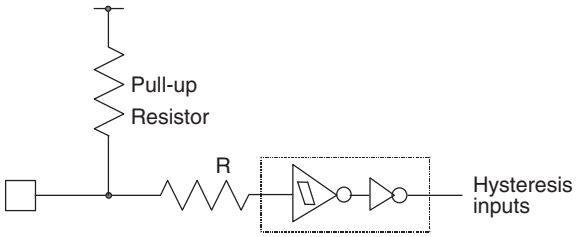
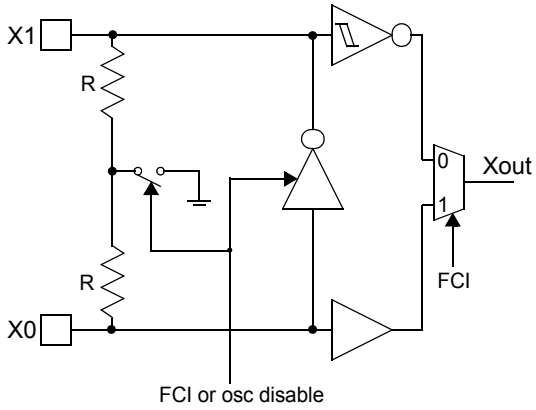
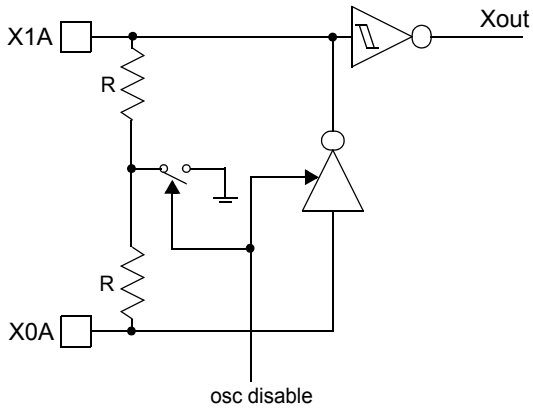
Pin no.	Pin name	I/O	Function
1, 23, 45, 67, 89, 101, 106, 111, 133, 155	VSS5	Supply	Ground pins
66, 88, 110, 132, 154	VDD5		Power supply pins
108, 109	VDD5R		Power supply pins for internal regulator
129	AVSS5		Analog ground pin for A/D converter
131	AVCC5		Power supply pin for A/D converter
130	AVRH5		Reference power supply pin for A/D converter
107	VCC18C		Capacitor connection pin for internal regulator
22, 44, 176	VDD35		Power supply pins for external bus part of I/O ring

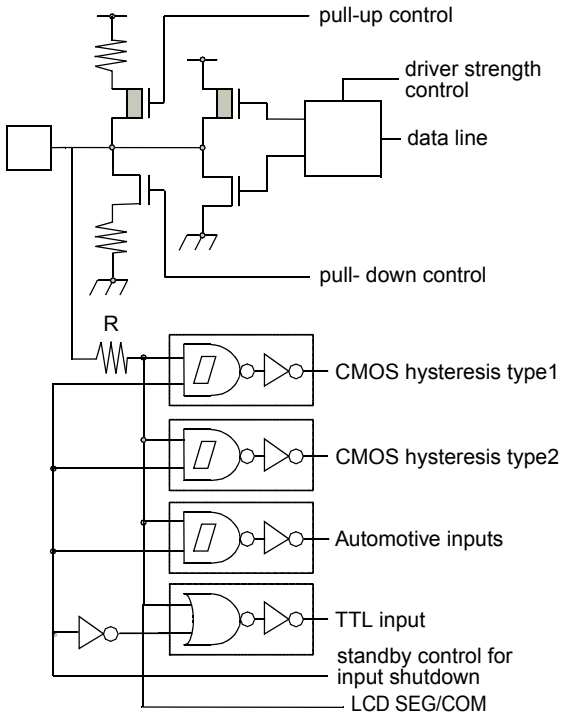
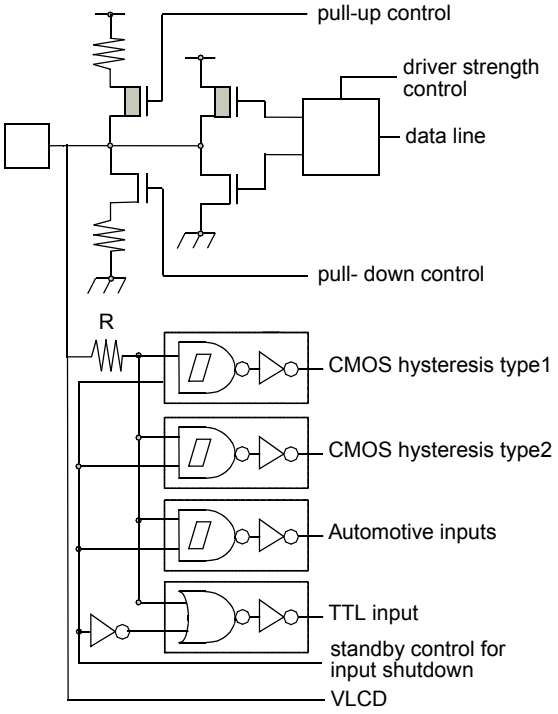
4. I/O Circuit Types

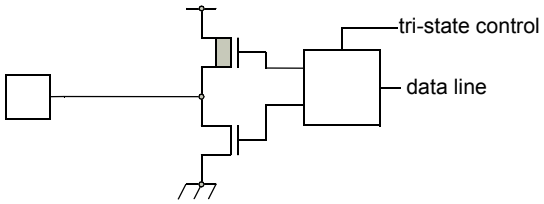
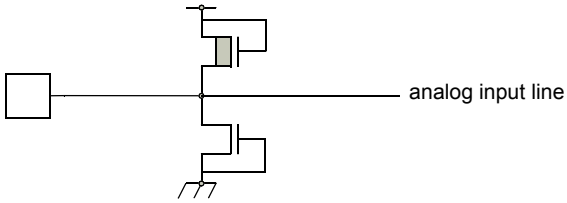
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

5. Port Multiplexing

5.1 PPMUX Register

CY91460P series uses port multiplexing. This means that there are more implemented resources than actual pins. Which ports/ resources are multiplexed to which pin depends on the PPMUX register setting.

	15	14	13	12	11	10	9	8
0x049A	PR17	PR16	PR15	PR14	PR13	PR12	PR11	PR10

	7	6	5	4	3	2	1	0
0x049B	PRPS0	PR0	PS5	PS4	PS3	PS2	PS1	PS0

The PPMUX register can only be written as a half-word. It is writable only once.
The PPMUX register is reset by INIT or by a soft reset (the initial value is 0x0000 then).

Note: Port relocation (via PRx) always has higher priority than Port Switching (via PSx).

5.2 PPMUX2 Register (CY91F467PA)

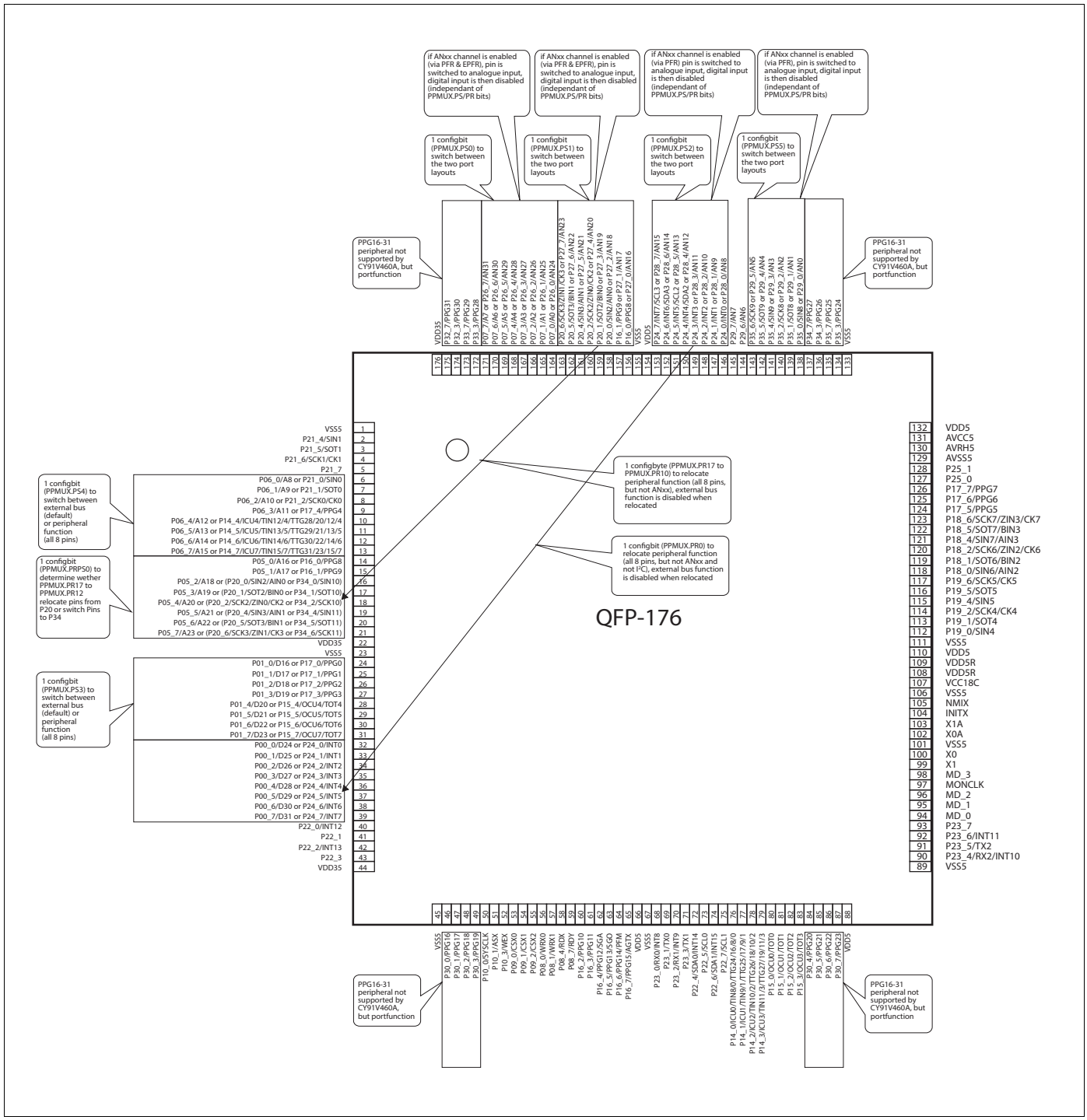
CY91F467PA has a second port multiplexing register, PPMUX2, for multiplexing of LIN-USART10,11.
The settings of PPMUX2 have priority over the settings of PPMUX.

	15	14	13	12	11	10	9	8
0x049C	-	-	PR5	PR4	PR3	PR2	PR1	PR0

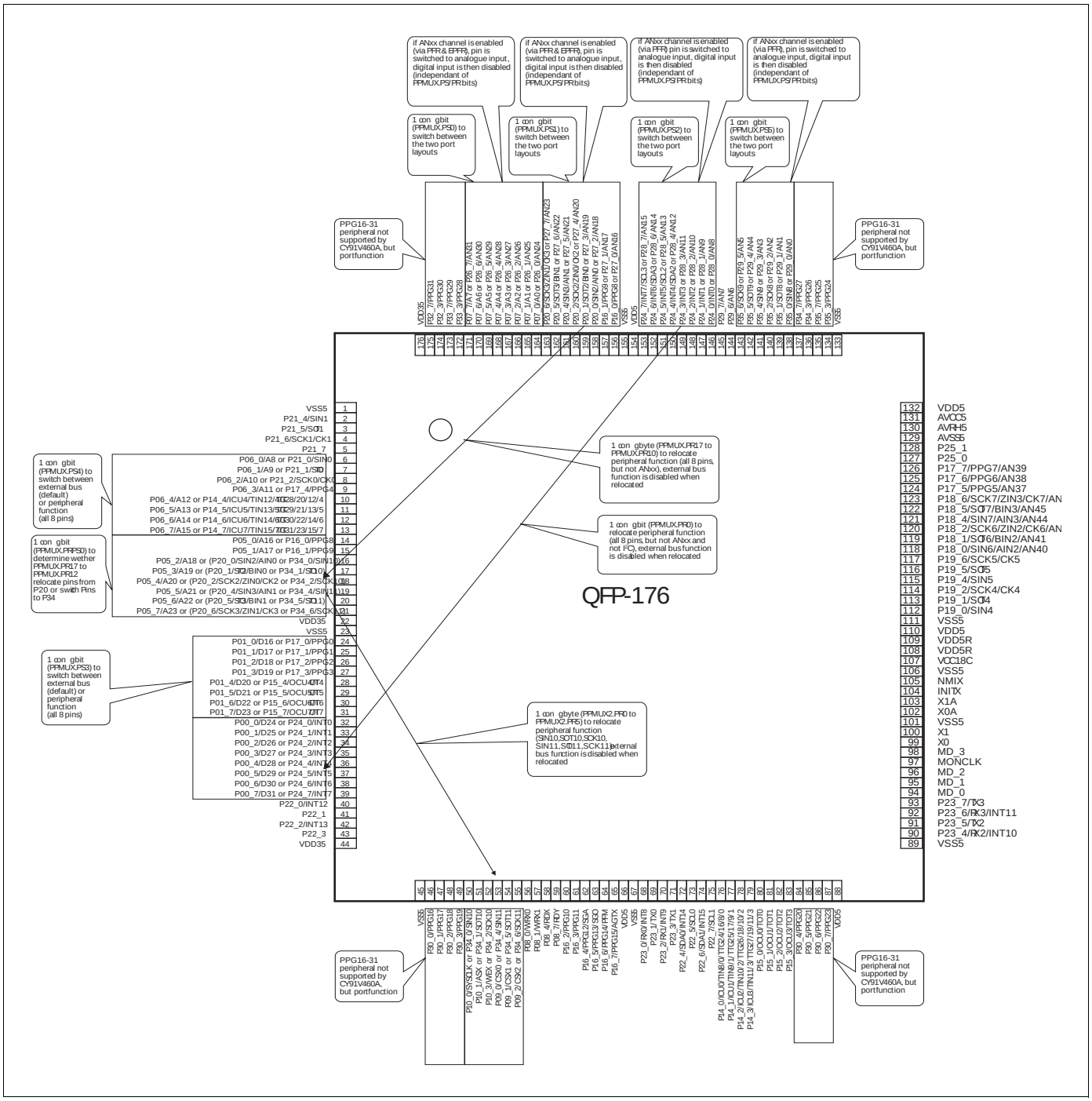
	7	6	5	4	3	2	1	0
0x049D	-	-	-	-	-	-	-	-

The PPMUX2 register can only be written as a half-word. It is writable only once.
The PPMUX2 register is reset by INIT or by a soft reset (the initial value is 0x00 then).

5.3 Multiplex Pinout CY91F465PA



5.4 Multiplex Pinout CY91F467PA



6. Reload Timer / New Features

6.1 Overview

The reload timer uses a 16 bit down counter to detect the input signal trigger and perform a count down.
The count length is 16 bits.

6.2 Features

Format: 16 bit down counter with reload register
Quantity: 16 (Output: 8 channels TOT[0 to 7])

Cascading clock mode: (only available for Reload timers 8,10,12,14)

- Count clock for Reload timer 8: Output of Reload timer 9
- Count clock for Reload timer 10: Output of Reload timer 11
- Count clock for Reload timer 12: Output of Reload timer 13
- Count clock for Reload timer 14: Output of Reload timer 15

Count active edge: When in external event mode, choose from 3 types.

- External trigger (rising /falling/both edges)
  Interrupt: Request generated by underflow
  Other 1: Counter stop in software/can be reopened
  Other 2: Control of other peripheral functions possible
- PPG activation trigger source:
  Reload timer 8 : PPG16, PPG17
  Reload timer 9 : PPG18, PPG19
  Reload timer 10 : PPG20, PPG21
  Reload timer 11 : PPG22, PPG23
  Reload timer 12 : PPG24, PPG25
  Reload timer 13 : PPG26, PPG27
  Reload timer 14 : PPG28, PPG29
  Reload timer 15 : PPG30, PPG31
- A/D converter activation trigger source (Reload timer 7 : A/D)

6.3 Registers

6.3.1 TMCSR: Reload Timer Control Status Register

The control status register controls the operation mode of the reload timer and interrupts.

- TMCSR8 (Reload timer 8): Address: 00596H (Access: Byte, Half-word)
- TMCSR9 (Reload timer 9): Address: 0059EEH (Access: Byte, Half-word)
- TMCSR10 (Reload timer 10): Address: 005A6H (Access: Byte, Half-word)
- TMCSR11 (Reload timer 11): Address: 005AEH (Access: Byte, Half-word)
- TMCSR12 (Reload timer 12): Address: 005B6H (Access: Byte, Half-word)
- TMCSR13 (Reload timer 13): Address: 005BEH (Access: Byte, Half-word)
- TMCSR14 (Reload timer 14): Address: 005C6H (Access: Byte, Half-word)
- TMCSR15 (Reload timer 15): Address: 005CEH (Access: Byte, Half-word)

15	14	13	12	11	10	9	8	bit
			CSL2	CSL1	CSL0	MOD2	MOD1	
-	-	-	0	0	0	0	0	Initial Value
RX/WX	RX/WX	RX/WX	R/W	R/W	R/W	R/W0	R/W	Attribute
								Rewrite during operation

7	6	5	4	3	2	1	0	bit
MOD0		OULT	RELD	INTE	UF	CNTE	TRG	
0	-	0	0	0	0	0	0	Initial Value
R/W	RX/WX	R/W	R/W	R/W	R(RM1),W	R/W	R0/W	Attribute
					O	O	O	Rewrite during operation

(O: can be rewritten, x: cannot be rewritten)

bit12-10: Count clock selection **CLKP: peripheral clock**

CSL2	CSL1	CSL0	Count clock	Remarks
0	0	0	Internal clock CLKP/2	
0	0	1	Internal clock CLKP/8	
0	1	0	Internal clock CLKP/32	
0	1	1	External event (external clock)	
1	0	1	Internal clock CLKP/64	
1	1	0	Internal clock CLKP/128	
1	1	1	RLT n+1 output	only allowed for RLT 8, 10, 12, 14

6.3.2 TMR: Timer Register

- TMR8 (Reload timer 8): Address: 0592H (Access: Half-word)
- TMR9 (Reload timer 9): Address: 059AH (Access: Half-word)
- TMR10 (Reload timer 10): Address: 05A2H (Access: Half-word)
- TMR11 (Reload timer 11): Address: 05AAH (Access: Half-word)
- TMR12 (Reload timer 12): Address: 05B2H (Access: Half-word)
- TMR13 (Reload timer 13): Address: 05BAH (Access: Half-word)
- TMR14 (Reload timer 14): Address: 05C2H (Access: Half-word)
- TMR15 (Reload timer 15): Address: 05CAH (Access: Half-word)

6.3.3 TMRC: Consistent Timer Register

- TMR89 (Reload timer 8, 9): Address: 05D0H (Access: Word)
- TMR1011 (Reload timer 10, 11): Address: 05D4H (Access: Word)
- TMR1213 (Reload timer 12, 13): Address: 05D8H (Access: Word)
- TMR1415 (Reload timer 14, 15): Address: 05DCH (Access: Word)

31	30	29	28	27	26	25	24	bit
D31	D30	D29	D28	D27	D26	D25	D24	
X	X	X	X	X	X	X	X	Initial Value
R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	Attribute

23	22	21	20	19	18	17	16	bit
D23	D22	D21	D20	D19	D18	D17	D16	
X	X	X	X	X	X	X	X	Initial Value
R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	Attribute

15	14	13	12	11	10	9	8	bit
D15	D14	D13	D12	D11	D10	D9	D8	
X	X	X	X	X	X	X	X	Initial Value
R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	Attribute

7	6	5	4	3	2	1	0	bit
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	X	X	Initial Value
R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	Attribute

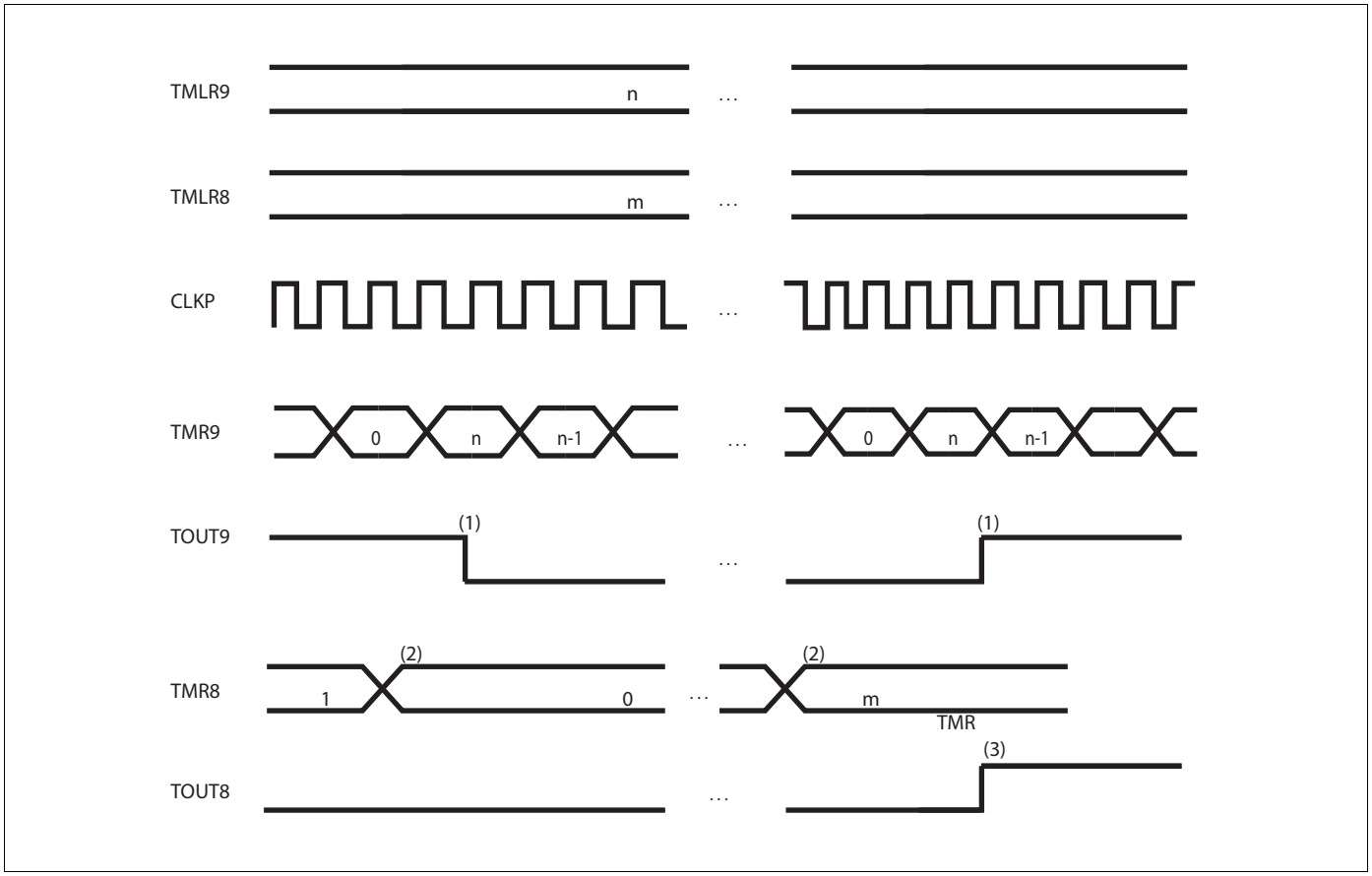
The count values of cascaded reload timers can be read out through the timer register TMRC at the same time. Upper halfword contain TMRn, lower halfword TMRn+1.
Please perform the read out using word access.

6.3.4 TMRLR: Reload register

- TMRLR8 (Reload timer 8): Address: 0590H (Access: Half-word)
- TMRLR9 (Reload timer 9): Address: 0598H (Access: Half-word)
- TMRLR10 (Reload timer 10): Address: 05A0H (Access: Half-word)
- TMRLR11 (Reload timer 11): Address: 05A8H (Access: Half-word)
- TMRLR12 (Reload timer 12): Address: 05B0H (Access: Half-word)
- TMRLR13 (Reload timer 13): Address: 05B8H (Access: Half-word)
- TMRLR14 (Reload timer 14): Address: 05C0H (Access: Half-word)
- TMRLR15 (Reload timer 15): Address: 05C8H (Access: Half-word)

6.4 Cascading Operation

In reload mode Reload timer 9 Output is set as Count event for Reload timer 8, both edge modes.



(1) TOUT9 signal change caused by underflow TMR9
(2) TMR8 decreased by TOUT9
(3) TOUT8 signal change caused by underflow of TMR8

7. Additional PPGs

7.1 Register

7.1.1 PCSR: PPG Cycle Setting Register

Controls the cycle of the PPG.

- PCSR16 (PPG16): Address 0512h (Access: Half-word)
- PCSR17 (PPG17): Address 0518h (Access: Half-word)
- PCSR18 (PPG18): Address 0522h (Access: Half-word)
- PCSR19 (PPG19): Address 0528h (Access: Half-word)
- PCSR20 (PPG20): Address 0532h (Access: Half-word)
- PCSR21 (PPG21): Address 0538h (Access: Half-word)
- PCSR22 (PPG22): Address 0542h (Access: Half-word)
- PCSR23 (PPG23): Address 0548h (Access: Half-word)
- PCSR24 (PPG24): Address 0552h (Access: Half-word)
- PCSR25 (PPG25): Address 0558h (Access: Half-word)
- PCSR26 (PPG26): Address 0562h (Access: Half-word)
- PCSR27 (PPG27): Address 0568h (Access: Half-word)
- PCSR28 (PPG28): Address 0572h (Access: Half-word)
- PCSR29 (PPG29): Address 0578h (Access: Half-word)
- PCSR30 (PPG30): Address 0582h (Access: Half-word)
- PCSR31 (PPG31): Address 0588h (Access: Half-word)

7.1.2 PDUT: PPG Duty Setting Register

Sets the duty of the PPG output waveform.

- PDUT16 (PPG16): Address 0514h (Access: Half-word)
- PDUT17 (PPG17): Address 051Ch (Access: Half-word)
- PDUT18 (PPG18): Address 0524h (Access: Half-word)
- PDUT19 (PPG19): Address 052Ch (Access: Half-word)
- PDUT20 (PPG20): Address 0534h (Access: Half-word)
- PDUT21 (PPG21): Address 053Ch (Access: Half-word)
- PDUT22 (PPG22): Address 0544h (Access: Half-word)
- PDUT23 (PPG23): Address 054Ch (Access: Half-word)
- PDUT24 (PPG24): Address 0554h (Access: Half-word)
- PDUT25 (PPG25): Address 055Ch (Access: Half-word)
- PDUT26 (PPG26): Address 0564h (Access: Half-word)
- PDUT27 (PPG27): Address 056Ch (Access: Half-word)
- PDUT28 (PPG28): Address 0574h (Access: Half-word)
- PDUT29 (PPG29): Address 057Ch (Access: Half-word)
- PDUT30 (PPG30): Address 0584h (Access: Half-word)
- PDUT31 (PPG31): Address 058Ch (Access: Half-word)

7.1.3 PCN: PPG Control Status register

Controls the operations and status of PPGs.

- PCN16 (PPG16): Address 0516h (Access: Byte, Half-word)
- PCN17 (PPG17): Address 051Eh (Access: Byte, Half-word)
- PCN18 (PPG18): Address 0526h (Access: Byte, Half-word)
- PCN19 (PPG19): Address 052Eh (Access: Byte, Half-word)
- PCN20 (PPG20): Address 0536h (Access: Byte, Half-word)
- PCN21 (PPG21): Address 053Eh (Access: Byte, Half-word)
- PCN22 (PPG22): Address 0546h (Access: Byte, Half-word)
- PCN23 (PPG23): Address 054Eh (Access: Byte, Half-word)
- PCN24 (PPG24): Address 0556h (Access: Byte, Half-word)
- PCN25 (PPG25): Address 055Eh (Access: Byte, Half-word)
- PCN26 (PPG26): Address 0566h (Access: Byte, Half-word)
- PCN27 (PPG27): Address 056Eh (Access: Byte, Half-word)
- PCN28 (PPG28): Address 0576h (Access: Byte, Half-word)
- PCN29 (PPG29): Address 057Eh (Access: Byte, Half-word)
- PCN30 (PPG30): Address 0586h (Access: Byte, Half-word)
- PCN31 (PPG31): Address 058Eh (Access: Byte, Half-word)

7.1.4 GCN1: General Control register 1

Selects a trigger input to PPG0 PPG16-PPG19, PPG20-PPG23, PPG24-PPG27 and PPG28-PPG31.

- GCN14 (PPG16-PPG19): Address 0500h (Access: Half-word)
- GCN15 (PPG20-PPG23): Address 0504h (Access: Half-word)
- GCN16 (PPG24-PPG27): Address 0505h (Access: Half-word)
- GCN17 (PPG28-PPG31): Address 050Ch (Access: Half-word)

7.1.5 GCN2: General Control register 2

Generates PPG16-PPG19, PPG20-PPG23, PPG24-PPG27 and PPG28-PPG31 internal trigger levels using software.

- GCN24 (PPG16-PPG19): Address 0503h (Access: Byte)
- GCN25 (PPG20-PPG23): Address 0507h (Access: Byte)
- GCN26 (PPG24-PPG27): Address 050Bh (Access: Byte)
- GCN27 (PPG28-PPG31): Address 050Fh (Access: Byte)

7.1.6 PTMR: PPG Timer Register

Reads the counts of PPGs.

- PTMR16 (PPG16): Address 0510h (Access: Half-word)
- PTMR17 (PPG17): Address 0518h (Access: Half-word)
- PTMR18 (PPG18): Address 0520h (Access: Half-word)
- PTMR19 (PPG19): Address 0528h (Access: Half-word)
- PTMR20 (PPG20): Address 0530h (Access: Half-word)
- PTMR21 (PPG21): Address 0538h (Access: Half-word)
- PTMR22 (PPG22): Address 0540h (Access: Half-word)
- PTMR23 (PPG23): Address 0548h (Access: Half-word)
- PTMR24 (PPG24): Address 0550h (Access: Half-word)
- PTMR25 (PPG25): Address 0558h (Access: Half-word)
- PTMR26 (PPG26): Address 0560h (Access: Half-word)
- PTMR27 (PPG27): Address 0568h (Access: Half-word)
- PTMR28 (PPG28): Address 0570h (Access: Half-word)
- PTMR29 (PPG29): Address 0578h (Access: Half-word)
- PTMR30 (PPG30): Address 0581h (Access: Half-word)
- PTMR31 (PPG31): Address 0588h (Access: Half-word)

8. A/D Converter / New Features (CY91F467PA)

CY91F467PA has two 10-bit A/D Converter macros. The original ADC, which is available on all CY91460 series devices, is now called “ADC 0”, the second macro is called “ADC 1”.

8.1 A/D Converter Features

- Both ADC 0 and ADC 1 are 10-bit / 1 µs macros used on other CY91460 series devices.
- Both ADCs have the new digital part with separated A/D Result registers and 4-channel Range Comparator, see chapter 9.“A/D Converter / Range Comparator (CY91F467PA)”.
- Both ADCs can be triggered from Reload Timer RLT7.
- Both ADCs can be triggered from the same external ATGX pin (GP16_7).
- On CY91F467PA, ADC0 and ADC1 share the same analog power and reference supply ($AV_{CC}5$,AVRH5,AV_{SS}).

8.2 Analog Input Connections

8.2.1 Global ADC Analog Channel Enable

The global ADC channel enable feature makes the ADC analog inputs independend of PFR/EPFR settings. It was introduced for 2 reasons:

- Some new ADC channels are assigned to ports whose PFR/EPFR combinations are already used completely for other resources.
- Customers may measure digital output signals with the ADC to check for external shortages. PFR/EPFR settings for ADC always switch the digital port to HiZ mode.

The global ADC channel enable is controlled by bit ADCHE in PORTEN register:

PORTEN Register Address: 0x0498 Access: Byte

7	6	5	4	3	2	1	0	Bit
-	-	-	-	-	**ADCHE**	CPORTEN	GPORTEN	
X	X	X	X	X	0	0	0	Initial value
RX, W0	RX, W0	RX, W0	RX, W0	RX, W0	R, W	R, W	R, W	Attribute

Bit7-3: Reserved bits. Always write 0 to these bits.

Bit2: ADCHE Global A/D Channel Enable.

ADCHE	Function
0 [initial]	Global A/D Channel Enable is OFF. The ADC analog lines of channels 0-31 are enabled by setting of the ADC enable bits (ADEn) in the ADERH,ADERL register and PFR/EPFR. PFR/EPFR will set the digital output to HiZ mode and disable the digital input lines of the port.
1	Global A/D Channel Enable is ON. The ADC analog lines of channels **6-7** are enabled by setting of the ADC enable bits (ADEn) in the ADERH,ADERL register only. ADEn will disable the digital input lines of the port, but the digital outputs are not changed. For analog measurement, the user has to switch the port to input direction.

This bit is cleared by software reset (RST) and can be written and read by CPU.

Note: For new ADC channels (AN32 to AN53, device depending), the ADCHE feature is always ON.
For old ADC channels (AN0 to AN31), the ADCHE feature is always OFF if the channels are re-located to other pins. On CY91F467PA, the ADCHE feature is only available on the non-relocated ADC channels 6-7 on ports P29[6,7].

Bit1:0: CPORTEN,GPORTEN Global Port Input Enable

CPORTEN	GPORTEN	Function
0 [initial]	0 [initial]	All port input lines are disabled.
1	0	The Port Input for LIN-USART 4 is enabled. This functionality is used by the Boot ROM to establish a serial communication with Softune for flash programming.
X	1	All port input lines are enabled.

- These bits are cleared by software reset (RST) and can be written and read by CPU.
- After execution of the Boot ROM the bits are in initial state.

8.2.2 ADC 0 Analog Inputs

ADC 0 serves the analog inputs AN0 to AN31. There are 2 methods for enabling the analog inputs:

- For all channels: Set ADC channel enable bits (ADEn) in the ADERH,ADERL register and set PFR/EPFR of the attached I/O port
- For channels 6-7: Set ADC channel enable bits (ADEn) in the ADERH,ADERL register and set global ADC channel enable, see 8.2.1“Global ADC Analog Channel Enable”.

Note : To use the channels AN0 to AN5 and AN8 to AN31, port multiplexing must be set. See chapter 5.“Port Multiplexing” and chapter 3.“Pin Description” for details. The ADC channel enable feature ADCHE is not available on the re-located channels.

8.2.3 ADC 1 Analog Inputs

ADC 1 serves the analog inputs AN37 to AN42, AN44 to AN46.

The analog inputs are enabled just by setting the ADC channel enable bits ADEn in the AD1ERH, AD1ERL registers. The Global ADC Analog Channel Enable feature is fixed ON here.

9. A/D Converter / Range Comparator (CY91F467PA)

The new A/D Converter with Range Comparator is available on CY91FV460B and CY91F467PA and is backward compatible to the A/D converter used on older devices.

This chapter provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

9.1 Overview of A/D Converter and A/D Range Comparator

The A/D converter converts analog input voltages into digital values and provides the following features. Any ADC channel can be assigned to one of 4 Range Comparators.

9.1.1 Features of the A/D converter:

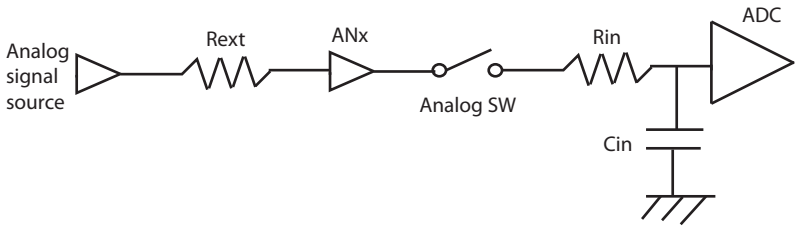
- Conversion time: minimum 1µs per channel.
- RC type successive approximation conversion with sample & hold circuit
- 10-bit or 8-bit resolution
- Program section analog input from 32 channels
- 1 common result data register and 32 dedicated channel result data registers
- Single conversion mode: Convert the specified channel(s) only once.
- Continuous mode: Repeatedly convert the specified channels.
- Scan conversion mode: Continuous conversion of multiple channels, programmable for up to 32 channels
- Stop mode: Convert one channel, then temporarily halt until the next activation. (Enables synchronization of the conversion start timing.)
- A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.
- A/D conversion of all enabled channels (scan conversion) can be followed by an A/D End of Scan interrupt request to CPU. The data is stored into dedicated channel result registers, which can be read out using DMA transfer.
- Conversion startup may be by software, external trigger (falling edge) or timer (rising edge).

9.1.2 Features of the A/D Range Comparator (RCO):

- 4 conversion result Range Comparator channels, comparing the upper 8 bit of the conversion result with an upper and a lower threshold. The thresholds are programmable for the 4 comparators independently.
- Any ADC channel can be assigned to one of the 4 range comparators.
- The comparison results will set “overflow” and “interrupt” flags per ADC channel, depending on the configuration. It is possible to configure the comparison for:
  - “out of range”: The flags are set if the A/D result is below the lower OR above the upper threshold.
  - “inside range”: The flags are set if the A/D result is above the lower AND below the upper threshold.
- The configuration can be set individually per ADC channel.
- Range comparison can be followed by an A/D Range Comparator interrupt request to CPU.

9.2 A/D Converter Input Impedance

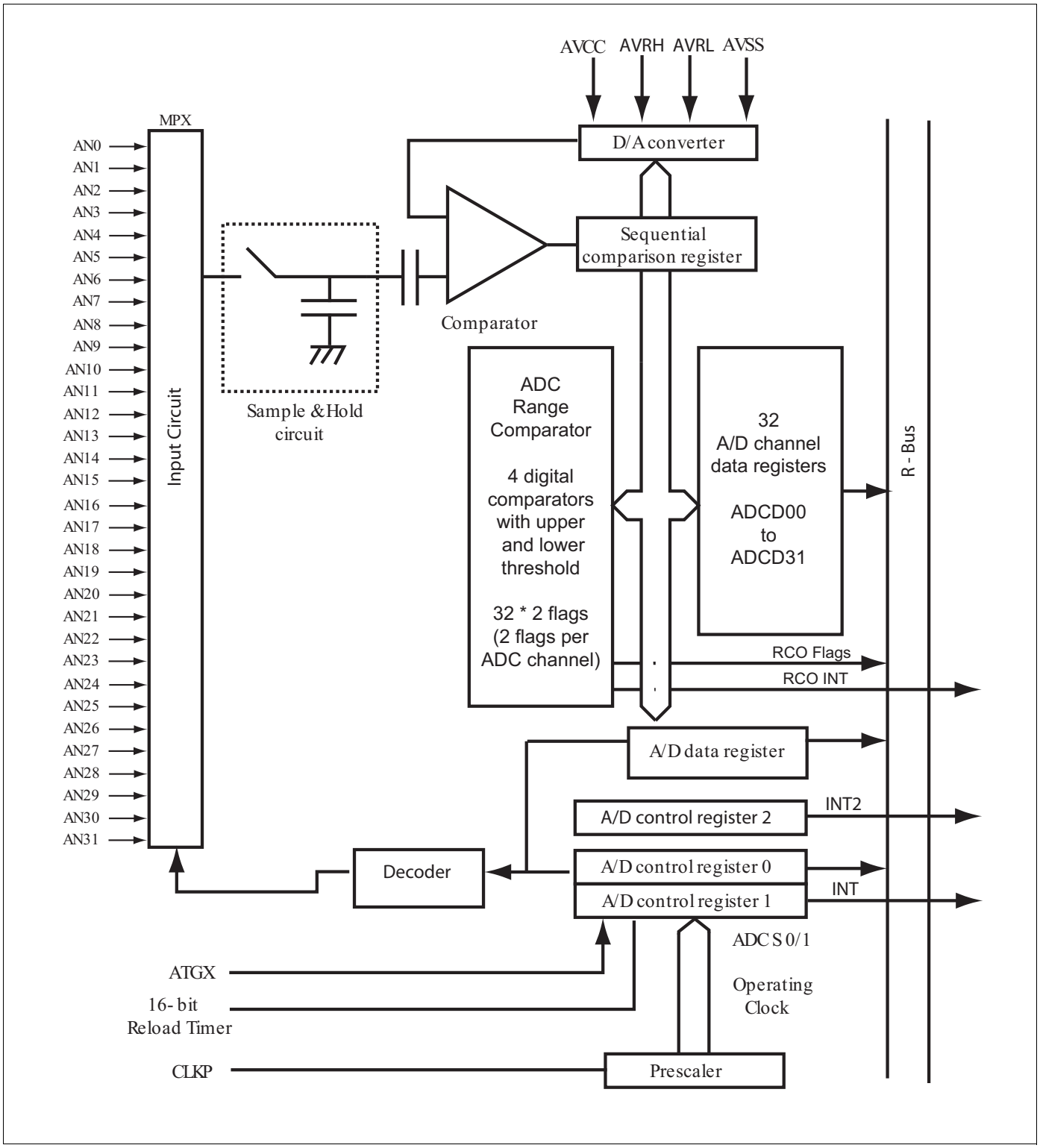
The following figure shows the sampling circuit of the A/D converter:



Do not set Rext over maximum sampling time (Tsamp).
Rext = Tsamp / (7*Cin) - Rin

9.3 Block Diagram of A/D Converter

The following figure shows block diagram of A/D converter.



9.4 Registers of the A/D Converter

The A/D converter with Range Comparator has the following registers:

Address (ADC 0)	Address (ADC 1)	x=0 or 1 for ADC0, ADC1 respectively				Register
		+0	+1	+2	+3	
$0001A0_H$	$0005E0_H$	ADxERH		ADxERL		A/D channel Enable register
$0001A4_H$	$0005E4_H$	ADxCS1	ADxCS0	ADxCR1	ADxCR0	A/D Control / Status register 0 + 1, A/D Conversion Result register
$0001A8_H$	$0005E8_H$	ADxCT1	ADxCT0	ADxSCH	ADxECH	Sampling timer setting register, Start Channel setting register, End Channel setting register
$0006B0_H$	$0006DC_H$	ADxCS2	-	-	-	A/D Control / Status register 2
000688_H	$0006B4_H$	RCOxH0	RCOxL0	RCOxH1	RCOxL1	Range Comparator 0,1 High/Low threshold registers
$00068C_H$	$0006B8_H$	RCOxH2	RCOxL2	RCOxH3	RCOxL3	Range Comparator 2,3 High/Low threshold registers
000690_H	$0006BC_H$	RCOxIRS				Range Comparator Inverted Range Select control
000694_H	$0006C0_H$	RCOxOF				Range Comparator Overflow flags
000698_H	$0006C4_H$	RCOxINT				Range Comparator Interrupt flags
$0006A0_H$	$0006CC_H$	ADxCC0	ADxCC1	ADxCC2	ADxCC3	Channel control for ch 0 to 7
$0006A4_H$	$0006D0_H$	ADxCC4	ADxCC5	ADxCC6	ADxCC7	Channel control for ch 8 to 16
$0006A8_H$	$0006D4_H$	ADxCC8	ADxCC9	ADxCC10	ADxCC11	Channel control for ch 16 to 23
$0006AC_H$	$0006D8_H$	ADxCC12	ADxCC13	ADxCC14	ADxCC15	Channel control for ch 24 to 31
$0006E0_H$	000720_H	ADCxD0		ADCxD1		ADC Channel Data register, channel 0,1
$0006E4_H$	000724_H	ADCxD2		ADCxD3		ADC Channel Data register, channel 2,3
$0006E8_H$	000728_H	ADCxD4		ADCxD5		ADC Channel Data register, channel 4,5
$0006EC_H$	$00072C_H$	ADCxD6		ADCxD7		ADC Channel Data register, channel 6,7
$0006F0_H$	000730_H	ADCxD8		ADCxD9		ADC Channel Data register, channel 8,9
$0006F4_H$	000734_H	ADCxD10		ADCxD11		ADC Channel Data register, channel 10,11
$0006F8_H$	000738_H	ADCxD12		ADCxD13		ADC Channel Data register, channel 12,13
$0006FC_H$	$00073C_H$	ADCxD14		ADCxD15		ADC Channel Data register, channel 14,15
000700_H	000740_H	ADCxD16		ADCxD17		ADC Channel Data register, channel 16,17
000704_H	000744_H	ADCxD18		ADCxD19		ADC Channel Data register, channel 18,19
000708_H	000748_H	ADCxD20		ADCxD21		ADC Channel Data register, channel 20,21
$00070C_H$	$00074C_H$	ADCxD22		ADCxD23		ADC Channel Data register, channel 22,23
000710_H	000750_H	ADCxD24		ADCxD25		ADC Channel Data register, channel 24,25
000714_H	000754_H	ADCxD26		ADCxD27		ADC Channel Data register, channel 26,27
000718_H	000758_H	ADCxD28		ADCxD29		ADC Channel Data register, channel 28,29
$00071C_H$	$00075C_H$	ADCxD30		ADCxD31		ADC Channel Data register, channel 30,31

9.4.1 A/D Input Enable Register (ADER)

This register enables the analog input functions of the A/D converter. On CY91F467PA, additionally the bit **ADCHE** in PORTEN register influences the enabling of analog input.

ADERH : Access: Word, Half-word, Byte

31	30	29	28	27	26	25	24	Bit
ADE31	**ADE30**	**ADE29**	**ADE28**	**ADE27**	**ADE26**	**ADE25**	**ADE24**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

23	22	21	20	19	18	17	16	Bit
ADE23	**ADE22**	**ADE21**	**ADE20**	**ADE19**	**ADE18**	**ADE17**	**ADE16**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

ADERL : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
ADE15	**ADE14**	**ADE13**	**ADE12**	**ADE11**	**ADE10**	**ADE9**	**ADE8**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

7	6	5	4	3	2	1	0	Bit
ADE7	**ADE6**	**ADE5**	**ADE4**	**ADE3**	**ADE2**	**ADE1**	**ADE0**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[ADE31-0]: A/D Input Enable

ADEn	PORTEN.ADCHE	Function
0 [initial]	X	Analog input of A/D channel n is disabled. The ADC will not sample/convert this channel.
1	0 [initial]	Analog input of the channel n is enabled. Additionally, the port function register (PFR,EPFR) of the corresponding port must be set . The PFR/EPFR will switch the port to input direction (output driver = HiZ) and disable the digital input lines.
	1	Analog input of the channel n is enabled. Setting the port function register(s) is not necessary. ADEn will disable the digital input lines of the ports, but it does not change the port's direction.

- Software reset (RST) clears ADEn and PORTEN.ADCHE to 0.
- Be sure to set start channel and end channel to cover all enabled channels.

9.4.2 A/D Control Status Registers (ADCS2, ADCS1, ADCS0)

The A/D control status registers control and show the status of A/D converter. Do not overwrite ADCS0 register during A/D converting.

ADCS2 : Access: Byte

15	14	13	12	11	10	9	8	Bit
BUSY	**INT**	**INTE**	**PAUS**	**-**	**-**	**INT2**	**INTE2**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R0	R0	R/W	R/W	Attribute

[bits 15:12] BUSY, INT, INTE, PAUS

These bits are a mirror of the corresponding bits in ADCS1, intended to quickly read out all status and interrupt information using only one register access. To write the bits, access them via ADCS1.

[bits 11:10] -

These bits do not exist. Read operation returns 0.

[bit 9] INT2 (End of Scan Flag)

The End of Scan flag is set when conversion data of the last channel is stored in ADCR, whereas the last channel is defined by ADECH register setting.

- If bit 8 (INTE2) is "1" when this bit is set, and the ADC runs in continuous conversion mode, an End of Scan interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a reset.
- If DMA is used, this bit is cleared at the end of DMA transfer.
- Read-modify-write operations read this bit as “1”.

[bit 8] INTE2 (Enable End of Scan Interrupt)

INTE2 enables the End of Scan interrupt in continuous conversion mode. In the other conversion modi, this bit has no effect. Additionally, setting INTE2 changes the protect function of converted data (see description of ADCS1.PAUS).

INTE2	Function
0 [initial]	Disable End of Scan interrupt, ADC result protection protects the ADCR register data.
1	Enable End of Scan interrupt, ADC result protection protects the ADCD0...ADCD31 register data (in continuous conversion mode only)

ADCS1 : Access: Half-word, Byte

15	14	13	12	11	10	9	8	Bit
BUSY	**INT**	**INTE**	**PAUS**	**STS1**	**STS0**	**STRT**	**reserved**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 15] BUSY (busy flag and stop)

BUSY	Function
Reading	A/D converter operation indication bit. Set on activation of A/D conversion and cleared on completion.
Writing	Writing "0" to this bit during A/D conversion forcibly terminates conversion. Use to forcibly terminate in continuous and stop modes.

- Read-modify-write instructions read the bit as "1".
- Cleared on the completion of A/D conversion in single conversion mode.
- In continuous and stop mode, the flag is not cleared until conversion is terminated by writing "0".
- Initialized to "0" by a software reset (RST).
- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

[bit 14] INT (End of Conversion Interrupt flag)

This bit is set when conversion data is stored in ADCR.

- If bit 5 (INTE) is "1" when this bit is set, an interrupt request is generated or, if activation of DMA is enabled, DMA is activated.
- Only clear this bit by writing "0" when A/D conversion is halted.
- Initialized to "0" by a software reset (RST).
- If DMA is used, this bit is cleared at the end of DMA transfer.

[bit 13] INTE (End of Conversion Interrupt enable)

This bit is enables or disables the conversion completion interrupt.

INTE	Function
0	Disable interrupt [Initial value]
1	Enable interrupt

- Cleared by a software reset (RST).

[bit 12] PAUS (A/D converter pause)

This bit is set when A/D conversion temporarily halts.

The A/D converter has one register to store the conversion result (ADCR) and additionally 32 ADC channel data registers. If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten.

To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time. A/D conversion resumes when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protect ADCR (the common result register)
Continuous	0	Protect ADCR (the common result register)
	1	Protect ADCD0...ADCD31 (the dedicated channel data registers)

- In continuous mode with INTE2==1, PAUS is set when data of the start channel (set by ADSCH) is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is active.
- In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active.
- PAUS is cleared by writing “0” or by a reset. (Not cleared at the end of DMA transfer.) However when waiting condition of DMA transfer, this bit cannot be cleared.
- Regarding protect function of converted data, see Section 9.6“Operation of A/D Converter”.

[bit 11, 10] STS1, STS0 (Start source select)

These bits select the A/D activation source.

STS1	STS0	Function
0	0	Software activation [Initial value]
0	1	External trigger pin activation and software activation
1	0	Timer activation and software activation
1	1	External trigger pin activation, timer activation and software activation

- These bits are initialized "00" by software reset (RST).
- In multiple-activation modes, the first activation to occur starts A/D conversion.
- The activation source changes immediately on writing to the register. Therefore care is required when switching activation mode during A/D operation.
- The A/D converter detects falling edges on the external trigger pin. When external trigger level is “L” and if these bits are changed to external trigger activation mode, A/D converting may starts.
- Selecting the timer selects the 16-bit reload timer 7.

[bit 9] STRT (Start)

Writing "1" to this bit starts A/D conversion (software activation).

- Write "1" again to restart conversion.
- Initialized to "0" by a software reset (RST).
- In continuous and stop mode, restarting is not occurred. Check BUSY bit before writing "1". (Activate conversion after clearing.)
- Do not specify forcible termination and software activation (BUSY="0" and STRT="1") at the same time.

[bit 8] reserved bit

Always write "0" to this bit.

ADCS0 : Access: Half-word, Byte

7	6	5	4	3	2	1	0	Bit
MD1	**MD0**	**S10**	**ACH4**	**ACH3**	**ACH2**	**ACH1**	**ACH0 / ACHMD**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R	R	R	R	R,**W**	Attribute

[bit 7, 6] MD1, MD0 (A/D converter mode set)

These bits the operation mode.

MD1	MD0	Operating mode
0	0	Single mode 1 (Reactivation during A/D conversion is allowed)
0	1	Single mode 2 (Reactivation during A/D conversion is not allowed)
1	0	Continuous mode (Reactivation during A/D conversion is not allowed)
1	1	Stop mode (Reactivation during A/D conversion is not allowed)

- Single mode: A/D conversion is continuous performed from the selected start channel (ADSCH) to the selected end channel (ADECH). The conversion stops once it has been done for all these channels.
- Continuous mode: A/D conversion is repeatedly performed from the selected start channel (ADSCH) to the selected end channel (ADECH) in a row.
- Stop mode: A/D conversion is performed from the selected start channel (ADSCH) to the selected end channel (ADECH), followed by a pause after each channel.
  The conversion is resumed upon activation.

When A/D conversion is started in continuous mode or stop mode, conversion operation continued until stopped by the BUSY bit.

Conversion is stopped by writing “0” to the BUSY bit.

On activation after forcibly stopping, conversion starts from the start channel, selected by ADSCH register.

Reactivation during A/D conversion is disabled for any of the timer, external trigger and software start sources in single mode 2, continuous and stop mode.

[bit 5] S10

This bit defines resolution of A/D conversion. If this bit set "0", the resolution is 10-bit. In the other case, resolution is 8-bit and the conversion result is stored to ADCR0 and in the lower 8 bits of the dedicated ADC result registers.

Initialized to "0" by a reset.

[bit 4 to 0] ACH4-0 (Analog convert select channel, read-only)

These bits show the number of the currently or previously converted analog channel, depending on bit ACHMD (see below).

ACH4	ACH3	ACH2	ACH1	ACH0	Converted channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
...					...
1	1	1	1	0	AN30
1	1	1	1	1	AN31

- Writing these bits has no effect (bit 0 is writable with special function ADCHMD).
- Initialized to "0000" by software reset (RST).

[bit 0] ACHMD (ACH register mode, write-only)

For reading out the ACH4-0 register bits (see below), there is a *direct* mode and a *latched* mode.

In direct mode, ACH4-0 shows the number of the ADC channel which is *currently in conversion*, e.g. the internal conversion channel pointer. This pointer is incremented immediately after a conversion is finished.

In latched mode, ACH4-0 shows the number of the ADC channel whose conversion was *finished previously.* After a conversion is finished, the conversion channel pointer is latched and the latched data can be read in this mode. At the end of the next conversion, the latch is overwritten if no PAUSE condition exists.

ACHMD	Function
0	Direct ACH register mode [Initial value]
1	Latched ACH register mode

- ACHMD is a write-only bit.
- Read- or read-modify-write access returns the value of bit ACH0, see below.
- Initial value is 0.

9.4.3 Common Data Register (ADCR1, ADCR0)

These registers store the conversion results of the A/D converter. ADCR0 stores lower 8-bit. ADCR1 stores upper 2-bit. The register values are updated at the completion of each conversion. The registers normally store the results of the previous conversion.

ADCR1 : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	**D9**	**D8**	
0	0	0	0	0	0	X	X	Initial value
R0, W0	R0, W0	R0, W0	R0, W0	R0, W0	R0, W0	R	R	Attribute

ADCR0 : Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

- Bit 15 to 10 of ADCR1 are read as "0".
- The A/D converter has a conversion data protection function. See the "Operation" section for further information.

9.4.4 Dedicated A/D Channel Data Register (ADCD0 to ADCD31)

There are 32 ADC result data registers, one per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCD0 is attached to channel 0, ADCD31 is attached to channel 31.

ADCD0 ... ADCD31 : Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	-	-	-	**D9**	**D8**	
0	0	0	0	0	0	X	X	Initial value
R0	R0	R0	R0	R0	R0	R	R	Attribute
7	6	5	4	3	2	1	0	Bit
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
X	X	X	X	X	X	X	X	Initial value
R	R	R	R	R	R	R	R	Attribute

- Bit 15 to 10 of the ADCD registers are read as "0".
- The A/D converter has a conversion data protection function. In continuous conversion mode, the protection function can be changed to protect the A/D Channel Data registers rather then the A/D Data Register (ADCR1).
  See section 9.6.6“Protection of the ADC Channel Data Registers” for further information.

9.4.5 Sampling Timer Setting Register (ADCT)

ADCT register controls the sampling time and comparison time of analog input. This register sets A/D conversion time. Do not update value of this register during A/D conversion operation.

ADCT1: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
CT5	**CT4**	**CT3**	**CT2**	**CT1**	**CT0**	**ST9**	**ST8**	
0	0	0	1	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

ADCT0: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
ST7	**ST6**	**ST5**	**ST4**	**ST3**	**ST2**	**ST1**	**ST0**	
0	0	1	0	1	1	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 15 to 10] CT5-0 (A/D comparison time set)

These bits specify clock division of comparison time.

- Setting "000001" means one division (=CLKP).
- Do not set these bits "000000".
- Initialized these bits to "000100" by software reset (RST).
- Comparison time = CT value * CLKP cycle * 10 + (4 * CLKP)
- Do not set comparison time over 500 µs.

[bit 9 to 0] ST9-0 (Analog input sampling time set)

These bits specify sampling time of analog input.

- Initialized these bits to "0000101100" by software reset (RST).
- Sampling time = ST value * CLKP cycle
- Do not set sampling time below 1.2 µs when AVCC is below 4.5 V.

Necessary sampling time and ST value are calculated by following.

- Necessary sampling time (Tsamp) = (Rext + Rin) * Cin * 7
- ST9 to ST0 = Tsamp / CLKP cycle

ST has to be set that sampling time is over Tsamp.
Example: CLKP = 32MHz, AVCC >= 4.5V, Rext = 200KΩ

Tsamp = ($200 * 10^3 + 2.52 * 10^3$) * 10.7 * 10^{-12} * 7 = 15.17 [µs]
ST = $15.17^{-6} / 31.25^{-9}$ = 485.44
ST has to be set over 486_D (111100110_B).

Tsamp is decided by Rext. Thus conversion time should be considered together with Rext.

9.4.6 A/D Channel Setting Register (ADSCH, ADECH)

These registers specify the channels for the A/D converter to convert. Do not update these registers while the A/D converting is operating.

ADSCH: Access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
-	-	-	ANS4	ANS3	ANS2	ANS1	ANS0	
-	-	-	0	0	0	0	0	Initial value
RX, W0	RX, W0	RX, W0	R/W	R/W	R/W	R/W	R/W	Attribute

ADECH : Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
-	-	-	ANE4	ANE3	ANE2	ANE1	ANE0	
-	-	-	0	0	0	0	0	Initial value
RX, W0	RX, W0	RX, W0	R/W	R/W	R/W	R/W	R/W	Attribute

These bits set the start and end channel for A/D converter.

- Setting of ANE4 to ANE0 the same channel as in ANS4 to ANS0 specifies conversion for that channel only. (Single conversion)
- In continuous or stop mode, conversion is performed up to the channel specified by ANE4 to ANE0. Conversion then starts again from the start channel specified by ANS4 to ANS0.
- If ANS > ANE, conversion starts with the channel specified by ANS, continuous up to channel 31, starts again from channel 0, and ends with the channel specified by ANE.
- Initialized to ANS="00000", ANE="00000" by a software reset (RST).

Example: Channel Setting ANS=30ch, ANE=3ch, single conversion mode

Operation : Conversion channel 30ch -> 31ch -> 0ch -> 1ch -> 2ch -> 3ch end

[bit 12 to 8] ANS4-0 (Analog start channel set)

[bit 4 to 0] ANE4-0 (Analog end channel set)

ANS4 ANE4	ANS3 ANE3	ANS2 ANE2	ANS1 ANE1	ANS0 ANE0	Start / End Channel
0	0	0	0	0	AN0
0	0	0	0	1	AN1
0	0	0	1	0	AN2
0	0	0	1	1	AN3
...					...
1	1	1	0	1	AN29
1	1	1	1	0	AN30
1	1	1	1	1	AN31

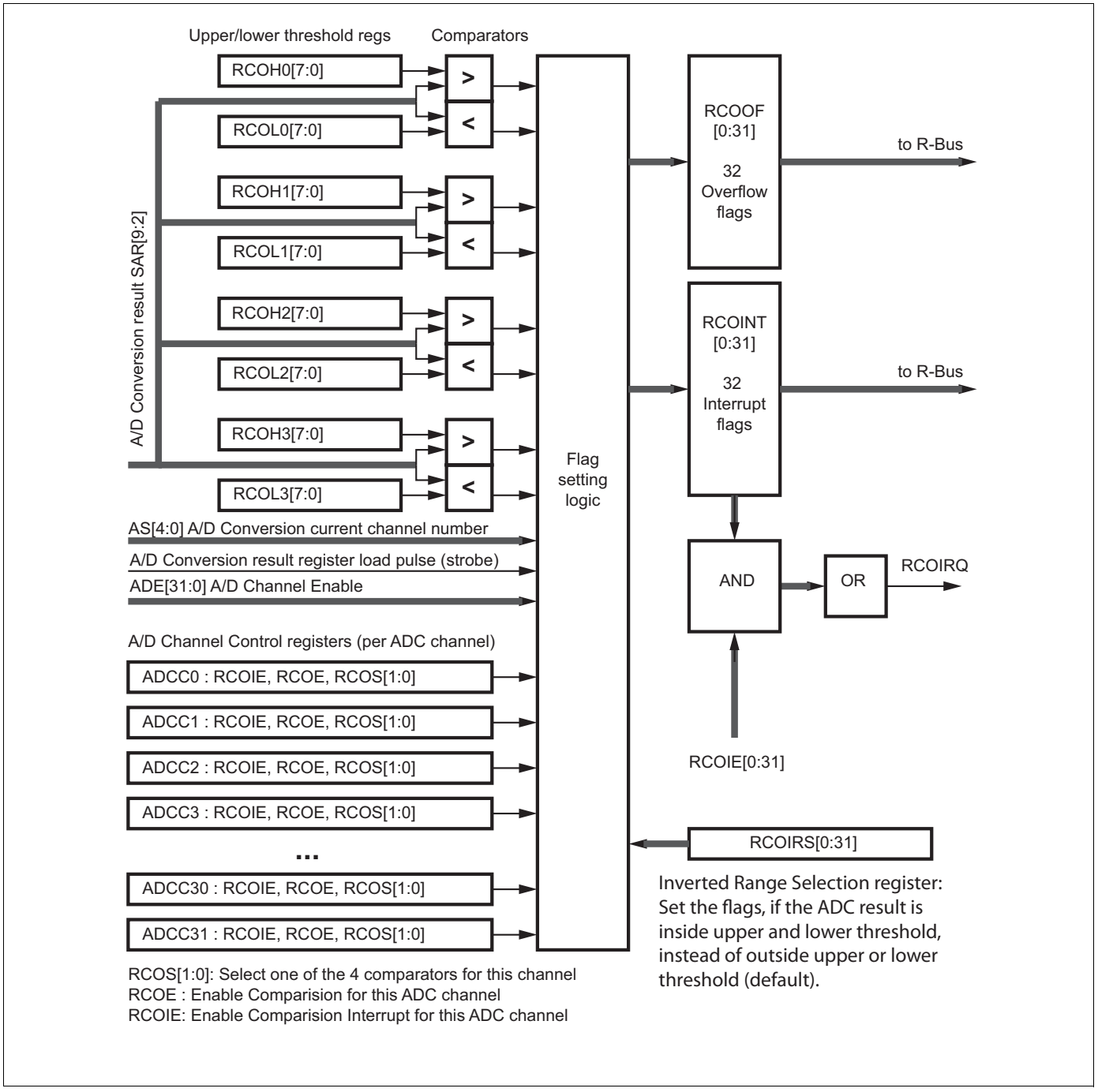
9.5 Range Comparator

9.5.1 Range Comparator Structure

The Range Comparator has 4 comparison groups with an upper and a lower threshold register each. The 32 ADC channels can be enabled for range comparison and assigned to one of the 4 comparators individually. If enabled, the comparison will set up to 2 flags for this ADC channel:

- An interrupt flag RCOINT, signalling that the ADC result is outside the range or, by “inverted” configuration, inside the range.
- An overflow flag RCOOF, showing that the range violation was an overflow and no underflow.

Furthermore, each ADC channel can be enabled to send an interrupt request to the CPU, if the RCOINT flag is set.



9.5.2 Range Comparator Registers

The Range Comparator (RCO) has the following registers:

- RCOHx[7:0] : Upper threshold register, one register per comparator block (x = 0...3)
- RCOLx[7:0] : Lower threshold register, one register per comparator block (x = 0...3)
- ADCCm[7:0] : ADC channel control, one register per 2 ADC channels (m = 0...15)
- RCOIRS[0:31] : RCO Inverted Range Selection, one bit per ADC channel
- RCOOF[0:31] : RCO Overflow Flags, one bit per ADC channel, read-only
- RCOINT[0:31] : RCO Interrupt Flags, one bit per ADC channel

Range Comparator Threshold registers (RCOH0/L0 to RCOH3/L3)

RCOH0-3 : Higher threshold, access: Word, Half-word, Byte

15	14	13	12	11	10	9	8	Bit
RCOH7	**RCOH6**	**RCOH5**	**RCOH4**	**RCOH3**	**RCOH2**	**RCOH1**	**RCOH0**	
1	1	1	1	1	1	1	1	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 7:0] RCOH[7:0] (Range Comparator High threshold)

The RCOH bits define the higher comparison threshold of the Range Comparator channel.

The upper Range Comparator compares that the upper 8 bits of the ADC conversion result are higher then RCOH[7:0] .

RCOL0-3 : Lower threshold, access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
RCOL7	**RCOL6**	**RCOL5**	**RCOL4**	**RCOL3**	**RCOL2**	**RCOL1**	**RCOL0**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

[bit 7:0] RCOL[7:0] (Range Comparator Low threshold)

The RCOL bits define the lower comparison threshold of the Range Comparator channel.

The lower Range Comparator compares that the upper 8 bits of the ADC conversion result are lower then RCOL[7:0] .

A/D Converter Channel Control registers (ADCC0 to ADCC15)

The A/D channel control registers serve 2 ADC channels per register and control the range comparison for these channels.

ADCC0 register controls A/D channels 0 + 1,
ADCC1 register controls A/D channels 2 + 3,
...
ADCC15 register controls A/D channels 30 + 31

ADCC0-15: Access: Word, Half-word, Byte

7	6	5	4	3	2	1	0	Bit
RCOIE1	**RCOE1**	**RCOS11**	**RCOS10**	**RCOIE0**	**RCOE0**	**RCOS01**	**RCOS00**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
Bits 7:4 control A/D channels 1,3,5,7,...31				Bits 3:0 control A/D channels 0,2,4,6,...,30				

[bit 7,3] RCOIE1, RCOIE0 (Range Comparator Interrupt enable)

The RCOIE bits enable the Range Comparator interrupt for the corresponding ADC channel.

RCOIE	Function
0	RCO interrupt for this ADC channel is disabled [default]
1	RCO interrupt for this ADC channel is enabled

[bit 6,2] RCOE1, RCOE0 (Range Comparator operation enable)

The RCOE bits enable the Range Comparison for the corresponding ADC channel:

RCOE	Function
0	RCO disabled, RCO flags for this ADC channel will not be set [default]
1	RCO enabled for this ADC channel

[bits 5:4,1:0] RCOS1[1:0], RCOS0[1:0] (converter channel select)

These bits select the A/D converter channel to be assigned to the Range Comparator channel:

RCOS[1:0]	Function
00	Select range comparator channel 0 for this ADC channel [default]
01	Select range comparator channel 1 for this ADC channel
10	Select range comparator channel 2 for this ADC channel
11	Select range comparator channel 3 for this ADC channel

Inverted Range Selection register

The RCOIRS register controls that the comparison should check for “out of range” or “inside range”.
The 32 bits of RCOIRS is organized “per ADC channel”. ADC channel 0 is located on the MSB of the register and ADC channel 31 is on the LSB.

RCOnIRS : Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOIRS0	**RCOIRS1**	**RCOIRS2**	**RCOIRS3**	**RCOIRS4**	**RCOIRS5**	**RCOIRS6**	**RCOIRS7**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
23	22	21	20	19	18	17	16	Bit
RCOIRS8	**RCOIRS9**	**RCOIRS10**	**RCOIRS11**	**RCOIRS12**	**RCOIRS13**	**RCOIRS14**	**RCOIRS15**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
15	14	13	12	11	10	9	8	Bit
RCOIRS16	**RCOIRS17**	**RCOIRS18**	**RCOIRS19**	**RCOIRS20**	**RCOIRS21**	**RCOIRS22**	**RCOIRS23**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute
7	6	5	4	3	2	1	0	Bit
RCOIRS24	**RCOIRS25**	**RCOIRS26**	**RCOIRS27**	**RCOIRS28**	**RCOIRS29**	**RCOIRS30**	**RCOIRS31**	
0	0	0	0	0	0	0	0	Initial value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOIRS[0:31] (Inverted Range Select)

The RCOIRS bits control how the Range Comparator result flags are set.

- If the RCOIRS[n] is 0, the flags are set when the ADC result is above the upper threshold OR below the lower threshold. That is called “**out of range**” mode.
- If the RCOIRS[n] is 1, the flags are set when the ADC result is below or equal the upper threshold AND above or equal the lower threshold. That is called “**inside range**” mode.

RCOIRSn	Function
0	Range comparison for this ADC channel checks for “out of range” (default)
1	Range comparison for this ADC channel checks for “inside range”

Range Comparator Result Flags

The result of range comparison is stored in 2 flag registers:

- RCOINT[0:31]:Range comparison interrupt flags
- RCOOF[0:31]: Range comparison overflow flags

The Range Comparator Result flags are organized “per ADC channel”. There are 32 Range Comparator overflow flags and 32 interrupt flags. In case of a RCO interrupt, all interrupt flags can be read out by one 32-bit read operation and analyzed using the Bit Search Unit. The Bit Search Unit will return the number of the interrupting channel. Since bit search works from MSB to LSB (from left to right), ADC channel 0 is located on the MSB of the registers and ADC channel 31 is on LSB.

RCOnINT : Access: Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOINT0	**RCOINT1**	**RCOINT2**	**RCOINT3**	**RCOINT4**	**RCOINT5**	**RCOINT6**	**RCOINT7**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
23	22	21	20	19	18	17	16	Bit
RCOINT8	**RCOINT9**	**RCOINT10**	**RCOINT11**	**RCOINT12**	**RCOINT13**	**RCOINT14**	**RCOINT15**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
15	14	13	12	11	10	9	8	Bit
RCOINT16	**RCOINT17**	**RCOINT18**	**RCOINT19**	**RCOINT20**	**RCOINT21**	**RCOINT22**	**RCOINT23**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute
7	6	5	4	3	2	1	0	Bit
RCOINT24	**RCOINT25**	**RCOINT26**	**RCOINT27**	**RCOINT28**	**RCOINT29**	**RCOINT30**	**RCOINT31**	
0	0	0	0	0	0	0	0	Initial value
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOINT[0:31] (Range Comparator Interrupt flags)

The RCOINT flags show that a “out of range” or “inside range” condition has been found on the ADC channel.

The bits are set under the following condition:

- the ADC channel is enabled — ADER.ADE[i] is set — and
- the range comparison for this channel is enabled — ADCCn.RCOE[i] is set — and
- the conversion of the ADC channel is just finished — and
- an interrupt condition was found (see the table on next page).

- The bits are cleared by writing 0 or by software reset (RST). Writing 1 has no effect.
- Read-modify-write operations read 1.

The interrupt condition depends on the comparison results and the RCOIRS setting for this channel:

Mode	RCOIRS	Upper threshold comparator	Lower threshold comparator	Interrupt condition
out of range	0	1	x	INT condition: above range, RCOOF is set
		0	0	-
		x	1	INT condition: below range, RCOOF is cleared
inside range	1	1	x	-
		0	0	INT condition: inside range
		x	1	-

Note: The upper threshold comparator returns 1 if the upper 8 bits of the ADC result are greater then the threshold value in RCOH[7:0]. The lower threshold comparator returns 1 if the upper 8 bits of the ADC result are smaller then the threshold value in RCOL[7:0].

RCOnOF : Access: Read-only, Word, Half-word, Byte

31	30	29	28	27	26	259	24	Bit
RCOOF0	**RCOOF1**	**RCOOF2**	**RCOOF3**	**RCOOF4**	**RCOOF5**	**RCOOF6**	**RCOOF7**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
23	22	21	20	19	18	17	16	Bit
RCOOF8	**RCOOF9**	**RCOOF10**	**RCOOF11**	**RCOOF12**	**RCOOF13**	**RCOOF14**	**RCOOF15**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
15	14	13	12	11	10	9	8	Bit
RCOOF16	**RCOOF17**	**RCOOF18**	**RCOOF19**	**RCOOF20**	**RCOOF21**	**RCOOF22**	**RCOOF23**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute
7	6	5	4	3	2	1	0	Bit
RCOOF24	**RCOOF25**	**RCOOF26**	**RCOOF27**	**RCOOF28**	**RCOOF29**	**RCOOF30**	**RCOOF31**	
0	0	0	0	0	0	0	0	Initial value
R	R	R	R	R	R	R	R	Attribute

Note that bit[31] is assigned to ADC channel 0, bit[30] is assigned to ADC channel one and so on.

[bits 31:0] RCOOF[0:31] (Range Comparator Overflow flag)

The RCOOF read-only flags store the output signal of the upper threshold comparator at the time when an interrupt condition (see above) appeared and the corresponding RCOINT flag was **not** set. So the RCOOF flags indicate the upper comparator state when the RCOINT flag had the last rising edge.

The RCOOF flag for a ADC channel is loaded with the upper threshold comparator output signal under the following condition:

- the corresponding RCOINT flag is not yet setand
- the corresponding RCOINT flag has a set condition in this cycle.

The flags are initialized by software reset (RST).

RCOOFn	Function
0	The output of the upper threshold comparator was 0 [default]
1	The output of the upper threshold comparator was 1

9.5.3 Range Comparator Interrupt request

The Range Comparator has one interrupt output line RCOIRQ. The interrupt output line becomes active if at least one of the Range Comparator interrupt flags RCOINT[31:0] is set and the corresponding interrupt enable bit in the ADCC registers is set.

It is not possible to activate a DMA request from the range comparator interrupts.

9.6 Operation of A/D Converter

The A/D converter operates using the successive approximation method with 10-bit or 8-bit resolution. There is one 16-bit register provided to store conversion results (ADCR), which is updated each time conversion completes. Additionally, there is one ADC Channel Data register per channel (ADCD0...31), which is updated each time the assigned channel is converted. The Channel Data registers especially improve the continuous conversion mode.
It is recommended to use the DMA service. The following describes the operation modes.

9.6.1 Single Mode

In single conversion mode, the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits. A/D conversion then ends. If the start channel and end channel are the same (ANS=ANE), only a single channel conversion is performed.

Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> AN1 -> AN2 -> AN3 -> End
- ANS=00010b, ANE=00010b
  Start -> AN2 -> End

9.6.2 Continuous Mode

In continuous mode the analog input signals selected by the ANS bits and ANE bits are converted in order until the completion of conversion on the end channel determined by the ANE bits, then the converter returns to the ANS channel for analog input and repeats the process continuously. When the start and end channels are the same (ANS=ANE), conversion is performed continuously for that channel.

Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> AN1 -> AN2 -> AN3 -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b
  Start -> AN2 -> AN2 -> AN2 ... -> repeat

In continuous mode, conversion is repeated until '0' is written to the BUSY bit. (Writing '0' to the BUSY bit forcibly stops the conversion operation.) Note that forcibly terminating operation halts the current conversion during mid-conversion. (If operation is forcibly terminated, the value in the conversion register is the result of the most recently completed conversion.)

9.6.3 Stop Mode

In stop mode the analog input signal selected by the ANS bits and ANE bits are converted in order, but conversion operation pauses after each channel. The pause is released by applying another start signal.

At the completion of conversion on the end channel determined by the ANE bits, the converter returns to the ANS channel for analog input signal and repeats the conversion process continuously. When the start and end channel are the same (ANS=ANE), only a signal channel conversion is performed.

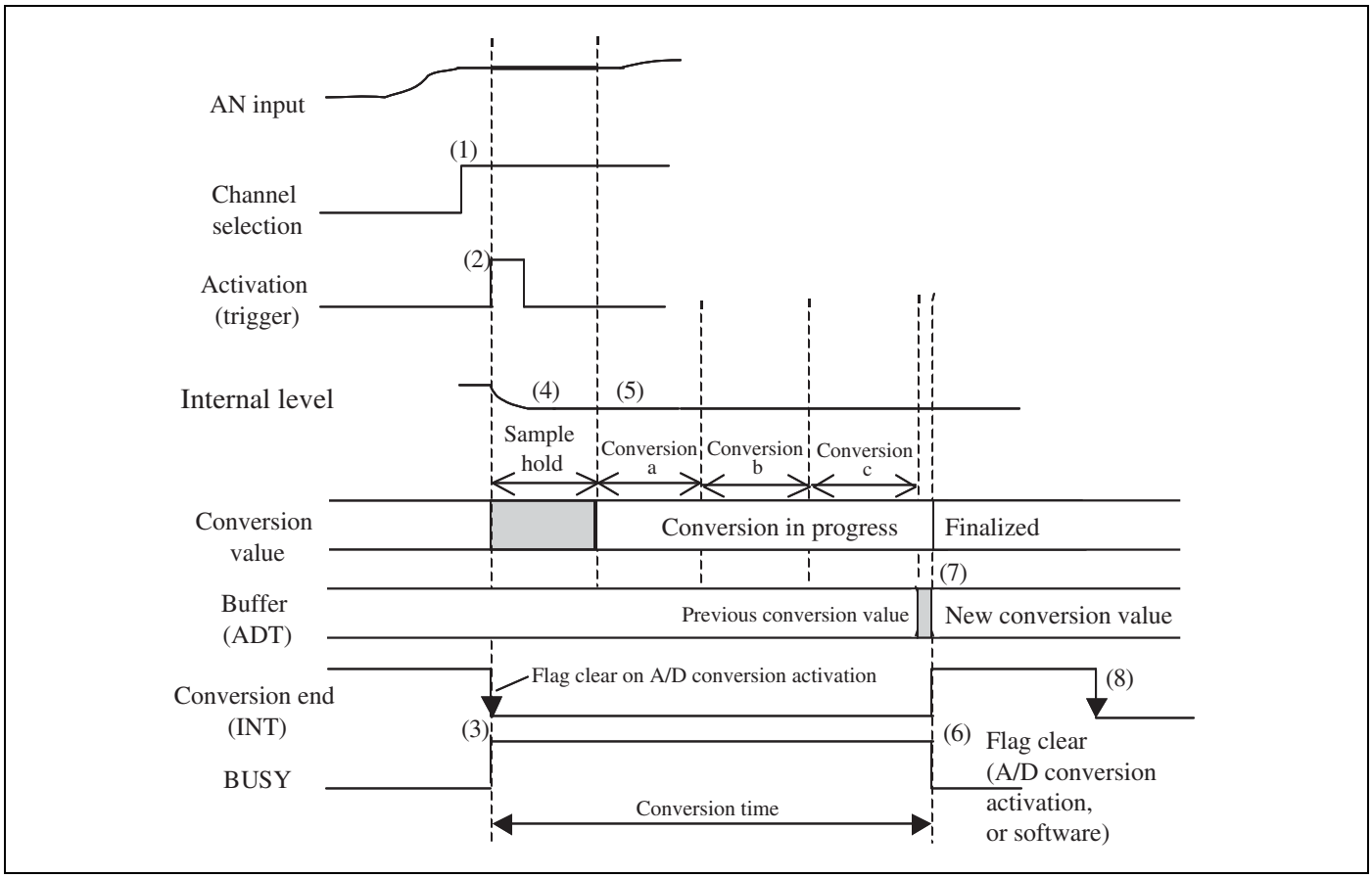
Examples:

- ANS=00000b, ANE=00011b
  Start -> AN0 -> stop -> start -> AN1 -> stop -> start -> AN2 -> stop -> start -> AN3 -> stop -> start -> AN0 ... -> repeat
- ANS=00010b, ANE=00010b
  Start -> AN2 -> stop -> start -> AN2 -> stop -> start -> AN2 ... -> repeat

In stop mode the startup source is the source determined by the STS1, STS0 bits. This mode enables synchronization of the conversion start signal.

9.6.4 Single-shot Conversion

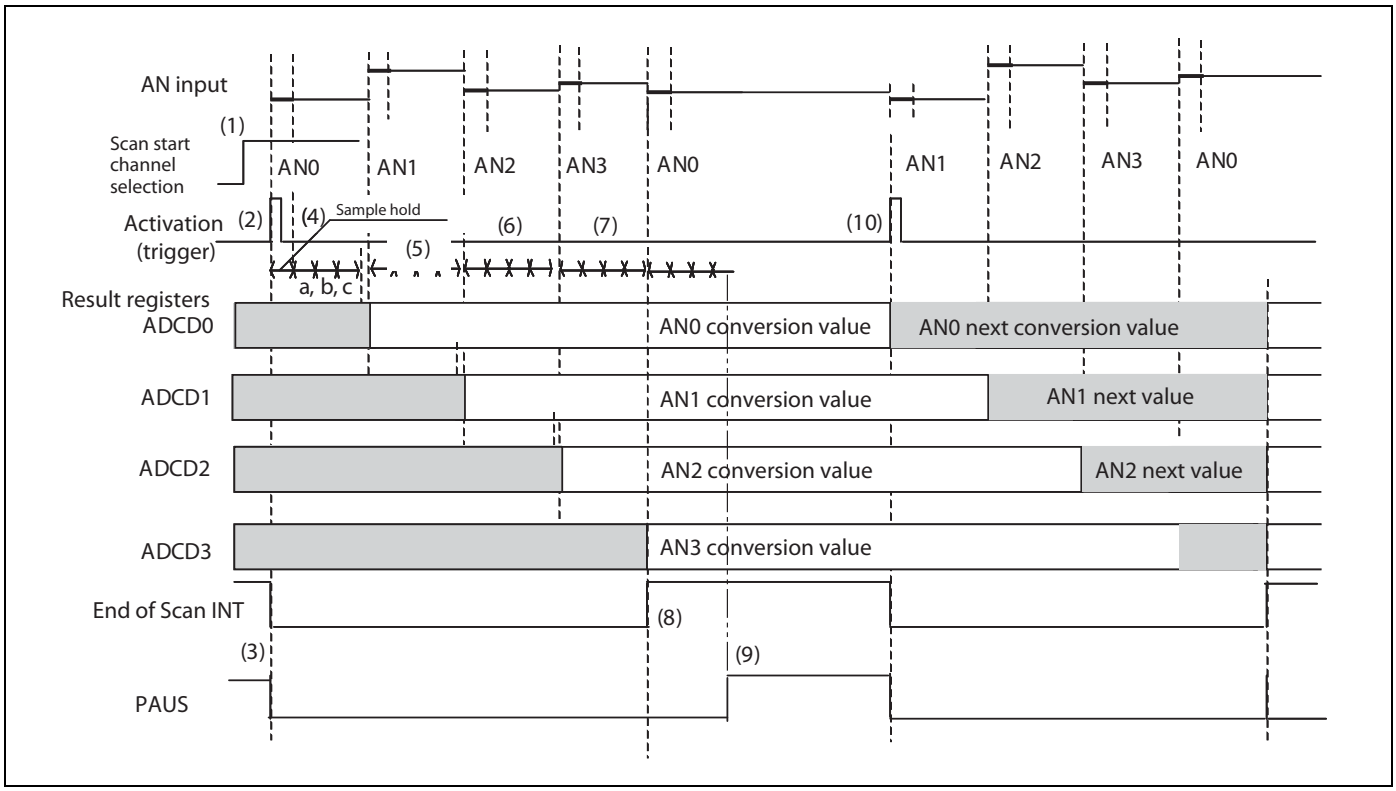
The following figure shows the operation of A/D converter in Single-shot conversion mode



(1) Channel selection
(2) A/D conversion activation (Trigger input: Software trigger/Reload timer/External trigger)
(3) INT flag clear, BUSY flag set
(4) Sample hold
(5) Conversion (Conversion a + Conversion b + Conversion c)
(6) Conversion end, INT flag set, BUSY flag clear
(7) Buffers the conversion value. Buffered data storage
(8) Software-based INT flag clear

9.6.5 Scan Conversion

The following figure shows the operation of A/D converter in Scan conversion mode



(1) Activation channel selection

(2) A/D activation (Trigger: Software trigger/Reload timer/External trigger)

(3) INT flag clear, PAUS flag clear

(4) AN0 conversion
a. Sample hold, conversion (conversion a + conversion b + conversion c)
b. Conversion end
c. Buffers the conversion value.

(5) AN1 conversion

(6) AN2 conversion

(7) AN3 conversion

(8) INT2 (End of Scan) flag is set, AN0 conversion starts

(9) Because INT2 has not been cleared yet, the ADC protects the result register of AN0 against overwriting and enters PAUSE state.

(10) INT2 flag cleared by DMA or by software, the ADC stores the result of AN0 and continues sampling AN1.

9.6.6 Protection of the ADC Channel Data Registers

There are 32 ADC result data registers, one register per channel. The registers are written by hardware at the end of conversion of the attached channel. ADCD0 is attached to channel 0, ADCD31 is attached to channel 31.

The CPU can read the data registers any time.

If a conversion is finished and the data of the previous conversion has not been read out before, previous data would be overwritten. To avoid this problem, the next conversion data is not stored in the data registers until the previous value has been read out (e.g. by DMA). A/D conversion halts during this time and the PAUS flag is set. A/D conversion restarts when the ADC interrupt flag ADCR1.INT is cleared.

The register protection function depends on the conversion mode and the setting of ADCR2.INTE2:

Mode	INTE2	Function
Single, Stop	X	Protection of ADCR
Continuous	0	Protection of ADCR
	1	Protection of ADCD0...ADCD31

Protection of ADCD0...31

In continuous mode with INTE2==1, PAUS is set when data of the **start channel (set by ADSCH)** is ready for writing to the registers, but IRQ2 (End of Scan interrupt) is already active.

Example: Start channel =4, end channel=7, continous mode, ADCS1.INTE=0, ADCS2.INTE2=1

Start by CPU --> convert channel 4 + safe data to ADCD4,
convert channel 5 + safe data to ADCD5,
convert channel 6 + safe data to ADCD6,
convert channel 7 + safe data to ADCD7 ---> End of Scan interrupt (IRQ2),
convert channel 4 + set PAUS (protect ADCD4...7).

After the CPU or DMA have read the data registers and cleared IRQ2, the scan conversion continues.

Protection of ADCR

In the other modes or if INTE2==0, PAUS is set when data of any channel is ready for writing to the registers, but IRQ (End of Conversion) is active. Because in this mode the protection function is active after each single conversion, the ADCR register is protected.

9.7 ADC Interrupt Generation and DMA Access

There are 2 ADC interrupt sources: End of Conversion and End of Scan.

9.7.1 End of Conversion

The End of Conversion (EoC) interrupt is enabled by ADCS1.INTE bit and is compatible to the A/D converts in old devices of CY91460 series. If EoC is enabled, it appears after any conversion cycle. It is recommended to use DMA transfer to read out the data from ADCR.

9.7.2 End of Scan

The End of Scan (EoS) interrupt is enabled by ADCS2.INTE2 bit. If EoS is enabled, it appeares after the conversion of the end channel, which is defined by the setting of ADECH register.

If the End of Conversion interrupt is enabled in parallel, both interrupt bits are set. In this case it is recommended that the interrupt routine reads out ADCS2 register (containing mirrored bits of ADCS1[7:4]) to check where the interrupt comes from.

9.7.3 DMA Transfer

DMA transfer can be triggered by End of Conversion interrupt or by End of Scan interrupt. The interrupts are assigned to separate DMA resource numbers (please refer to the Interrupt Vector Table).

The automatic interrupt clear after DMA transfer works for End of Conversion and for End of Scan separately.

10. Handling Devices

10.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

10.2 Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

10.3 Power supply pins

In CY91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the CY91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

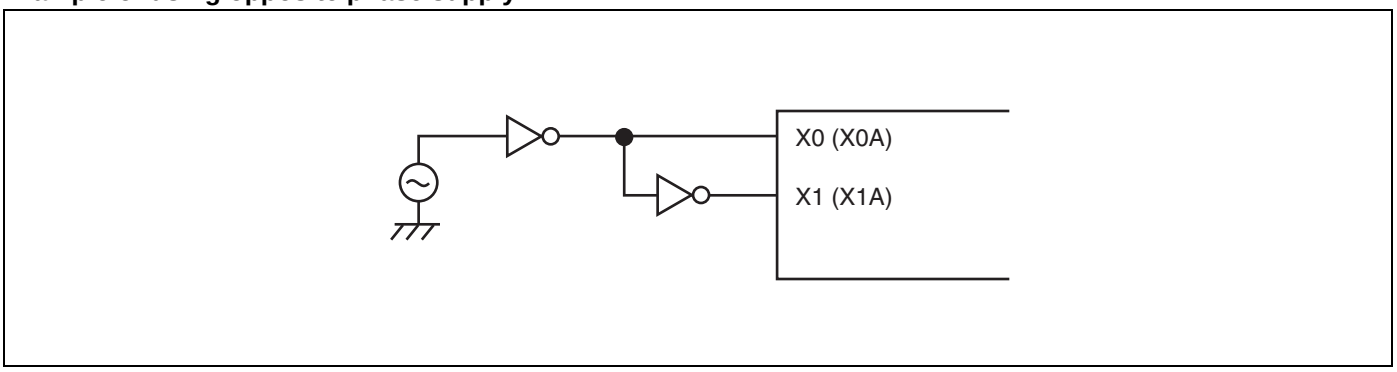
10.4 Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

10.5 Notes on using external clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of using opposite phase supply



10.6 Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

10.7 Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

10.8 Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

11. Notes on Debugger

11.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

11.2 Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

11.3 Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

11.4 Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

(a) a user interrupt or NMI is accepted;

(b) single-step execution is performed;

(c) execution breaks due to a data event or from the emulator menu.

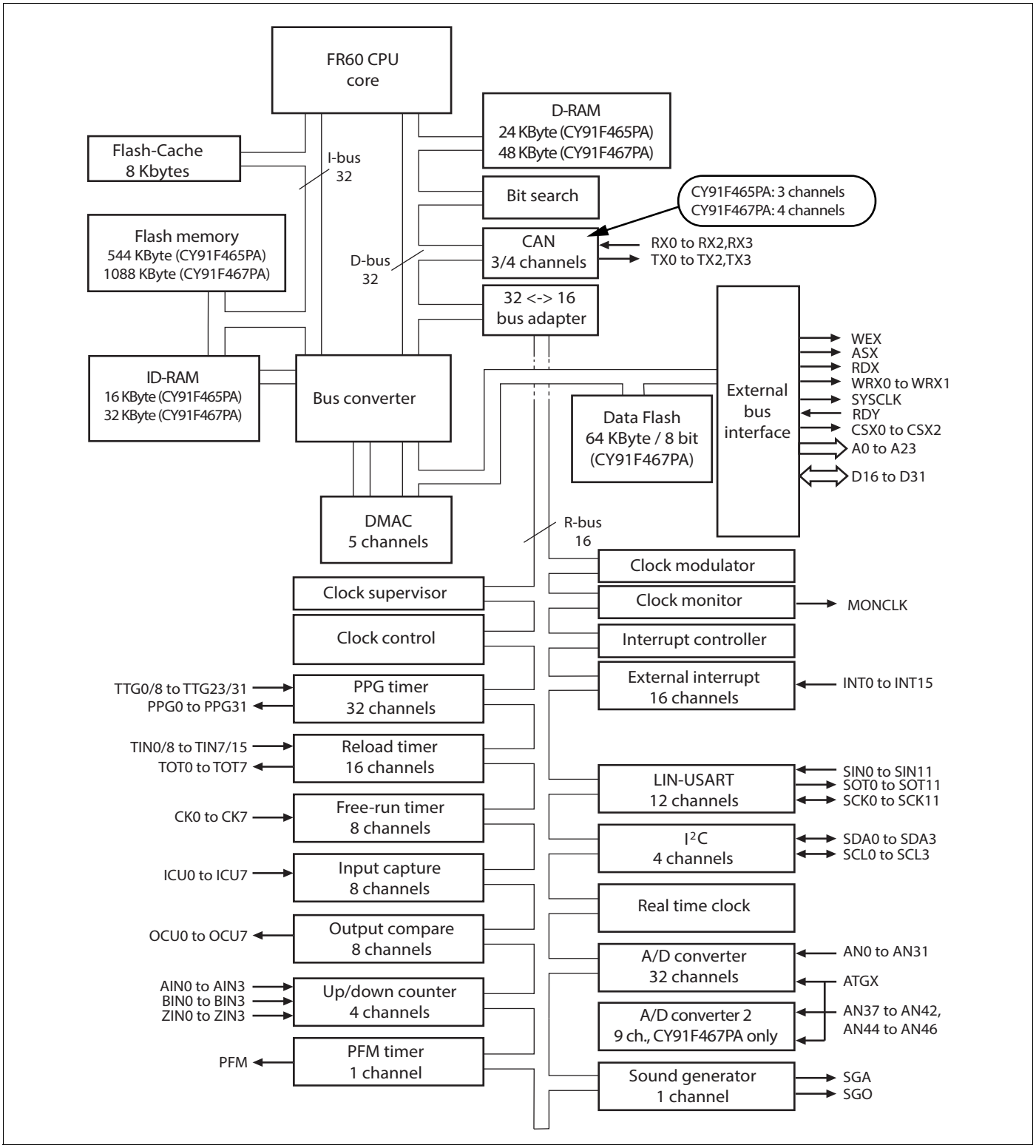
1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

12. Block Diagram

12.1 CY91F465PA, CY91F467PA



13. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

13.1 Features

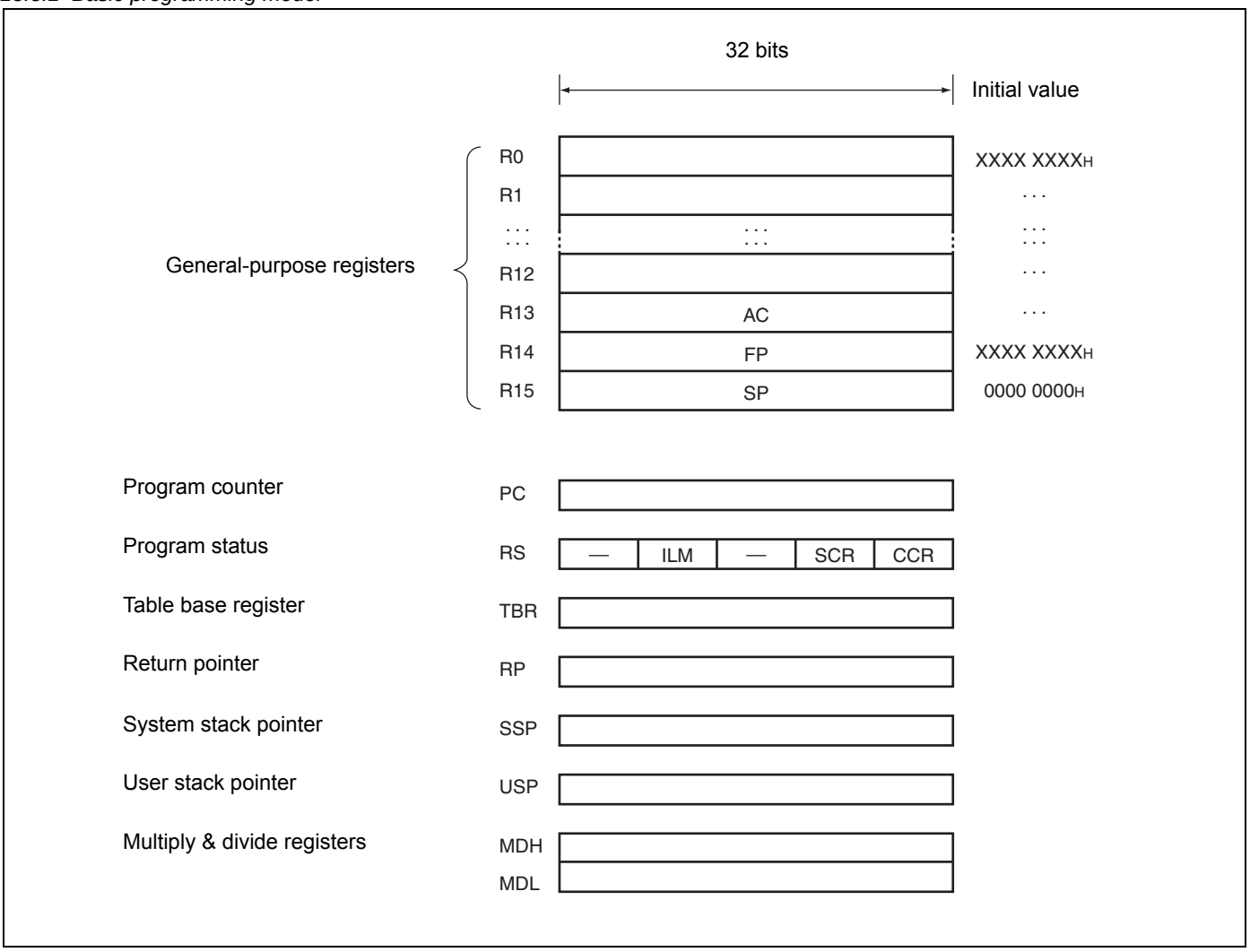
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

13.2 Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

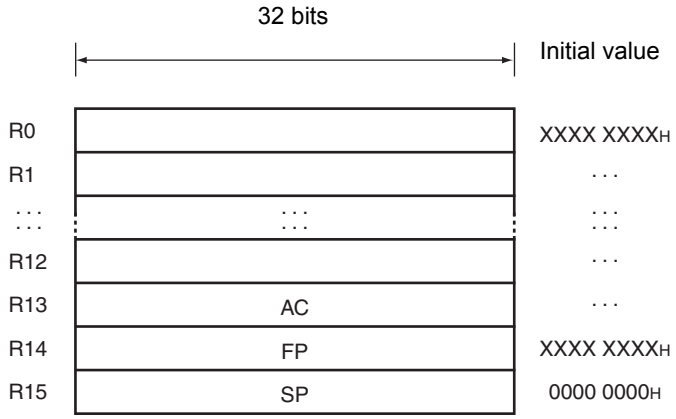
13.3 Programming model

13.3.1 Basic programming model



13.4 Registers

13.4.1 General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

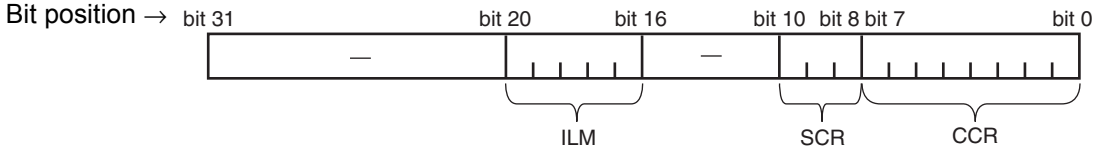
Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator
R14 : Frame pointer
R15 : Stack pointer

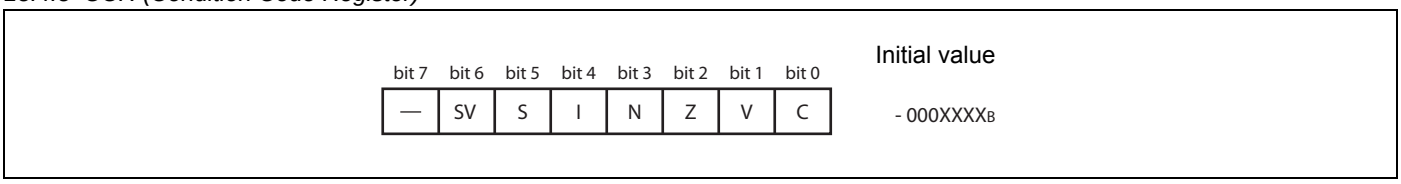
Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

13.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.
All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.

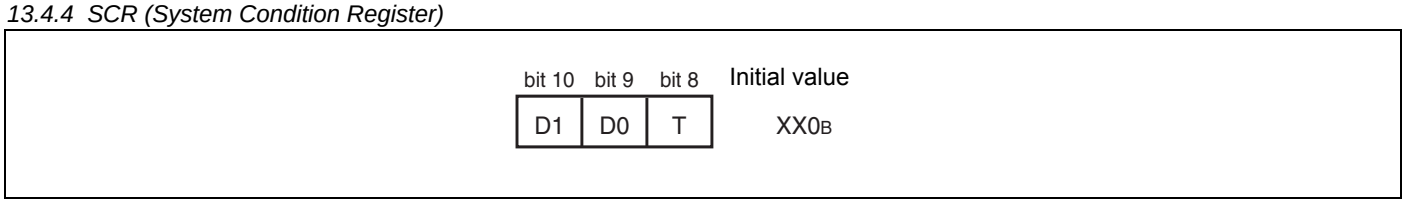


13.4.3 CCR (Condition Code Register)



SV : Supervisor flag
S : Stack flag
I : Interrupt enable flag
N : Negative enable flag
Z : Zero flag
V : Overflow flag
C : Carry flag

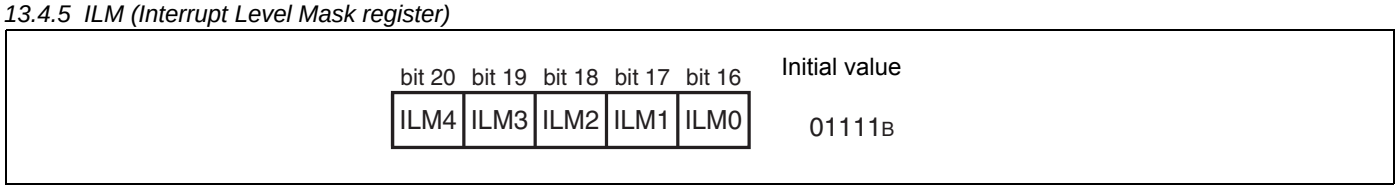
13.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

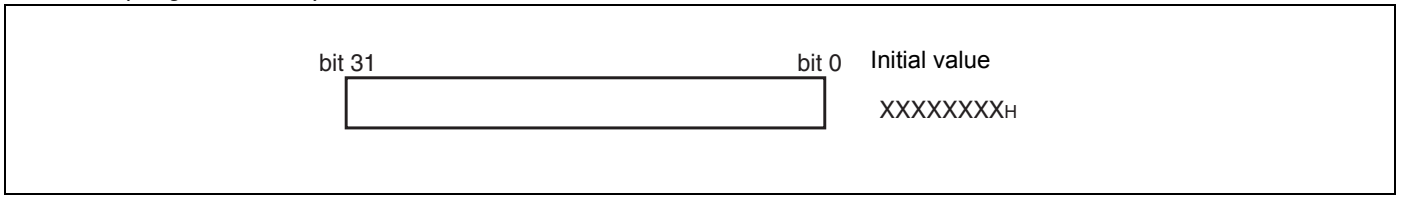
Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

13.4.5 ILM (Interrupt Level Mask register)



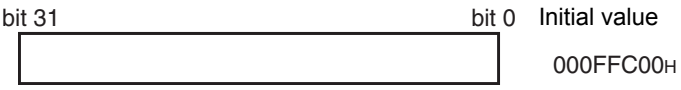
This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.
The register is initialized to value "01111_B" at reset.

13.4.6 PC (Program Counter)



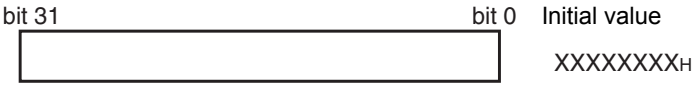
The program counter indicates the address of the instruction that is being executed.
The initial value at reset is undefined.

13.4.7 TBR (Table Base Register)



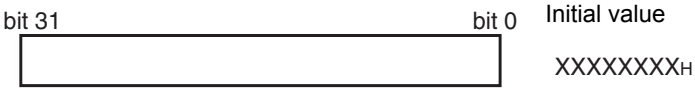
The table base register stores the starting address of the vector table used in EIT processing.
The initial value at reset is $000FFC00_H$.

13.4.8 RP (Return Pointer)



The return pointer stores the address for return from subroutines.
During execution of a CALL instruction, the PC value is transferred to this RP register.
During execution of a RET instruction, the contents of the RP register are transferred to PC.
The initial value at reset is undefined.

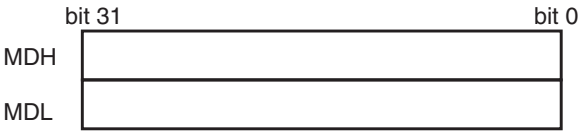
13.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

13.4.10 Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.
The initial value at reset is undefined.

14. Embedded Program/Data Memory (Flash)

14.1 Flash features

- CY91F465PA: 544 KBytes (8 × 64 Kbytes + 4 × 8 KBytes = 4.25 Mbits)
- CY91F467PA: 1088 KBytes (16 × 64 Kbytes + 8 × 8 KBytes = 8.5 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

14.2 Operation modes:

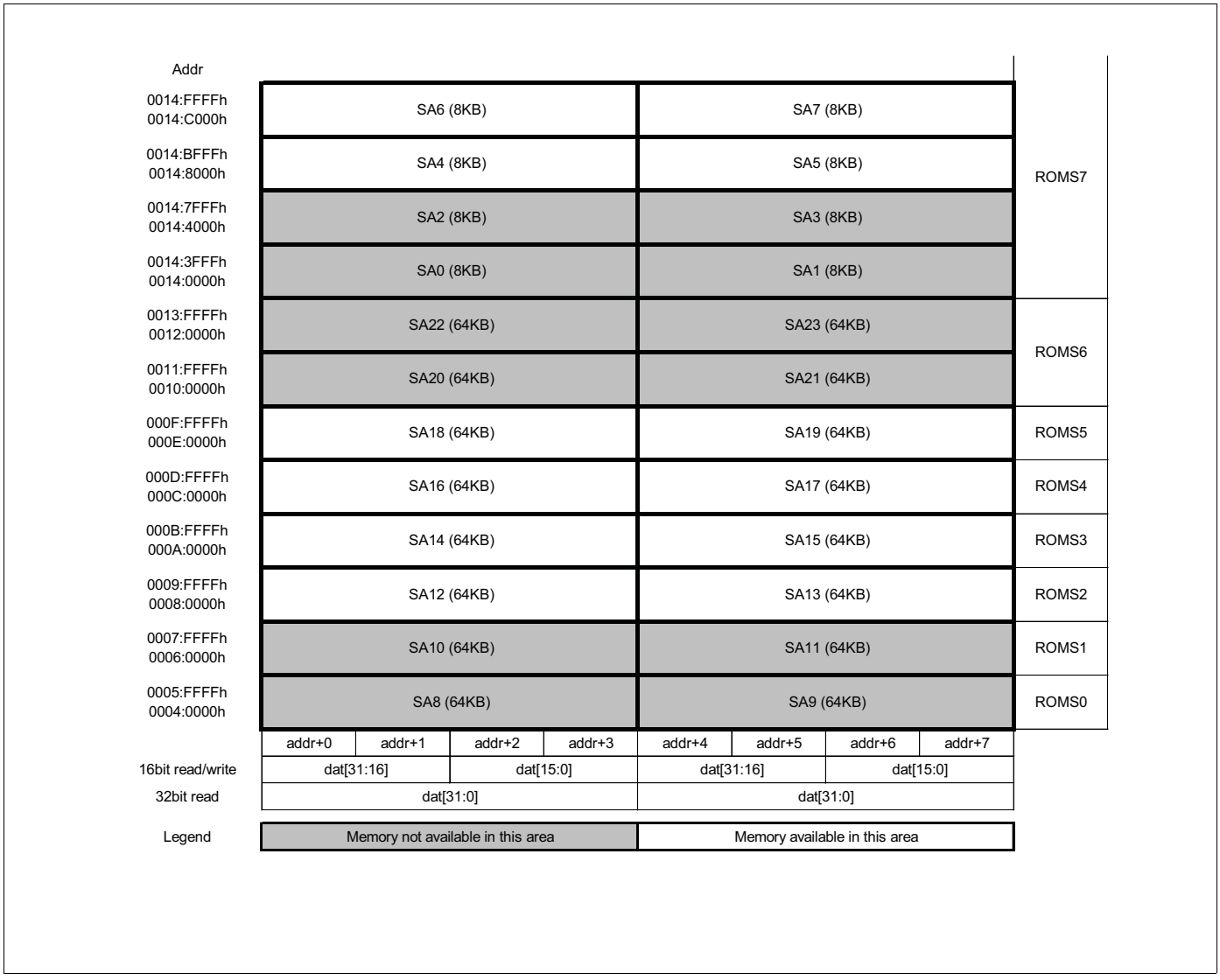
1. 64-bit CPU mode (available on CY91F467PA only) :
   - CPU reads and executes programs in word (32-bit) length units.
   - Flash writing is not possible.
   - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode:
   - CPU reads and executes programs in word (32-bit) length units.
   - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode:
   - CPU reads and writes in half-word (16-bit) length units.
   - Program execution from the Flash is not possible.
   - Actual Flash Memory access is performed in word (16-bit) length units.

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 “Flash Access Mode Switching”.

14.3 Flash access in CPU mode

14.3.1 Flash configuration

Flash memory map CY91F465PA



Flash memory map CY91F467PA

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

14.3.2 Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 100 MHz	1	1	3	-	4	

Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	1	8	

14.3.3 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Address mapping CY91F465PA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
08:0000h to 13F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
08:0000h to 13F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 10:0000h offset for parallel Flash programming.
Set offset by keeping FA[20] = 1 as described in section “Parallel Flash programming mode”.

Address mapping CY91F467PA

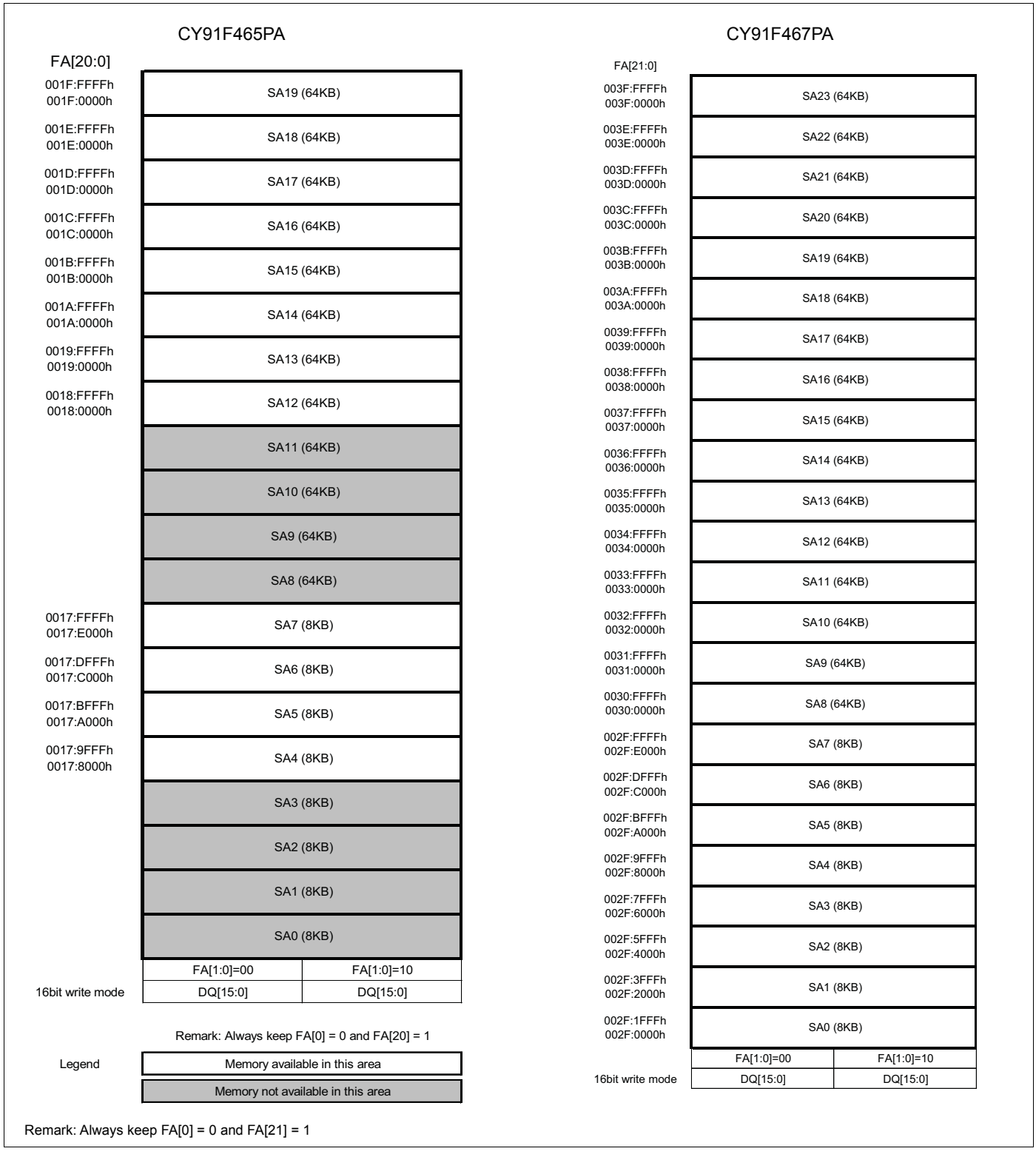
CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h + 01:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

14.4 Parallel Flash programming mode

14.4.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):



14.4.2 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TCExternal pins	FR-CPU mode	CY91F465PA, CY91F467PA external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	104	
RESET	-	FRSTX	NMIX	105	
-	-	MD_2	MD_2	96	Set to ‘1’
-	-	MD_1	MD_1	95	Set to ‘1’
-	-	MD_0	MD_0	94	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	P19_0	112	
BYTE	Internally fixed to ‘H’	BYTEX	P19_2	114	
WE	Internal control signal + control via interface circuit	WEX	P18_0	118	
OE		OEX	P19_6	117	
CE		CEX	P19_5	116	
-		ATDIN	MD_3	98	Set to ‘0’
-		EQIN	MONCLK	97	Set to ‘0’
-		TESTX	P19_4	115	Set to ‘1’
-		RDYI	P19_1	113	Set to ‘0’
A-1	Internal address bus	FA0	P17_5	124	Set to ‘0’
A0 to A7		FA1 to FA8	P06_0 to P06_7	6 to 13	
A8 to A15		FA9 to FA16	P05_0 to P05_7	14 to 21	
A16 to A18		FA17 to FA19	P18_1, P18_2, P18_4	119, 120, 121	
A19		FA20	P18_5	122	Set to ‘1’ on CY91F465PA
—		FA21	P18_6	123	Not needed on CY91F465PA; Set to ‘1’ on CY91F467PA
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P01_0 to P01_7	24 to 31	
DQ8 to DQ15		DQ8 to DQ15	P00_0 to P00_7	32 to 39	

14.5 Poweron Sequence in parallel programming mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

14.6 Flash Security

14.6.1 Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

14.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to ‘0’	set to ‘0’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘0’	Write Protection (all device modes, without exception)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes)
set all to ‘0’	set to ‘1’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘0’	Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”)

FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0 (CY91F467PA)	set to “0”	set to “1”	not available
FSV1[1]	SA1 (CY91F467PA)	set to “0”	set to “1”	not available
FSV1[2]	SA2 (CY91F467PA)	set to “0”	set to “1”	not available
FSV1[3]	SA3 (CY91F467PA)	set to “0”	set to “1”	not available
FSV1[4]	SA4	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[8]	—	set to “0”	set to “1”	not available
FSV1[9]	—	set to “0”	set to “1”	not available
FSV1[10]	—	set to “0”	set to “1”	not available
FSV1[11]	—	set to “0”	set to “1”	not available
FSV1[12]	—	set to “0”	set to “1”	not available
FSV1[13]	—	set to “0”	set to “1”	not available
FSV1[14]	—	set to “0”	set to “1”	not available
FSV1[15]	—	set to “0”	set to “1”	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organization of the Flash Memory.

14.6.3 Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 kByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8 (CY91F467PA)	set to “0”	set to “1”	
FSV2[1]	SA9 (CY91F467PA)	set to “0”	set to “1”	
FSV2[2]	SA10 (CY91F467PA)	set to “0”	set to “1”	
FSV2[3]	SA11 (CY91F467PA)	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[12]	SA20 (CY91F467PA)	set to “0”	set to “1”	
FSV2[13]	SA21 (CY91F467PA)	set to “0”	set to “1”	
FSV2[14]	SA22 (CY91F467PA)	set to “0”	set to “1”	
FSV2[15]	SA23 (CY91F467PA)	set to “0”	set to “1”	
FSV2[31:16]	—	set to “0”	set to “1”	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

14.7 Notes About Flash Memory CRC Calculation

The Flash Security macro contains a feature to calculate the 32-bit checksum over addresses located in the Flash Memory address space. This feature is described in the CY91460 Series Hardware Manual, chapter 55.4.1 “Flash Security Control Register”.

Additional notes are given here:

The CRC calculation runs on the internal RC clock. It is recommended to switch the RC clock frequency to 2 MHz for shortening the calculation time. However, the CPU clock (CLKB) must be faster then RC clock, otherwise the CRC calculation may not start correctly.

15. Embedded Data Flash (CY91F467PA)

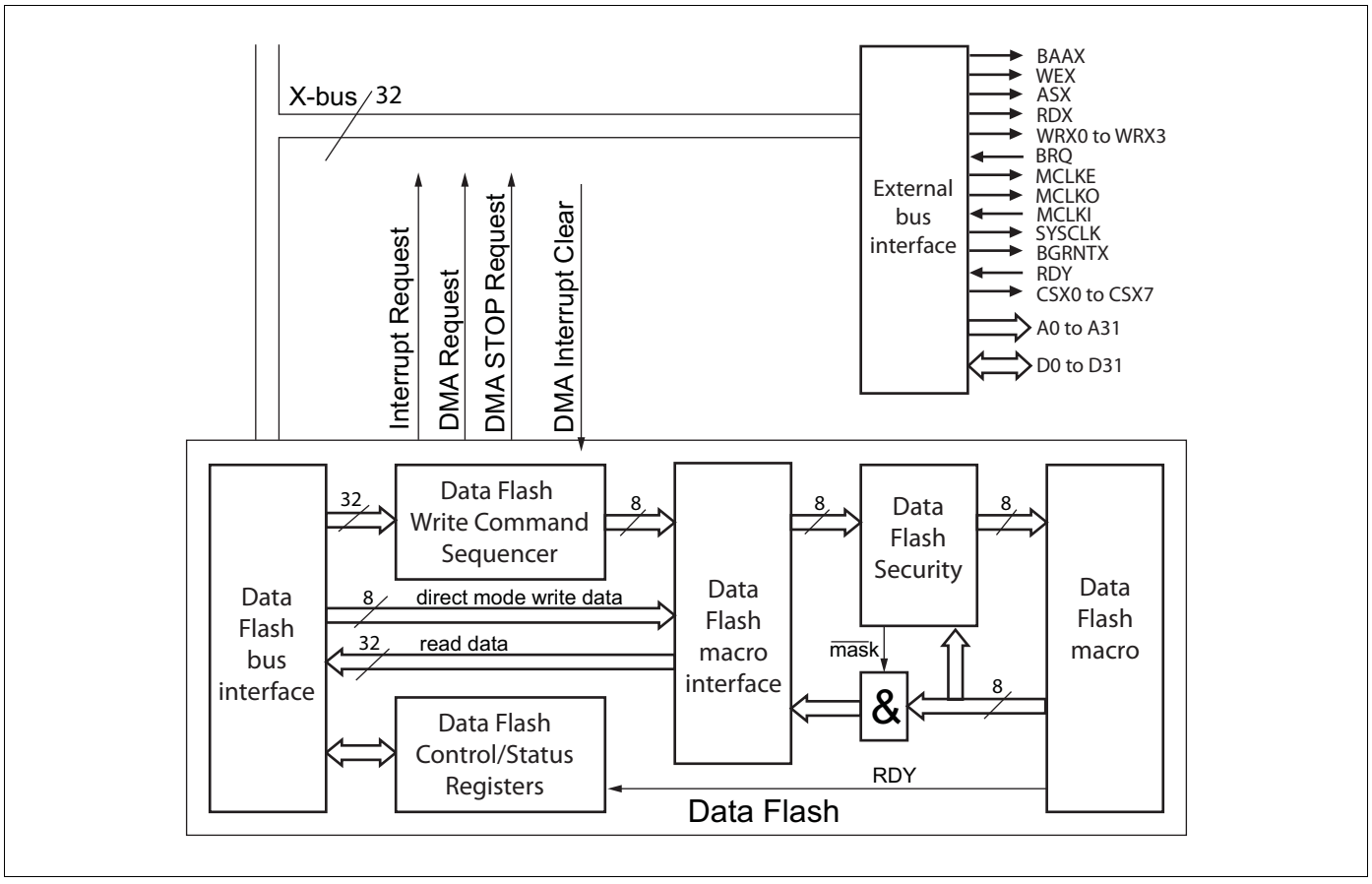
CY91F467PA contains a 64 KByte internal data flash.

15.1 Data Flash Features

- CY91F467PA: 64 Kbytes (4 × 16 Kbytes + 1 × 256 bytes security sector)
- Data width of flash macro: 8 bit
- Synchronous flash interface and flash macro
- 2 access modes (direct access, command sequencer access)
- Read access 8/16/32-bit by internal sequencer hardware
- Write access 8-bit in direct access mode, 8/16/32-bit in command sequencer write mode
- Programmable wait states for read/write access
- Data Flash Security feature (read and write protection)
- CRC calculation feature
- Interrupt- and DMA request, DMA stop request

15.2 Data Flash Block Diagram

The Data Flash consists of the flash macro and interface, control, status, command sequencer and security logic. On CY91460 series devices, the Data Flash is connected to the X-Bus in parallel to the External Bus interface:



15.3 Data Flash Operation Modes

The data flash is located in the top address space of external bus area. Per **default** (after software reset RST), the data flash is **disabled** and does not accept any read/write access. The data flash can be enabled by setting the bit DFCS:FLASHEN (DFCS is the Data Flash Control/Status register).

15.3.1 Direct Access mode:

The Direct Access mode provides data flash access similar to the access of the embedded program/data flash (main flash). For write/program operations, the flash command sequences must be written by the CPU. The command sequences are the same as used for the embedded program/data flash (main flash).

- CPU reads data in byte, halfword or word (8/16/32-bit) length units, whereas 16- or 32-bit read operations are split into 2 or 4 sequential 8-bit flash macro read accesses by hardware.
- CPU writes data in byte (8-bit) width units.
- For write/program operations, the flash command sequences must be written by the CPU.
- The flash macro auto algorithms (Chip Erase, Sector Erase, Sector Erase Suspend,...) can only be activated in direct access mode.
- Direct access mode is the default mode after software reset (RST).

15.3.2 Command Sequencer Mode:

In command sequencer mode, the flash macro command sequences for data write operation are generated by hardware.

- CPU reads data in byte, halfword or word (8/16/32-bit) length units (same as in direct access mode).
- CPU writes data in byte, halfword or word (8/16/32-bit) length units using normal “store” instructions. The flash macro command sequences are generated by internal command sequencer hardware. For 16- or 32-bit write, 2 or 4 command sequences are generated, respectively.
- The data flash interface will not issue wait states after a command sequencer write operation was started. The CPU can continue working during data flash programming.
- If a command sequencer write operation is ongoing, and the CPU writes data again, this second write request is ignored! The error flag DFWS:PAERF is set in case of such a prohibited access. It is recommended to use the data flash interrupts, which indicate that the proceeding write sequence was finished and successful.
- If a command sequencer write operation is ongoing, and the CPU tries to read data, 0x00 is returned and the error flag DFWS:PAERF is set.
- The flash macro auto algorithms (Chip Erase, Sector Erase, Sector Erase Suspend,...) cannot be activated.
- Command Sequencer mode is enabled by setting the bit DFWC:WE (Data Flash Write Control register).
- After software reset (RST), the command sequencer mode is disabled.

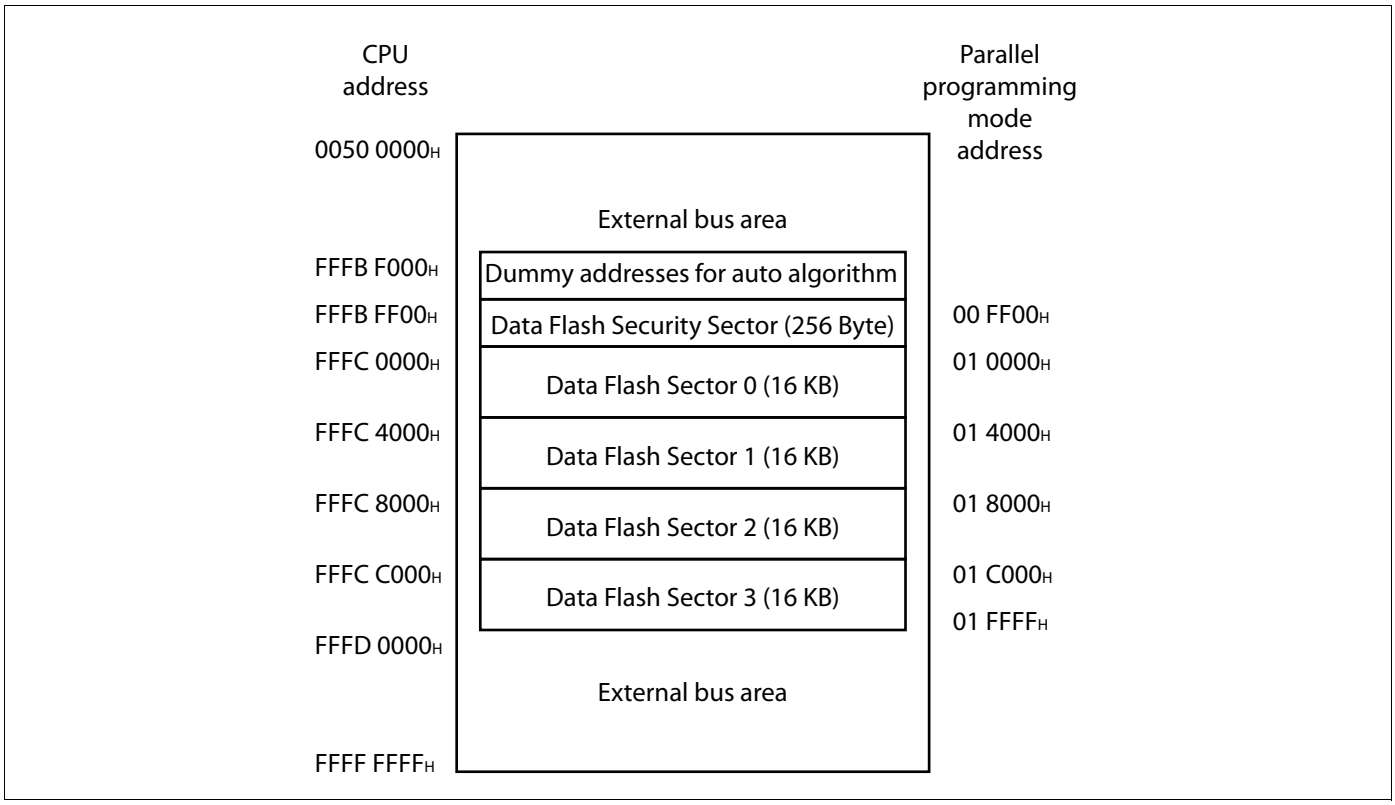
15.3.3 Parallel Programming mode:

- The parallel programming mode works similar to the main flash memory. The function/timing of some external control lines are different.
- In parallel programming mode, it is not necessary to set the Data Flash enable bit (DFCS:FLASHEN).
- Data Flash Memory access is performed in byte (8-bit) length units.

15.4 Data Flash access in CPU mode

15.4.1 Data Flash memory map CY91F467PA

The Data Flash macro is 8 bit wide. It is located in the top address space of external bus area:



Note: The address in parallel programming mode is listed here without 10:0000h offset.
Set the offset by keeping FA[22:20] = 001 the same kind as used for programming of the main flash.

Note: The “Dummy addresses for auto algorithm” are accepted although they are located below the physical addresses of the flash macro. This address space is needed to apply correct addresses in auto algorithms.
See the example in 15.4.4“Auto Program Algorithms”. However, toggle flags cannot be read using the dummy addresses.

15.4.2 Data Flash and External Bus

If the Data Flash is disabled (see 15.3“Data Flash Operation Modes”), the complete address space can be used for the external bus.

If the Data Flash is enabled, the user should take care that no external bus chip select area overlaps the address range of the Data Flash.

If a chip select area overlaps the Data Flash addresses, the following scenario may appear:

- Write operations will be sent to data flash and external bus in parallel. This may cause heavy problems, especially if the data flash is written in direct mode, where the CPU sends the command sequences for programming (see 15.3.1“Direct Access mode:”).
- Read operations will return unpredictable results.

15.4.3 Flash access timing settings in CPU mode

The Data Flash can be accessed up to CLKB = 100 MHz. For timing and wait state setup, please refer to the description of the bits TMG2, TMG1, TMG0 in 15.5.1“Data Flash Control and Status Register”.

Although the data flash is located in the address space of external bus, there is no dependency between external bus timing and data flash timing.

15.4.4 Auto Program Algorithms

The auto program algorithms can only be applied in direct access mode, while the “Program” sequence can be generated by hardware if the Command Sequencer Mode is used.
The data flash supports command sequences similar to the main flash:

Command Sequence	Bus Write Cycle	1st bus Write cycle		2nd bus Write cycle		3rd bus Write cycle		4th bus Write cycle		5th bus Write cycle		6th bus Write cycle	
		Address	Data	Address	Data	Address	Data			Address	Data	Address	Data
Read/Reset	1	XXX	F0	RA	RD								
Read/Reset	3	AA8	AA	554	55	AA8	F0	RA	RD				
Program	4	AA8	AA	554	55	AA8	A0	PA	PD				
Chip Erase	6	AA8	AA	554	55	AA8	80	AA8	AA	554	55	AA8	10
Sector Erase	6	AA8	AA	554	55	AA8	80	AA8	AA	554	55	SA	30
Sector Erase Suspend		Sector Erase Suspend by input of address “XXX" and data “B0”											
Sector Erase Resume		Sector Erase Resume by input of address “XXX" and data “30”											
Unlock Bypass set	3	AA8	AA	554	55	AA8	20						
Unlock Bypass program	2	XXX	A0	PA	PD								
Unlock Bypass Reset	2	XXX	90	XXX	F0/ 00								

PA: Program Address
PD: Program Data. Data to be programmed at location PA.
RA: Read Address
RD: Data to read at location RA.
SA: Sector Address (points into the sector to be erased)

It is recommended that the addresses “AA8” and “554” point to the sector which is to be programmed.
For **example**, to program a byte into sector SAS, the following sequence should be used:

AddressPA=0xFFFBFF83 is inside sector SAS.

1. write addr=0xFFFBFAA8 data=0xAA
2. write addr=0xFFFBF554 data=0x55
3. write addr=0xFFFBFAA8 data=0xA0
4. write addr=0xFFFBFF83 =PA data=PD

Note: The address for the write sequence (1., 2., 3. write) points into the “Dummy addresses for auto algorithm” here. For polling of toggle bits, an address pointing inside the programmed sector has to be used, for example the programmed address (PA) itself.

15.4.5 Data Flash Hardware Sequence Flags (Toggle Bits)

In direct access mode, the data flash returns toggle bits shown in the following table.
In command sequencer mode, it is not necessary to read the toggle bits because they are observed by the command sequencer automatically.

Status				DQ7	DQ6	DQ5	DQ4	DQ3	DQ2
In Progress	Embedded Program Algorithm			~DQ7	Toggle	0	0	0	1
	Embedded Erase Algorithm (Erase Suspended Sector)	Busy to suspend		0	Toggle	0	1	1	Toggle
		Ready to suspend					0		
	Embedded Erase Algorithm (Non-Erase Suspended Sector)		Busy to suspend	0	Toggle	0	1	1	1
			Ready to suspend				0		
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)		1	1	0	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)		Data	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)		~DQ7	Toggle	0	0	0	1
Exceeded Time Limits	Embedded Program Algorithm			~DQ7	Toggle	1	0	0	1
	Embedded Erase Algorithm			0	Toggle	1	N/A	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)		~DQ7	Toggle	1	0	0	N/A

Note: For polling of toggle bits, an address pointing inside the programmed sector has to be used, for example the programmed address itself. Do not use a “Dummy addresses for auto algorithm”.

15.5 Data Flash Registers

The Data Flash has the following control/status registers:

DFCS : Data Flash Control and Status Register

Address	31	30	29	28	27	26	25	24	bit
07114_H	RDYI	TMG2	TMG1	TMG0	FLASHEN	INTE	RDYINT	RDY	
	0	1	1	1	0	0	0	1	Initial value
	R/W	R/W	R/W	R/W	R/W	R/W	R/W0	R	Attribute

DFWC : Data Flash Write Command Sequencer Control Register

Address	23	22	21	20	19	18	17	16	bit
07115_H	-	-	-	ERINTE	FININTE	IDLINTE	IDLDMAE	WE	
	x	x	x	0	0	0	0	0	Initial value
	-	-	-	R/W	R/W	R/W	R/W	R/W	Attribute

DFWS : Data Flash Write Command Sequencer Status Register

Address	15	14	13	12	11	10	9	8	bit
07116_H	PAERF	WIERINT	WERINT	TOERINT	FININT	IDLINT	ST1	ST0	
	0	0	0	0	0	0	0	0	Initial value
	R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R	R	Attribute

DFSCR0 : Data Flash Security Control Register 0

Address	31:24	23:16	15:8	7:0	bit
07118_H	DFSCR0[31:0]				
	1111 1111	1111 1111	1111 1111	1111 1111	Initial value
	R/W, R	R	R	R	Attribute

DFSCR1 : Data Flash Security Control Register 1

Address	31:24	23:16	15:8	7:0	bit
$0711C_H$	DFSCR1[31:0]				
	0 - - - 0001	0000 0000	0000 0000	0000 0000	Initial value
	R, R/W	R, R/W	R, R/W	R, R/W	Attribute

15.5.1 Data Flash Control and Status Register

This section explains the Data Flash Control and Status register.

DFCS : Data Flash Control and Status register

Addr: 0x07114

31	30	29	28	27	26	25	24	bit
RDYI	TMG2	TMG1	TMG0	FLASHEN	INTE	RDYINT	RDY	
0	1	1	1	0	0	0	1	initial
R/W	R/W	R/W	R/W	R/W	R/W	R/W0	R	attribute

RDYI	Ready Inversion
0	(default) Normal flash operation
1	Setting this bit to ’1’ activates the RDYI input of the Flash. As a result, the RDY output of the Flash goes to ’0’ (used for test purposes only). Always write 0 to this bit.

- This bit is cleared by software reset (RST).
- Always write 0 to this bit.

TMG2	TMG1	TMG0	Data Flash Timing Control		
			CLKB Frequency up to	CLKB Cycles per Read Operation	CLKB Cycles per Write Operation
0	0	0	6.2 MHz	3	3
0	0	1	16.7 MHz	4	3
0	1	0	33.3 MHz	5	3
0	1	1	50 MHz	6	3
1	0	0	66.6 MHz	8	4
1	0	1	83.3 MHz	9	5
1	1	0	100 MHz	10	6
1	1	1	(default) 100 MHz	11	6

- These bits control the number of wait cycles for read and write operations.
- The bits are set to “111” by software reset (RST) and can be read and written

FLASHEN	Data Flash Enable
0	(default) Data Flash is disabled and does not accept read and write access
1	Data Flash is enabled and can be read and written depending on data flash security settings.

- This bit is cleared by software reset (RST) and can be read and written
- Before setting this bit, the user has to take care that no External Bus Chip Select area overlaps the data flash address space.

INTE	Ready Interrupt Enable
0	(default) Disable the interrupt of the RDYINT flag
1	Enable the interrupt of the RDYINT flag

- If this bit is cleared, no interrupt is generated when the RDYINT flag is set.
- If this bit is set, the interrupt by RDYINT flag is enabled.
- This bit is cleared by software reset (RST) and can be read and written.

RDYINT	Ready Interrupt Flag
0	(default) The flash macro has not entered the READY state
1	The flash macro has entered the READY state

- This bit is set after a rising edge of the RDY status line of the flash macro.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- Read-modify-write operations will read 1.

RDY	Flash Macro Ready Status
0	Indicates that a program/erase command is currently executed. Only the reset and suspend commands are accepted in this state.
1	(default) Indicates that no program/erase command is currently executed. Any command can be written to the Flash.

- This bit shows the RDY status line of the flash macro after a certain response time t_{BUSY}:
  In direct access mode, t_{BUSY} is minimum 90 ns after the last write access of a program sequence.
  In write sequencer mode, the command sequencer cares about RDY signal. There is no need to poll RDY.
- This bit is read-only.

15.5.2 Data Flash Write Command Sequencer Control Register

This section explaines the Data Flash Sequencer Control register

DFWC : Data Flash Write Command Sequencer Control

Addr: 0x07115

23	22	21	20	19	18	17	16	bit
-	-	-	ERINTE	FININTE	IDLINTE	IDLDMAE	WE	
x	x	x	0	0	0	0	0	initial
-	-	-	R/W	R/W	R/W	R/W	R/W	attribute

- Always write 0 to the bits 7:5.

ERINTE	Error Interrupt Enable
0	(default) Disable the interrupt of the error flags
1	Enable the interrupt of the error flag

- If this bit is cleared, no interrupt is generated when a error flag (TOERINT, WERINT and WIERINT) is set.
- If this bit is set, an interrupt is generated when one of the error flags is set.
- This bit is cleared by software reset (RST) and can be read and written.

FININTE	Finish Interrupt Enable
0	(default) Disable the interrupt of the FININT flag
1	Enable the interrupt of the FININT flag

- If this bit is cleared, no interrupt is generated when the FININT flag is set.
- If this bit is set, an interrupt is generated when the FININT flag is set.
- This bit is cleared by software reset (RST) and can be read and written.

IDLINTE	Idle Interrupt Enable
0	(default) Disable the interrupt of the IDLINT flag
1	Enable the interrupt of the IDLINT flag

- If this bit is cleared, no interrupt is generated when the IDLINT flag is set.
- If this bit is set, an interrupt is generated when the IDLINT flag is set.
- This bit is cleared by software reset (RST) and can be read and written.

IDLDMAE	Idle DMA Enable
0	(default) Disable the DMA transfer request
1	Enable the DMA transfer request if the IDLINT flag is set

- If this bit is cleared, no DMA transfer request is generated when the IDLINT flag is set.
- If this bit is set, an DMA transfer request is generated when the IDLINT flag is set.
- This bit is cleared by software reset (RST) and can be read and written.

WE	Write Command Sequencer Enable
0	(default) Disable the Write Command Sequencer, Data Flash operates in direct mode
1	Enable the Write Command Sequencer Mode

- This bit enables the Command Sequencer mode.
- This bit is cleared by software reset (RST) and can be read and written.

15.5.3 Data Flash Write Command Sequencer Status Register

This section explaines the Data Flash Command Sequencer Status register.

DFWS : Data Flash Write Command Sequencer Status

Addr: 0x07116

15	14	13	12	11	10	9	8	bit
PAERF	WIERINT	WERINT	TOERINT	FININT	IDLINT	ST1	ST0	
0	0	0	0	0	0	0	0	initial
R/W0	R/W0	R/W0	R/W0	R/W0	R/W0	R	R	attribute

The command sequencer status flags are only set if the command sequencer is enabled (DFWC:WE=1).

PAERF	Prohibited Access Error Flag
0	(default) No prohibited access detected
1	Prohibited access detected

- This flag is set if the CPU tried to read or write into the Data Flash area while the Data Flash is accessed by the Command Sequencer.
- This flag cannot generate an interrupt.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- Read-modify-write operations will read 1.

WIERINT	Write Incomplete Error Flag
0	(default) Command sequencer write operation was completed
1	Command sequencer was disabled while a write operation was ongoing

- This flag is set when the command sequencer is disabled (set DFWC:WE=0) in “not idle” state.
- If this flag is 0, it is no guarantee that the write operation was successful. Use the FININT flag!
- This flag can generate an interrupt if DFWC:ERINTE is set.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- Read-modify-write operations will read 1.

WERINT	Write Error Flag
0	(default) No write error detected
1	Write operation returned error

- This flag is set after a write access returned error:
  - tried to write to an erase-suspended or write-protected sector,
  - tried to write a bit “1” although it is already “0” in flash.
- This flag can generate an interrupt if DFWC:ERINTE is set.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- Read-modify-write operations will read 1.

TOERINT	Timeout Error Flag
0	(default) No timeout error detected
1	A write operation ended with timeout error

- This flag is set after a write operation ended in timeout state.
- This flag can generate an interrupt if DFWC:ERINTE is set.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- Read-modify-write operations will read 1.

FININT	Command Sequence Finished Flag
0	(default) Write command was not (yet) finished successfully
1	Write command was finished successfully

- This flag is set after a command sequencer write operation was finished successfully.
- This flag can generate an interrupt if DFWC:FININTE is set.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- This bit is also cleared after a DMA transfer (caused by IDLINT) was finished.
- Read-modify-write operations will read 1.

IDLINT	Command Sequencer Idle Flag
0	(default) Command sequencer is disabled or not in IDLE state
1	Command sequencer entered the IDLE state

- This flag is set after the command sequencer was enabled (set DFWC:WE=1) or entered the IDLE state after a write operation was finished.
- This flag can generate an interrupt if DFWC:INTE is set.
- This flag can generate a DMA transfer request if DFWC:IDLDMAE is set.
- This bit is cleared by software reset (RST) or by writing 0. Writing 1 has no effect.
- This bit is also cleared after a DMA transfer was finished.
- Read-modify-write operations will read 1.

ST1	ST0	Command Sequencer Status Flags
0	0	(default) Command sequencer is disabled or in IDLE state
0	1	Command sequencer is submitting the write command
1	0	Command sequencer is waiting for Flash program finish
1	1	Command sequencer was disabled in "not idle" state

- Status bit {ST1,ST0} =2'b11 show that the command sequencer was disabled in "not idle" state and direct access to Flash is not yet permitted (wait for proceeding Flash sequence to finish). Max duration of this wait can be 11 clock cycle after disabling Command Sequencer.

15.5.4 Data Flash security Control Register 0,1

Please refer to 15.8.5"Data Flash Security Registers".

15.6 Data Flash Interrupts and DMA Access

If a command sequencer write operation is ongoing, and the CPU writes data again, this second write request is ignored! Therefore, it is recommended to use the data flash interrupts or DMA, which indicates that the write sequence is finished and successful.

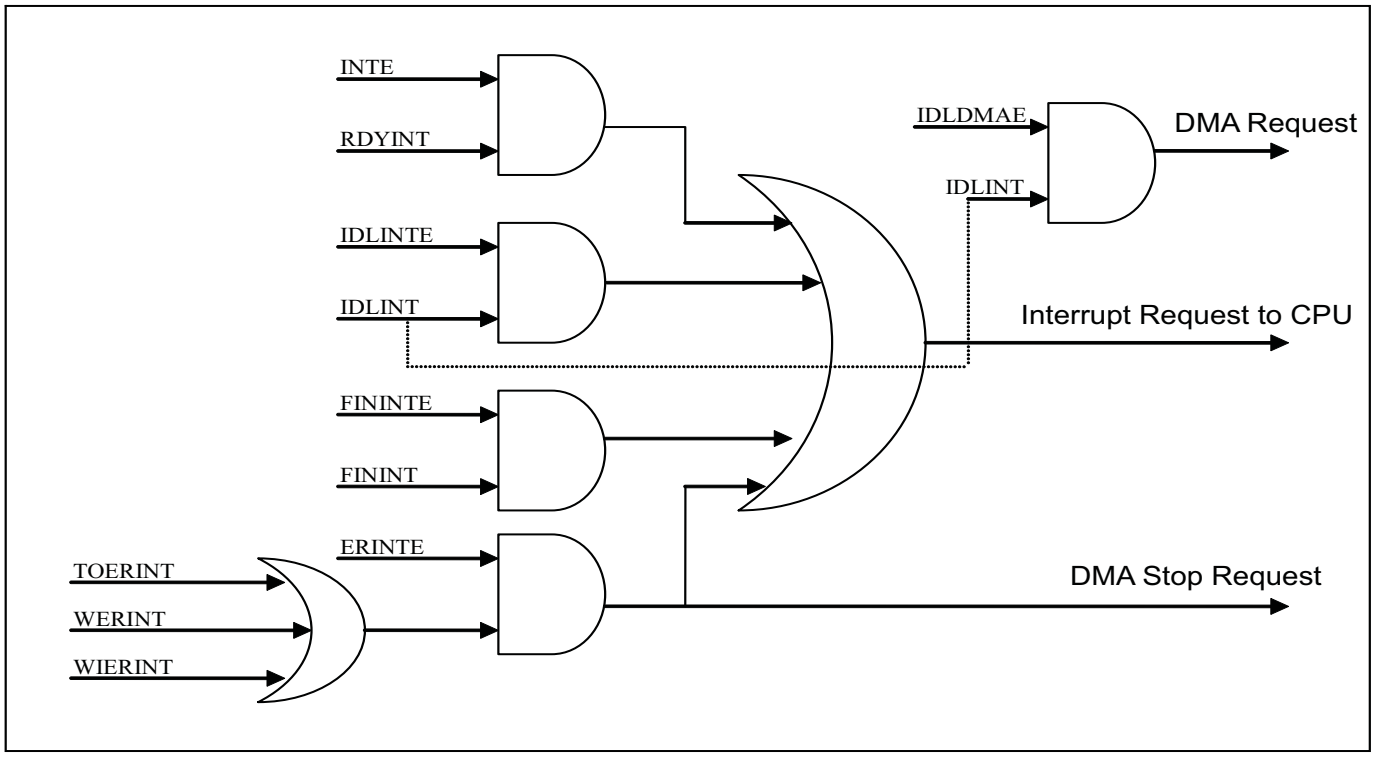
15.6.1 Data Flash Interrupt Flag Overview

The Data Flash interface has 6 interrupt flags with certain relationship to the 3 output lines for interrupt / DMA request:

Interrupt Flags:

- IDLINT — IDLE flag, indicates that the command sequencer has entered the IDLE state after a write sequence. This flag is also set just after the command sequencer was enabled by setting DFWC:WE.
- RDYINT — READY flag, indicates that the flash macro has entered READY state.
- FININT — FINISH flag, indicates that the command sequencer finished a write sequence successfully.
- TOERINT — TIMEOUT Error flag, indicates that a command sequencer write sequence ended in TIMEOUT error state.
- WERINT — Suspend Sector Write Error flag, indicates that there was a write request to a sector which is erase suspended or write-protected and not ready for writing.
- WIERINT — Write Incomplete Error flag, indicates that the command sequencer was disabled (DFWC:WE = 0) while a write sequence was ongoing.
- PAERF — Prohibited Access Error flag, indicates that the CPU tried a read or write access while a command sequencer write was ongoing. PAERF is a status flag and cannot generate an interrupt.

The following picture shows the interrupt flags and their enable bits.



The DMA request can be activated by the IDLE flag only and has a separate enable bit (DFWC:IDLDMAE).
DMA Stop request is activated by the error flags.

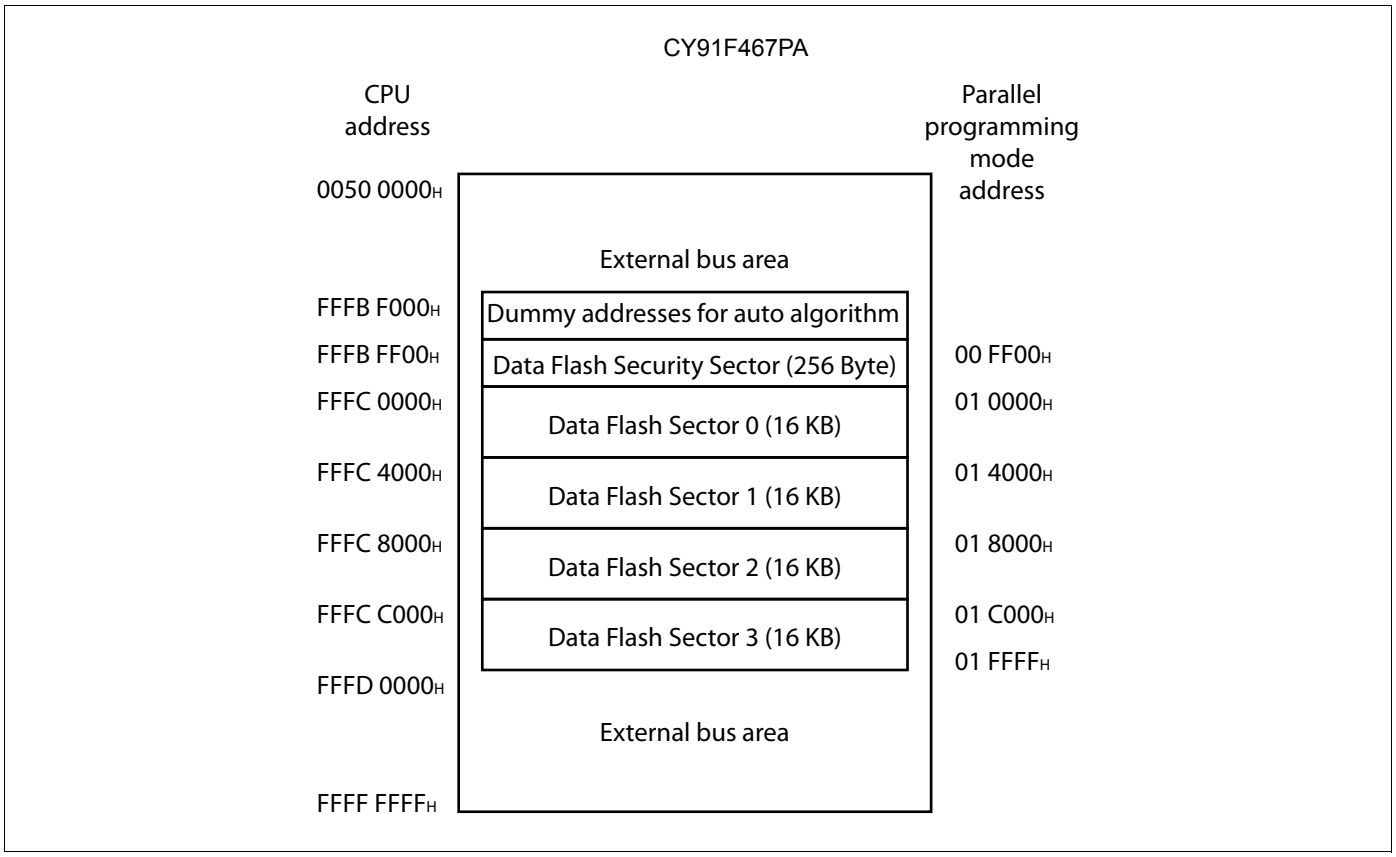
The CPU interrupt can be activated by all interrupt flags.

15.7 Data Flash parallel programming mode

Note: The currently available parallel flash programmers do not support the programming of the data flash. The programmers may be updated on request. This chapter is for information only.

15.7.1 Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD[2:0] = 111):



Note: The address in parallel programming mode is listed here without 10:0000h offset.
Set the offset by keeping FA[22:20] = 001 the same kind as used for programming of the main flash.

Note: The “Dummy addresses for auto algorithm” are accepted although they are located below the physical addresses of the flash macro. This address space is needed to apply correct addresses in auto algorithms.
See the example in 15.4.4“Auto Program Algorithms”.

15.7.2 Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to data flash macro addresses which are used in parallel programming.

Address mapping CY91F467PA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
FFFB:FF00h to FFFC:FFFFh	-	SAS, SA0, SA1, SA2, SA3 (256 Byte + 64 Kbyte)	FA := addr - 0B:0000h

Note: FA result is without 10:0000h offset for parallel Flash programming .
Set the offset by keeping FA[22:20] = 001 the same kind as used for programming of the main flash.

15.7.3 Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Data Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the Data Flash memory's Auto Algorithms are available.

Correspondence between flash macro and Flash Memory Control Signasl

Data Flash macro pins	FR-CPU mode	**CY91F467PA** external pins			Comment
—	INITX	—	INITX	104	
FRSTX	—	FRSTX	NMIX	105	
—	—	MD_2	MD_2	96	Set to '1'
—	—	MD_1	MD_1	95	Set to '1'
—	—	MD_0	MD_0	94	Set to '1'
RDY	FMCS:RDY bit	RY/BYX	P19_0	112	
FCLK		FCLK	P19_2	114	Clock input
WEX	Internal control signal + control via interface circuit	WEX	P18_0	118	
OEX		OEX	P19_6	117	
CEX		CEX	P19_5	116	
RAS		RAS	MD_3	98	
EQIN		EQIN	MONCLK	97	
LTIN		LTIN	P23_0	68	Set to '0'
—		TESTX	P19_4	115	Set to '1'
—		RDYI	P19_1	113	Set to '0'
FA0	Internal address bus	FA0	P17_5	125	
FA1 to FA8		FA1 to FA8	P06_0 to P06_7	6 to 13	
FA9 to FA16	Internal address bus	FA9 to FA16	P05_0 to P05_7	14 to 21	
—		FA17 to FA19	P18_1, P18_2, P18_4	119, 120, 121	Set to '0'
—		FA20,FA21	P18_5, P18_6	122, 123	Set to "10"
DI0 to DI7, DO0 to DO7	Internal data bus	DQ0 to DQ7	P01_0 to P01_7	24 - 31	

15.7.4 Wait time before data flash access in parallel programming mode

After power-on or the end of a Setting Initialization Request (INITX), the internal data flash security module fetches the security information. The parallel programmer cannot access the flash until the security vector fetch is finished and has to wait for the following time:

- Min waittime after VDD5/VDD5R power on : 2.9 ms
- Min waittime after INITX rising : 1.0 ms

15.8 Data Flash Security

15.8.1 Data Flash Security Operation

The data flash security protects the flash against unauthorized read and write access.

- A **read** access to protected flash will return data=0x00 without notification. There is no flag indicating that the read access was masked by data flash security module.
- A **write** access to a write-protected sector will be cancelled.
  The flash macro will be put into RESET state, and the security macro will re-fetch the security information.
  It may take up to 600µs until the data flash can be accessed again.
  In direct access mode, the toggle bits will not change and the bit DFCS:RDY will not go to low state.
  In command sequencer mode, the flag DFWS:WERINT is set, indicating that the write operation was not successful.
- The only possible write operation to a protected sector is Chip Erase.
- The data flash security can be disabled by setting the external pin FSC_DISABLE = 1.
- After INIT, please wait 3 ms before accessing the data flash. This time is needed for the security vector fetch as well as internal signal synchronization. This time is valid also if FSC_DISABLE = 1.

15.8.2 Security Vectors

Two 16-bit Data Flash Security Vectors (DFSV1, DFSV2) are located in the 256 byte security sector, controlling the protection functions of the Data Flash Security module:

DFSV1[15:0]: 0xFFFB:FF00
DFSV2[15:0]: 0xFFFB:FF02

	Vectors				
Address	**+0**	**+1**	**+2**	**+3**	**Block**
$FFFBFF00_H$	DFSV1[15:0]		DFSV2[15:0]		Data Flash Security Vectors

15.8.3 Security Vector DFSV1 (bit15 to bit0)

The setting of the Flash Security Vector DFSV1 is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector DFSV1 [15:0]

DFSV1[15:3]	DFSV1[2] Write Protection Level	DFSV1[1] Write Protection	DFSV1[0] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC [1])
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC) and Write Protection (all device modes, without exception)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC) and Write Protection (all device modes, except INTVEC)

1. INTVEC mode is the Internal Vector Fetch mode (MD[2:0] = “000”)

Note : If Read Protection is set and the device is not in INTVEC mode and the data flash is written using the Command Sequencer write access, then the command sequencer will set the error flag because it cannot check that the flash programming was successful.

15.8.4 Security Vector DFSV2

The setting of the Flash Security Vector DFSV2 bits [15:0] is responsible for the individual write protection of the Data Flash sectors. It is only evaluated if write protection bit DFSV1 [1] is set.

Explanation of the bits in the Flash Security Vector DFSV2[15:0]

DFSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
DFSV2[0]	SA0	set to “0”	set to “1”	
DFSV2[1]	SA1	set to “0”	set to “1”	
DFSV2[2]	SA2	set to “0”	set to “1”	
DFSV2[3]	SA3	set to “0”	set to “1”	
DFSV2[7:4]	—	—	—	sectors not available
DFSV2[8]	SAS	set to “0”	—	write protection is mandatory!
DFSV2[15:9]	—	—	—	sectors not available

Note : It is mandatory to always set the sector where the Flash Security Vectors DFSV1 and DFSV2 are located to write protected (here sector SAS). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section 15.4“Data Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

15.8.5 Data Flash Security Registers

The Data Flash Security module can be used to calculate a CRC over the Data Flash contents. And it is possible to force a security vector re-fetch by using the following registers.

DFSCR0 : Data Flash Security Control Register 0

Address	31:24	23:16	15:8	7:0	bit
07118_H	S[7:0] CRC[31:24]	CRC[23:0]			
	1111 1111	1111 1111	1111 1111	1111 1111	Initial value
	W, R	R	R	R	Attribute

S[7:0]	Sequence Activation
0xA5 --> 0x5A	Start of a Flash Security Vector Re-Fetch Sequence (write only)
0xF0 --> 0x0F	Start of a Flash Memory CRC32 Checksum Sequence (write only)

- Continuously writing “$A5_H$”, “$5A_H$” in the DFSCR0[31:24] register will start a Flash Security Vector Re-fetch sequence immediately after writing “$5A_H$”. There is no time restrictions between “$A5_H$” and “$5A_H$”, but if “$A5_H$” is written followed by the one other than “$5A_H$”, it must be written “$A5_H$” again. If not, the Re-Fetch sequence cannot be started even if “$5A_H$” is written.
- Continuously writing “$F0_H$”, “$0F_H$” in the DFSCR0[31:24] register will start a CRC32 checksum sequence immediately after writing “$0F_H$”. There is no time restrictions between “$F0_H$” and “$0F_H$”, but if “$F0_H$” is written followed by the one other than “$0F_H$”, it must be written “$F0_H$” again. If not, the CRC checksum sequence cannot be started even if “$0F_H$” is written.
- These bits are cleared by an INIT signal from external pin (INITX) or hardware watchdog and can be written only.

Note: The Flash Security Vector Re-Fetch sequence is especially intended to be used after a chip erase command to update the security status without the need of applying an external INITX reset or after changing the status of the DFSV1 security vector.

Note: The CRC calculation runs on the internal RC clock. It is recommended to switch the RC clock frequency to 2 MHz for shortening the calculation time. However, the CPU clock (CLKB) must be faster then RC clock, otherwise the CRC calculation may not start correctly.

CRC[31:0]	CRC checksum result
	CRC checksum result (read only)

- This register contains the CRC32 checksum result after completion of the CRC32 checksum sequence (the sequence completion is indicated by DFSCR1.RDY). The CRC checksum is calculated in a standard CRC32/AAL5 algorithm with the polygon x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1.
- These bits are set to 0xFFFFFFFF by an INIT signal from external pin (INITX) or hardware watchdog and can be read only.

DFSCR1 : Data Flash Security Control Register 1

Address	31:24	23:16	15:8	7:0	bit
$0711C_H$	SVF_RDY--- --- RDY	- - - - CSZ[3:0]	CSA[15:0]		
	0xxx xxx1	0000 0000	0000 0000	0000 0000	Initial value
	R/Wx	R, R/W	R/W	R/W	Attribute

- Bit30-25: Reserved bits. The read value is always “X”.
- Bit23-20: Reserved bits. The read value is always “0”.

Bit 31:

SVF_RDY	Security Vector Fetch Ready (flag)
0	The security vector has not been fetched. The data flash is protected against read and write access. Read operations to data flash return 0x00. Write operations are ignored.
1	The security vector has been done. The data flash can be accessed according to the security settings.

Bit 24:

RDY	CRC Sequence Ready (flag)
0	CRC sequence running or not yet started
1	CRC sequence ready (data in the DFSCR0 register is valid)

Bit 19-16:

CSZ[3:0]	CRC Size Mask
0000	CRC size mask is 256 Byte
0001	CRC size mask is 512 Byte
0010	CRC size mask is 1 KByte
0011	CRC size mask is 2 KByte
0100	CRC size mask is 4 KByte
0101	CRC size mask is 8 KByte
0110	CRC size mask is 16 KByte
0111	CRC size mask is 32 KByte
1000	CRC size mask is 64 KByte
1001 - 1111	Not supported

- CSZ3-0 is used as an OR-mask for the address given by CSA15-0. See address calculation below.
- These bits are cleared by an INIT signal from external pin (INITX) or hardware watchdog.

Bit 15-0

CSA[15:0]	CRC Calculation Start Address
0x00FF	CRC start address is 0x0FF00 (sector SAS start)
0x0100	CRC start address is 0x10000 (sector SA0 start)
0x0140	CRC start address is 0x14000 (sector SA1 start)

Notes: The values given above are just examples. The addresses to be written in this register are flash memory addresses like used in the flash parallel programming mode and not the mapped addresses which are used in CPU mode. See 15.7.2“Address mapping from CPU to parallel programming mode”.

- The CSA register contains the CRC start address which is aligned to 256 Byte addresses. It is only possible to calculate the CRC checksum over addresses located in the Data Flash Memory address space. Other addresses are invalid and might lead to wrong checksums.

Calculation of the CRC Start- and End-addresses

The CSZ3-0 setting is first translated into a mask value:

CSZ3-0	MASK
0000	0000_0000_0000_0000
0001	0000_0000_0000_0001
0010	0000_0000_0000_0011
0011	0000_0000_0000_0111
0100	0000_0000_0000_1111
0101	0000_0000_0001_1111
0110	0000_0000_0011_1111
0111	0000_0000_0111_1111
1000	0000_0000_1111_1111
1001-1111	and so on...

- CRC Start address = CSA[15:0] << 8 + 0x00
- CRC End address = (CSA[15:0] or MASK) << 8 + 0xFF

16. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

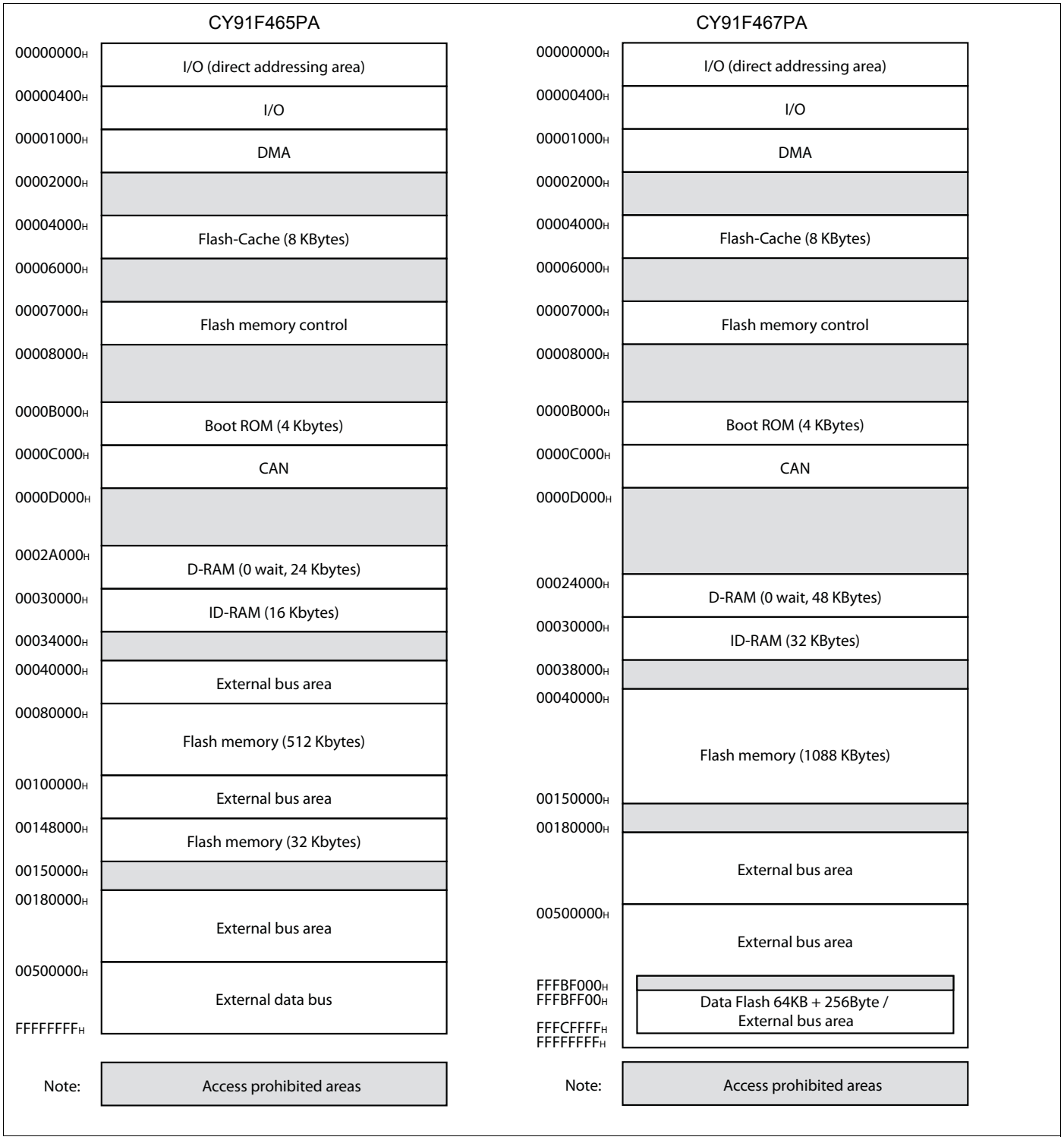
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

17. Memory Maps

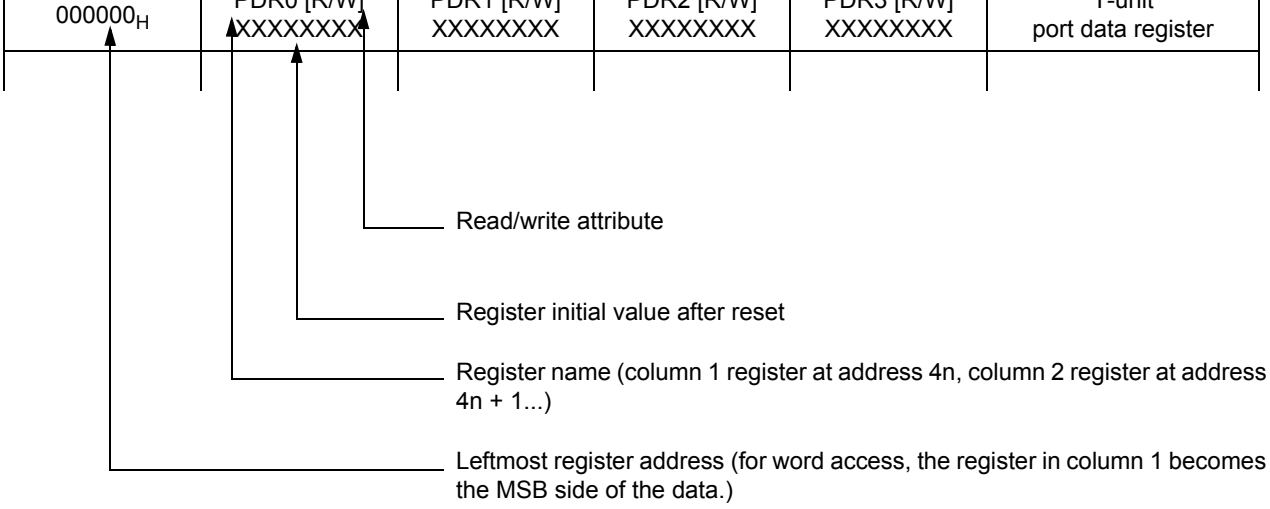
17.1 CY91F465PA, CY91F467PA



18. I/O Map

18.1 CY91F465PA, CY91F467PA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:
" 1 " : Initial value " 1 "
" 0 " : Initial value " 0 "
" X " : Initial value " undefined "
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004_H	Reserved	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] X - - X - -XX	PDR09 [R/W] - - - - - XXX	PDR10 [R/W] - - - - X - XX	Reserved	
$00000C_H$	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] XXXX - XXX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	PDR25 [R/W] - - - - - - XX	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] - -XXXXX	PDR29 [R/W] XXXXXXXX	PDR30 [R/W] XXXXXXXX	Reserved	
000020_H	PDR32 [R/W] X - - - X - - -	PDR33 [R/W] X - - - X - - -	PDR34 [R/W] XXXXXXXX	PDR35 [R/W] XXXXXXXX	
000024_H to $00002C_H$	Reserved				
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7) NMI
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay interrupt
$00003C_H$	Reserved				
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048_H	SCR01 [R/W,W] 00000000	SMR01 [R/W,W] 00000000	SSR01 [R/W,R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART 1
$00004C_H$	ESCR01 [R/W] 00000X00	ECCR01 [R/W,R,W] -00000XX	Reserved		
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000058_H	SCR03[R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR02 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baudrate Generator LIN-USART 0 to 7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H to $0000CC_H$	Reserved				
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	

Address	Register				Block
	+0	+1	+2	+3	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	
$0000E8_H$ to $0000FC_H$	Reserved				
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H	P0TMCSRH [R/W] - 0000000	P0TMCSRL [R/W] 01000000	P1TMCSRH [R/W] - 0000000	P1TMCSRL [R/W] 01000000	Pulse Frequency Modulator
000174_H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178_H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
$00017C_H$	Reserved				
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	

Address	Register				Block
	+0	+1	+2	+3	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter 0
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved				
$0001B0_H$	TMRLRC0 [W] XXXXXXXX XXXXXXXX		TMRC0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0-1)
$0001B4_H$	Reserved		TMCSRCH0 [R/W] - - - 00000	TMCSRCL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLRC1 [W] XXXXXXXX XXXXXXXX		TMRC1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2-3)
$0001BC_H$	Reserved		TMCSRCH1 [R/W] - - - 00000	TMCSRCL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLRC2 [W] XXXXXXXX XXXXXXXX		TMRC2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4-5)
$0001C4_H$	Reserved		TMCSRCH2 [R/W] - - - 00000	TMCSRCL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLRC3 [W] XXXXXXXX XXXXXXXX		TMRC3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6-7)
$0001CC_H$	Reserved		TMCSRCH3 [R/W] - - - 00000	TMCSRCL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLRC4 [W] XXXXXXXX XXXXXXXX		TMRC4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8 to 9)
$0001D4_H$	Reserved		TMCSRCH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
$0001D8_H$	TMRLRC5 [W] XXXXXXXX XXXXXXXX		TMRC5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG10 to 11)
$0001DC_H$	Reserved		TMCSRCH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLRC6 [W] XXXXXXXX XXXXXXXX		TMRC6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 8 to 9)
$0001E4_H$	Reserved		TMCSRCH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMRC7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14 to 15)
$0001EC_H$	Reserved		TMCSRCH7 [R/W] - - - 00000	TMCSRCL7 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0 to 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (OCU 2 to 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0 to 1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2 to 3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 00 - - 0000	Reserved			
000244_H to $00027C_H$	Reserved				
000280_H	SCR08 [R/W,W] 00000000	SMR08 [R/W,W] 00000000	SSR08 [R/W,R] 00001000	RDR08/TDR08 [R/W] 00000000	LIN-USART 8
000284_H	ESCR08 [R/W] 00000X00	ECCR08 [R/W,R,W] -00000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000288_H	SCR09 [R/W,W] 00000000	SMR09 [R/W,W] 00000000	SSR09 [R/W,R] 00001000	RDR09/TDR09 [R/W] 00000000	LIN-USART 9
$00028C_H$	ESCR09 [R/W] 00000X00	ECCR09 [R/W,R,W] -00000XX	Reserved		
000290_H	SCR10 [R/W,W] 00000000	SMR10 [R/W,W] 00000000	SSR10 [R/W,R] 00001000	RDR10/TDR10 [R/W] 00000000	LIN-USART 10
000294_H	ESCR10 [R/W] 00000X00	ECCR10 [R/W,R,W] -00000XX	Reserved		
000298_H	SCR11 [R/W,W] 00000000	SMR11 [R/W,W] 00000000	SSR11 [R/W,R] 00001000	RDR11/TDR11 [R/W] 00000000	LIN-USART 11
$00029C_H$	ESCR11 [R/W] 00000X00	ECCR11 [R/W,R,W] -00000XX	Reserved		
$0002A0_H$ to $0002BC_H$	Reserved				
$0002C0_H$	BGR108 [R/W] 00000000	BGR008 [R/W] 00000000	BGR109 [R/W] 00000000	BGR009 [R/W] 00000000	Baudrate Generator LIN-USART 8 to 11
$0002C4_H$	BGR110 [R/W] 00000000	BGR010 [R/W] 00000000	BGR111 [R/W] 00000000	BGR011 [R/W] 00000000	
$0002C8_H$ to $0002CC_H$	Reserved				
$0002D0_H$	Reserved	ICS45 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - -0 - -00 0000 - -00		OCS67 [R/W] - - -0 - -00 0000 - -00		Output Compare 4 to 7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ to $0002EC_H$	Reserved				
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4 to 5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6 to 7)

Address	Register				Block
	+0	+1	+2	+3	
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4 to 5)
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6 to 7)
000300_H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00000000	Reserved	UDCS0 [R/W] 00000000	
000308_H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00000000	Reserved	UDCS1 [R/W] 00000000	
$00030C_H$	Reserved				
000310_H	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2 to 3
000314_H	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00000000	Reserved	UDCS2 [R/W] 00000000	
000318_H	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00000000	Reserved	UDCS3 [R/W] 00000000	
$00031C_H$	Reserved				
000320_H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324_H to $00032C_H$	Reserved				
000330_H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334_H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338_H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
$00033C_H$	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340_H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344_H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348_H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
$00034C_H$	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000368_H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] - - - - - - 00	ITBAL2 [R/W] 00000000	I^2C 2
$00036C_H$	ITMKH2 [R/W] 00 - - - - 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370_H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	Reserved	
000374_H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] - - - - - - 00	ITBAL3 [R/W] 00000000	I^2C 3
000378_H	ITMKH3 [R/W] 00 - - - - 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 0000000	
$00037C_H$	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] - 0011111	Reserved	
000380_H to $00038C_H$	Reserved				
000390_H	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Control Unit
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX – 00	CTBR [W] XXXXXXXX	Clock Control Unit
000484_H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - 00000	PLLDIVN [R/W] - - - 00000	PLLDIVG [R/W] - - - 00000	PLLDIVG [W] 00000000	PLL Clock Gear Unit
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control

Address	Register				Block
	+0	+1	+2	+3	
000498_H	PORTEN [R/W] - - - - - 000	Reserved	PPMUX [R/W] *1 00000000 00000000		Port Input Enable Control / PortMux Control
$00049C_H$	PPMUX2 [R/W] *2 - - 00 0000 - - - - - - - -		Reserved		PortMux Control 2 (CY91F467PA)
$0004A0_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 – 00 – 0		Real Time Clock (Watch Timer)
$0004A4_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration Unit of Sub Oscillation
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulation
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - - 0000 *3	Reserved	Reserved	CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	LV Detection / Hardware-Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilization Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control Main/Sub Regulator Control
000500_H	GCN14 [R/W] 00110010 00010000		Reserved	GCN24 [R/W] - - - - 0000	PPG Control 16 to 19
000504_H	GCN15 [R/W] 00110010 00010000		Reserved	GCN25 [R/W] - - - - 0000	PPG Control 20 to 23
000508_H	GCN16 [R/W] 00110010 00010000		Reserved	GCN26 [R/W] - - - - 0000	PPG Control 24 to 27
$00050C_H$	GCN17 [R/W] 00110010 00010000		Reserved	GCN27 [R/W] - - - - 0000	PPG Control 28 to 31
000510_H	PTMR16 [R] 11111111 11111111		PCSR16 [W] XXXXXXXX XXXXXXXX		PPG 16
000514_H	PDUT16 [W] XXXXXXXX XXXXXXXX		PCNH16 [R/W] 0000000 -	PCNL16 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000518_H	PTMR17 [R] 11111111 11111111		PCSR17 [W] XXXXXXXX XXXXXXXX		PPG 17
$00051C_H$	PDUT17 [W] XXXXXXXX XXXXXXXX		PCNH17 [R/W] 0000000 -	PCNL17 [R/W] 000000 - 0	
000520_H	PTMR18 [R] 11111111 11111111		PCSR18 [W] XXXXXXXX XXXXXXXX		PPG 18
000524_H	PDUT18 [W] XXXXXXXX XXXXXXXX		PCNH18 [R/W] 0000000 -	PCNL18 [R/W] 000000 - 0	
000528_H	PTMR19 [R] 11111111 11111111		PCSR19 [W] XXXXXXXX XXXXXXXX		PPG 19
$00052C_H$	PDUT19 [W] XXXXXXXX XXXXXXXX		PCNH19 [R/W] 0000000 -	PCNL19 [R/W] 000000 - 0	
000530_H	PTMR20 [R] 11111111 11111111		PCSR20 [W] XXXXXXXX XXXXXXXX		PPG 20
000534_H	PDUT20 [W] XXXXXXXX XXXXXXXX		PCNH20 [R/W] 0000000 -	PCNL20 [R/W] 000000 - 0	
000538_H	PTMR21 [R] 11111111 11111111		PCSR21 [W] XXXXXXXX XXXXXXXX		PPG 21
$00053C_H$	PDUT21 [W] XXXXXXXX XXXXXXXX		PCNH21 [R/W] 0000000 -	PCNL21 [R/W] 000000 - 0	
000540_H	PTMR22 [R] 11111111 11111111		PCSR22 [W] XXXXXXXX XXXXXXXX		PPG 22
000544_H	PDUT22 [W] XXXXXXXX XXXXXXXX		PCNH22 [R/W] 0000000 -	PCNL22 [R/W] 000000 - 0	
000548_H	PTMR23 [R] 11111111 11111111		PCSR23 [W] XXXXXXXX XXXXXXXX		PPG 23
$00054C_H$	PDUT23 [W] XXXXXXXX XXXXXXXX		PCNH23 [R/W] 0000000 -	PCNL23 [R/W] 000000 - 0	
000550_H	PTMR24 [R] 11111111 11111111		PCSR24 [W] XXXXXXXX XXXXXXXX		PPG 24
000554_H	PDUT24 [W] XXXXXXXX XXXXXXXX		PCNH24 [R/W] 0000000 -	PCNL24 [R/W] 000000 - 0	
000558_H	PTMR25 [R] 11111111 11111111		PCSR25 [W] XXXXXXXX XXXXXXXX		PPG 25
$00055C_H$	PDUT25 [W] XXXXXXXX XXXXXXXX		PCNH25 [R/W] 0000000 -	PCNL25 [R/W] 000000 - 0	
000560_H	PTMR26 [R] 11111111 11111111		PCSR26 [W] XXXXXXXX XXXXXXXX		PPG 26
000564_H	PDUT26 [W] XXXXXXXX XXXXXXXX		PCNH26 [R/W] 0000000 -	PCNL26 [R/W] 000000 - 0	
000568_H	PTMR27 [R] 11111111 11111111		PCSR27 [W] XXXXXXXX XXXXXXXX		PPG 27
$00056C_H$	PDUT27 [W] XXXXXXXX XXXXXXXX		PCNH27 [R/W] 0000000 -	PCNL27 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000570_H	PTMR28 [R] 11111111 11111111		PCSR28 [W] XXXXXXXX XXXXXXXX		PPG 28
000574_H	PDUT28 [W] XXXXXXXX XXXXXXXX		PCNH28 [R/W] 0000000 -	PCNL28 [R/W] 000000 - 0	
000578_H	PTMR29 [R] 11111111 11111111		PCSR29 [W] XXXXXXXX XXXXXXXX		PPG 29
$00057C_H$	PDUT29 [W] XXXXXXXX XXXXXXXX		PCNH29 [R/W] 0000000 -	PCNL29 [R/W] 000000 - 0	
000580_H	PTMR30 [R] 11111111 11111111		PCSR30 [W] XXXXXXXX XXXXXXXX		PPG 30
000584_H	PDUT30 [W] XXXXXXXX XXXXXXXX		PCNH30 [R/W] 0000000 -	PCNL30 [R/W] 000000 - 0	
000588_H	PTMR31 [R] 11111111 11111111		PCSR31 [W] XXXXXXXX XXXXXXXX		PPG 31
$00058C_H$	PDUT31 [W] XXXXXXXX XXXXXXXX		PCNH31 [R/W] 0000000 -	PCNL31 [R/W] 000000 - 0	
000590_H	TMRLR8 [W] XXXXXXXX XXXXXXXX		TMR8 [R] XXXXXXXX XXXXXXXX		Reload Timer 8 (PPG 16 to 19)
000594_H	Reserved		TMCSRH8 [R/W] - - 000000	TMCSRL8 [R/W] 0 - 000000	
000598_H	TMRLR9 [W] XXXXXXXX XXXXXXXX		TMR9 [R] XXXXXXXX XXXXXXXX		Reload Timer 9 (PPG 16 to 19)
$00059C_H$	Reserved		TMCSRH9 [R/W] - - 000000	TMCSRL9 [R/W] 0 - 000000	
$0005A0_H$	TMRLR10 [W] XXXXXXXX XXXXXXXX		TMR10 [R] XXXXXXXX XXXXXXXX		Reload Timer 10 (PPG 20 to 23)
$0005A4_H$	Reserved		TMCSRH10 [R/W] - - 000000	TMCSRL10 [R/W] 0 - 000000	
$0005A8_H$	TMRLR11 [W] XXXXXXXX XXXXXXXX		TMR11 [R] XXXXXXXX XXXXXXXX		Reload Timer 11 (PPG 20 to 23)
$0005AC_H$	Reserved		TMCSRH11 [R/W] - - 000000	TMCSRL11 [R/W] 0 - 000000	
$0005B0_H$	TMRLR12 [W] XXXXXXXX XXXXXXXX		TMR12 [R] XXXXXXXX XXXXXXXX		Reload Timer 12 (PPG 24 to 27)
$0005B4_H$	Reserved		TMCSRH12 [R/W] - - 000000	TMCSRL12 [R/W] 0 - 000000	
$0005B8_H$	TMRLR13 [W] XXXXXXXX XXXXXXXX		TMR13 [R] XXXXXXXX XXXXXXXX		Reload Timer 13 (PPG 24 to 27)
$0005BC_H$	Reserved		TMCSRH13 [R/W] - - 000000	TMCSRL13 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0005C0_H$	TMRLR14 [W] XXXXXXXX XXXXXXXX		TMR14 [R] XXXXXXXX XXXXXXXX		Reload Timer 14 (PPG 28 to 31)
$0005C4_H$	Reserved		TMCSRH14 [R/W] - - 000000	TMCSRL14 [R/W] 0 - 000000	
$0005C8_H$	TMRLR15 [W] XXXXXXXX XXXXXXXX		TMR15 [R] XXXXXXXX XXXXXXXX		Reload Timer 15 (PPG 28 to 31)
$0005CC_H$	Reserved		TMCSRH15 [R/W] - - 000000	TMCSRL15 [R/W] 0 - 000000	
$0005D0_H$	TMR89 [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Reload Timers 8 + 9
$0005D4_H$	TMR1011 [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Reload Timers 10 + 11
$0005D8_H$	TMR1213 [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Reload Timers 12 + 13
$0005DC_H$	TMR1415 [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Reload Timers 14 + 15
$0005E0_H$	AD1ERH [R/W] 00000000 00000000		AD1ERL [R/W] 00000000 00000000		A/D Converter 1 *4 (CY91F467PA)
$0005E4_H$	AD1CS1 [R/W] 00000000	AD1CS0 [R/W] 00000000	AD1CR1 [R] 000000XX	AD1CR0 [R] XXXXXXXX	
$0005E8_H$	AD1CT1 [R/W] 00010000	AD1CT0 [R/W] 00101100	AD1SCH [R/W] - - - 00000	AD1ECH [R/W] - - - 00000	
$0005EC_H$ to $00063F_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000 *5		External Bus Unit
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01111111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IORW0 [R/W] XXXXXXXX	IORW1 [R/W] XXXXXXXX	IORW2 [R/W] XXXXXXXX	Reserved	
$00067C_H$	Reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *6	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H	RCO0H0 [R/W] 11111111	RCO0L0 [R/W] 0000 0000	RCO0H1 [R/W] 1111111	RCO0L1 [R/W] 0000 0000	A/D Converter 0 Range Comparator *7 (CY91F467PA)
$00068C_H$	RCO0H2 [R/W] 1111111	RCO0L2 [R/W] 0000 0000	RCO0H3 [R/W] 1111111	RCO0L3 [R/W] 0000 0000	
000690_H	RCO0IRS [R/W] 00000000 00000000 00000000 00000000				
000694_H	RCO0OF [R] 00000000 00000000 00000000 00000000				
000698_H	RCO0INT [R/W0] 00000000 00000000 00000000 00000000				
$00069C_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$0006A0_H$	AD0CC0 [R/W] 0000 0000	AD0CC1 [R/W] 0000 0000	AD0CC2 [R/W] 0000 0000	AD0CC3 [R/W] 0000 0000	A/D Converter 0 Channel Control (CY91F467PA)
$0006A4_H$	AD0CC4 [R/W] 0000 0000	AD0CC5 [R/W] 0000 0000	AD0CC6 [R/W] 0000 0000	AD0CC7 [R/W] 0000 0000	
$0006A8_H$	AD0CC8 [R/W] 0000 0000	AD0CC9 [R/W] 0000 0000	AD0CC10 [R/W] 0000 0000	AD0CC11 [R/W] 0000 0000	
$0006AC_H$	AD0CC12 [R/W] 0000 0000	AD0CC13 [R/W] 0000 0000	AD0CC14 [R/W] 0000 0000	AD0CC15 [R/W] 0000 0000	
$0006B0_H$	AD0CS2 [RW] 0000 - - 00	reserved			A/D Converter 0 Control register 2 (CY91F467PA)
$0006B4_H$	RCO1H0 [R/W] 11111111	RCO1L0 [R/W] 0000 0000	RCO1H1 [R/W] 11111111	RCO1L1 [R/W] 0000 0000	A/D Converter 1 Range Comparator (CY91F467PA)
$0006B8_H$	RCO1H2 [R/W] 11111111	RCO1L2 [R/W] 0000 0000	RCO1H3 [R/W] 11111111	RCO1L3 [R/W] 0000 0000	
$0006BC_H$	RCO1IRS [R/W] 00000000 00000000 00000000 00000000				
$0006C0_H$	RCO1OF [R] 00000000 00000000 00000000 00000000				
$0006C4_H$	RCO1INT [R/W0] 00000000 00000000 00000000 00000000				
$0006C8_H$	reserved				
$0006CC_H$	AD1CC0 [R/W] 0000 0000	AD1CC1 [R/W] 0000 0000	AD1CC2 [R/W] 0000 0000	AD1CC3 [R/W] 0000 0000	A/D Converter 1 Channel Control (CY91F467PA)
$0006D0_H$	AD1CC4 [R/W] 0000 0000	AD1CC5 [R/W] 0000 0000	AD1CC6 [R/W] 0000 0000	AD1CC7 [R/W] 0000 0000	
$0006D4_H$	AD1CC8 [R/W] 0000 0000	AD1CC9 [R/W] 0000 0000	AD1CC10 [R/W] 0000 0000	AD1CC11 [R/W] 0000 0000	
$0006D8_H$	AD1CC12 [R/W] 0000 0000	AD1CC13 [R/W] 0000 0000	AD1CC14 [R/W] 0000 0000	AD1CC15 [R/W] 0000 0000	
$0006DC_H$	AD1CS2 [RW] 0000 - - 00	reserved			A/D Converter 1 Control register 2 (CY91F467PA)

Address	Register				Block
	+0	+1	+2	+3	
$0006E0_H$	ADC0D0 [R] ------XX XXXXXXXX		ADC0D1 [R] ------XX XXXXXXXX		A/D Converter 0 Channel Data registers *8 (CY91F467PA)
$0006E4_H$	ADC0D2 [R] ------XX XXXXXXXX		ADC0D3 [R] ------XX XXXXXXXX		
$0006E8_H$	ADC0D4 [R] ------XX XXXXXXXX		ADC0D5 [R] ------XX XXXXXXXX		
$0006EC_H$	ADC0D6 [R] ------XX XXXXXXXX		ADC0D7 [R] ------XX XXXXXXXX		
$0006F0_H$	ADC0D8 [R] ------XX XXXXXXXX		ADC0D9 [R] ------XX XXXXXXXX		
$0006F4_H$	ADC0D10 [R] ------XX XXXXXXXX		ADC0D11 [R] ------XX XXXXXXXX		
$0006F8_H$	ADC0D12 [R] ------XX XXXXXXXX		ADC0D13 [R] ------XX XXXXXXXX		
$0006FC_H$	ADC0D14 [R] ------XX XXXXXXXX		ADC0D015 [R] ------XX XXXXXXXX		
000700_H	ADC0D16 [R] ------XX XXXXXXXX		ADC0D17 [R] ------XX XXXXXXXX		
000704_H	ADC0D18 [R] ------XX XXXXXXXX		ADC0D19 [R] ------XX XXXXXXXX		
000708_H	ADC0D20 [R] ------XX XXXXXXXX		ADC0D21 [R] ------XX XXXXXXXX		
$00070C_H$	ADC0D22 [R] ------XX XXXXXXXX		ADC0D23 [R] ------XX XXXXXXXX		
000710_H	ADC0D24 [R] ------XX XXXXXXXX		ADC0D25 [R] ------XX XXXXXXXX		
000714_H	ADC0D26 [R] ------XX XXXXXXXX		ADC0D27 [R] ------XX XXXXXXXX		
000718_H	ADC0D28 [R] ------XX XXXXXXXX		ADC0D29 [R] ------XX XXXXXXXX		
$00071C_H$	ADC0D30 [R] ------XX XXXXXXXX		ADC0D31 [R] ------XX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
000720_H	ADC1D0 [R] ------XX XXXXXXXX		ADC1D1 [R] ------XX XXXXXXXX		A/D Converter 1 Channel Data registers (CY91F467PA)
000724_H	ADC1D2 [R] ------XX XXXXXXXX		ADC1D3 [R] ------XX XXXXXXXX		
000728_H	ADC1D4 [R] ------XX XXXXXXXX		ADC1D5 [R] ------XX XXXXXXXX		
$00072C_H$	ADC1D6 [R] ------XX XXXXXXXX		ADC1D7 [R] ------XX XXXXXXXX		
000730_H	ADC1D8 [R] ------XX XXXXXXXX		ADC1D9 [R] ------XX XXXXXXXX		
000734_H	ADC1D10 [R] ------XX XXXXXXXX		ADC1D11 [R] ------XX XXXXXXXX		
000738_H	ADC1D12 [R] ------XX XXXXXXXX		ADC1D13 [R] ------XX XXXXXXXX		
$00073C_H$	ADC1D14 [R] ------XX XXXXXXXX		ADC1D015 [R] ------XX XXXXXXXX		
000740_H	ADC1D16 [R] ------XX XXXXXXXX		ADC1D17 [R] ------XX XXXXXXXX		
000744_H	ADC1D18 [R] ------XX XXXXXXXX		ADC1D19 [R] ------XX XXXXXXXX		
000748_H	ADC1D20 [R] ------XX XXXXXXXX		ADC1D21 [R] ------XX XXXXXXXX		
$00074C_H$	ADC1D22 [R] ------XX XXXXXXXX		ADC1D23 [R] ------XX XXXXXXXX		
000750_H	ADC1D24 [R] ------XX XXXXXXXX		ADC1D25 [R] ------XX XXXXXXXX		
000754_H	ADC1D26 [R] ------XX XXXXXXXX		ADC1D27 [R] ------XX XXXXXXXX		
000758_H	ADC1D28 [R] ------XX XXXXXXXX		ADC1D29 [R] ------XX XXXXXXXX		
$00075C_H$	ADC1D30 [R] ------XX XXXXXXXX		ADC1D31 [R] ------XX XXXXXXXX		
000760_H to $0007F8_H$	Reserved				
$0007FC_H$	Reserved	MODR [W] XXXXXXXX	Reserved	Reserved	Mode Register
000800_H to $000BFC_H$	Reserved				
$000C00_H$	reserved			IOS [R/W] *9 ------10	I-Unit
$000C04_H$ to $000CFC_H$	reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved	Reserved	R-bus Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] X - -X - -XX	PDRD09 [R] - - - - - XXX	PDRD10 [R] - - - - X - XX	Reserved	
$000D0C_H$	Reserved	Reserved	PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] XXXX - XXX	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	PDRD25 [R] - - - - - - XX	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	PDRD30 [R] XXXXXXXX	Reserved	
$000D20_H$	PDRD32 [R] X - - - X - - -	PDRD33 [R] X - - - X - - -	PDRD34 [R] XXXXXXXX	PDRD35 [R] XXXXXXXX	
$000D24_H$ to $000D3C_H$	Reserved				
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0 - - 0 - - 00	DDR09 [R/W] - - - - - 000	DDR10 [R/W] - - - - 0 - 00	Reserved	
$000D4C_H$	Reserved	Reserved	DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] 0000 - 000	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	DDR25 [R/W] - - - - - - 00	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	DDR30 [R/W] 00000000	Reserved	
$000D60_H$	DDR32 [R/W] 0 - - - 0 - - -	DDR33 [R/W] 0 - - - 0 - - -	DDR34 [R/W] 00000000	DDR35 [R/W] 00000000	
$000D64_H$ to $000D7C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000D80_H$	PFR00 [R/W] 00000000 *10	PFR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Function Register
$000D84_H$	Reserved	PFR05 [R/W] 00000000	PFR06 [R/W] 00000000	PFR07 [R/W] 00000000	
$000D88_H$	PFR08 [R/W] 0 - - 0- - 00	PFR09 [R/W] - - - - - 000	PFR10 [R/W] - - - - 0 - 00	Reserved	
$000D8C_H$	Reserved	Reserved	PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
$000D90_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - 000 - 000	PFR22 [R/W] 00000000	PFR23 [R/W] 00000000	
$000D98_H$	PFR24 [R/W] 00000000	PFR25 [R/W] - - - - - - 00	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	PFR30 [R/W] 00000000	Reserved	
$000DA0_H$	PFR32 [R/W] 0 - - - 0 - - -	PFR33 [R/W] 0 - - - 0 - - -	PFR34 [R/W] 00000000	PFR35 [R/W] 00000000	
$000DA4_H$ to $000DBC_H$	Reserved				
$000DC0_H$ to $000DC8_H$	Reserved				
$000DCC_H$	Reserved	Reserved	EPFR10 [R/W] - - - - - - - 0	Reserved	R-bus Port Extra Function Register
$000DCC_H$	Reserved	Reserved	EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
$000DD0_H$	EPFR16 [R/W] 0000 - - - -	EPFR17 [R/W] 00000000	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0 - - - 0 - -	
$000DD4_H$	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - 0 - - - 0 - -	Reserved	Reserved	
$000DD8_H$	EPFR24 [R/W] 0000 - - - -	Reserved	EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
$000DDC_H$	Reserved	Reserved	EPFR30 [R/W] 00000000	Reserved	
$000DE0_H$	EPFR32 [R/W] 0 - - - 0 - - -	EPFR33 [R/W] 0 - - - 0 - - -	EPFR34 [R/W] 00000000	EPFR35 [R/W] 00000000	
$000DE4_H$ to $000DFC_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000E00_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Output Drive Select Register
$000E04_H$	Reserved	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
$000E08_H$	PODR08 [R/W] 0 - -0 - - 00	PODR09 [R/W] - - - - - 000	PODR10 [R/W] - - - - 0 - 00	Reserved	
$000E0C_H$	Reserved	Reserved	PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
$000E14_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] 0000 - 000	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
$000E18_H$	PODR24 [R/W] 00000000	PODR25 [R/W] - - - - - - 00	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] 0000000	PODR29 [R/W] 00000000	PODR30 [R/W] 00000000	Reserved	
$000E20_H$	PODR32 [R/W] 0 - - - 0 - - -	PODR33 [R/W] 0 - - - 0 - - -	PODR34 [R/W] 00000000	PODR35 [R/W] 00000000	
$000E24_H$ to $000E3C_H$	Reserved				
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Input Level Select Register
$000E44_H$	Reserved	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 0 - - 0 - - 00	PILR09 [R/W] - - - - - 000	PILR10 [R/W] - - - - 0 - 00	Reserved	
$000E4C_H$	Reserved	Reserved	PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] 0000 - 000	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
$000E58_H$	PILR24 [R/W] 00000000	PILR25 [R/W] - - - - - - 00	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	PILR30 [R/W] 00000000	Reserved	
$000E60_H$	PILR32 [R/W] 0 - - - 0 - - -	PILR33 [R/W] 0 - - - 0 - - -	PILR34 [R/W] 00000000	PILR35 [R/W] 00000000	
$000E64_H$ to $000E7C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Extra Input Level Select Register
$000E84_H$	Reserved	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 0 - - 0 - - 00	EPILR09 [R/W] - - - - - 000	EPILR10 [R/W] - - - - 0 - 00	Reserved	
$000E8C_H$	Reserved	Reserved	EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] 0000 - 000	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
$000E98_H$	EPILR24 [R/W] 00000000	EPILR25 [R/W] - - - - - - 00	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	EPILR30 [R/W] 00000000	Reserved	
$000EA0_H$	EPILR32 [R/W] 0 - - - 0 - - -	EPILR33 [R/W] 0 - - - 0 - - -	EPILR34 [R/W] 00000000	EPILR35 [R/W] 00000000	
$000EA4_H$ to $000EBC_H$	Reserved				
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved	Reserved	R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 0 - - 0 - - 00	PPER09 [R/W] - - - - - 000	PPER10 [R/W] - - - - 0 - 00	Reserved	
$000ECC_H$	Reserved	Reserved	PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] 0000 - 000	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	PPER25 [R/W] - - - - - - 00	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 0000000	PPER29 [R/W] 00000000	PPER30 [R/W] 00000000	Reserved	
$000EE0_H$	PPER32 [R/W] 0 - - - 0 - - -	PPER33 [R/W] 0 - - - 0 - - -	PPER34 [R/W] 00000000	PPER35 [R/W] 00000000	
$000EE4_H$ to $000EFC_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000F00_H$	PPCR00 [R/W] 00000000	PPCR01 [R/W] 00000000	Reserved	Reserved	R-bus Port Pull-Up/Down Control Register
$000F04_H$	Reserved	PPCR05 [R/W] 00000000	PPCR06 [R/W] 00000000	PPCR07 [R/W] 00000000	
$000F08_H$	PPCR08 [R/W] 0 - - 0 - - 00	PPCR09 [R/W] - - - - - 000	PPCR10 [R/W] - - - - 0 - 00	Reserved	
$000F0C_H$	Reserved	Reserved	PPCR14 [R/W] 00000000	PPCR15 [R/W] 00000000	
$000F10_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 000 - 000	PPCR19 [R/W] - 000 - 000	
$000F14_H$	PPCR20 [R/W] - 000 - 000	PPCR21 [R/W] 0000 - 000	PPCR22 [R/W] 00000000	PPCR23 [R/W] 00000000	
$000F18_H$	PPCR24 [R/W] 00000000	PPCR25 [R/W] - - - - - - 00	PPCR26 [R/W] 00000000	PPCR27 [R/W] 00000000	
$000F1C_H$	PPCR28 [R/W] 0000000	PPCR29 [R/W] 00000000	PPCR30 [R/W] 00000000	Reserved	
$000F20_H$	PPCR32 [R/W] 0 - - - 0 - - -	PPCR33 [R/W] 0 - - - 0 - - -	PPCR34 [R/W] 00000000	PPCR35 [R/W] 00000000	
$000F24_H$ to $000FFC_H$	Reserved				
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $001FFC_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
002000_H to $006FFC_H$	CY91F465PA: Flash-cache size is 8 Kbytes : 004000_H to $005FFC_H$ CY91F467PA: Flash-cache size is 8 Kbytes : 004000_H to $005FFC_H$				Flash-cache / I-RAM area
007000_H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ F - Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - - - 00000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - - - 00000 00000000 00000000				
007014_H to $0070FC_H$	Reserved				
007100_H	FSCR0 [R/W, R] 11111111 11111111 11111111 11111111				Flash Security CRC Control register
007104_H	FSCR1 [R , R/W] 0 - - - 0001 00000000 00000000 00000000				
007108_H to 007110_H	Reserved				
007114_H	DFCS [R/W] 0000 000X	DFWC [R/W] - - - 0 0000	DFWS [R/W,R] 0000 0000	reserved	Data Flash Control register
007118_H	DFSCR0 [R/W, R] 11111111 11111111 11111111 11111111				Data Flash Security CRC control
$00711C_H$	DFSCR1 [R , R/W] 0 - - - 0000 00000000 00000000 00000000				
007120_H to $007FFC_H$	Reserved				
008000_H to $00BFFC_H$	CY91F465PA: Boot-ROM size is 4Kbytes: $00B000_H$ to $00BFFC_H$ CY91F467PA: Boot-ROM size is 4Kbytes: $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 waitcycle)				Boot ROM area
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ to $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$ to $00C03C_H$	Reserved				
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ to $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved				
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved				
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved				
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved				
$00C100_H$	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
$00C104_H$	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
$00C108_H$	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
$00C10C_H$	BRPE1 [R/W] 00000000 00000000		Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$00C110_H$	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
$00C114_H$	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
$00C118_H$	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
$00C11C_H$	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
$00C120_H$	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
$00C124_H$	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
$00C128_H$ to $00C12C_H$	Reserved				
$00C130_H$	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
$00C134_H$	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
$00C138_H$ to $00C13C_H$	Reserved				
$00C140_H$	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
$00C144_H$	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
$00C148_H$	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
$00C14C_H$	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
$00C150_H$	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
$00C154_H$	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
$00C158_H$ to $00C15C_H$	Reserved				
$00C160_H$	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
$00C164_H$	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
$00C168_H$ to $00C17C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C180_H$	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
$00C184_H$ to $00C18C_H$	Reserved				
$00C190_H$	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
$00C194_H$ to $00C19C_H$	Reserved				
$00C1A0_H$	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		
$00C1A4_H$ to $00C1AC_H$	Reserved				
$00C1B0_H$	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
$00C1B4_H$ to $00C1FC_H$	Reserved				
$00C200_H$	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
$00C204_H$	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
$00C208_H$	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
$00C20C_H$	BRPE2 [R/W] 00000000 00000000		Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$00C210_H$	IF1CREQ2 [R/W] 00000000 00000001		IF1CMSK2 [R/W] 00000000 00000000		CAN 2 IF 1 Register
$00C214_H$	IF1MSK22 [R/W] 11111111 11111111		IF1MSK12 [R/W] 11111111 11111111		
$00C218_H$	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
$00C21C_H$	IF1MCTR2 [R/W] 00000000 00000000		Reserved		
$00C220_H$	IF1DTA12 [R/W] 00000000 00000000		IF1DTA22 [R/W] 00000000 00000000		
$00C224_H$	IF1DTB12 [R/W] 00000000 00000000		IF1DTB22 [R/W] 00000000 00000000		
$00C228_H$ to $00C22C_H$	Reserved				
$00C230_H$	IF1DTA22 [R/W] 00000000 00000000		IF1DTA12 [R/W] 00000000 00000000		
$00C234_H$	IF1DTB22 [R/W] 00000000 00000000		IF1DTB12 [R/W] 00000000 00000000		
$00C238_H$ to $00C23C_H$	Reserved				
$00C240_H$	IF2CREQ2 [R/W] 00000000 00000001		IF2CMSK2 [R/W] 00000000 00000000		CAN 2 IF 2 Register
$00C244_H$	IF2MSK22 [R/W] 11111111 11111111		IF2MSK12 [R/W] 11111111 11111111		
$00C248_H$	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
$00C24C_H$	IF2MCTR2 [R/W] 00000000 00000000		Reserved		
$00C250_H$	IF2DTA12 [R/W] 00000000 00000000		IF2DTA22 [R/W] 00000000 00000000		
$00C254_H$	IF2DTB12 [R/W] 00000000 00000000		IF2DTB22 [R/W] 00000000 00000000		
$00C258_H$ to $00C25C_H$	Reserved				
$00C260_H$	IF2DTA22 [R/W] 00000000 00000000		IF2DTA12 [R/W] 00000000 00000000		
$00C264_H$	IF2DTB22 [R/W] 00000000 00000000		IF2DTB12 [R/W] 00000000 00000000		
$00C268_H$ to $00C27C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C280_H$	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		CAN 2 Status Flags
$00C284_H$ to $00C28C_H$	Reserved				
$00C290_H$	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
$00C294_H$ to $00C29C_H$	Reserved				
$00C2A0_H$	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
$00C2A4_H$ to $00C2AC_H$	Reserved				
$00C2B0_H$	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		
$00C2B4_H$ to $00C2FC_H$	Reserved				
$00C300_H$	CTRLR3 [R/W] 00000000 00000001		STATR3 [R/W] 00000000 00000000		CAN 3 Control Register (CY91F467PA)
$00C304_H$	ERRCNT3 [R] 00000000 00000000		BTR3 [R/W] 00100011 00000001		
$00C308_H$	INTR3 [R] 00000000 00000000		TESTR3 [R/W] 00000000 X0000000		
$00C30C_H$	BRPE3 [R/W] 00000000 00000000		Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$00C310_H$	IF1CREQ3 [R/W] 00000000 00000001		IF1CMSK3 [R/W] 00000000 00000000		CAN 3 IF 1 Register (CY91F467PA)
$00C314_H$	IF1MSK23 [R/W] 11111111 11111111		IF1MSK13 [R/W] 11111111 11111111		
$00C318_H$	IF1ARB23 [R/W] 00000000 00000000		IF1ARB13 [R/W] 00000000 00000000		
$00C31C_H$	IF1MCTR3 [R/W] 00000000 00000000		Reserved		
$00C320_H$	IF1DTA13 [R/W] 00000000 00000000		IF1DTA23 [R/W] 00000000 00000000		
$00C324_H$	IF1DTB13 [R/W] 00000000 00000000		IF1DTB23 [R/W] 00000000 00000000		
$00C328_H$ to $00C32C_H$	Reserved				
$00C330_H$	IF1DTA23 [R/W] 00000000 00000000		IF1DTA13 [R/W] 00000000 00000000		
$00C334_H$	IF1DTB23 [R/W] 00000000 00000000		IF1DTB13 [R/W] 00000000 00000000		
$00C338_H$ to $00C33C_H$	Reserved				
$00C340_H$	IF2CREQ3 [R/W] 00000000 00000001		IF2CMSK3 [R/W] 00000000 00000000		CAN 3 IF 2 Register (CY91F467PA)
$00C344_H$	IF2MSK23 [R/W] 11111111 11111111		IF2MSK13 [R/W] 11111111 11111111		
$00C348_H$	IF2ARB23 [R/W] 00000000 00000000		IF2ARB13 [R/W] 00000000 00000000		
$00C34C_H$	IF2MCTR3 [R/W] 00000000 00000000		Reserved		
$00C350_H$	IF2DTA13 [R/W] 00000000 00000000		IF2DTA23 [R/W] 00000000 00000000		
$00C354_H$	IF2DTB13 [R/W] 00000000 00000000		IF2DTB23 [R/W] 00000000 00000000		
$00C358_H$ to $00C35C_H$	Reserved				
$00C360_H$	IF2DTA23 [R/W] 00000000 00000000		IF2DTA13 [R/W] 00000000 00000000		
$00C364_H$	IF2DTB23 [R/W] 00000000 00000000		IF2DTB13 [R/W] 00000000 00000000		
$00C368_H$ to $00C37C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00C380_H$	TREQR23 [R] 00000000 00000000		TREQR13 [R] 00000000 00000000		CAN 3 Status Flags (CY91F467PA)
$00C384_H$ to $00C38C_H$	Reserved				
$00C390_H$	NEWDT23 [R] 00000000 00000000		NEWDT13 [R] 00000000 00000000		
$00C394_H$ to $00C39C_H$	Reserved				
$00C3A0_H$	INTPND23 [R] 00000000 00000000		INTPND13 [R] 00000000 00000000		
$00C3A4_H$ to $00C3AC_H$	Reserved				
$00C3B0_H$	MSGVAL23 [R] 00000000 00000000		MSGVAL13 [R] 00000000 00000000		
$00C3B4_H$ to $00EFFC_H$	Reserved				
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--0000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $023FFC_H$	Reserved				
024000_H to $02FFFC_H$	CY91F467PA: D-RAM size is 48Kbytes: 024000_H to $02FFFC_H$ CY91F465PA: D-RAM size is 24Kbytes: $02A000_H$ to $02FFFC_H$ (data access is 0 wait cycles)				D-RAM area
030000_H to $037FFC_H$	CY91F465PA: ID-RAM size is 16Kbytes: 030000_H to $033FFC_H$ CY91F467PA: ID-RAM size is 32Kbytes: 030000_H to $037FFC_H$ (instruction access is 0 waitcycles, data access is 1 wait cycle)				ID-RAM area

1. Writable only once and only as half-word. PPMUX is reset by INIT and RST.
2. PPMUX2 is available on CY91F467PA only. Writable only once and only as half-word, reset by INIT and RST.
3. Depends on the number of available CAN channels:
   CY91F465PA has 3 CAN channels - bits[2:0] exist
   CY91F467PA has 4 CAN channels - bits[3:0] exist

4. ADC1 is only available on CY91F467PA.
5. ACRO[11:10] depends on Modevector fetch information on buswidth.
6. TCR [3:0] INIT value = 0000, keeps value after RST.
7. Range Comparator for ADC0, ADC1 are only available on CY91F467PA.
8. ADC0, ADC1 channel data registers are only available on CY91F467PA.
9. On CY91F467PA, always write 1 to bit IOS[1].
10. PFR initial values for ports 00--10 depend on the selected mode at the modepins MD_0--MD_2:
    internal vector fetch mode (MD=000): PFR00--PFR10 initialized to all '0'
    external vector fetch mode (MD=001): PFR00--PFR10 initialized to all '1'

18.2 Flash Memory, Data Flash and External Bus Area

32bit read/write *1	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000_H to $05FFFC_H$	SA8 (64KB, CY91F467PA) External bus (CY91F465PA)				SA9 (64KB, CY91F467PA) External bus (CY91F465PA)				ROMS0
060000_H to $07FFFC_H$	SA10 (64KB, CY91F467PA) External bus (CY91F465PA)				SA11 (64KB, CY91F467PA) External bus (CY91F465PA)				ROMS1
080000_H to $09FFFC_H$	SA12(64kB)				SA13(64kB)				ROMS2
$0A0000_H$ to $0BFFFC_H$	SA14(64kB)				SA15(64kB)				ROMS3
$0C0000_H$ to $0DFFFC_H$	SA16(64kB)				SA17(64kB)				ROMS4
$0E0000_H$ to $0FFFF4_H$	SA18(64kB)				SA19(64kB)				ROMS5
$0FFFFC_H$	FMV [R] *2 $06\ 00\ 00\ 00_H$				FRV [R] $00\ 00\ BF\ F8_H$				
100000_H to $11FFF8_H$	SA20 (64KB, CY91F467PA) External bus (CY91F465PA)				SA21 (64KB, CY91F467PA) External bus (CY91F465PA)				ROMS6
120000_H to $13FFF8_H$	SA22 (64KB, CY91F467PA) External bus (CY91F465PA)				SA23 (64KB, CY91F467PA) External bus (CY91F465PA)				
140000_H to $143FFC_H$	SA0 (8KB, CY91F467PA) Reserved (CY91F465PA)				SA1 (8KB, CY91F467PA) Reserved (CY91F465PA)				ROMS7
144000_H to $17FFC_H$	SA2 (8KB, CY91F467PA) Reserved (CY91F465PA)				SA3 (8KB, CY91F467PA) Reserved (CY91F465PA)				
148000_H to $14BFFC_H$	SA4(8kB)				SA5(8kB)				
$14C000_H$ to $14FFFC_H$	SA6(8kB)				SA7(8kB)				
150000_H to $17FFFC_H$	Reserved								ROMS7 (continued)

32bit read/write *1	dat[31:0]				dat[31:0]				Block
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000_H to $1BFFFC_H$	External Bus Area								ROMS8
$1C0000_H$ to $1FFFFC_H$									ROMS9
200000_H to $27FFFC_H$									ROMS10
280000_H to $2FFFFC_H$									ROMS11
300000_H to $37FFFC_H$									ROMS12
380000_H to $3FFFFC_H$									ROMS13
400000_H to $47FFFC_H$									ROMS14
480000_H to $4FFFFC_H$									ROMS15
500000_H - $FFFBEFFC_H$	External Bus Area								External Bus
$FFFBF000_H$ - $FFFCFFFC_H$	Data Flash area (if enabled) or External Bus area, Data Flash on CY91F467PA is 64 KB + 256 Byte								Data Flash area *3
$FFFD0000_H$ - $FFFFFFFC_H$	External Bus Area								External bus area

1. 32-bit write to flash memory only available on CY91F467PA.
2. Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read.
3. Data Flash is only available on CY91F467PA.

18.3 Data Flash memory sector organisation

The Data Flash sectors can be accessed only after the data flash has been enabled by setting DFCS:FLASHEN. If the data flash is enabled, the user must ensure that no chip select area overlaps the data flash address space.

	CY91F467PA				
32bit access	**dat[31:0]**				
16bit access	**dat[31:16]**		**dat[15:0]**		
8bit access	**dat[7:0]**	**dat[7:0]**	**dat[7:0]**	**dat[7:0]**	
Address	**+ 0**	**+ 1**	**+ 2**	**+ 3**	**Comments**
... to FFFB EFFC$_H$	External bus area				
FFFB F000$_H$ to FFFB FEFC$_H$	Dummy area for flash auto algorithm addressing (write sequences)				Data Flash
FFFB FF00$_H$ to FFFB FFFC$_H$	SAS (256 Byte) Security Sector				
FFFC 0000$_H$ to FFFC 3FFC$_H$	SA0 (16 KB)				
FFFC 4000$_H$ to FFFC 7FFC$_H$	SA1 (16 KB)				
FFFC 8000$_H$ to FFFC BFFC$_H$	SA2 (16 KB)				
FFFC C000$_H$ to FFFC FFFC$_H$	SA3 (16 KB)				
FFFD 0000$_H$ to FFFF FFFC$_H$	External bus area				

19. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	000FFFFC	—
Mode vector	1	01	—	—	$3F8_H$	000FFFF8	—
System reserved	2	02	—	—	$3F4_H$	000FFFF4	—
System reserved	3	03	—	—	$3F0_H$	000FFFF0	—
System reserved	4	04	—	—	$3EC_H$	000FFFEC	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	$3E8_H$	000FFFE8	—
Memory Protection exception *5	6	06	—	—	$3E4_H$	000FFFE4	—
System reserved	7	07	—	—	$3E0_H$	000FFFE0	—
System reserved	8	08	—	—	$3DC_H$	000FFFDC	—
System reserved	9	09	—	—	$3D8_H$	000FFFD8	—
System reserved	10	0A	—	—	$3D4_H$	000FFFD4	—
System reserved	11	0B	—	—	$3D0_H$	000FFFD0	—
System reserved	12	0C	—	—	$3CC_H$	000FFFCC	—
System reserved	13	0D	—	—	$3C8_H$	000FFFC8	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	000FFFC4	—
NMI request	15	0F	F_H fixed		$3C0_H$	000FFFC0	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	000FFFBC	0, 16
External Interrupt 1	17	11			$3B8_H$	000FFFB8	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	000FFFB4	2, 18
External Interrupt 3	19	13			$3B0_H$	000FFFB0	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	000FFFAC	20
External Interrupt 5	21	15			$3A8_H$	000FFFA8	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	000FFFA4	22
External Interrupt 7	23	17			$3A0_H$	000FFFA0	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	000FFF9C	—
External Interrupt 9	25	19			398_H	000FFF98	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	000FFF94	—
External Interrupt 11	27	1B			390_H	000FFF90	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	000FFF8C	—
External Interrupt 13	29	1D			388_H	000FFF88	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	000FFF84	—
External Interrupt 15	31	1F			380_H	000FFF80	—
Reload Timer 0 Reload Timer 8	32	20	ICR08	448_H	$37C_H$	000FFF7C	4, 32 128
Reload Timer 1 Reload Timer 9	33	21			378_H	000FFF78	5, 33 129

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reload Timer 2 Reload Timer 10	34	22	ICR09	449_H	374_H	000FFF74	34 130
Reload Timer 3 Reload Timer 11	35	23			370_H	000FFF70	35 131
Reload Timer 4 Reload Timer 12	36	24	ICR10	$44A_H$	$36C_H$	000FFF6C	36 132
Reload Timer 5 Reload Timer 13	37	25			368_H	000FFF68	37 133
Reload Timer 6 Reload Timer 14	38	26	ICR11	$44B_H$	364_H	000FFF64	38 134
Reload Timer 7 Reload Timer 15	39	27			360_H	000FFF60	39 135
Free Run Timer 0	40	28	ICR12	$44C_H$	$35C_H$	000FFF5C	40
Free Run Timer 1	41	29			358_H	000FFF58	41
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	000FFF54	42
Free Run Timer 3	43	2B			350_H	000FFF50	43
Free Run Timer 4	44	2C	ICR14	$44E_H$	$34C_H$	000FFF4C	44
Free Run Timer 5	45	2D			348_H	000FFF48	45
Free Run Timer 6	46	2E	ICR15	$44F_H$	344_H	000FFF44	46
Free Run Timer 7	47	2F			340_H	000FFF40	47
CAN 0	48	30	ICR16	450_H	$33C_H$	000FFF3C	—
CAN 1	49	31			338_H	000FFF38	—
CAN 2	50	32	ICR17	451_H	334_H	000FFF34	—
CAN 3 *6	51	33			330_H	000FFF30	—
Reserved	52	34	ICR18	452_H	$32C_H$	000FFF2C	—
Reserved	53	35			328_H	000FFF28	—
LIN-USART 0 RX	54	36	ICR19	453_H	324_H	000FFF24	6, 48
LIN-USART 0 TX	55	37			320_H	000FFF20	7, 49
LIN-USART 1 RX	56	38	ICR20	454_H	$31C_H$	000FFF1C	8, 50
LIN-USART 1 TX	57	39			318_H	000FFF18	9, 51
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	000FFF14	52
LIN-USART 2 TX	59	3B			310_H	000FFF10	53
LIN-USART 3 RX	60	3C	ICR22	456_H	$30C_H$	000FFF0C	54
LIN-USART 3 TX	61	3D			308_H	000FFF08	55
System reserved	62	3E	ICR23 *3	457_H	304_H	000FFF04	—
Delayed Interrupt	63	3F			300_H	000FFF00	—
System reserved *4	64	40	(ICR24)	(458_H)	$2FC_H$	000FFEFC	—
System reserved *4	65	41			$2F8_H$	000FFEF8	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	000FFEF4	10, 56
LIN-USART (FIFO) 4 TX	67	43			$2F0_H$	000FFEF0	11, 57

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
LIN-USART (FIFO) 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	000FFEEC	12, 58
LIN-USART (FIFO) 5 TX	69	45			$2E8_H$	000FFEE8	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	000FFEE4	60
LIN-USART (FIFO) 6 TX	71	47			$2E0_H$	000FFEE0	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	$45C_H$	$2DC_H$	000FFEDC	62
LIN-USART (FIFO) 7 TX	73	49			$2D8_H$	000FFED8	63
I^2C 0 / I^2C 2	74	4A	ICR29	$45D_H$	$2D4_H$	000FFED4	—
I^2C 1 / I^2C 3	75	4B			$2D0_H$	000FFED0	—
LIN-USART 8 RX	76	4C	ICR30	$45E_H$	$2CC_H$	000FFECC	64
LIN-USART 8 TX	77	4D			$2C8_H$	000FFEC8	65
LIN-USART 9 RX	78	4E	ICR31	$45F_H$	$2C4_H$	000FFEC4	66
LIN-USART 9 TX	79	4F			$2C0_H$	000FFEC0	67
LIN-USART 10 RX	80	50	ICR32	460_H	$2BC_H$	000FFEBC	68
LIN-USART 10 TX	81	51			$2B8_H$	000FFEB8	69
LIN-USART 11 RX	82	52	ICR33	461_H	$2B4_H$	000FFEB4	70
LIN-USART 11 TX	83	53			$2B0_H$	000FFEB0	71
Reserved	84	54	ICR34	462_H	$2AC_H$	000FFEAC	72
Reserved	85	55			$2A8_H$	000FFEA8	73
Reserved	86	56	ICR35	463_H	$2A4_H$	000FFEA4	74
Reserved	87	57			$2A0_H$	000FFEA0	75
Reserved	88	58	ICR36	464_H	$29C_H$	000FFE9C	76
Reserved	89	59			298_H	000FFE98	77
Reserved	90	5A	ICR37	465_H	294_H	000FFE94	78
Reserved	91	5B			290_H	000FFE90	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	000FFE8C	80
Input Capture 1	93	5D			288_H	000FFE88	81
Input Capture 2	94	5E	ICR39	467_H	284_H	000FFE84	82
Input Capture 3	95	5F			280_H	000FFE80	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	000FFE7C	84
Input Capture 5	97	61			278_H	000FFE78	85
Input Capture 6	98	62	ICR41	469_H	274_H	000FFE74	86
Input Capture 7	99	63			270_H	000FFE70	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	000FFE6C	88
Output Compare 1	101	65			268_H	000FFE68	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	000FFE64	90
Output Compare 3	103	67			260_H	000FFE60	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	000FFE5C	92
Output Compare 5	105	69			258_H	000FFE58	93

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	000FFE54	94
Output Compare 7	107	6B			250_H	000FFE50	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	000FFE4C	—
Phase Frequency Modulator	109	6D			248_H	000FFE48	—
System reserved	110	6E	ICR47 *3	$46F_H$	244_H	000FFE44	—
System reserved	111	6F			240_H	000FFE40	—
PPG0 PPG16	112	70	ICR48	470_H	$23C_H$	000FFE3C	15, 96 144
PPG1 PPG17	113	71			238_H	000FFE38	97 145
PPG2 PPG18	114	72	ICR49	471_H	234_H	000FFE34	98 146
PPG3 PPG19	115	73			230_H	000FFE30	99 147
PPG4 PPG20	116	74	ICR50	472_H	$22C_H$	000FFE2C	100 148
PPG5 PPG21	117	75			228_H	000FFE28	101 149
PPG6 PPG22	118	76	ICR51	473_H	224_H	000FFE24	102 150
PPG7 PPG23	119	77			220_H	000FFE20	103 151
PPG8 PPG24	120	78	ICR52	474_H	$21C_H$	000FFE1C	104 152
PPG9 PPG25	121	79			218_H	000FFE18	105 153
PPG10 PPG26	122	7A	ICR53	475_H	214_H	000FFE14	106 154
PPG11 PPG27	123	7B			210_H	000FFE10	107 155
PPG12 PPG28	124	7C	ICR54	476_H	$20C_H$	000FFE0C	108 156
PPG13 PPG29	125	7D			208_H	000FFE08	109 157
PPG14 PPG30	126	7E	ICR55	477_H	204_H	000FFE04	110 158
PPG15 PPG31	127	7F			200_H	000FFE00	111 159
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	000FFDFC	—
Up/Down Counter 1	129	81			$1F8_H$	000FFDF8	—
Up/Down Counter 2	130	82	ICR57	479_H	$1F4_H$	000FFDF4	—
Up/Down Counter 3	131	83			$1F0_H$	000FFDF0	—

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	000FFDEC	—
Calibration Unit	133	85			$1E8_H$	000FFDE8	—
A/D Converter 0 A/D Converter 0 End of Scan *6	134	86	ICR59	$47B_H$	$1E4_H$	000FFDE4	14, 112 120 *6
A/D Converter 1 *6 A/D Converter 1 End of Scan *6	135	87			$1E0_H$	000FFDE0	113 *6 121 *6
Reserved	136	88	ICR60	$47C_H$	$1DC_H$	000FFDDC	—
Reserved	137	89			$1D8_H$	000FFDD8	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	000FFDD4	—
Reserved	139	8B			$1D0_H$	000FFDD0	—
Timebase Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	000FFDCC	—
PLL Clock Gear Data Flash Write Complete *6	141	8D			$1C8_H$	000FFDC8	— 195 *6
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	000FFDC4	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	000FFDC0	—
Security vector	144	90	—	—	$1BC_H$	000FFDBC	—
Used by the INT instruction	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	000FFDB8 to 000FFC00	—

Notes:

*1 The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$). The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.

*3 ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])

*4 Used by REALOS

*5 Memory Protection Unit (MPU) support

*6 CAN 3, Data Flash, ADC1 and ADC0 (End of Scan) interrupts are available on CY91F467PA only.

20. Recommended Settings

20.1 PLL and Clockgear settings

Please note that for CY91F465PA the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

20.2 Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	88	79.5	98.5
1	3	026F	84	76.1	93.8
1	3	026F	80	72.6	89.1
1	5	02AE	80	68.7	95.8
2	3	046E	80	68.7	95.8
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
1	7	02ED	76	62	98.1
2	3	046E	76	65.3	90.8
3	3	066D	76	62	98.1
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
3	3	066D	72	58.8	92.7
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
1	11	036B	64	47.6	97.6
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1
5	3	0A6B	64	47.6	97.6
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
1	11	036B	60	44.7	91.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
3	5	06AA	56	39.9	93.8
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
6	3	0C6A	56	39.9	93.8
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
1	15	03E9	52	35.5	96.9
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
7	3	0E69	52	35.5	96.9
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
2	9	0528	44	28.9	92.1
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
8	3	1068	44	28.9	92.1
1	3	026F	40	37	43.6
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
9	3	1267	40	25.3	95.8
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

21. Electrical Characteristics

21.1 Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	$V_{DD}5R$	− 0.3	+ 6.0	V	
Power supply voltage 2*1	$V_{DD}5$	− 0.3	+ 6.0	V	
Power supply voltage 3*1	$V_{DD}35$	− 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	At least one of the pins P07, P16, P20, P24, or P29 (ANn) is used as digital input or output.
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	All pins of the ports P07, P16, P20, P24, or P29 (ANn) follow the condition of V_{IA}
Analog power supply voltage*1	$AV_{CC}5$	− 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH	− 0.3	+ 6.0	V	*2
Input voltage 1*1	V_{I1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Input voltage 2*1	V_{I2}	Vss5 − 0.3	$V_{DD}35$ + 0.3	V	External bus
Analog pin input voltage*1	V_{IA}	AVss5 − 0.3	AVcc5 + 0.3	V	
Output voltage 1*1	V_{O1}	Vss5 − 0.3	$V_{DD}5$ + 0.3	V	
Output voltage 2*1	V_{O2}	Vss5 − 0.3	$V_{DD}35$ + 0.3	V	External bus
Maximum clamp current	I_{CLAMP}	− 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
“L” level maximum output current*4	I_{OL}	—	10	mA	
“L” level average output current*5	I_{OLAV}	—	8	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current*6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current*4	I_{OH}	—	− 10	mA	
“H” level average output current*5	I_{OHAV}	—	− 4	mA	
“H” level total maximum output current	ΣI_{OH}	—	− 100	mA	
“H” level total average output current*6	ΣI_{OHAV}	—	− 25	mA	
Permitted operating frequency	$f_{max, CLKB}$	—	100	MHz	$T_A \leq 105$ °C
	$f_{max, CLKP}$	—	50		
	$f_{max, CLKT}$	—	50		
	$f_{max, CLKCAN}$	—	50		

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted operating frequency	$f_{max, CLKB}$	—	96	MHz	$T_A \leq 125$ °C
	$f_{max, CLKP}$	—	48		
	$f_{max, CLKT}$	—	48		
	$f_{max, CLKCAN}$	—	48		
Permitted power dissipation *7	P_D	—	1250 *8	mW	$T_A \leq 85$ °C
		—	630 *8	mW	$T_A \leq 105$ °C
		—	1400 *8	mW	$T_A \leq 105$ °C, no Flash program/erase *9
		—	1100 *8	mW	$T_A \leq 115$ °C, no Flash program/erase *9
		—	780 *8	mW	$T_A \leq 125$ °C, no Flash program/erase *9
Operating temperature	T_A	− 40	+ 125	°C	
Storage temperature	Tstg	− 55	+ 150	°C	

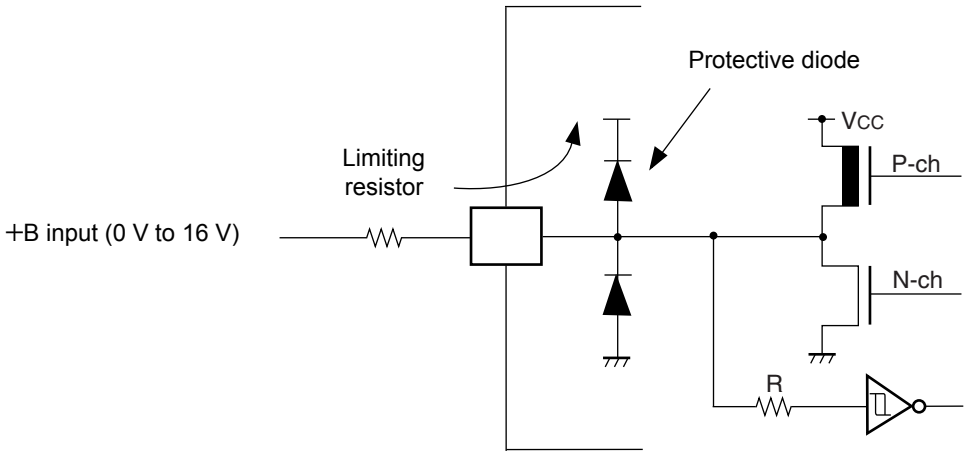
*1 : The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.

*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5$ + 0.3 V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

- Do not leave +B input pins open.
- Example of recommended circuit :

Input/output equivalent circuit



*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

*7 : The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.

The actual power dissipation depends on the customer application and can be calculated as follows:

$P_D = P_{IO} + P_{INT}$

$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} + I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)

$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * I_A + AVRH5 * I_R$ (internal power dissipation)

*8 : Worst case value for the QFP package mounted on a 4-layer PCB at specified T_A without air flow.

*9 : Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

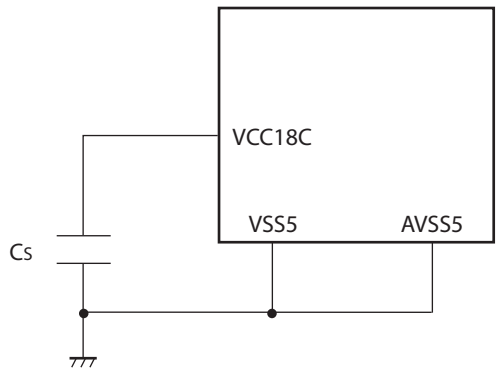
21.2 Recommended operating conditions

($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$V_{DD}35$	3.0	—	5.5	V	External bus
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kΩ $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	$VDD_{CORE} \geq 1.65V$

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
Users considering application outside the listed conditions are advised to contact their representatives beforehand.



21.3 DC characteristics

Note: In the following tables, "V_{DD}" means $V_{DD}35$ for pins of ext. bus or $V_{DD}5$ for other pins.
In the following tables, "V_{SS}" means ground Pins $V_{SS}5$ for the other pins.
($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				$0.74 \times V_{DD}$	—	$V_{DD} + 0.3$	V	3 V ≤ V_{DD} < 4.5 V
		—	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
		—	Port inputs if TTL input is selected	2.0	—	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_2 to MD_0	—	$V_{DD} - 0.3$	—	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{DD}$	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				$V_{SS} - 0.3$	—	$0.46 \times V_{DD}$	V	3 V ≤ V_{DD} < 4.5 V
		—	Port inputs if TTL input is selected	$V_{SS} - 0.3$	—	0.8	V	
	V_{ILR}	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_2 to MD_0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	$V_{SS} - 0.3$	—	0.5	V	External clock in "Oscillation mode"

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	V_{SS} − 0.3	—	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 2mA	V_{DD} − 0.5	—	—	V	Driving strength set to 2 mA
			3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = − 1.6mA					
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 5mA	V_{DD} − 0.5	—	—	V	Driving strength set to 5 mA
			3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = − 3mA					
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = − 3mA	V_{DD} − 0.5	—	—	V	
Output “L” voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 2mA	—	—	0.4	V	Driving strength set to 2 mA
			3.0V ≤ V_{DD} ≤ 4.5V, I_{OL} = + 1.6mA					
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 5mA	—	—	0.4	V	Driving strength set to 5 mA
			3.0V ≤ V_{DD} ≤ 4.5V, I_{OL} = + 3mA					
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OL} = + 3mA	—	—	0.4	V	
Input leakage current	I_{IL}	Pnn_m *1	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	− 1	—	+ 1	µA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	− 3	—	+ 3		
Analog input leakage current	I_{AIN}	ANn *2	3.0V ≤ V_{DD} ≤ 5.5V T_A=25 °C	− 1	—	+ 1	µA	
			3.0V ≤ V_{DD} ≤ 5.5V T_A=125 °C	− 3	—	+ 3	µA	
Pull-up resistance	R_{UP}	Pnn_m* 3, INITX	3.0V ≤V_{DD} ≤3.6V	40	100	160	kΩ	
			4.5V ≤V_{DD} ≤5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m* 4	3.0V ≤V_{DD} ≤3.6V	40	100	180	kΩ	
			4.5V ≤V_{DD} ≤5.5V	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	-	5	15	pF	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current CY91-F465PA	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	-	30	150	µA	At stop mode *5
			T_A = + 105 °C	-	0.3	2.0	mA	
			T_A = + 125 °C	-	0.75	5.0	mA	
			T_A = + 25 °C	-	100	500	µA	RTC : 4 MHz mode *5
			T_A = + 105 °C	-	0.5	2.4	mA	
			T_A = + 125 °C	-	0.85	5.4	mA	
			T_A = + 25 °C	-	50	250	µA	RTC : 100 kHz mode *5
			T_A = + 105 °C	-	0.4	2.2	mA	
			T_A = + 125 °C	-	0.8	5.2	mA	
	I_{LVE}	$V_{DD}5$	—	—	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)
Power supply current CY91-F467PA *6	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	130	160	mA	Code fetch from Flash, Data Flash enabled
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	-	30	150	µA	At stop mode *7
			T_A = + 105 °C	-	0.3	2.0	mA	
			T_A = + 125 °C	-	0.75	5.0	mA	
			T_A = + 25 °C	-	100	500	µA	RTC : 4 MHz mode
			T_A = + 105 °C	-	0.5	2.4	mA	
			T_A = + 125 °C	-	0.85	5.4	mA	
			T_A = + 25 °C	-	50	250	µA	RTC : 100 kHz mode
			T_A = + 105 °C	-	0.4	2.2	mA	
			T_A = + 125 °C	-	0.8	5.2	mA	
	I_{LVE}	$V_{DD}5$	—	—	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)

1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
2. ANn includes all pins where AN channels are enabled.
3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.

4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.
6. CY91F467PA target data
7. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

21.4 A/D converter characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	− 3	—	+ 3	LSB	
Nonlinearity error	—	—	− 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	− 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL−1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRH−3.5 LSB	AVRH−1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}	—	0.6	—	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤5.5
			2.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	− 1	—	+ 1	µA	T_A = + 25 °C
			− 3	—	+ 3	µA	T_A = + 125 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	$0.75 \times AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5 \times 0.25$	V	
Power supply current per ADC macro *3	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current per ADC macro *3	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*3 : The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation

$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11pF \times 7$; for $4.5V \leq AV_{CC}5 \leq 5.5V$

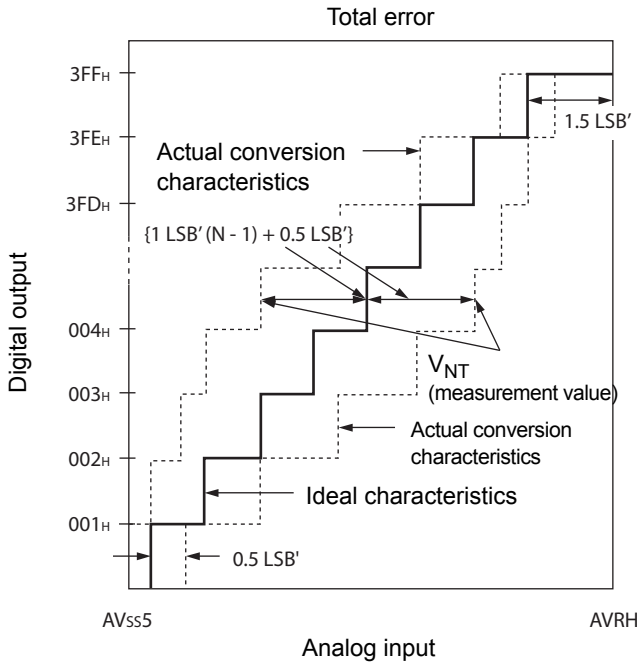
$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11pF \times 7$; for $3.0V \leq AV_{CC}5 \leq 4.5V$

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Nonlinearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).
- Differential nonlinearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



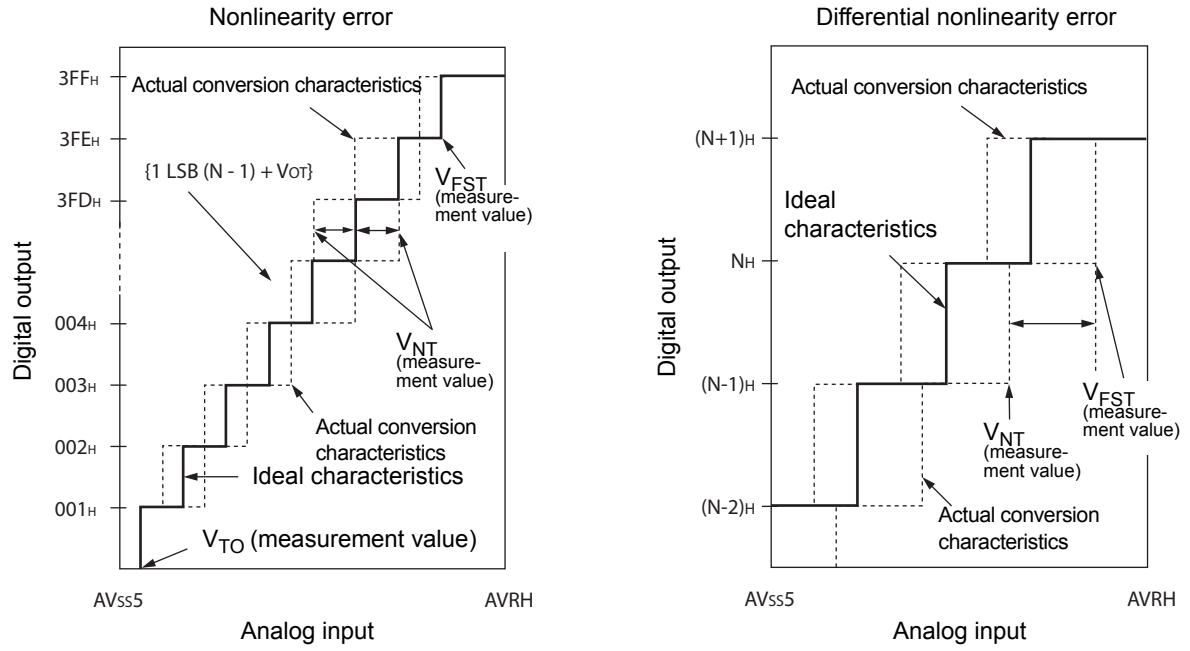
$$1LSB' \text{ (ideal value)} = \frac{AVRH - AV_{SS}5}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
V_{FST}' (ideal value) = AVRH − 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

21.5 FLASH memory program/erase characteristics

21.5.1 CY91F465PA

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

21.5.2 CY91F467PA

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16 or 32-bit width) programming time	-	6	100	µs	System overhead time not included
Program/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

21.5.3 CY91F467PA DATA FLASH

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, T_A = -40 °C to + 105 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
	-	0.8	3.6	s	Erasure programming time is included
Bye programming time	-	15	100	µs	System overhead time not included
Word programming time (32bit width command sequencer write *1)	-	63	403	µs	System overhead time is included CLKB = 64 MHz
Program/Erase cycle	100 000			cycle	at Tj=<105 °C / 10,000 cycle at Tj>105 °C

1. The time from CPU write access until the interrupt flag DFWS:FININT is set.
   It includes 4 byte programming times + 180 CLKB cycles for write sequence, RDY polling and result verification done by the command sequencer. Does not include the interrupt latency time of the CPU.

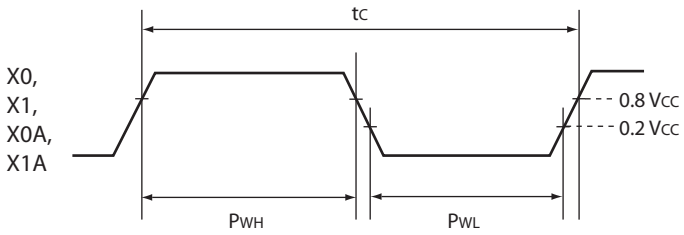
21.6 AC characteristics

21.6.1 Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

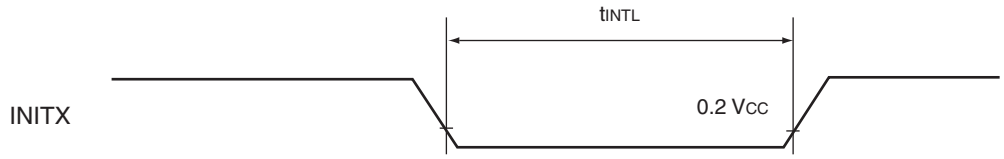
Clock timing condition



21.6.2 Reset input ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



21.6.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements

  All AC tests were measured under the following conditions:

  - IO_{drive} = 5 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - T_a = -40 ·C to +125 ·C
  - C_l = 50 pF (load capacity value of pins when testing)
  - VOL = 0.2 x $V_{DD}5$
  - VOH = 0.8 x $V_{DD}5$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

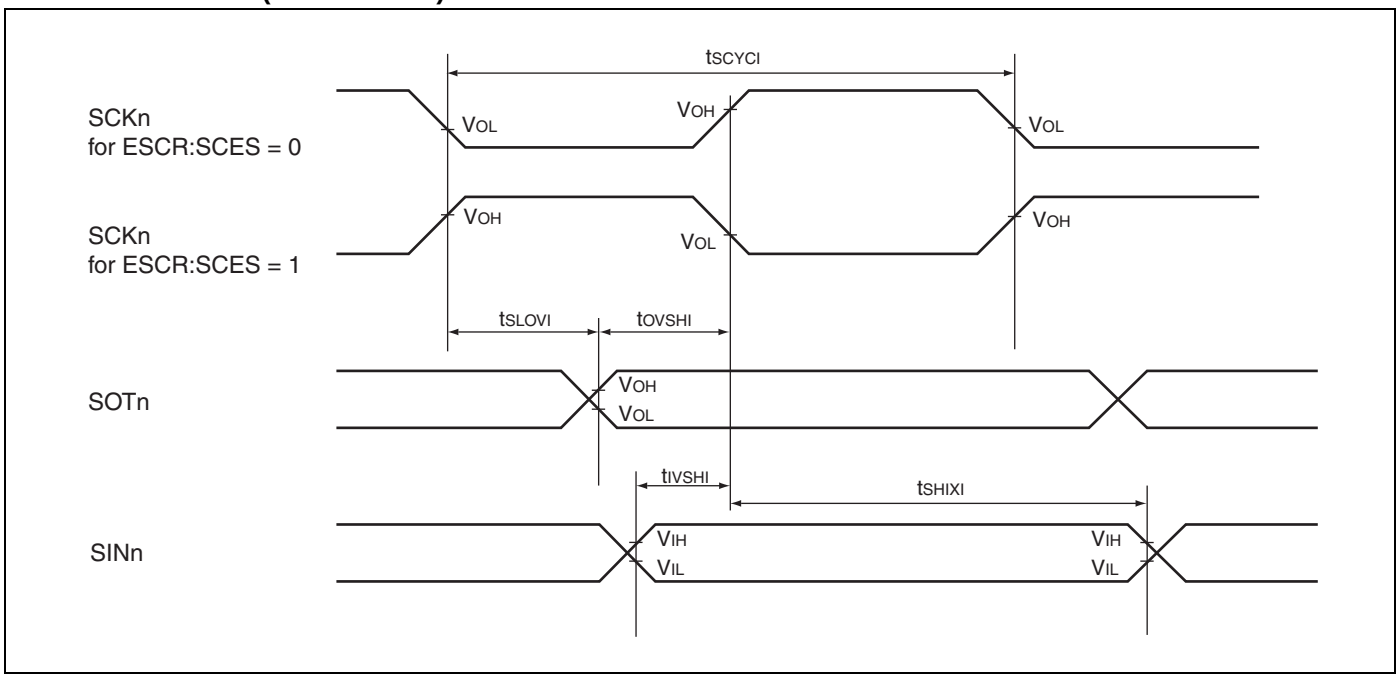
Parameter	Symbol	Pin name	Condition	$V_{DD}5 = 3.0$ V to 4.5 V		$V_{DD}5 = 4.5$ V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		− 30	30	− 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} − 30*	—	m × t_{CLKP} − 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :

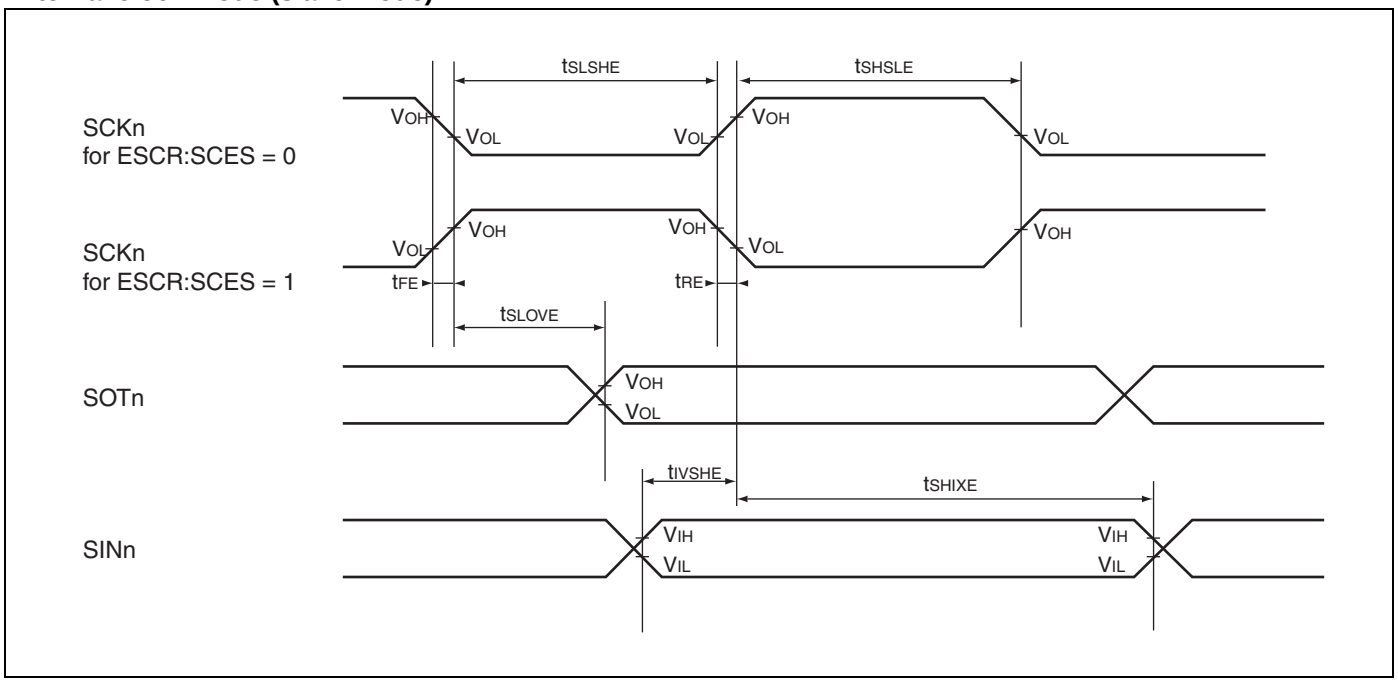
- if $t_{SCYCI} = 2*k*t_{CLKP}$, then m = k, where k is an integer > 2
- if $t_{SCYCI} = (2*k + 1)*t_{CLKP}$, then m = k + 1, where k is an integer > 1

Notes :
- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

Internal clock mode (master mode)



External clock mode (slave mode)



21.6.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements

  All AC tests were measured under the following conditions:

  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = −40 °C to + 125 °C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

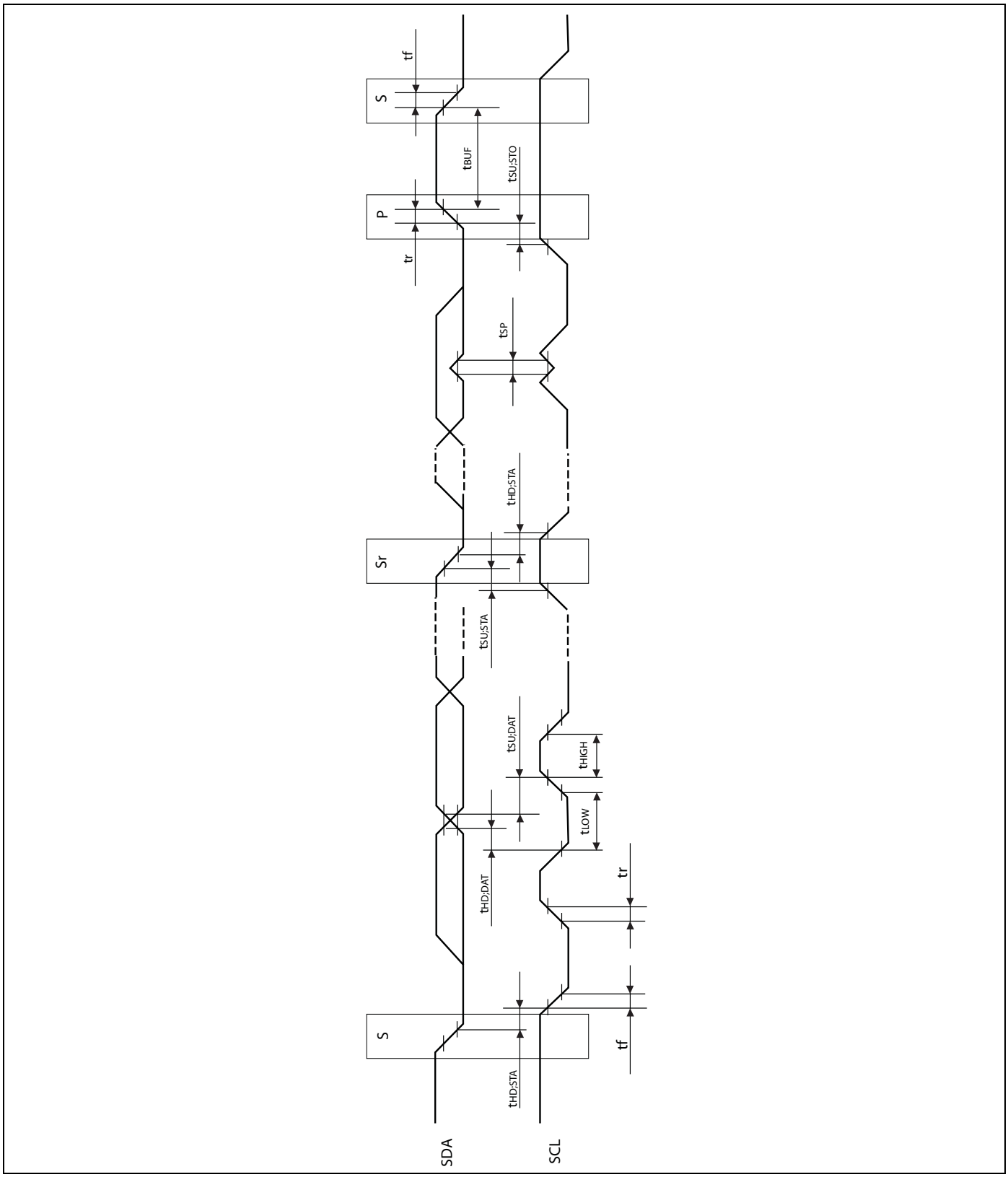
Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = −40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1C_b	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1C_b	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1: The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

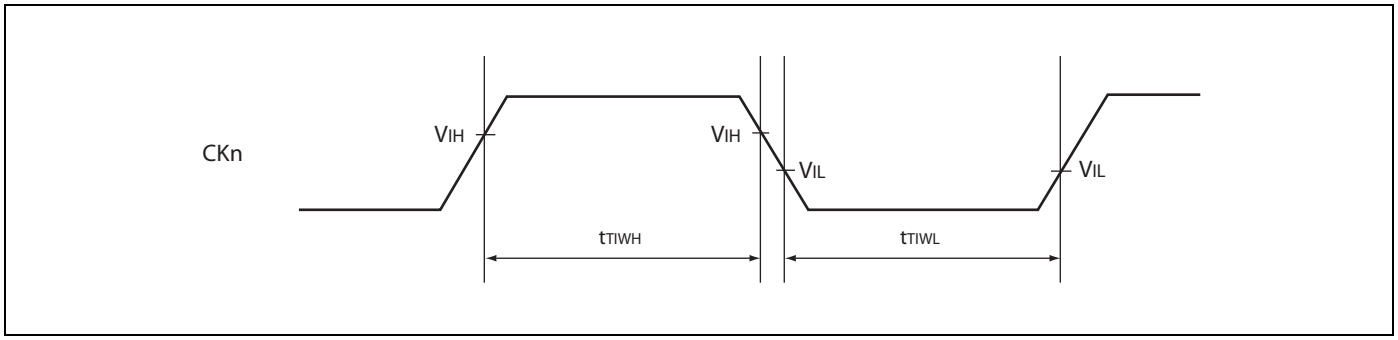

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
tf
S
tHD;STA
SDA
SCL

21.6.5 Free-run timer clock

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

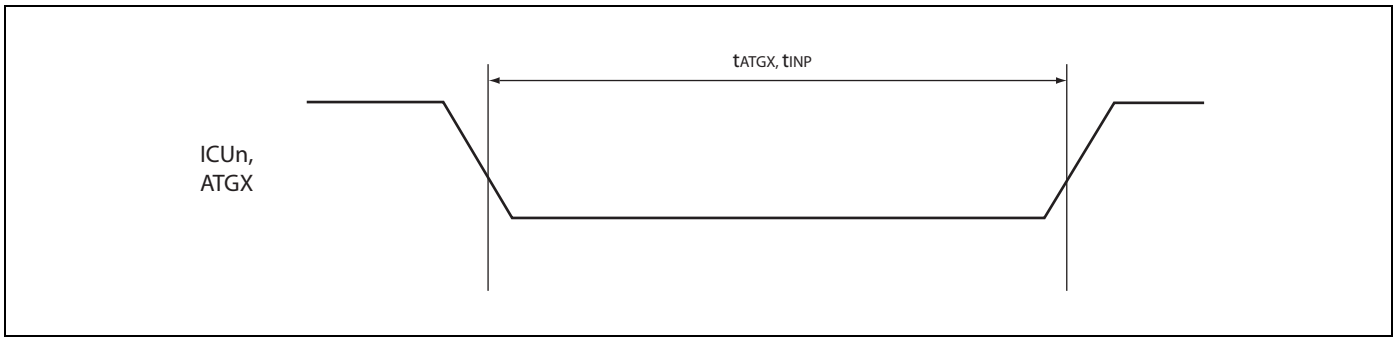


21.6.6 Trigger input timing

($V_{DD}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.



21.6.7 External Bus AC Timings at $V_{DD}35$ = 4.5 to 5.5 V

- Conditions during AC measurements

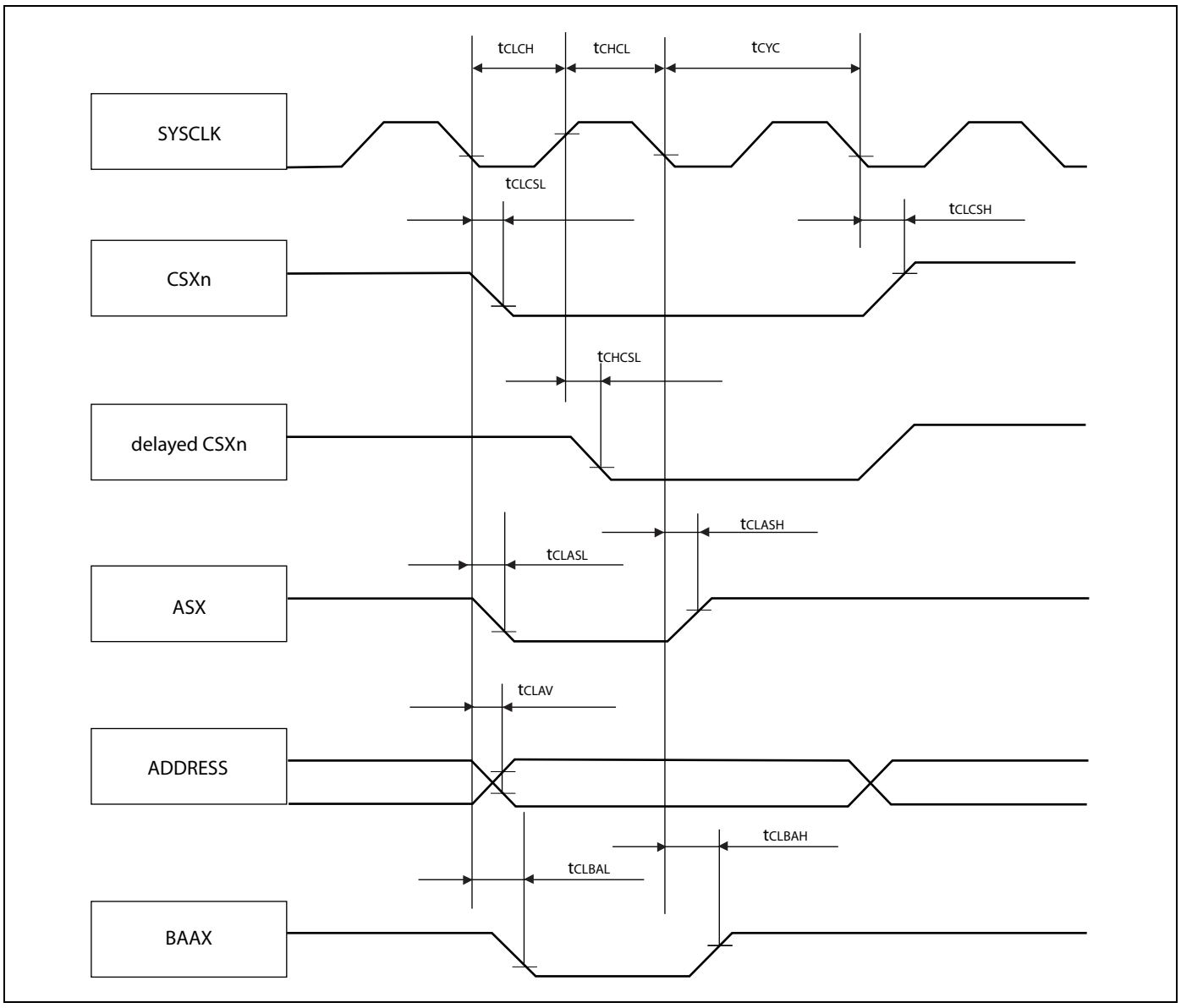
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 5 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40 °C to + 125 °C
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$
  - VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

Basic Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 × t_{CLKT} − 4	1/2 × t_{CLKT} + 2	ns
	t_{CHCL}		1/2 × t_{CLKT} − 2	1/2 × t_{CLKT} + 4	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	12	ns
	t_{CLCSH}		—	9	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		3	8	ns
SYSCLK ↓ to ASX delay time	t_{CLASL}	SYSCLK ASX	—	13	ns
	t_{CLASH}		—	12	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A23 to A0	—	13	ns

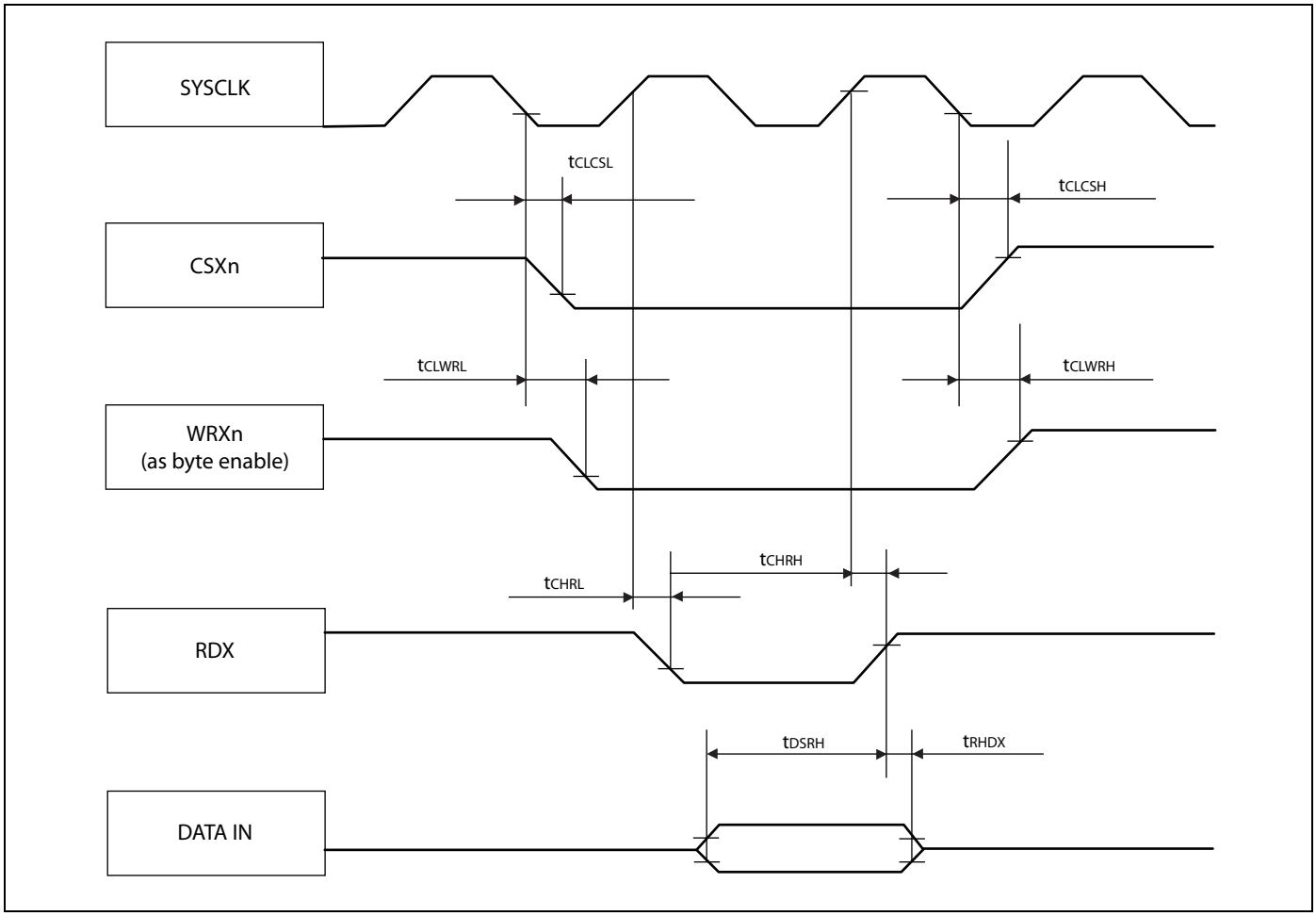
Note : t_{CLKT} is the cycle time of the external bus clock.


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous read access

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

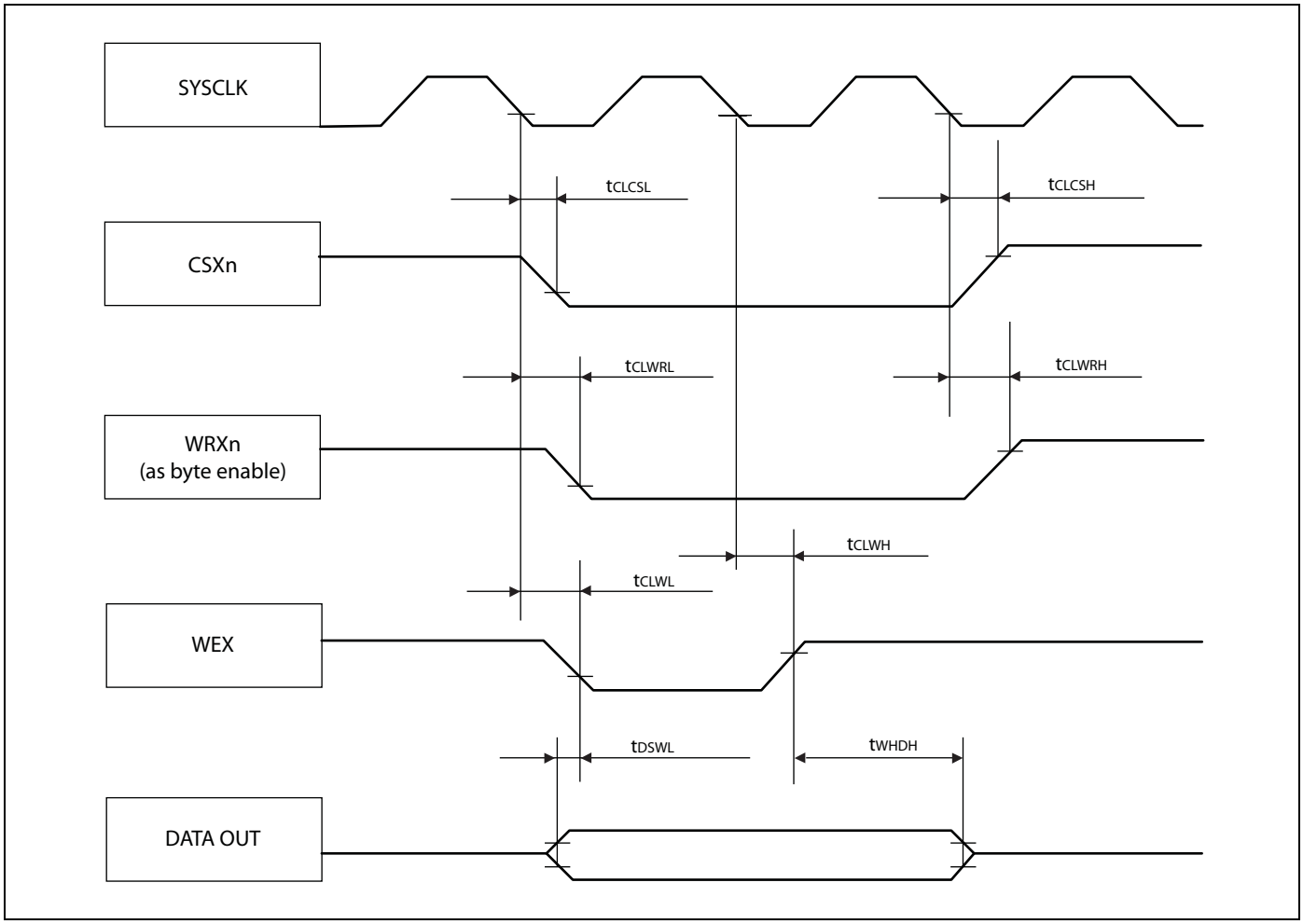
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	2	7	ns
	TCHRH		2	9	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	20	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	12	ns
	TCLWRH		3	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	12	ns
	TCLCSH		—	9	ns



Synchronous write access - byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

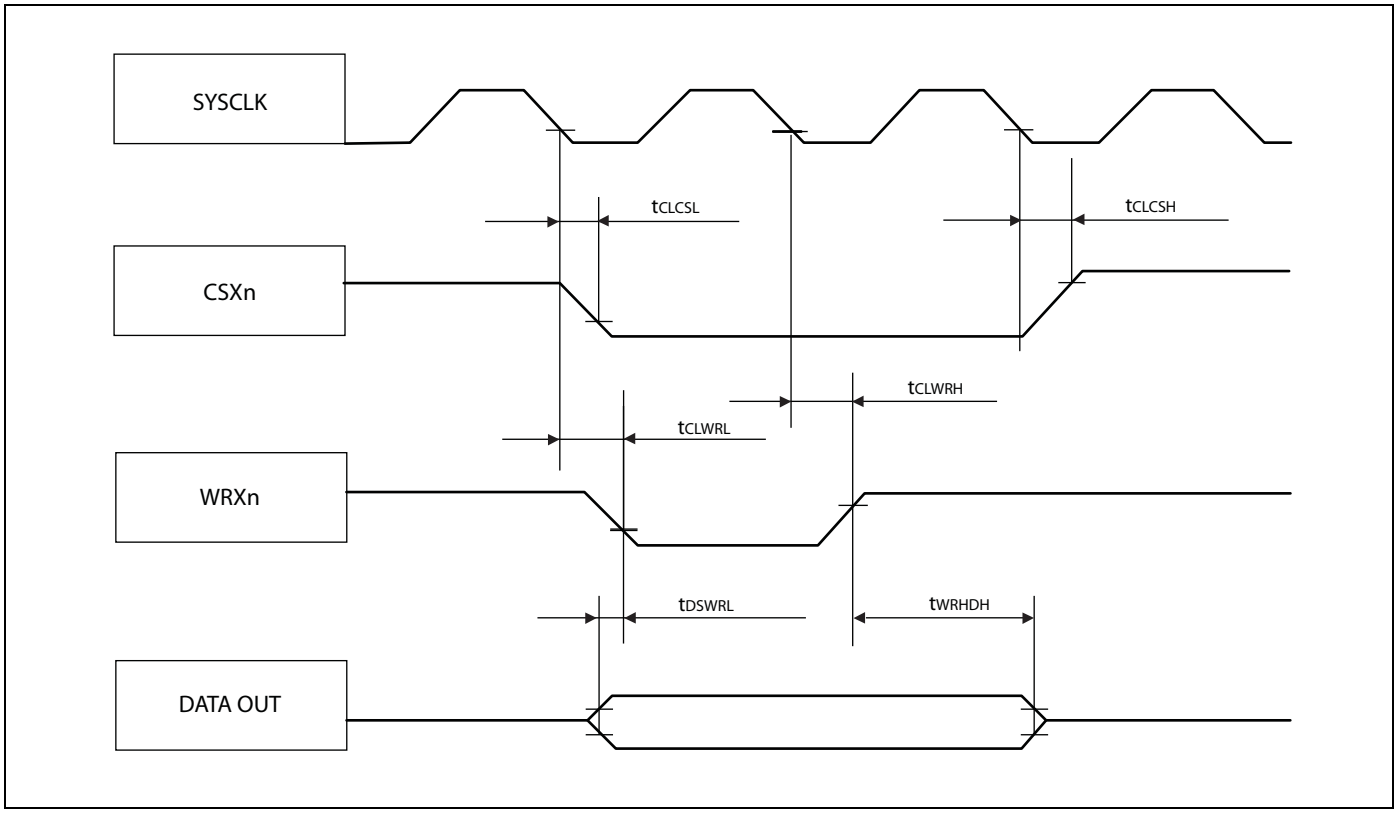
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WEX delay time	TCLWL	SYSCLK WEX	—	12	ns
	TCLWH		2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D16	− 2	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D16	t_{CLKT} − 9	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	12	ns
	TCLWRH		3	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	12	ns
	TCLCSH		—	9	ns



Synchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

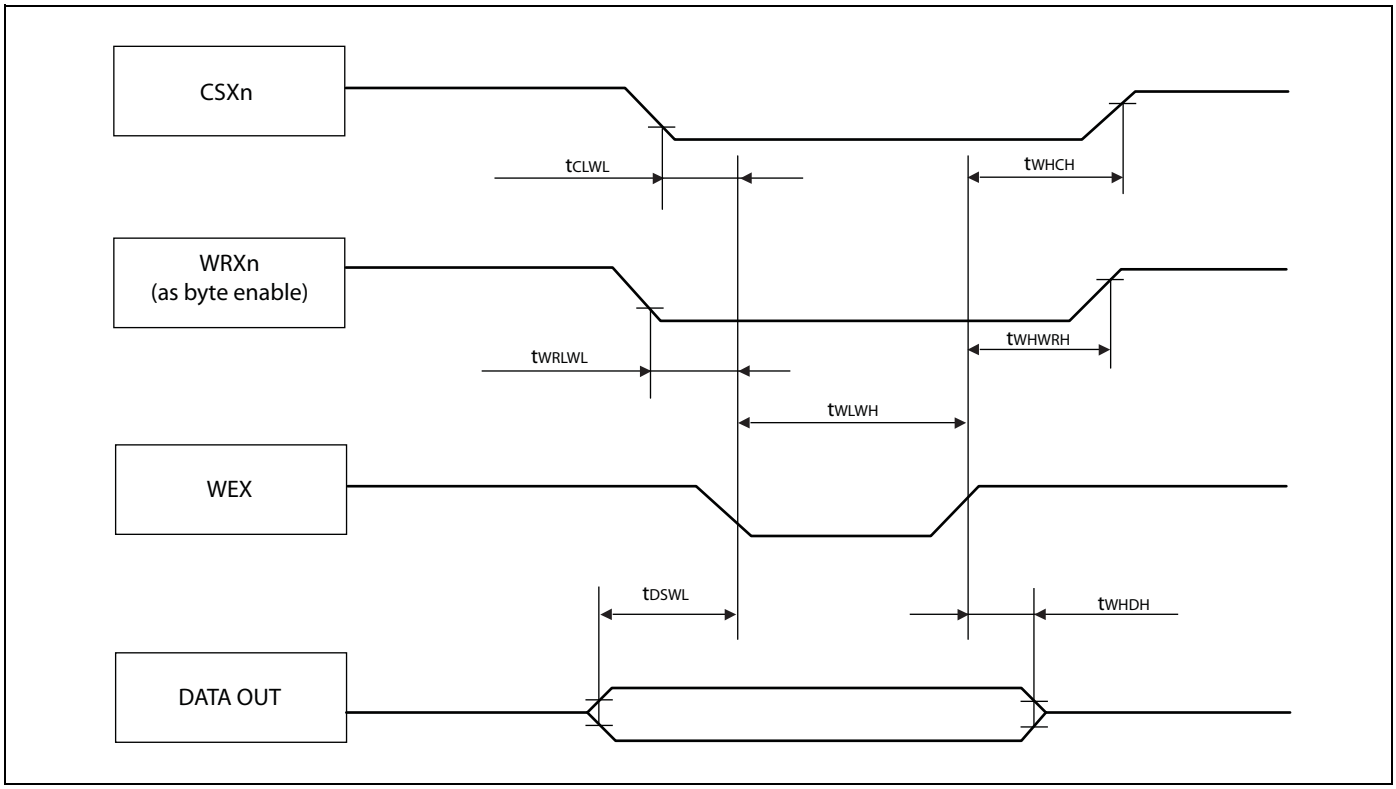
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	12	ns
	TCLWRH		3	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	− 1	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} − 9	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	12	ns
	TCLCSH		—	9	ns



Asynchronous write access - byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

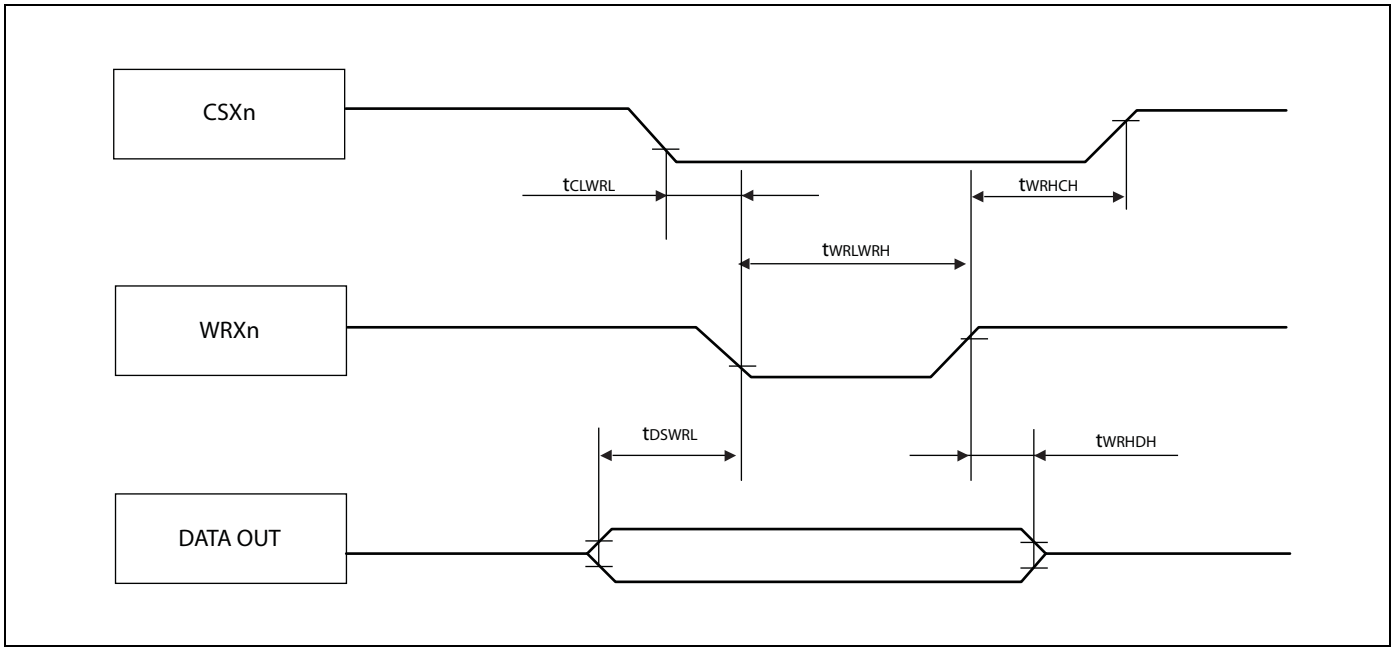
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CLKT} − 8	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D16	1/2 × t_{CLKT} − 1	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D16	1/2 × t_{CLKT} − 9	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CLKT} + 1	ns
	TWHWRH		1/2 × t_{CLKT} − 0	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CLKT} + 7	ns
	TWHCH		1/2 × t_{CLKT} − 1	—	ns



Asynchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

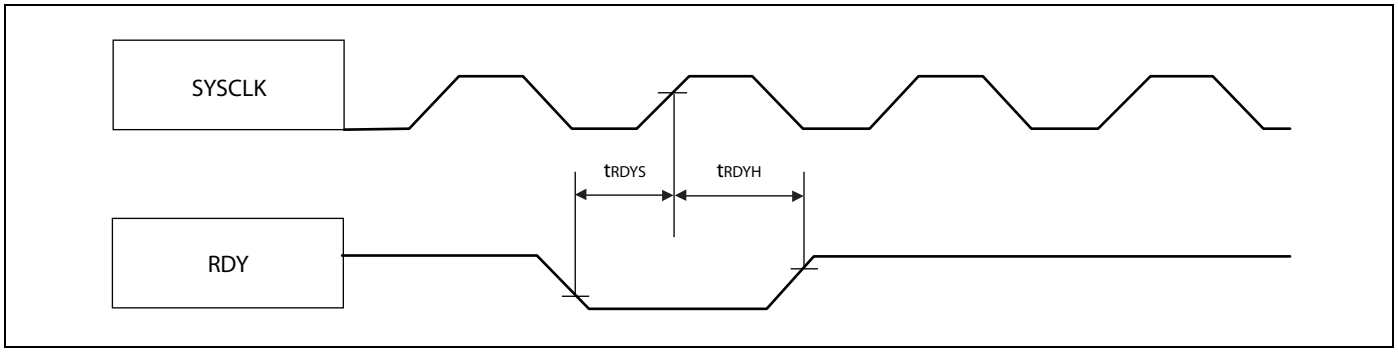
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT} − 7	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} − 1	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} − 9	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT} + 7	ns
	TWRHCH		1/2 × t_{CLKT} − 1	—	ns



RDY waitcycle insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	16	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns



21.6.8 External Bus AC Timings at $V_{DD}35$ = 3.0 to 4.5 V

- Conditions during AC measurements

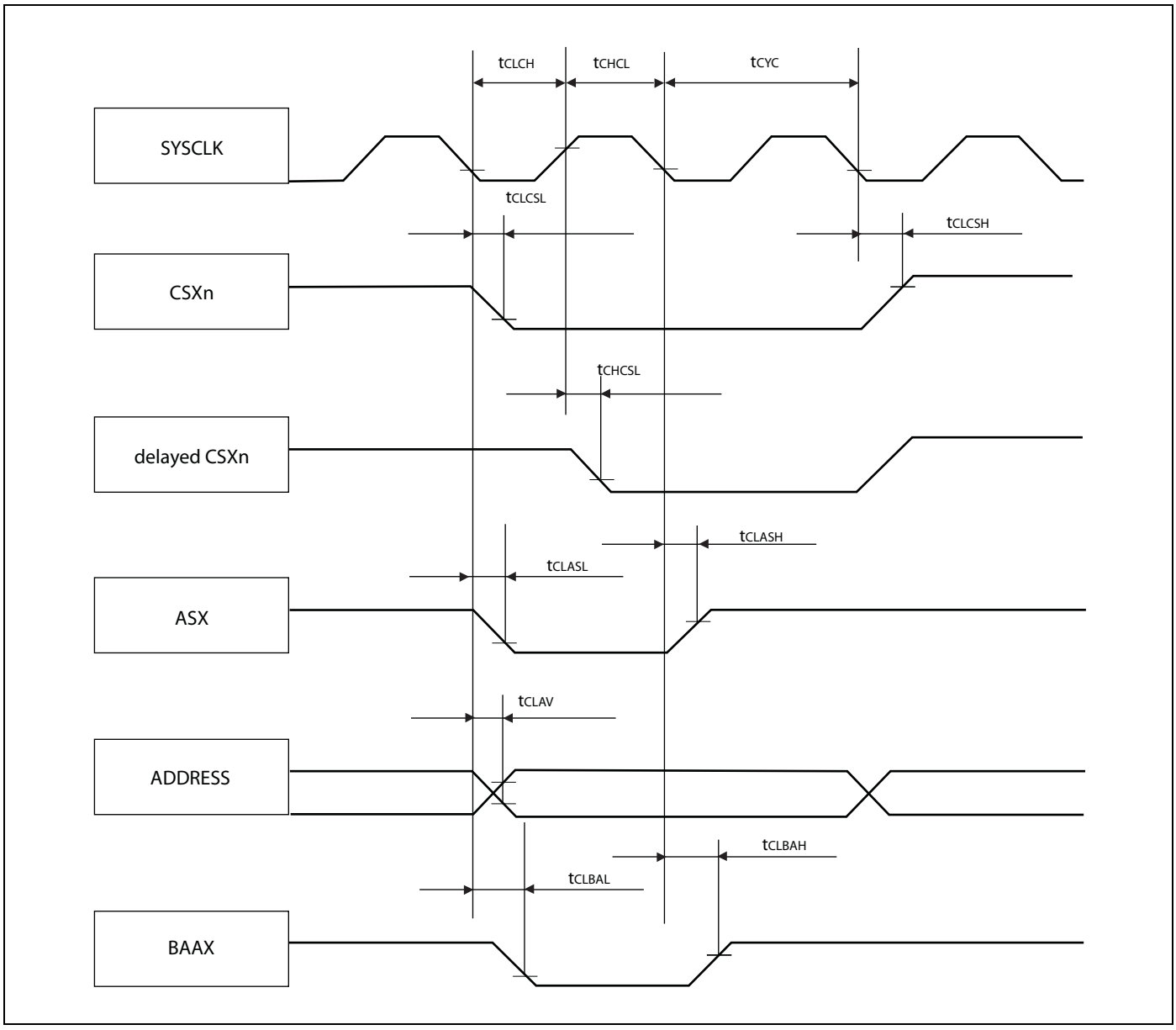
  All AC tests were measured under the following conditions:

  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 3.0 V to 4.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = − 40 °C to + 125 °C
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$
  - VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

Basic Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 125 °C)

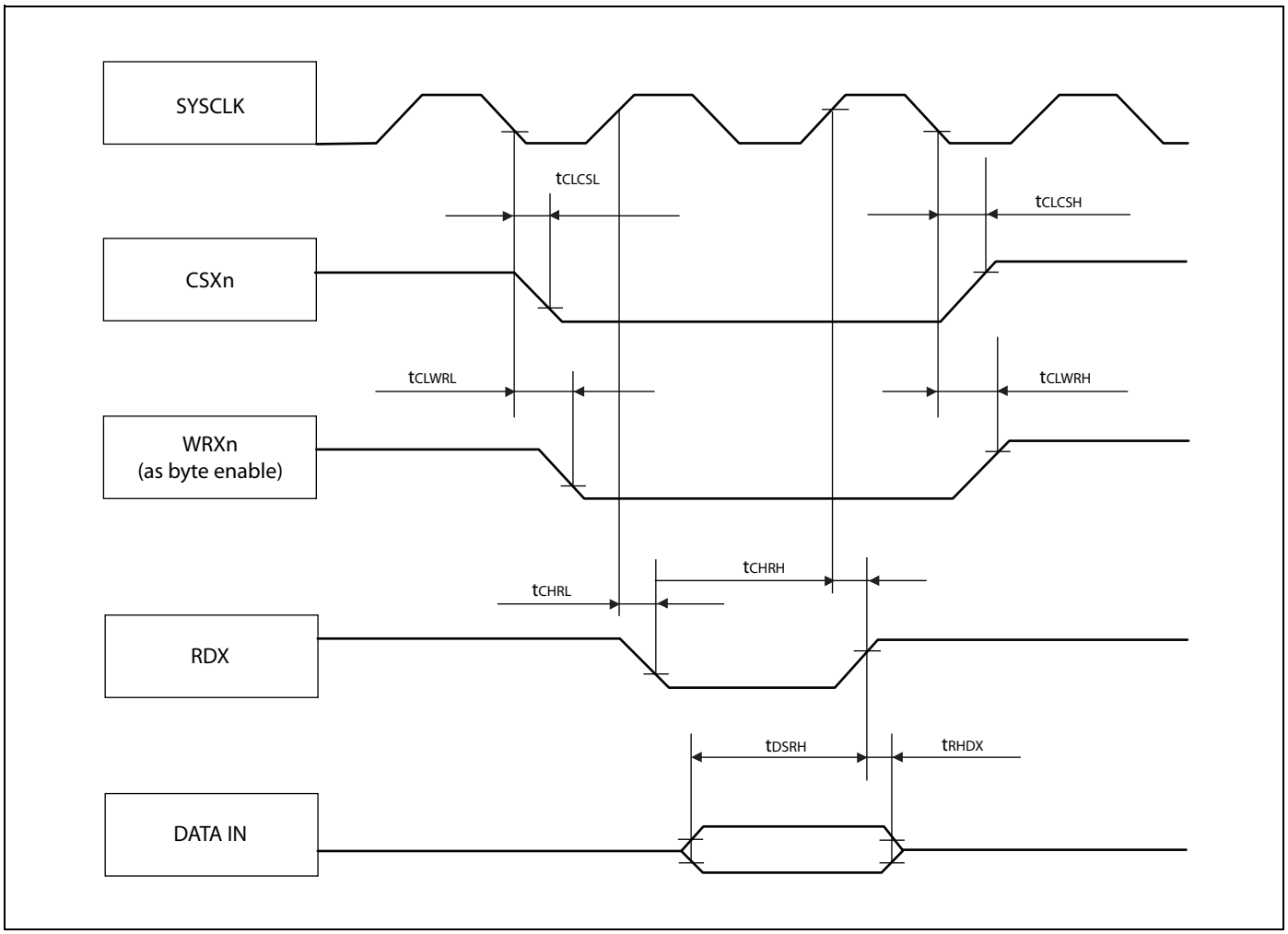
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	TCLCH	SYSCLK	1/2 × t_{CLKT} − 4	1/2 × t_{CLKT} + 5	ns
	TCHCL		1/2 × t_{CLKT} − 5	1/2 × t_{CLKT} + 4	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	9	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	TCHCSL		1	8	ns
SYSCLK ↓ to ASX delay time	TCLASL	SYSCLK ASX	—	8	ns
	TCLASH		—	9	ns
SYSCLK ↓ to Address valid delay time	TCLAV	SYSCLK A23 to A0	—	12	ns


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous read access

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

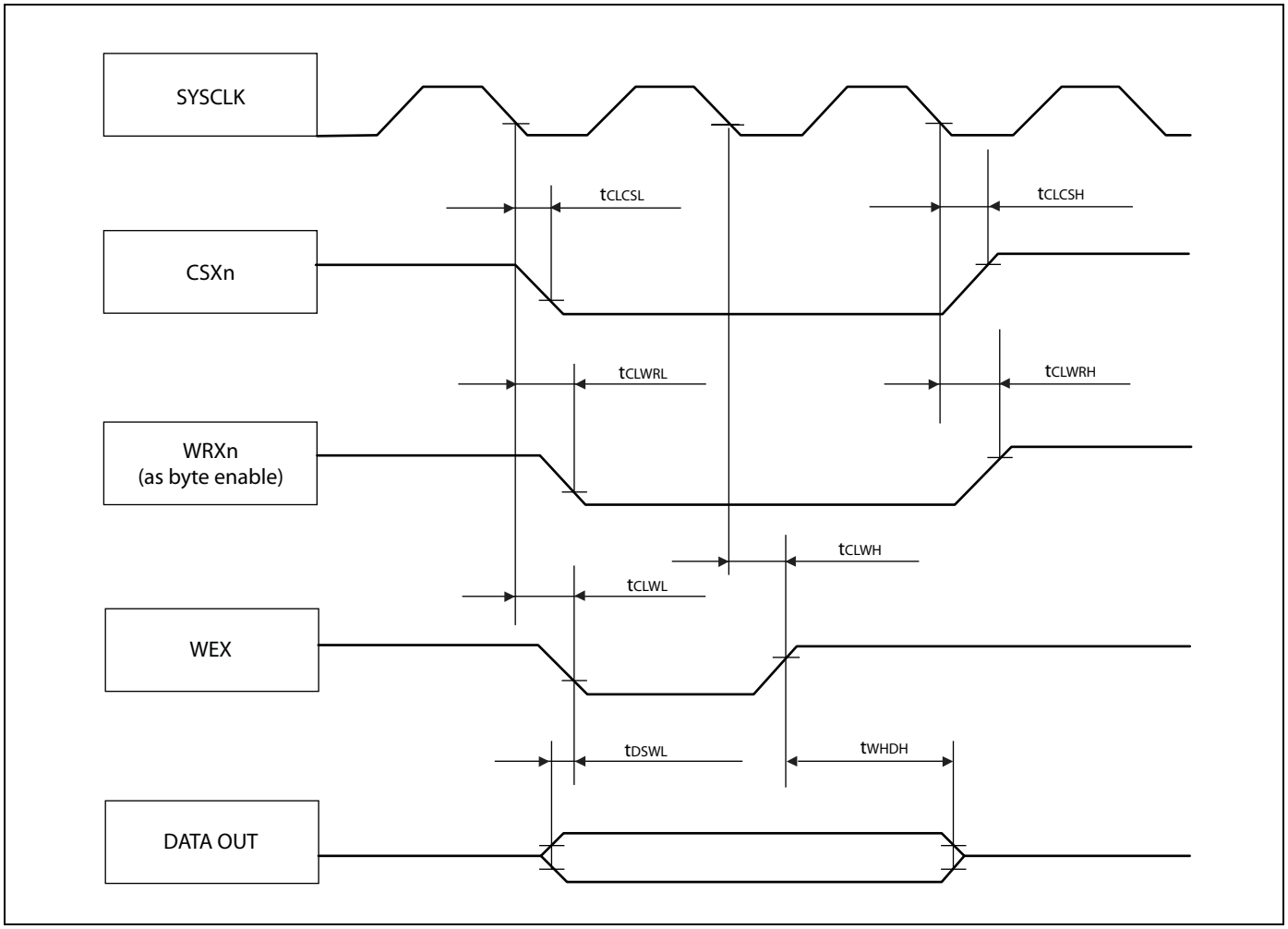
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	1	8	ns
	TCHRH		2	8	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	26	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	9	ns
	TCLWRH		3	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	9	ns



Synchronous write access - byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

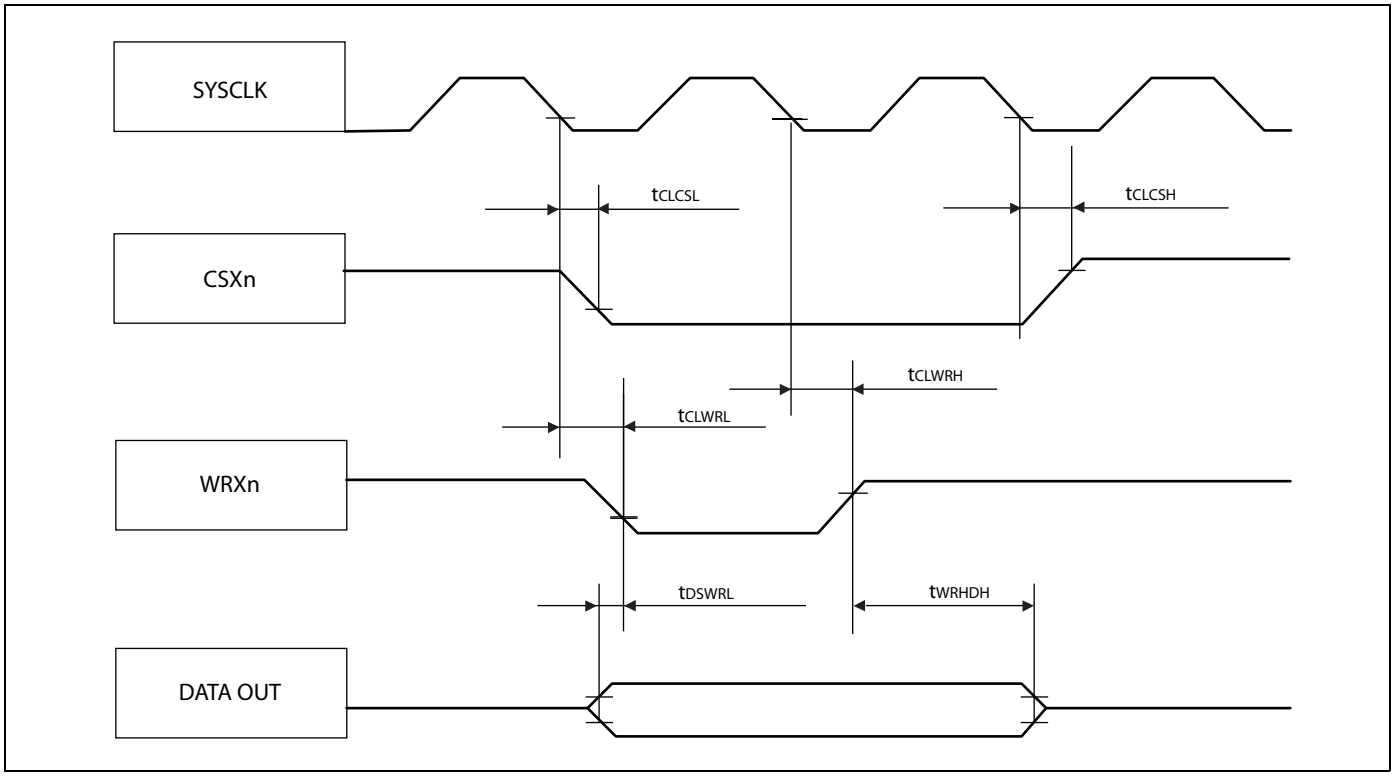
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WEX delay time	TCLWL	SYSCLK WEX	—	9	ns
	TCLWH		3	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D16	− 6	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D16	t_{CLKT} − 13	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	9	ns
	TCLWRH		4	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	9	ns



Synchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

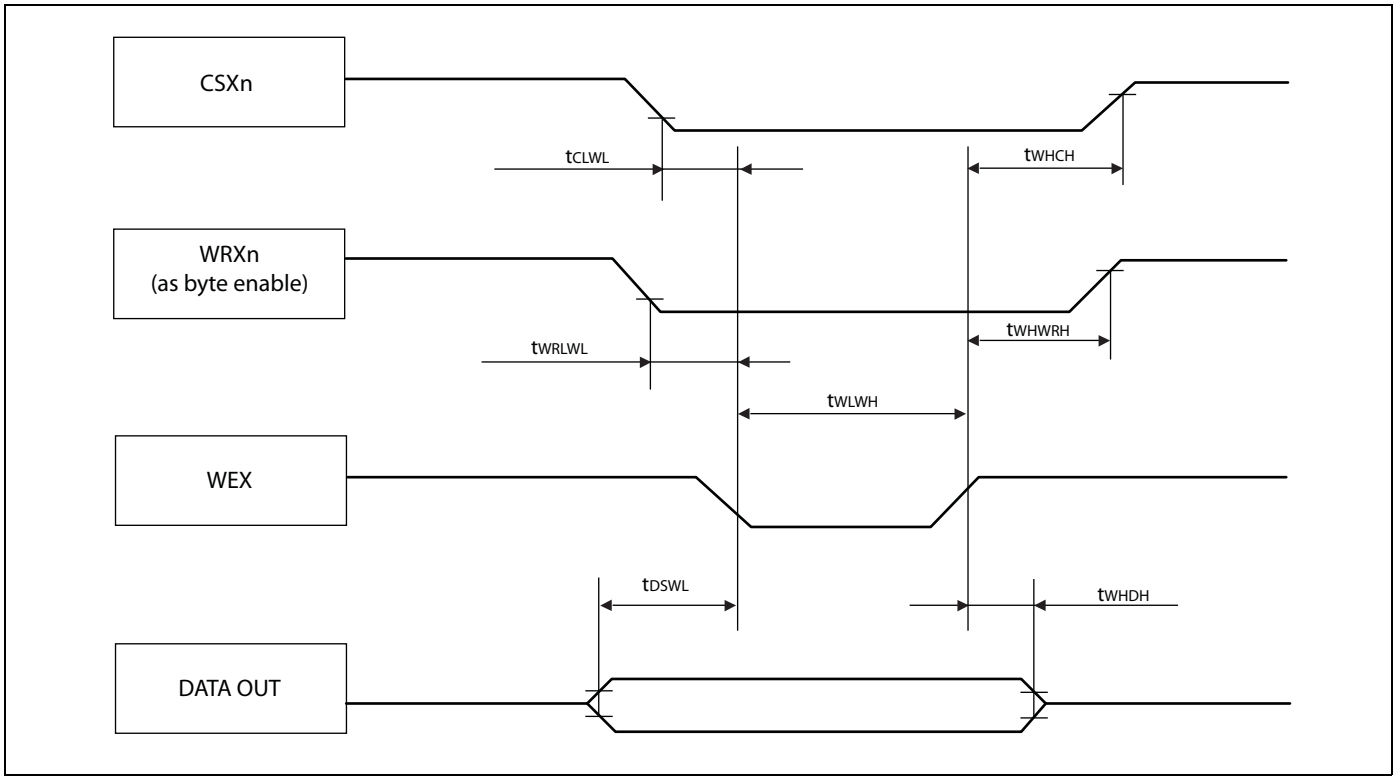
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	9	ns
	TCLWRH		4	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	− 6	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} − 15	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	9	ns



Asynchronous write access - byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

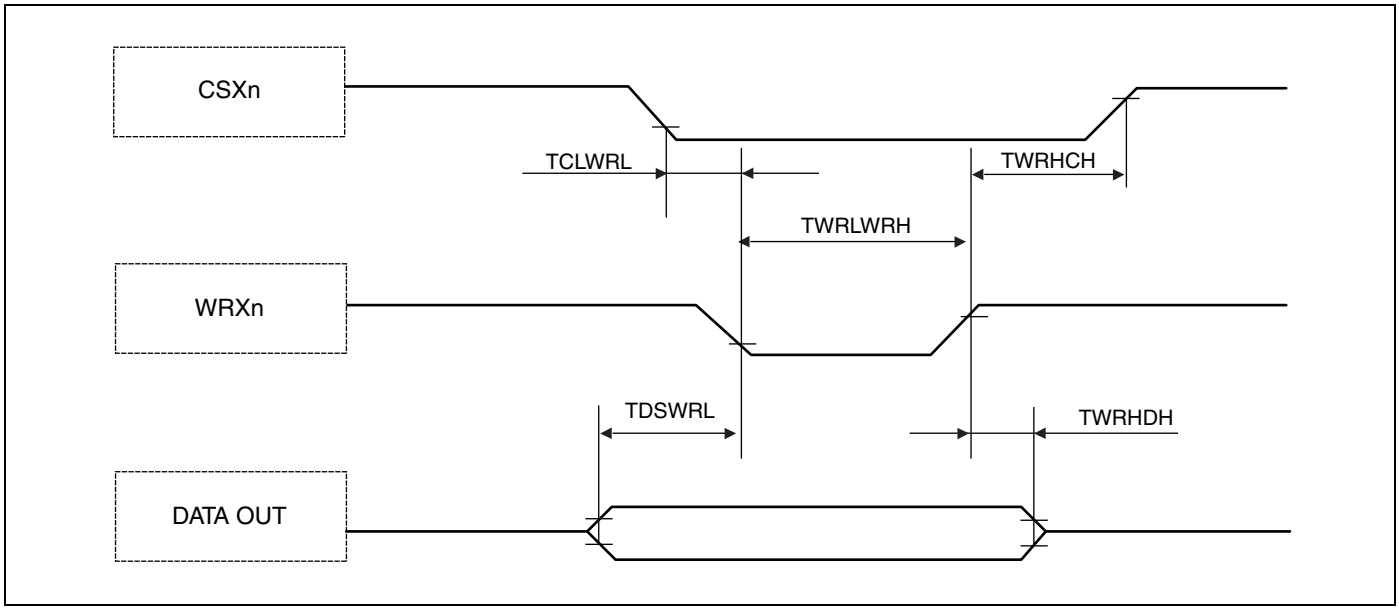
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CLKT} − 4	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D16	1/2 × t_{CLKT} − 6	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D16	1/2 × t_{CLKT} − 13	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CLKT} + 1	ns
	TWHWRH		1/2 × t_{CLKT} − 1	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CLKT} + 1	ns
	TWHCH		1/2 × t_{CLKT} − 0	—	ns



Asynchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

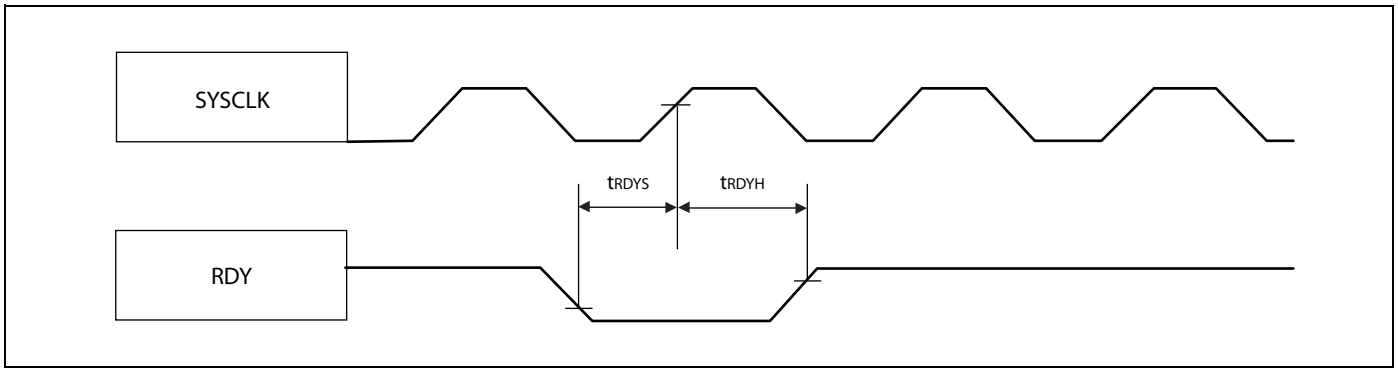
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT} − 2	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} − 6	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} − 14	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT} + 1	ns
	TWRHCH		1/2 × t_{CLKT} − 0	—	ns



RDY waitcycle insertion

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

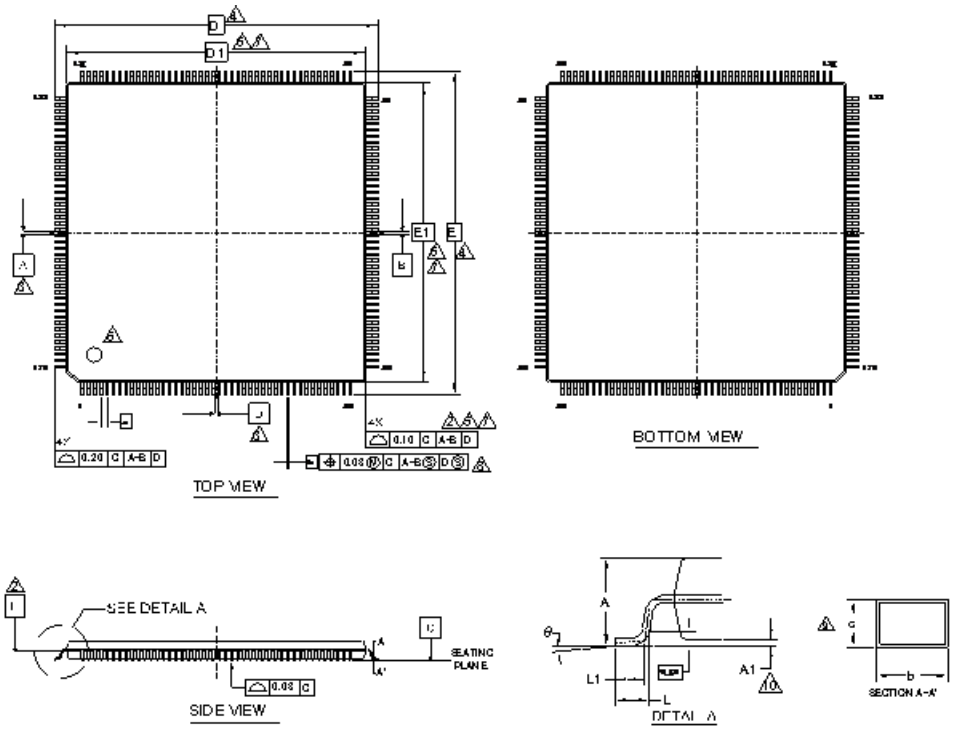
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	21	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns



22. Ordering Information

Part number	Package	Remarks
CY91F465PAPMC-GS-UJE1	176-pin plastic LQFP (LQP176)	Lead-free package
CY91F465PAPMC-GS-UJE2	176-pin plastic LQFP (LQP176)	Lead-free package
CY91F467PAPMC-GS-UJE2	176-pin plastic LQFP (LQP176)	Lead-free package

23. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQFP176 REV**

24. Revision History

Version	Date	Remark
2.0	2008-06-10	Initial version
2.1	2008-08-15	Handling devices: Section Notes on PS Register changed for better understanding Interrupt Vector Table: corrected the footnotes FLASH: Added note about the flash operation mode switching, added section "Poweron Sequence in parallel programming mode" Absolute maximum ratings: Removed the note that analog input/output pins cannot accept +B signal input. DC Characteristics: Updated PullUp/Down resistors, updated the footnotes splitted ILV into external and internal LV detection AD Converter characteristics updated (complete section)
2.2	2008-09-04	Added MB91F467PA with Data Flash and 2 ADC macros: - added chapter A/D Converter / New Features - added chapter A/D Converter / Range Comparator - added chapter Embedded Data Flash
2.3	2008-09-23	A/D CONVERTER / NEW FEATURES (MB91F467PA): The ADC Channel Enable feature is only available on the non-relocated ADC channels 6-7. IO MAP: Added IOS register (addr. 0xC03) with note "always write 1 to IOS[1]"; Added bookmarks inside IO MAP; the IO MAP is common for MB91F465PA and MB91F467PA. EMBEDDED DATA FLASH (MB91F467PA): Added info about read operation during Command Sequencer write is active.
3.0	2008-09-23	Data Flash: Corrected text about Command Sequencer Mode (DFWC:WE bit); corrected TMG2,TMG1,TMG0=000 to max. 6.2MHz Corrected notes about CRC calculation (CLKB faster then RC clock) Embedded Program/Data Memory (Flash): Added section 7 "Notes About Flash Memory CRC Calculation" (CLKB must be faster then the RC clock) Pin Assignment: Corrected "SYSCLK7" Pin Description: Added X0/X1 pinning spec of F467PA Added Ta=125C characteristics
3.1	not released yet	Embedded Data Flash: Added 3 notes that "Dummy addresses for auto algorithm" cannot be used for toggle bit polling. DFCS register bit description: corrected INTEN into INTE, Data flash security: Added information about FSC_DISABLE. FLASH memory program/erase characteristics: Added 5.3 MB91F467PA DATA FLASH (erase / programming times)

25. Major Changes

Spansion Publication Number: DS07-16615-2E

Page	Section	Change Results
31	Port Multiplexing	Corrected the text bubbles in Figure “3. Multiplex Pinout MB91F465PA”.
32		Corrected the text bubbles in Figure “4. Multiplex Pinout MB91F467PA”.
Rev *B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
188 189	22. Ordering Information 23. Package Dimension	Package description modified to JEDEC description. (Before) FPT-176P-M07 (After) LQP176
188	22. Ordering Information	Revised the following parts number. Before) MB91F465PAPMC-GSE2 MB91F467PAPMC-GSE2 After) CY91F465PAPMC-GS-UJE2 CY91F467PAPMC-GS-UJE2 Added the following parts number. CY91F465PAPMC-GS-UJE1

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY91460P Series FR60 32-bit Microcontroller Document Number: 002-04619				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/01/2010	Migrated to Cypress and assigned document number 002-04619. No change to document contents or format.
*A	5221463	AKIH	04/14/2016	Updated to Cypress format.
*B	6178926	GSHI	05/18/2016	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 23.Package Dimension 22.Ordering Information For details, please see 25.Major Changes

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2009-2018. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.