MPQ6615-AEC1

40V, 8A, H-Bridge DC Motor Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6615-AEC1 is an H-bridge DC motor driver. The H-bridge consists of four N-channel power MOSFETs. The on resistance of each MOSFET is 11mΩ when the junction temperature (T_J) is 25°C. It also integrates pre-drivers, gate driver power supplies, and current-sense amplifiers.

The MPQ6615-AEC1 operates on a motor power supply voltage from 4.75V to 40V, which can deliver up to 8A of continuous output current (I_{OUT}), depending on thermal and PCB conditions.

The device's internal charge pump generates the gate driver supply voltages for the high-side MOSFETs (HS-FETs), and a trickle charge circuit maintains sufficient gate driver voltages for 100% duty cycle operation.

Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO) protection, and thermal shutdown.

The MPQ6615-AEC1 is available in a TQFN-26 (6mmx6mm) package.

FEATURES

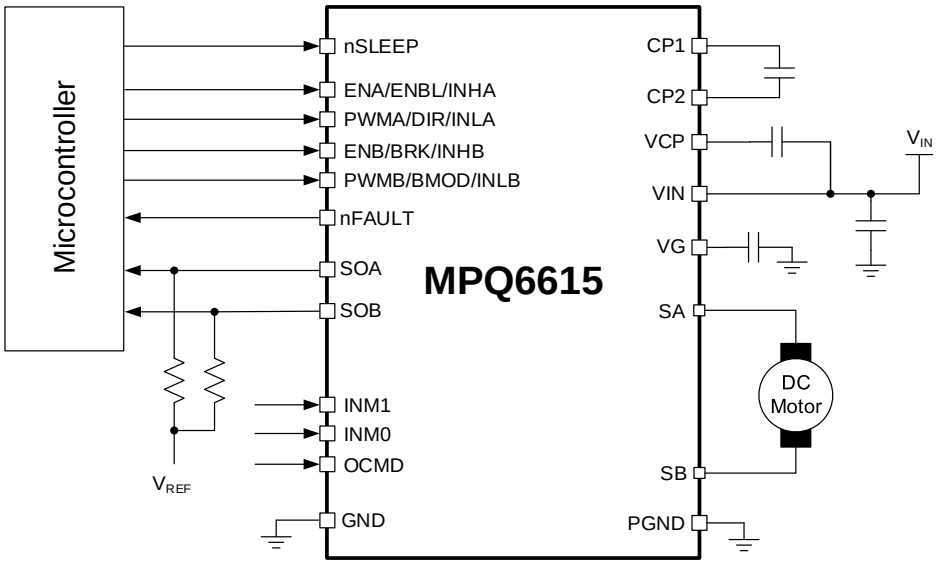
- 4.75V to 40V Operating Input Voltage (V_{IN}) Range
- Internal Full H-Bridge Driver Supports 100% Duty Cycle
- 8A Continuous Output Current (I_{OUT})
- 11mΩ MOSFET On Resistance
- Internal Charge Pump
- Under-Voltage Lockout (UVLO) Protection and Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Thermal Shutdown
- Integrated Bidirectional Current-Sense Amplifiers
- Available in a TQFN-26 (6mmx6mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Brushed DC Motors
- Door Lock and Latch Motors
- Seat Actuators

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6615GQKTE-AEC1*	TQFN-26 (6mmx6mm)	*See Below*	1

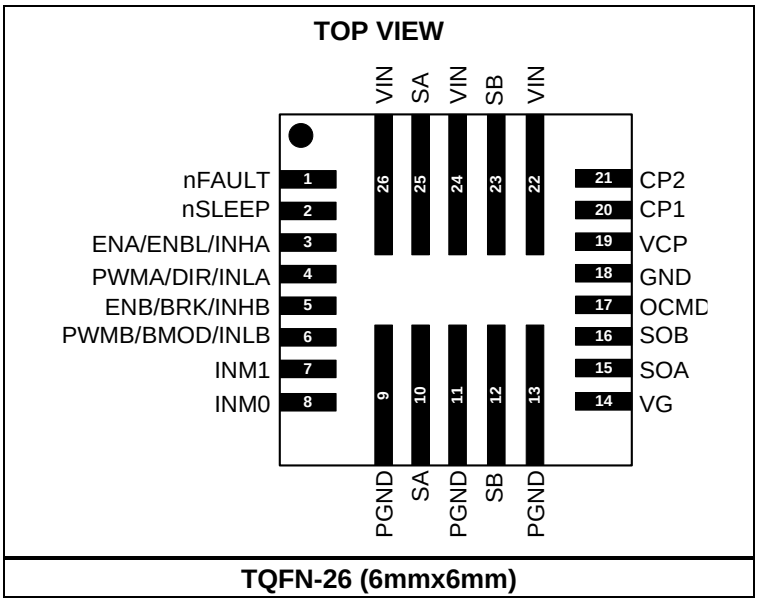
* For Tape & Reel, add suffix -Z (e.g. MPQ6615GQKTE-AEC1-Z).

TOP MARKING

MPSYYWW
MP6615
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP6615: Part number
LLLLLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE



TQFN-26 (6mmx6mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output. If a fault occurs, nFAULT is pulled to logic low.
2	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin to logic low to enter low-power sleep mode; pull nSLEEP to logic high for normal operation. nSLEEP has an internal pull-down resistor.
3	ENA/ENBL/ INHA	**Can be configured for the ENA, ENBL, or INHA function.** ENA: If INM[1:0] = 00, this pin acts as the enable input for phase A. Pull ENA high to enable phase A. ENBL: If INM[1:0] = 01, this pin acts as the enable input for the H-bridge. Pull ENBL high to enable the entire H-bridge. INHA: If INM[1:0] = 10, this pin acts as the enable input for the phase A high-side MOSFET (HS-FET).
4	PWMA/DIR/ INLA	**Can be configured for the PWMA, DIR, or INLA function.** PWMA: If INM[1:0] = 00, this pin acts as the pulse-width modulation (PWM) input for phase A. DIR: If INM[1:0] = 01, this pin acts as the direction input for the H-bridge. INLA: If INM[1:0] = 10, this pin acts as the enable input for the phase A low-side MOSFET (LS-FET).
5	ENB/BRK/ INHB	**Can be configured for the ENB, BRK, or INHB function.** ENB: If INM[1:0] = 00, this pin acts as the enable input for phase B. Pull ENB high to enable phase B. BRK: If INM[1:0] = 01, this pin acts as the brake input for the H-bridge. Pull BRK high to force the H-bridge to enter brake mode. INHB: If INM[1:0] = 10, this pin acts as the enable input for the phase B HS-FET.
6	PWMB/ BMOD/INLB	**Can be configured for the PWMB, BMOD, or INLB function.** PWMB: If INM[1:0] = 00, this pin acts as the PWM input for phase B. BMOD: If INM[1:0] = 01, this pin acts as the brake mode input for the H-bridge. Pull BMOD high to force the HS-FETs to enter brake mode. Pull BMOD low to force the LS-FETs to enter brake mode. INLB: If INM[1:0] = 10, this pin acts as the enable input for the phase B LS-FET.
7	INM1	**Input mode selection 1.** If INM[1:0] = 00, INMx sets the ENx/PWMx input logic. If INM[1:0] = 01, INMx sets the ENBL/DIR input logic. If INM[1:0] = 10, INMx sets the INHx/INLx input logic.
8	INM0	**Input mode selection 0.** If INM[1:0] = 00, INMx sets the ENx/PWMx input logic. If INM[1:0] = 01, INMx sets the ENBL/DIR input logic. If INM[1:0] = 10, INMx sets the INHx/INLx input logic.
9, 11, 13	PGND	**Power ground.** Connect the PGND pin directly to GND.
10, 25	SA	**Phase A output.**
22, 24, 26	VIN	**Input supply voltage.**
12, 23	SB	**Phase B output.**
14	VG	**Low-side gate driver output.** Connect a 4.7μF, 10V ceramic capacitor with X7R dielectrics between the VG and GND pins.
15	SOA	**Current-sense output A.**
16	SOB	**Current-sense output B.**

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
17	OCMD	**Over-current protection (OCP) mode.** Connect OCMD to GND for latch-off mode. Leave OCMD open or connect OCMD to a logic high voltage for retry mode.
18	GND	**Ground.**
19	VCP	**Charge pump output.** Connect a 1μF, 16V ceramic capacitor with X7R dielectrics between the VCP and VIN pins.
20	CP1	**Charge pump capacitor pin 1.** Connect a 100nF ceramic capacitor with X7R dielectrics rated for ≥V_{IN} between the CP1 and CP2 pins.
21	CP2	**Charge pump capacitor pin 2.** Connect a 100nF ceramic capacitor with X7R dielectrics rated for ≥V_{IN} between the CP1 and CP2 pins.

ABSOLUTE MAXIMUM RATINGS (1)

Input voltage (V_{IN}) .....-0.3V to +45V
CP2, VCP ..... V_{IN} to (V_{IN} + 6.5V)
SA, SB .....-0.3V to +45V
All other pins to GND/PGND.....-0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
TQFN-26 (6mmx6mm)…….. 5.84W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... +150°C
Lead temperature (solder) ..... +260°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM) 2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4.75V to 40V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-26 (6mmx6mm)..... 21.4….12.8...°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the device to go into thermal shutdown.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{PGND} = V_{GND} = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage	V_{IN}		4.75		40	V
Quiescent current	I_Q	nSLEEP = 1, ENx = 0		2.6	5	mA
Quiescent current in sleep mode	I_{SLEEP}	nSLEEP = 0		1		µA
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Input logic low current	I_{INL}	V_{IL} = 0V	-20		+20	µA
Input logic high current	I_{INH}	V_{IH} = 5V	-20		+20	µA
Start-up delay	t_{SU_DELAY}	At V_{IN} rising or nSLEEP rising		1		ms
Internal pull-down resistance	R_{PD}	All logic inputs		500		kΩ
nFAULT pull-down resistance	R_{nFAULT}			10		Ω
Protection Circuits						
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$	V_{IN} rising	4.1	4.4	4.75	V
UVLO hysteresis	ΔV_{UVLO}			480		mV
Over-voltage protection (OVP) rising threshold	V_{OVP_RISING}	V_{IN} rising	45	48	51	V
OVP hysteresis	ΔV_{OVP}			1.6		V
High-side (HS) over-current protection (OCP) threshold	I_{OCP_HS}		16	25		A
Low-side (LS) OCP threshold	I_{OCP_LS}		16	25		A
OCP deglitch time (5)	$t_{OCP_DEGLITCH}$			0.4		µs
OCP retry time	t_{OCP_RETRY}			2		ms
Thermal shutdown (5)	T_{SD}			150		°C
Thermal shutdown hysteresis (5)	ΔT_{SD}			25		°C
Current Sense (CS) (SOx)						
CS ratio		Phase A	1/ 12700	1/ 11000	1/ 10000	A/A
		Phase B	1/ 11900	1/ 10500	1/ 9600	A/A
CS output offset current	I_{SOx}	Phase A current = 0A	-30	-5	+20	µA
		Phase B current = 0A	-32	-5	+22	µA
CS voltage (V_{SOx}) swing (5)			0		5	V
CS minimum load resistance (5)		Pull-up		1.8		kΩ
		Pull-down		1		kΩ

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, V_{PGND} = V_{GND} = 0V, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Outputs						
HS-FET on resistance	$R_{DS(ON)_HS}$	I_{OUT} = 1A, T_J = 25°C		11	19	mΩ
LS-FET on resistance	$R_{DS(ON)_LS}$	I_{OUT} = 1A, T_J = 25°C		11	19	mΩ
Output rising time (5)		I_{OUT} = 1A		0.47		V/ns
Output falling time (5)		I_{OUT} = 1A		1.27		V/ns
Charge Pump						
Charge pump output voltage	V_{VCP}			V_{IN} + 5		V
Charge pump frequency	f_{CP}			2000		kHz

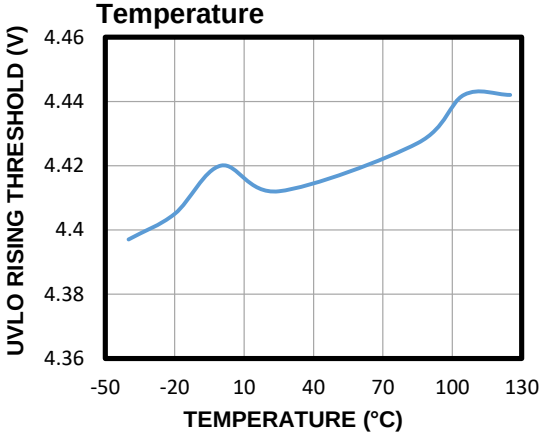
Note:

5) Not tested in production.

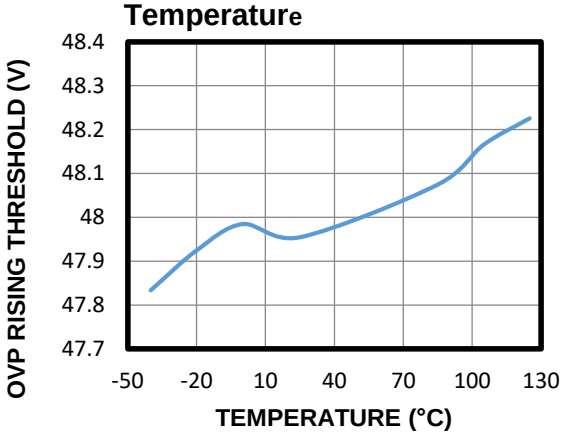
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TYPICAL CHARACTERISTICS

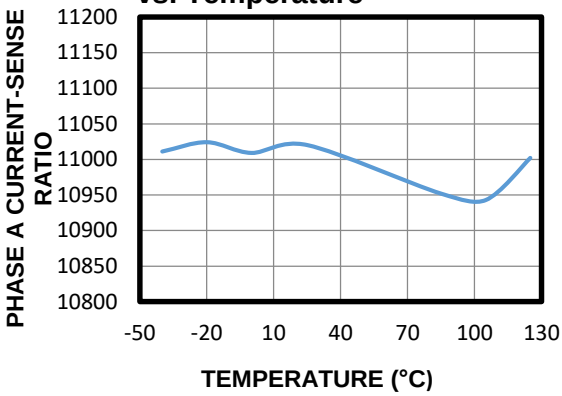
UVLO Rising Threshold vs. Temperature



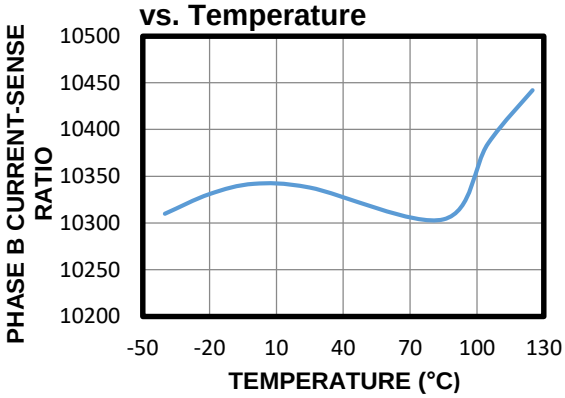
OVP Rising Threshold vs. Temperature



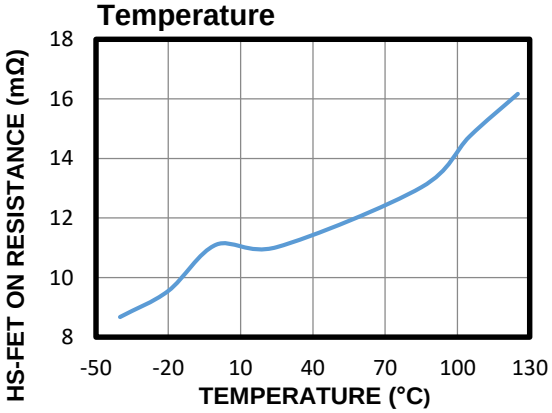
Phase A Current-Sense Ratio vs. Temperature



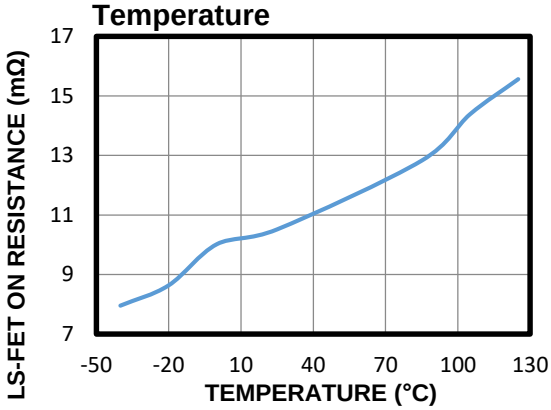
Phase B Current-Sense Ratio vs. Temperature



HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

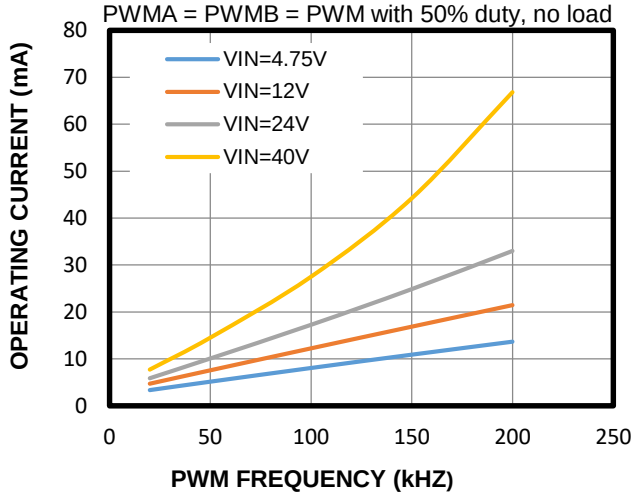


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TYPICAL CHARACTERISTICS *(continued)*

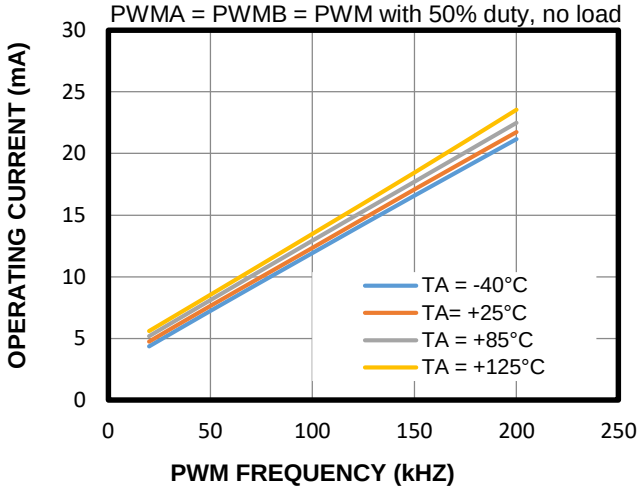
Operating Current vs. PWM Frequency

T_A= 25°C, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load



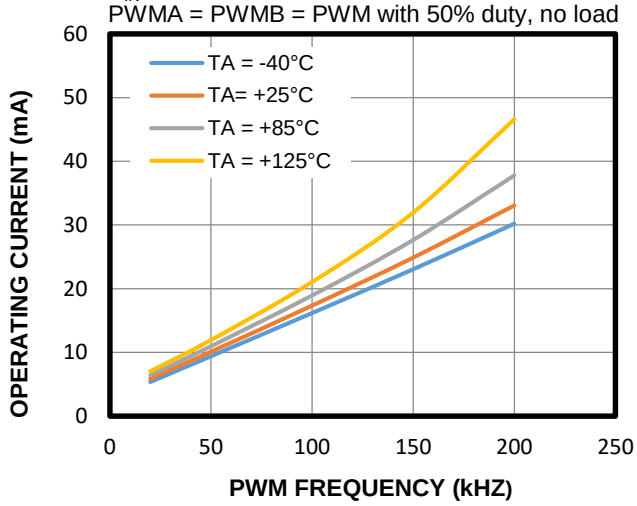
Operating Current vs. PWM Frequency

V_{IN} = 12V, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load



Operating Current vs. PWM Frequency

V_{IN} = 24V, INM1 = INM0 = 0, ENA = ENB = 1, PWMA = PWMB = PWM with 50% duty, no load

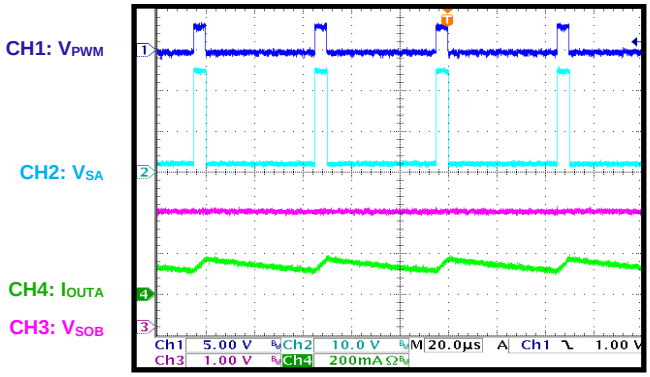


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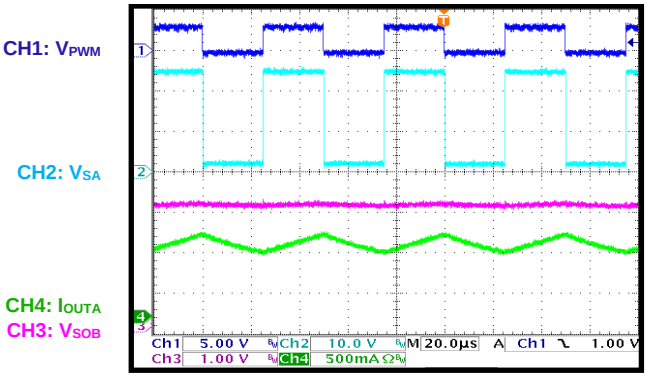
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{INM0} = V_{INM1} = 0V, V_{ENA} = V_{ENB} = 5V, f_{PWMA} = 20kHz, V_{PWMB} = 0V, V_{REF} = 5V, CS resistor divider = 5kΩ, T_A = 25°C, resistor + inductance: 10Ω + 2mH, unless otherwise noted.

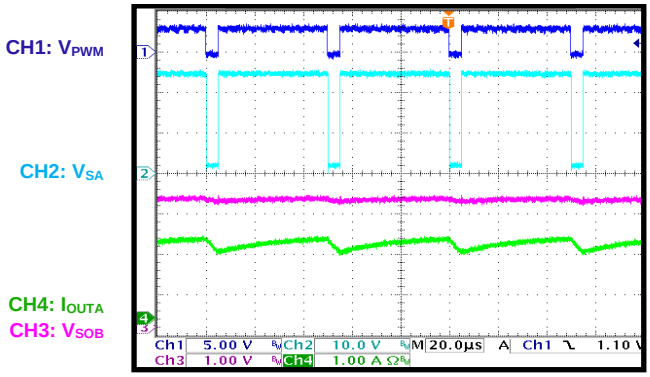
Steady State
Duty = 10%



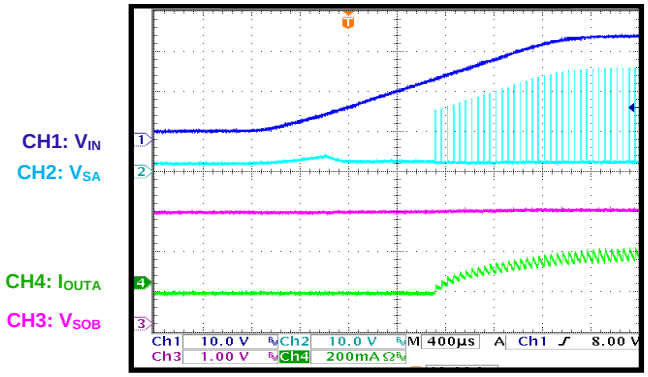
Steady State
Duty = 50%



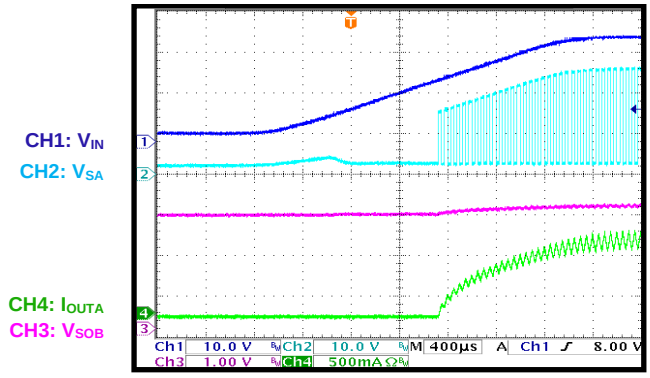
Steady State
Duty = 90%



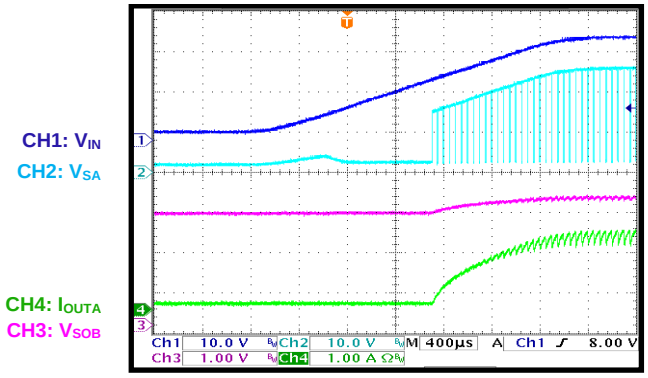
Start-Up
Duty = 10%



Start-Up
Duty = 50%



Start-Up
Duty = 90%

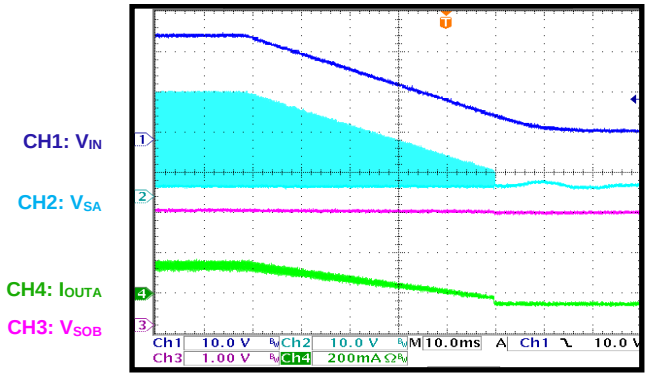


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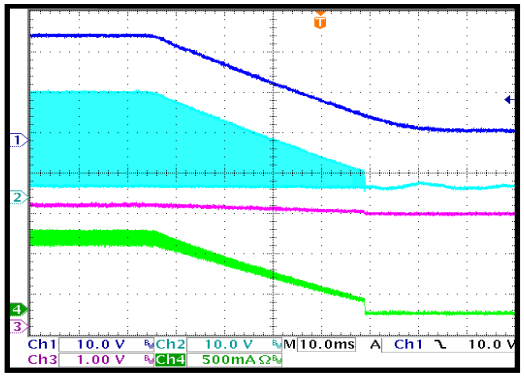
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{INM0} = V_{INM1} = 0V, V_{ENA} = V_{ENB} = 5V, f_{PWMA} = 20kHz, V_{PWMB} = 0V, V_{REF} = 5V, CS resistor divider = 5kΩ, T_A = 25°C, resistor + inductance: 10Ω + 2mH, unless otherwise noted.

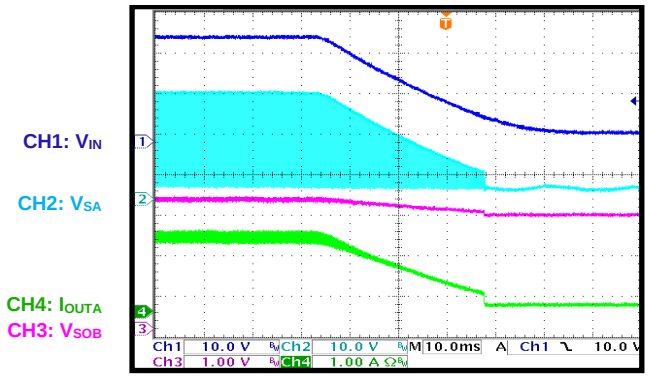
Shutdown
Duty = 10%



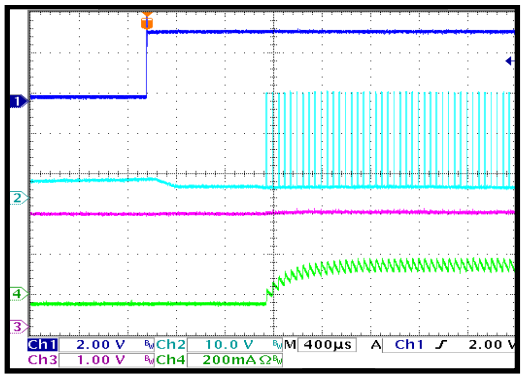
Shutdown
Duty = 50%



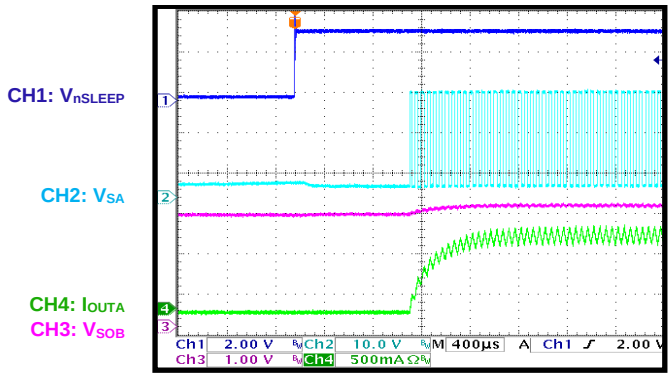
Shutdown
Duty = 90%



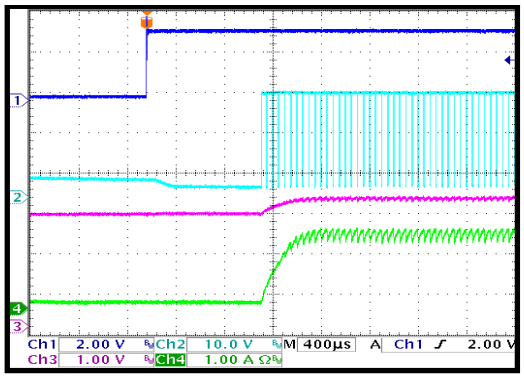
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



Sleep Recovery
Duty = 90%

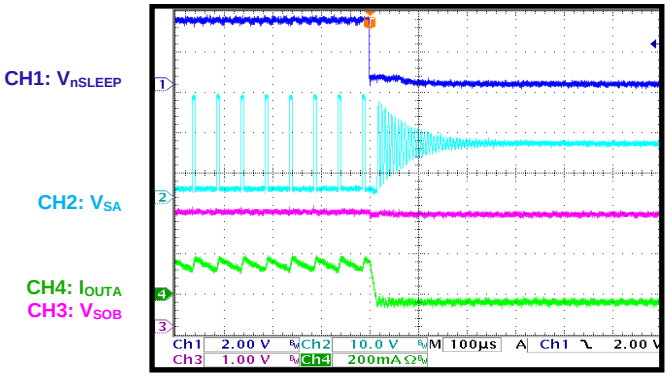


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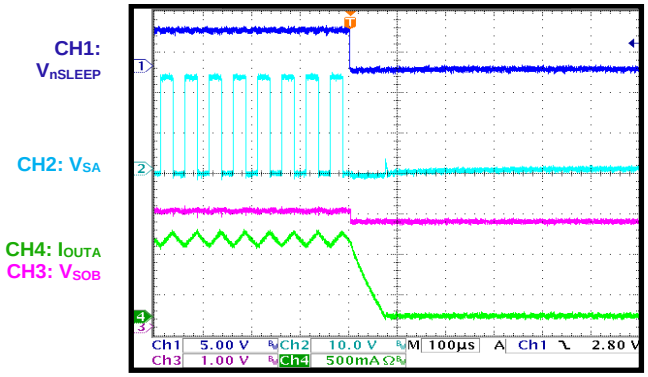
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{INM0} = V_{INM1} = 0V, V_{ENA} = V_{ENB} = 5V, f_{PWMA} = 20kHz, V_{PWMB} = 0V, V_{REF} = 5V, CS resistor divider = 5kΩ, T_A = 25°C, resistor + inductance: 10Ω + 2mH, unless otherwise noted.

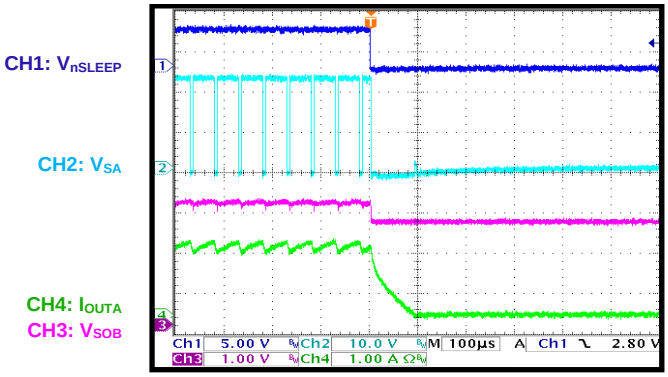
Sleep Entry
Duty = 10%



Sleep Entry
Duty = 50%



Sleep Entry
Duty = 90%



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FUNCTIONAL BLOCK DIAGRAM

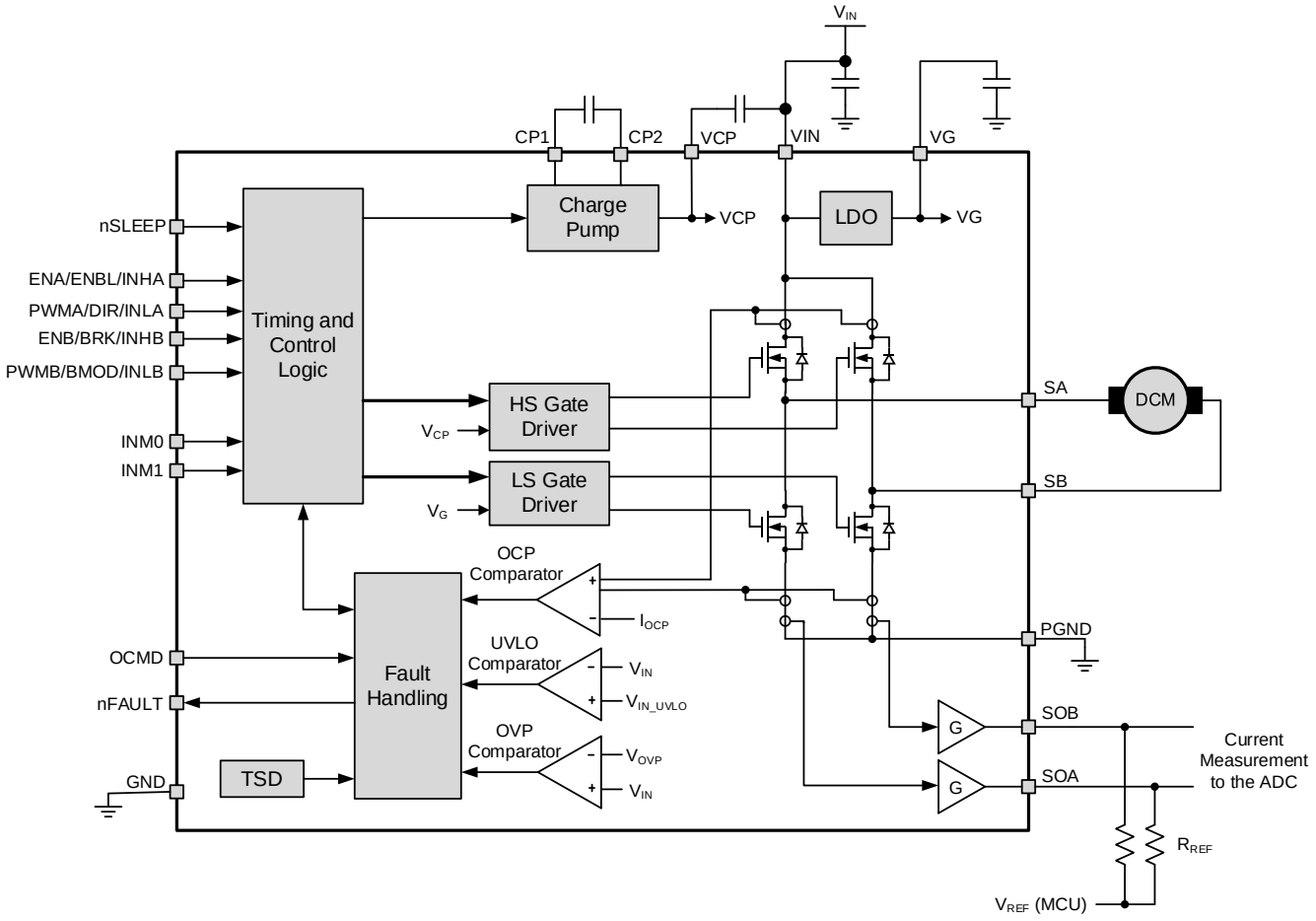


Figure 1: Functional Block Diagram

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OPERATION

Input Logic

The MPQ6615-AEC1 has three configurable input modes, which allows for several different control methods. The INM1 and INM0 pins configure the input interface. Table 1 shows the input logic truth table for when INM[1:0] = 00.

Table 1: Input Logic (INM[1:0] = 00)

ENx	PWMx	Sx
High	High	VIN
High	Low	GND
Low	-	High impedance (Hi-Z)

Table 2 shows the input logic truth table for when INM[1:0] = 01.

Table 2: Input Logic (INM[1:0] = 01)

ENBL	DIR	BRK	BMOD	SA	SB
Low	-	-	-	Hi-Z	Hi-Z
High	-	High	Low	GND	GND
High	-	High	High	VIN	VIN
High	Low	Low	-	GND	VIN
High	High	Low	-	VIN	GND

Table 3 shows the input logic truth table for when INM[1:0] = 10.

Table 3: Input Logic (INM[1:0] = 10)

INHx	INLx	Sx
Low	Low	Hi-Z
Low	High	GND
High	Low	VIN
High	High	Hi-Z

The logic inputs have internal, 500kΩ pull-down resistors.

nSLEEP Operation

Pull nSLEEP low to force the device into a low-power sleep state. In this state, all of the internal circuitry is disabled. All inputs are ignored when nSLEEP is active low. When the MPQ6615-AEC1 exits sleep mode, it takes about 1ms before the device responds to the inputs. The nSLEEP input has a 500kΩ pull-down resistor.

Current Sensing

The current flowing through the two Sx outputs is sensed by the internal current-sensing circuits. Each phase has an output pin that sources or sinks a current proportional to each phase's output current (I_{OUT}). Only the current flowing through the low-side MOSFET (LS-FET) is sensed. This current is sensed in both the forward and reverse directions.

To convert this current into a voltage (i.e. to input the voltage into an analog-to-digital converter [ADC]), connect a termination resistor (R_{REF}) between the SOx pin and a reference voltage (V_{REF}). When no current is flowing, the resulting SOx voltage (V_{SOx}) is equal to V_{REF}. When current is flowing, V_{SOx} can be above or below V_{REF}. V_{SOx} can be calculated with Equation (1):

$$V_{SOx} = V_{REF} + (R_{REF} \times I_{LOAD}) / 11{,}000 \quad (1)$$

To terminate the outputs when using an ADC with inputs that are ratiometric to its supply voltage, connect two equal-value resistors to the ADC supply and GND. The resulting ADC code is half-scale at 0A.

Figure 2 shows the current measurement circuit.

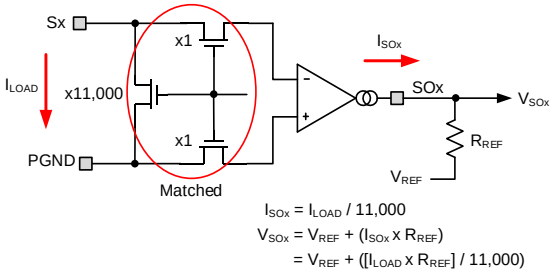


Figure 2: Current Measurement Circuit

Automatic Synchronous Rectification

When driving a current through an inductive load while the output MOSFETs are off, the recirculation current must continue flowing. This current typically passes through the MOSFET's body diodes. To prevent excess power dissipation in the body diodes, the MPQ6615-AEC1 implements automatic synchronous rectification.

When both the high-side MOSFET (HS-FET) and LS-FET turn off and the Sx voltage (V_{Sx}) is pulled to ground, the LS-FET turns on until its current approaches 0A or the HS-FET turns on. If V_{Sx} exceeds V_{IN}, the HS-FET turns on until its current approaches 0A or the LS-FET turns on.

nFAULT Output

The MPQ6615-AEC1 provides an nFAULT output pin that is pulled active low if a fault

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occurs (e.g. if an over-current [OC] or over-temperature [OT] fault occurs). nFAULT is an open-drain output that must be pulled up by an external pull-up resistor.

Input Under-Voltage Lockout (UVLO)

If the input voltage (V_{IN}) falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Over-Voltage Protection (OVP)

If V_{IN} exceeds the over-voltage protection (OVP) threshold, all output MOSFETs are disabled. The nFAULT pin is not pulled to active low. Operation resumes automatically when V_{IN} falls below the OVP threshold.

Thermal Shutdown

If the die temperature exceeds the safe limits, all output MOSFETs are disabled, and nFAULT is driven low. Once the die temperature falls to a safe level, operation resumes automatically.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by disabling its gate driver. If the OCP threshold is reached and lasts longer than the OCP deglitch time, all four output MOSFETs are disabled, the outputs are in a high-impedance (Hi-Z) state, and nFAULT is pulled low. During this time, synchronous rectification is used to decay the current.

If the OCMD pin is pulled to logic low or connected directly to GND, the device remains latched off until V_{IN} falls below the UVLO threshold. If OCMD is open or pulled to logic high, the outputs are disabled for 2ms, then enabled again automatically.

If an over-current (OC) fault occurs on either the HS-FET or LS-FET (e.g. a short to ground, supply, or across the motor winding occurs), an OC shutdown is triggered.

Figure 3 shows the OCP circuit for one output.

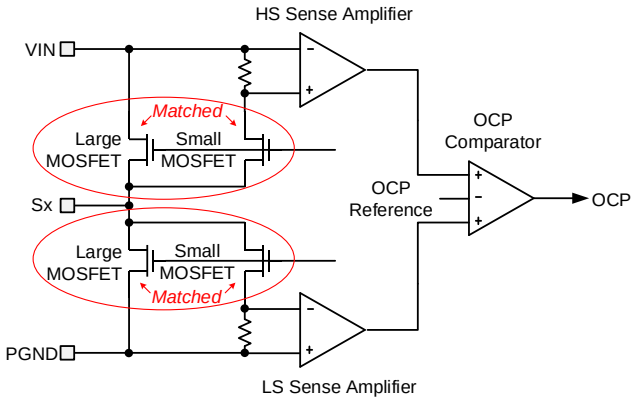


Figure 3: OCP Measurement Circuit

Charge Pump and VG Regulator

An internal LDO regulator generates a low-side gate driver voltage (about 5.5V). Place a 4.7µF to 10µF bypass capacitor between VG and ground.

A charge pump generates the gate driver voltage for the HS-FETs. The charge pump requires two external capacitors: a 0.1µF ceramic capacitor rated for ≥V_{IN} connected between the CP1 and CP2 pins, and a 1µF ceramic capacitor rated for ≥10V connected between the VIN and VCP pins.

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APPLICATION INFORMATION

Selecting the Charge Pump's External Capacitors

Table 4 lists the recommended external charge pump capacitors.

Table 4: Recommended External Charge Pump Capacitors

Charge Pump and VG Capacitors	Min	Typ	Max	Units
CP1 to CP2 capacitance		0.1		µF
CP1 to CP2 capacitor voltage	V_{IN}			V
VCP to VIN capacitance		1		µF
VCP to VIN capacitor voltage	10			V
VG capacitance	4.7		10	µF
VG capacitor voltage	10			V

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and Figure 5, and follow the guidelines below:

1. Place the supply bypass capacitors and charge pump capacitors as close to the IC as possible (ideally, place these capacitors on the same PCB layer between VIN and GND, VG and GND, CP1 and CP2, and VCP and VIN).
2. Supply bypass capacitors and charge pump capacitors can also be placed on the opposite side of the PCB directly under the IC. Use vias to make these connections.
3. Place as much copper on the long pads as possible.
4. Place large copper areas on the pads and on the same outer copper layer as the IC.
5. Place thermal vias inside the pad area to dissipate heat to the copper layers.
6. If via-in-pad construction is not possible, place multiple vias just outside the pad area.

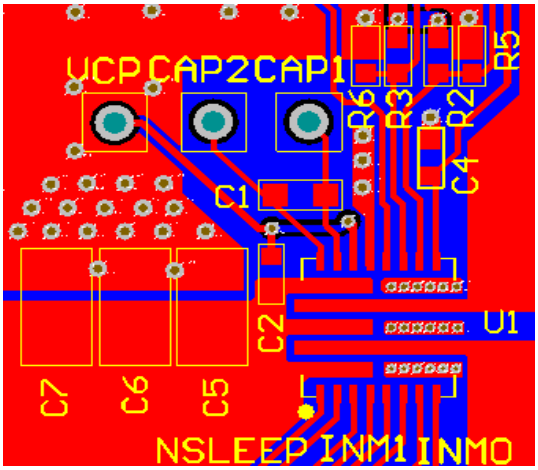


Figure 4: Recommended PCB Layout

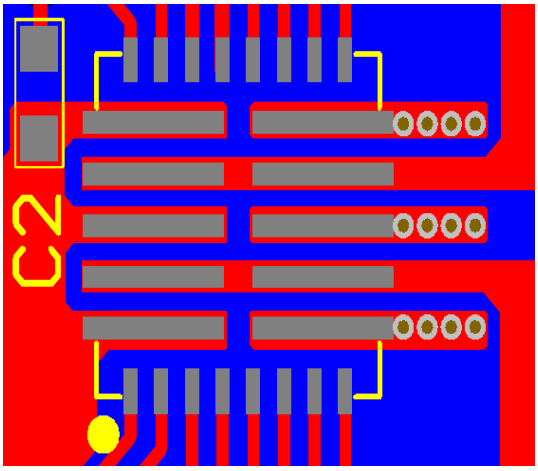


Figure 5: Thermal Vias outside the Pads

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TYPICAL APPLICATION CIRCUIT

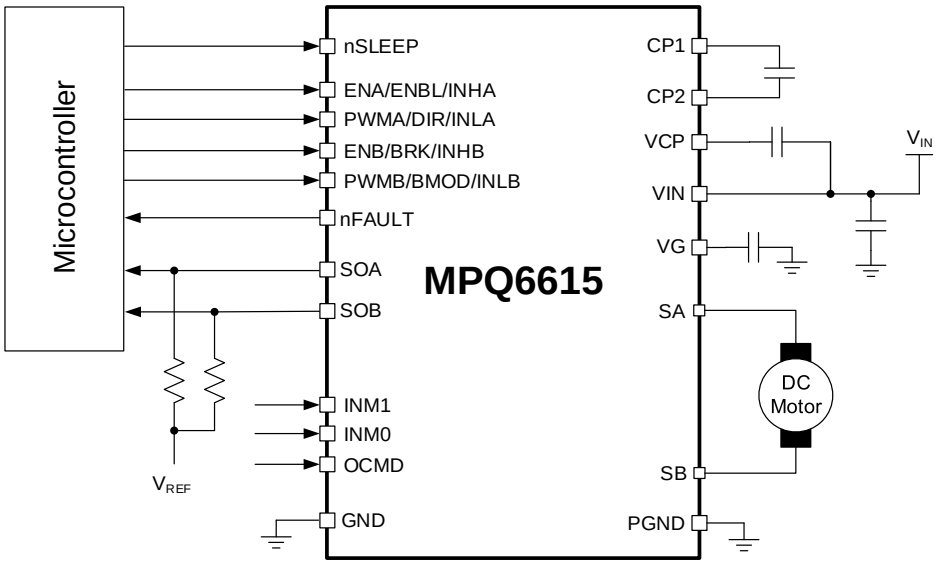
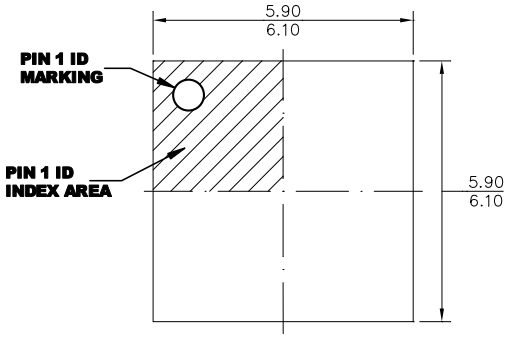


Figure 6: Typical Application Circuit

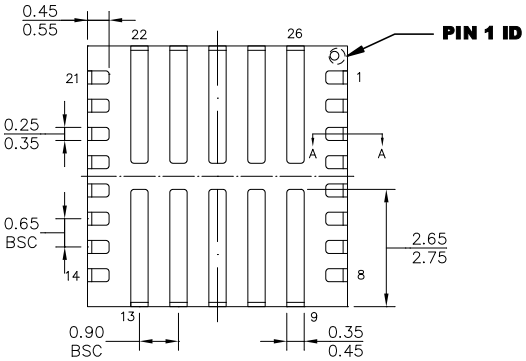
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PACKAGE INFORMATION

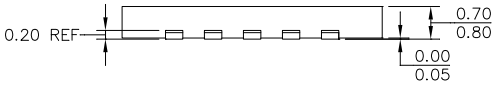
TQFN-26 (6mmx6mm)
Wettable Flank



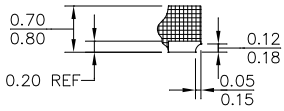
TOP VIEW



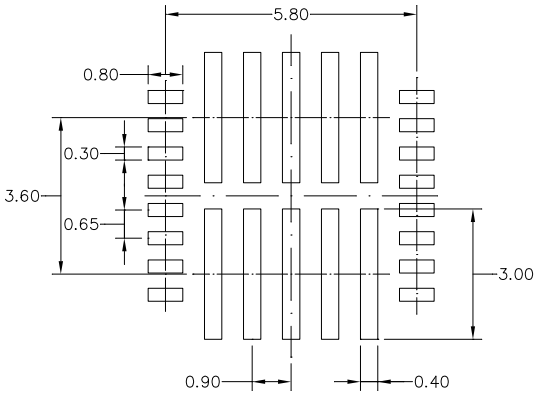
BOTTOM VIEW



SIDE VIEW



SECTION A-A



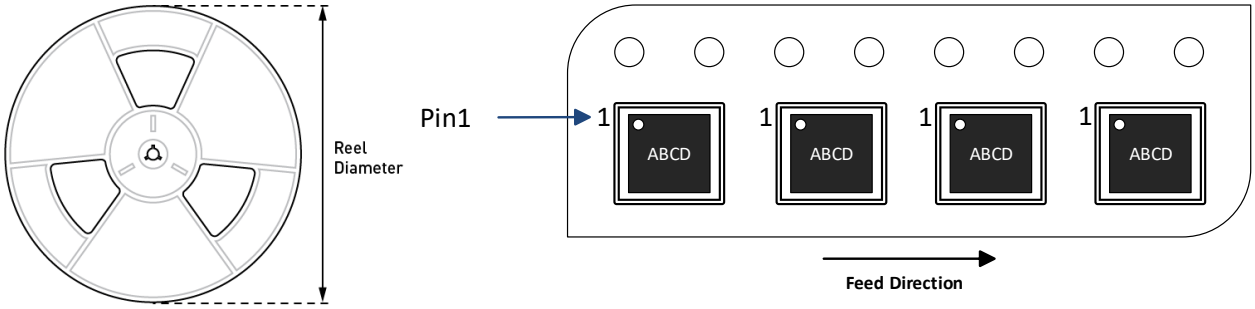
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6615GQKTE-AEC1-Z	TQFN-26 (6mmx6mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/21/2023	Initial Release	-

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