NTTFS5826NL

MOSFET – Power, Single, N-Channel, μ8FL
60 V, 24 mΩ

Features
- Small Footprint (3.3 x 3.3 mm) for Compact Designs
- Low $Q_{G(TOT)}$ to Minimize Switching Losses
- Low Capacitance to Minimize Driver Losses
- These are Pb−Free Devices

Applications
- Motor Drivers
- DC−DC Converters
- Synchronous Rectification
- Power Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\Psi J-mb}$ (Notes 1, 2, and 3)	Steady State	T_{mb} = 25°C	I_D	20	A
		T_{mb} = 100°C		14	
Power Dissipation $R_{\Psi J-mb}$ (Notes 1, 2, and 3)		T_{mb} = 25°C	P_D	19	W
		T_{mb} = 100°C		10	
Continuous Drain Current $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25°C	I_D	8	A
		T_A = 100°C		6	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 3)		T_A = 25°C	P_D	3.1	W
		T_A = 100°C		1.6	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	133	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	20	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, $I_{L(pk)}$ = 14.4 A, L = 1.0 mH, R_G = 25 Ω)			E_{AS}	20	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Mounting Board (top) − Steady State (Notes 2, 3)	$R_{\Psi J-mb}$	7.9	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	48	

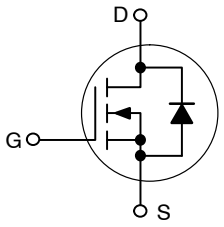
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

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$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
60 V	24 mΩ @ 10 V	20 A
	32 mΩ @ 4.5 V	

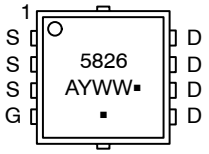
N−Channel





WDFN8
(μ8FL)
CASE 511AB

MARKING DIAGRAM



5826	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS5826NLTAG	WDFN8 (Pb−Free)	1500/Tape & Reel
NTTFS5826NLTWG	WDFN8 (Pb−Free)	5000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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2. Psi (Ψ) is used as required per JESD51−12 for packages in which substantially less than 100% of the heat flows to single case surface.
3. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				58.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 7.5 A		19	24	mΩ
		V_{GS} = 4.5 V	I_D = 7.5 A		25	32	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 5.0 A			8		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			850		pF
Output Capacitance	C_{oss}				85		
Reverse Transfer Capacitance	C_{rss}				50		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 5.0 A			8.4		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate−to−Source Charge	Q_{GS}				2.5		
Gate−to−Drain Charge	Q_{GD}				3.9		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48V, I_D = 5.0A			16	25	nC
Gate Resistance	R_G	T_A = 25°C			1.5		Ω
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 5.0 A, R_G = 2.5 Ω			9.0	18	ns
Rise Time	t_r				15	28	
Turn−Off Delay Time	$t_{d(off)}$				14	25	
Fall Time	t_f				5.4	12	
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 5.0 A, R_G = 2.5 Ω			7.0	12	ns
Rise Time	t_r				10	20	
Turn−Off Delay Time	$t_{d(off)}$				17	30	
Fall Time	t_f				3.5	6.0	
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 7.5 A	T_J = 25°C		0.8	2.3	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 5.0 A			15		ns
Charge Time	t_a				12		
Discharge Time	t_b				4		
Reverse Recovery Charge	Q_{RR}				13		nC

4. Pulse Test: pulse width = 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

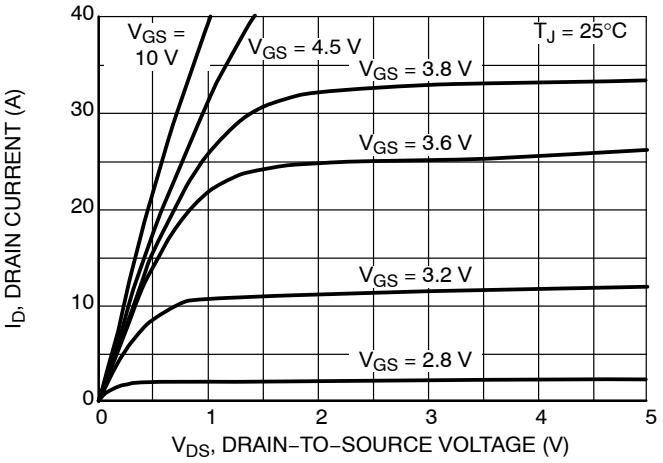


Figure 1. On−Region Characteristics

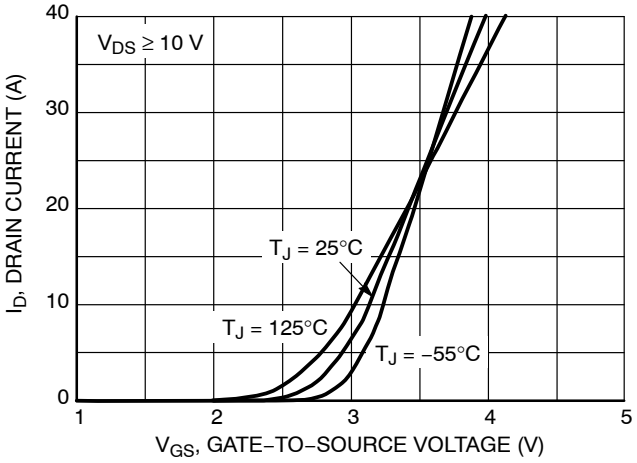


Figure 2. Transfer Characteristics

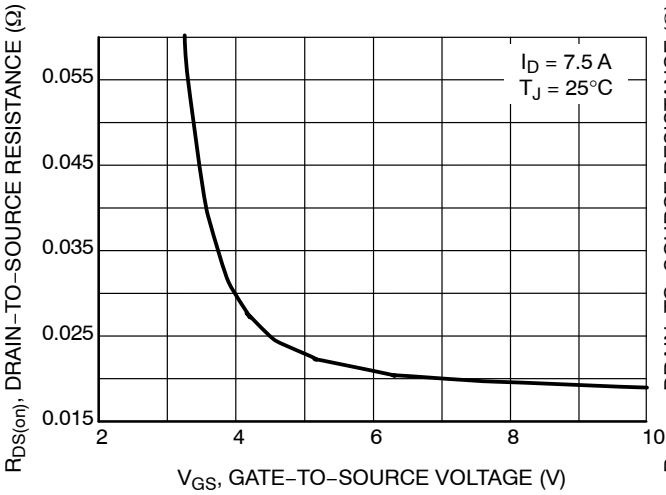


Figure 3. On−Resistance vs. Gate−to−Source Voltage

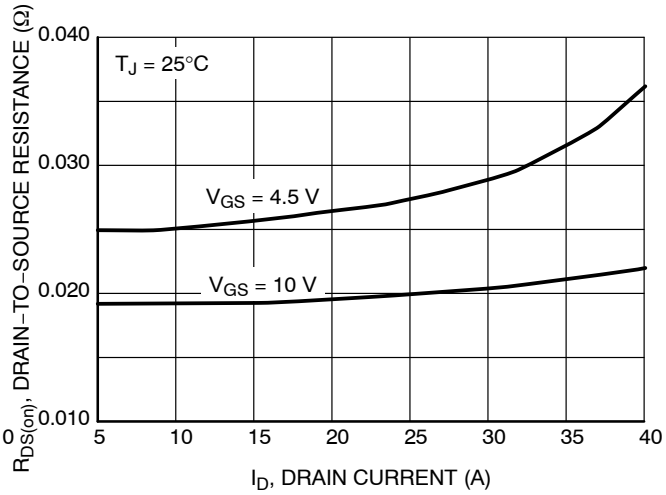


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

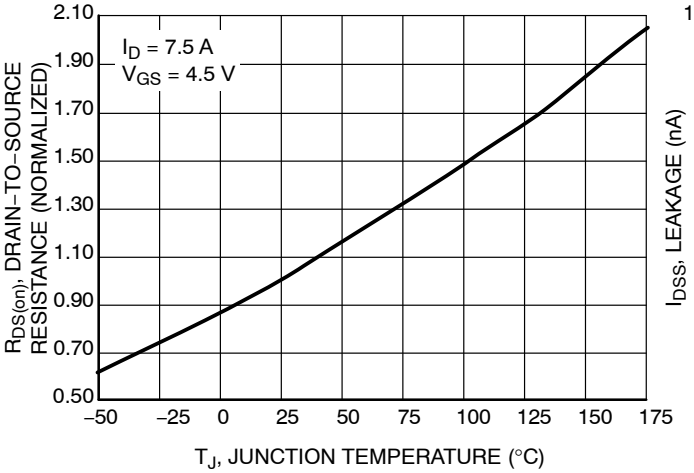


Figure 5. On−Resistance Variation with Temperature

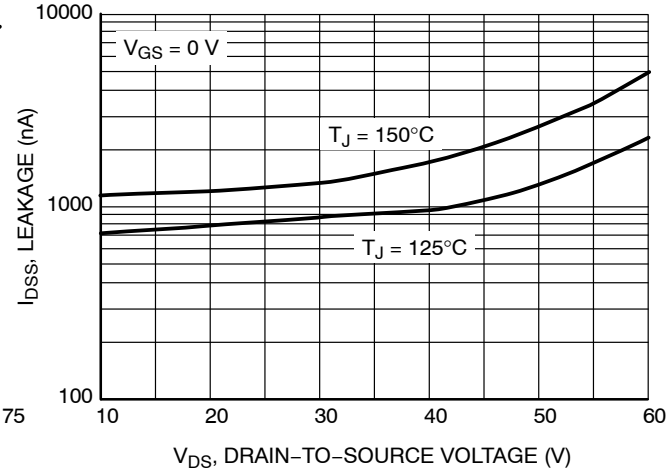


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

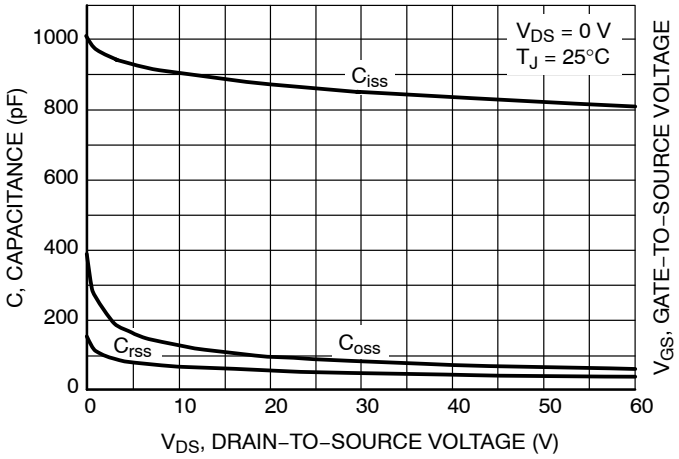


Figure 7. Capacitance Variation

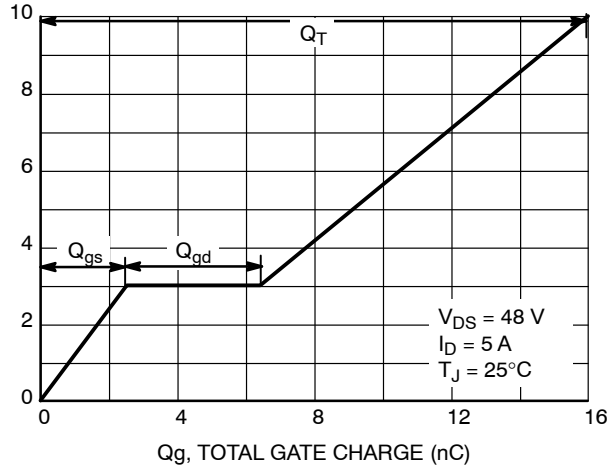


Figure 8. Gate−to−Source vs. Total Charge

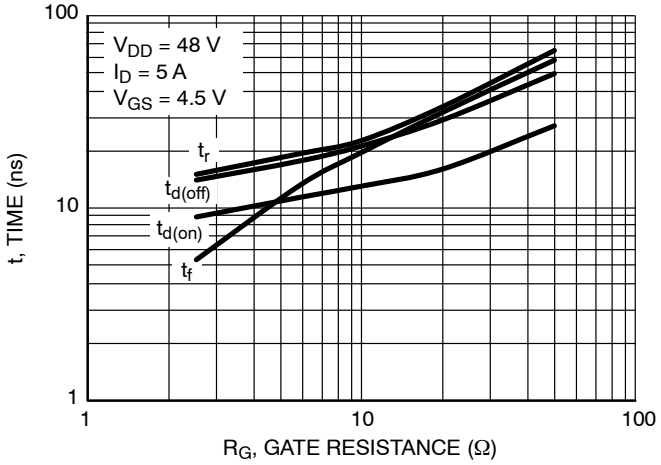


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

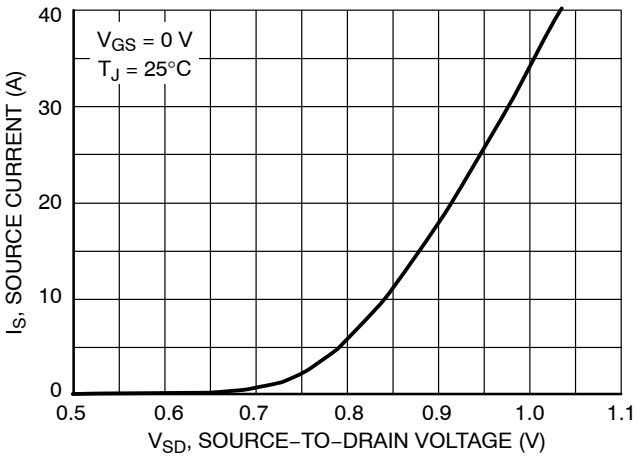


Figure 10. Diode Forward Voltage vs. Current

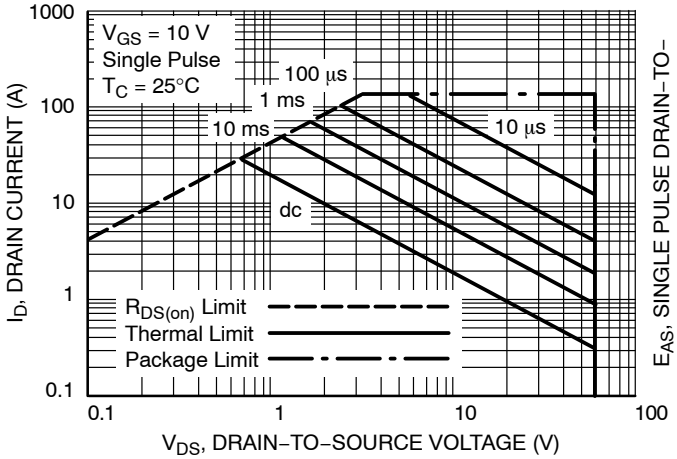


Figure 11. Maximum Rated Forward Biased Safe Operating Area

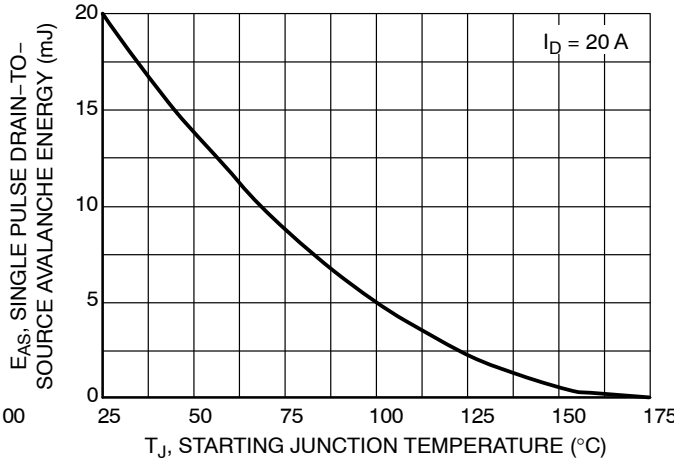


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

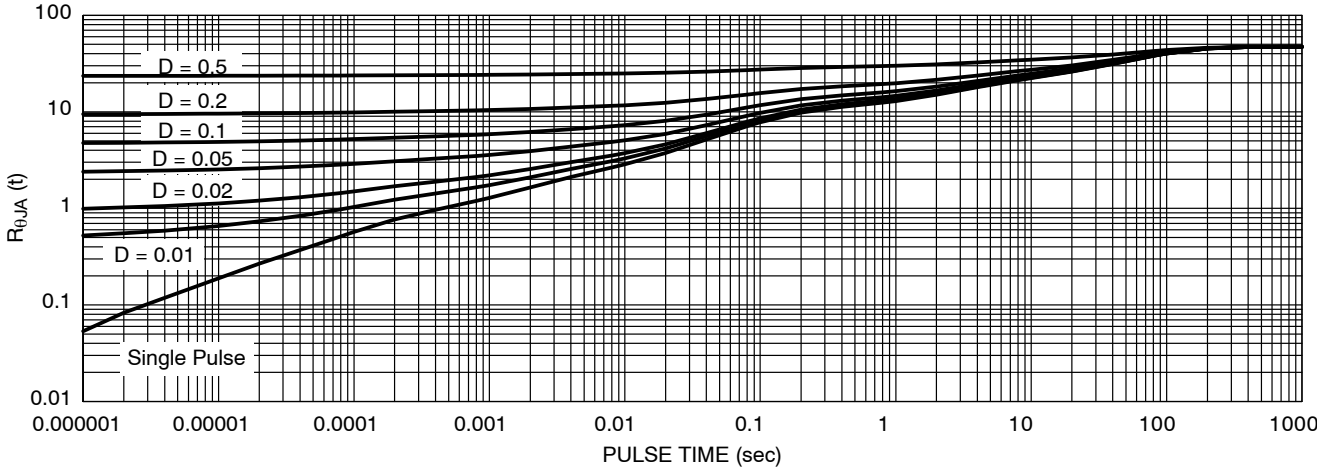


Figure 13. Thermal Response

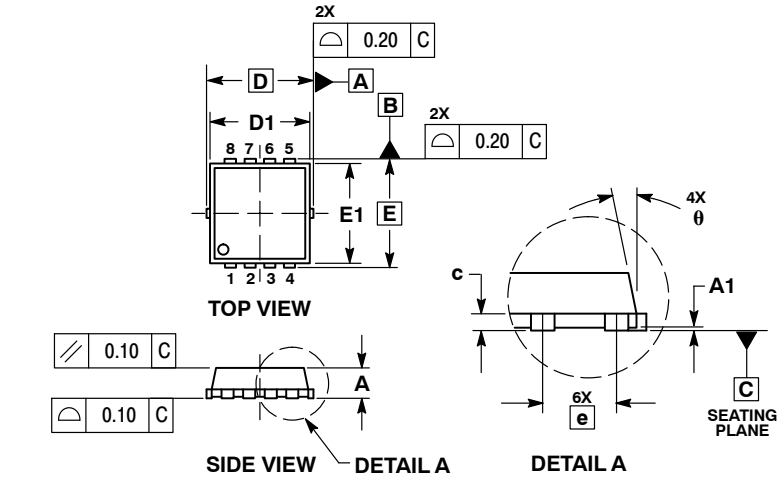
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 2:1

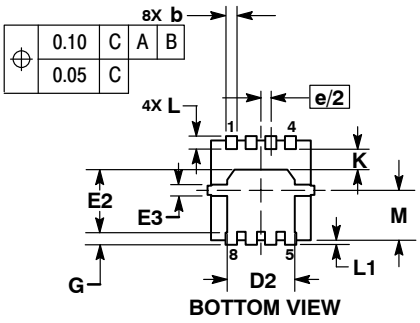
WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

DATE 23 APR 2012

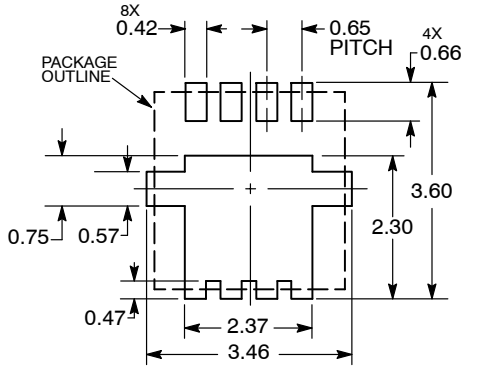


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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