NCP81382

Integrated Driver and MOSFET

The NCP81382 integrates a MOSFET driver, high−side MOSFET and low−side MOSFET into a single package.

The driver and MOSFETs have been optimized for high−current DC−DC buck power conversion applications. The NCP81382 integrated solution greatly reduces package parasitics and board space compared to a discrete component solution.

Features

- Capable of Average Currents up to 35 A
- Capable of Switching at Frequencies up to 2 MHz
- Capable of Peak Currents up to 70 A
- Compatible with 3.3 V or 5 V PWM Input
- Responds Properly to 3−level PWM Inputs
- Option for Zero Cross Detection with 3−level PWM
- ZCD_EN Input for Diode Emulation with 2−level PWM
- Internal Bootstrap Diode
- Undervoltage Lockout
- Supports Intel® Power State 4
- Thermal Warning output
- Thermal Shutdown
- This is a Pb−Free Device

Applications

- Desktop & Notebook Microprocessors

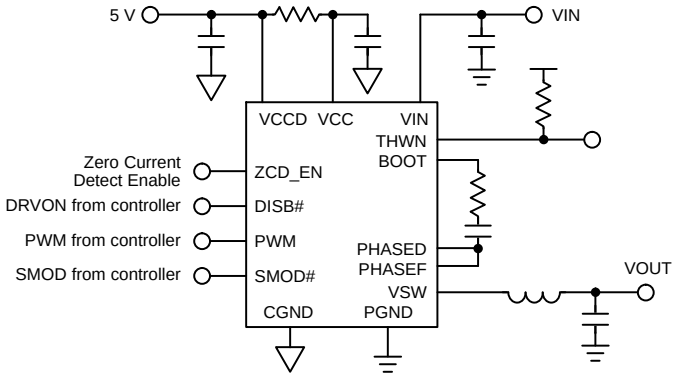

Figure 1. Application Schematic

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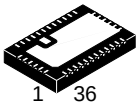
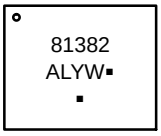
MARKING DIAGRAM



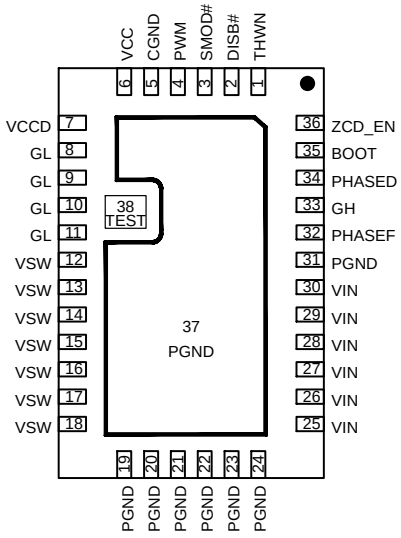
QFN36 6x4
CASE 485DZ



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81382MNTXG	QFN36 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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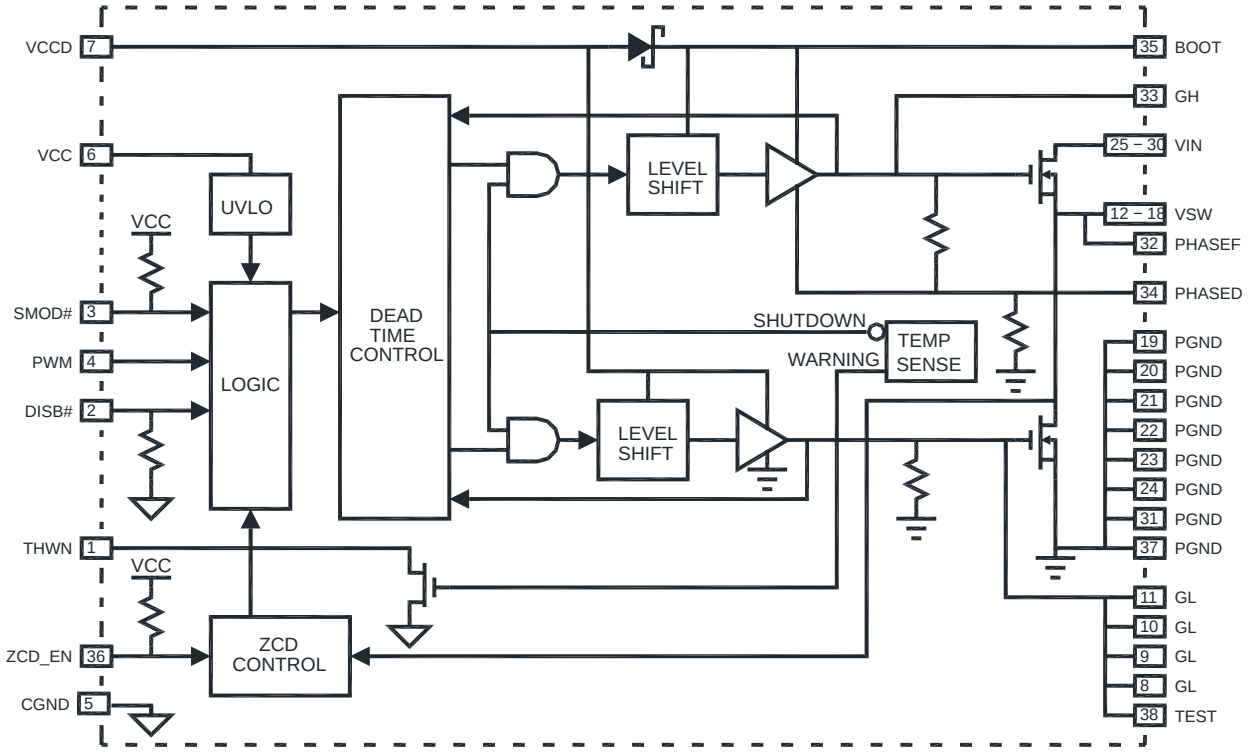

Figure 2. Block Diagram

PIN LIST AND DESCRIPTIONS

Pin No.	Symbol	Description
1	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver die reaches T_{THWN}, this pin is pulled low.
2	DISB#	Output disable pin. When this pin is pulled to a logic high level, the driver is enabled. There is an internal pull−down resistor on this pin.
3	SMOD#	Skip Mode pin. 3−state input (see Table 1 LOGIC TABLE): SMOD# = High → States of ZCD_EN and PWM determine whether the NCP81382 performs ZCD or not. SMOD# = Mid → Connects PWM to internal resistor divider placing a bias voltage on PWM pin. Otherwise, logic is equivalent to SMOD# in the high state. SMOD# = Low → Placing PWM into mid−state pulls GH and GL low without delay. There is an internal pull−up resistor to VCC on this pin.
4	PWM	PWM Control Input and Zero Current Detection Enable
5	CGND	Signal Ground
6	VCC	Control Power Supply Input
7	VCCD	Driver Power Supply Input
8	GL	Low Side FET Gate Access
9	GL	Low Side FET Gate Access
10	GL	Low Side FET Gate Access
11	GL	Low Side FET Gate Access
12	VSW	Switch Node Output
13	VSW	Switch Node Output
14	VSW	Switch Node Output
15	VSW	Switch Node Output
16	VSW	Switch Node Output
17	VSW	Switch Node Output
18	VSW	Switch Node Output

PIN LIST AND DESCRIPTIONS (continued)

Pin No.	Symbol	Description
19	PGND	Power Ground
20	PGND	Power Ground
21	PGND	Power Ground
22	PGND	Power Ground
23	PGND	Power Ground
24	PGND	Power Ground
25	VIN	Conversion Supply Power Input
26	VIN	Conversion Supply Power Input
27	VIN	Conversion Supply Power Input
28	VIN	Conversion Supply Power Input
29	VIN	Conversion Supply Power Input
30	VIN	Conversion Supply Power Input
31	PGND	Power Ground
32	PHASEF	Bootstrap Capacitor Return (must be connected to PHASED)
33	GH	High Side FET Gate Access
34	PHASED	Driver Phase Connection (must be connected to PHASEF)
35	BOOT	Bootstrap Voltage
36	ZCD_EN	PWM drive logic and zero current detection enable. 3−state input: PWM = High → GH is high, GL is low. PWM = Mid → Diode emulation mode. PWM = Low → GH is low. State of GL is dependent on states of SMOD# and ZCD_EN (see Table 1 LOGIC TABLE).
37	PGND	Power Ground
38	TEST	No connection should be made to this pin. No pad is needed on the PCB footprint

ABSOLUTE MAXIMUM RATINGS (Electrical Information − all signals referenced to PGND unless noted otherwise) (Note 1)

Pin Name	Min	Max	Unit
VCC, VCCD	−0.3	6.5	V
GH to PHASED (DC)	−0.3	$V_{BOOT} - V_{SW} + 0.3$	V
GH to PHASED (< 50 ns)	−5.0	7.7	V
VIN	−0.3	30	V
BOOT (DC)	−0.3	35	V
BOOT (< 20 ns)	−0.3	40	V
BOOT to PHASED (DC)	−0.3	6.5	V
VSW, PHASED, PHASEF (DC)	−0.3	30	V
VSW, PHASED, PHASEF (< 20 ns)	−1.0	−	V
VSW, PHASED, PHASEF (< 5 ns)	−5.0	37	V
All Other Pins	−0.3	$V_{VCC} + 0.3$	V
Single−Pulse Drain−to−Source Avalanche Energy, High−Side FET (T_J = 25°C, V_{GS} = 5 V, L = 0.1 mH, R_G = 25 Ω, I_L = 54 A_{PK})	−	144	mJ
Single−Pulse Drain−to−Source Avalanche Energy, Low−Side FET (T_J = 25°C, V_{GS} = 5 V, L = 0.3 mH, R_G = 25 Ω, I_L = 31.5 A_{PK})	−	180	mJ
Single−Pulse Drain−to−Source Avalanche Energy, High−Side FET (T_J = 25°C, L = 0.15 μH, I_L = 90 A_{PK}, V_{DS} dV/dt= 30 V / 2 ns)	−	200	μJ
Single−Pulse Drain−to−Source Avalanche Energy, Low−Side FET (T_J = 25°C, L = 150 nH, I_L = 90 A_{PK}, V_{DS} dV/dt= 30 V / 4 ns)	−	200	μJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Absolute Maximum Ratings are not tested in production.

THERMAL INFORMATION

Rating	Symbol	Value	Unit
Thermal Resistance	θ_{JA}	22	°C/W
	$R\Psi_{J-BT}$	2	°C/W
	$R\Psi_{J-CT}$	4	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−40 to +150	°C
Operating Ambient Temperature Range		−40 to +125	°C
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Maximum Power Dissipation		10	W
Moisture Sensitivity Level	MSL	3	

2. The maximum package power dissipation must be observed.
3. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
4. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Conditions	Min	Typ	Max	Unit
Supply Voltage Range	VCC, VCCD		4.5	5.0	5.5	V
Conversion Voltage	VIN		4.5	12	20	V
Continuous Output Current		F_{SW} = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.1 V			30	A
		F_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 1.1 V			35	A
Peak Output Current		F_{SW} = 500 kHz, V_{IN} = 12 V, V_{OUT} = 1.1 V, Duration = 10 ms, Period = 1 s			70	A
Operating Temperature			−40		100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC SUPPLY CURRENT						
Operating		DISB# = 5 V, ZCD_EN = 5 V, PWM = 400 kHz	−	1	2	mA
No switching, ZCD enabled		DISB# = 5 V, ZCD_EN = 5 V, PWM = 0 V	−	−	2	mA
No switching, ZCD disabled		DISB# = 5 V, ZCD_EN = 0 V, PWM = 0 V	−	−	1.8	mA
Disabled		DISB# = 0 V ZCD_EN = VCC, SMOD# = VCC	−	0.1	1	μA
		DISB# = 0 V ZCD_EN = VCC, SMOD# = GND		10	13	μA
		DISB# = 0 V ZCD_EN = SMOD# = GND	−	27	40	μA
UVLO Start Threshold	V_{UVLO}	VCC rising	2.9	−	3.3	V
UVLO Hysteresis			150	−	−	mV
VCCD SUPPLY CURRENT						
Operating		DISB# = 5 V, ZCD_EN = 5 V, PWM = 400 kHz	−	−	20	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCCD SUPPLY CURRENT						
Enabled, No switching		DISB# = 5 V, PWM = 0 V, V_{PHASED} = 0 V	–	175	300	μA
Disabled		DISB# = 0 V	–	0.1	1	μA
DISB# INPUT						
Input Resistance		To Ground, @ 25°C	–	461	–	kΩ
Upper Threshold	V_{UPPER}		–	–	2.0	V
Lower Threshold	V_{LOWER}		0.8	–	–	V
Hysteresis		V_{UPPER} – V_{LOWER}	200	–	–	mV
Enable Delay Time	t_{ENABLE}	Time from DISB# transitioning HI to when VSW responds to PWM.	–	–	40	μs
Disable Delay Time	$t_{DISABLE}$	Time from DISB# transitioning LOW to when both output FETs are off.	–	25	50	ns
PWM INPUT						
Input High Voltage	V_{PWM_HI}		2.65	–	–	V
Input Mid−state Voltage	V_{PWM_MID}		1.4	–	2.0	V
Input Low Voltage	V_{PWM_LO}		–	–	0.7	V
Input Resistance	R_{PWM_HIZ}	SMOD# = $V_{SMOD\#_HI}$ or $V_{SMOD\#_LO}$	10	–	–	MΩ
Input Resistance	R_{PWM_BIAS}	SMOD# = $V_{SMOD\#_MID}$	–	63	–	kΩ
PWM Input Bias Voltage	V_{PWM_BIAS}	SMOD# = $V_{SMOD\#_MID}$	–	1.7	–	V
PWM Propagation Delay, Rising	$tpdl_{GL}$	PWM = 2.25 V to GL = 90%; SMOD# = LOW	–	25	35	ns
PWM Propagation Delay, Falling	$tpdl_{GH}$	PWM = 0.75 V to GH = 90%	–	15	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−Low	$T_{PWM_EXIT_L}$	PWM = Mid−to−Low to GL = 10%, ZCD_EN = High	–	13	25	ns
Exiting PWM Mid−state Propagation Delay, Mid−to−High	$T_{PWM_EXIT_H}$	PWM = Mid−to−High to GH = 10%	–	13	25	ns
SMOD# INPUT						
SMOD# Input Voltage High	V_{SMOD_HI}		2.65	–	–	V
SMOD# Input Voltage Mid−state	$V_{SMOD\#_MID}$		1.4	–	2.0	V
SMOD# Input Voltage Low	V_{SMOD_LO}		–	–	0.7	V
SMOD# Input Resistance	$R_{SMOD\#_UP}$	Pull−up resistance to VCC	–	440	–	kΩ
SMOD# Propagation Delay, Falling	$T_{SMOD\#_PD_F}$	SMOD# = Low to GL = 90%, PWM = Low	–	26	30	ns
SMOD# Propagation Delay, Rising	$T_{SMOD\#_PD_R}$	SMOD# = High to GL = 10%, ZCD_EN = High, PWM = Low	–	15	30	ns
ZCD_EN INPUT						
ZCD_EN Input Voltage High	$V_{ZCD_EN_HI}$		2.0	–	–	V
ZCD_EN Input Voltage Low	$V_{ZCD_EN_LO}$		–	–	0.8	V
ZCD_EN Hysteresis	$V_{ZCD_EN_HYS}$		–	250	–	mV
ZCD_EN Input Resistance	$R_{ZCD_EN_PU}$	to VCC	–	270	–	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (continued)
(V_{VCC} = V_{VCCD} = 5.0 V, V_{VIN} = 12 V, $V_{DISB\#}$ = 2.0 V, C_{VCCD} = C_{VCC} = 0.1 μF unless specified otherwise) Min/Max values are valid for the temperature range −40°C ≤ T_A ≤ 125°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ZCD_EN INPUT						
ZCD_EN Propagation Delay, Rising	T_{ZCD_EN,PD_R}	SMOD# = High, ZCD_EN = High to GL = 10%	−	40	45	ns
ZCD_EN Propagation Delay, Falling	T_{ZCD_EN,PD_F}	SMOD# = High, ZCD_EN = Low to GL = 90%	−	25	40	ns
ZCD FUNCTION						
Zero Cross Detect Threshold	V_{ZCD}		−	−6.5	−	mV
ZCD Blanking + Debounce Time	t_{BLNK}		−	330	−	ns
NON−OVERLAP DELAYS						
Non−overlap Delay, Leading Edge	$tpdh_{GH}$	GL Falling = 1 V to GH−VSW Rising = 1 V	−	13	−	ns
Non−overlap Delay, Trailing Edge	$tpdh_{GL}$	GH−VSW Falling = 1 V to GL Rising = 1 V	−	12	−	ns
THERMAL WARNING & SHUTDOWN						
Thermal Warning Temperature	T_{THWN}	Temperature at Driver Die	−	150	−	°C
Thermal Warning Hysteresis	T_{THWN_HYS}		−	15	−	°C
Thermal Shutdown Temperature	T_{THDN}	Temperature at Driver Die	−	180	−	°C
Thermal Shutdown Hysteresis	T_{THDN_HYS}		−	25	−	°C
THWN Open Drain Current	I_{THWN}		−	−	5	mA
BOOSTSTRAP DIODE						
Forward Voltage		Forward Bias Current = 2.0 mA	−	300	−	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

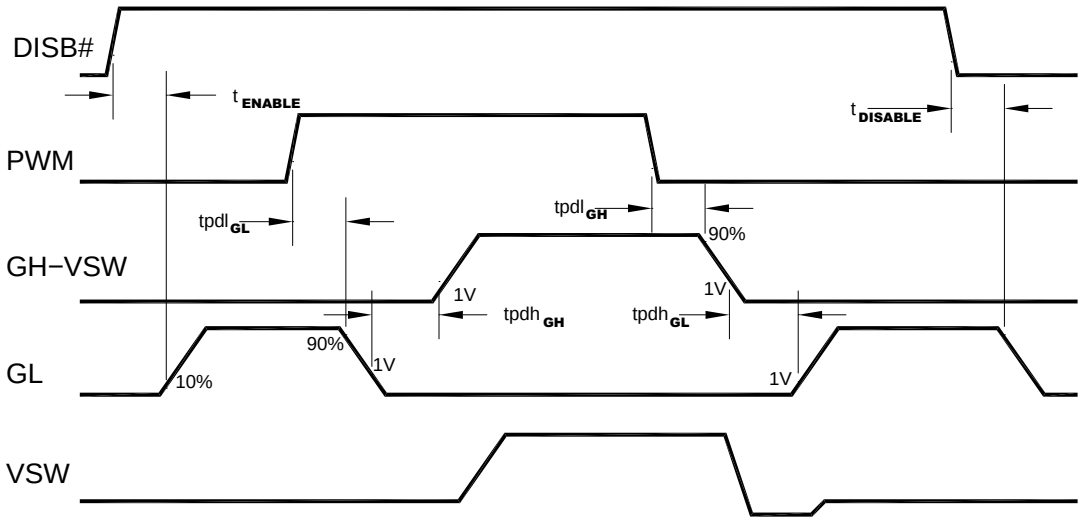

Figure 3. Timing Diagram

Table 1. LOGIC TABLE

INPUT TRUTH TABLE					
DISB#	**PWM**	**SMOD#** (Note 5)	**ZCD_EN**	**GH**	**GL**
L	X	X	X	L	L
H	H	X	X	H	L
H	L	X	L	L	L
H	L	X	H	L	H
H	MID	H or MID	H	L	ZCD (Note 6)
H	MID	X	L	L	L (Note 7)
H	MID	L	X	L	L (Note 7)

5. PWM input is driven to mid−state with internal divider resistors when SMOD# is driven to mid−state and PWM input is undriven externally.
6. GL goes low following 80 ns de−bounce time, 250 ns blanking time and then SW exceeding ZCD threshold.
7. There is no delay before GL goes low.

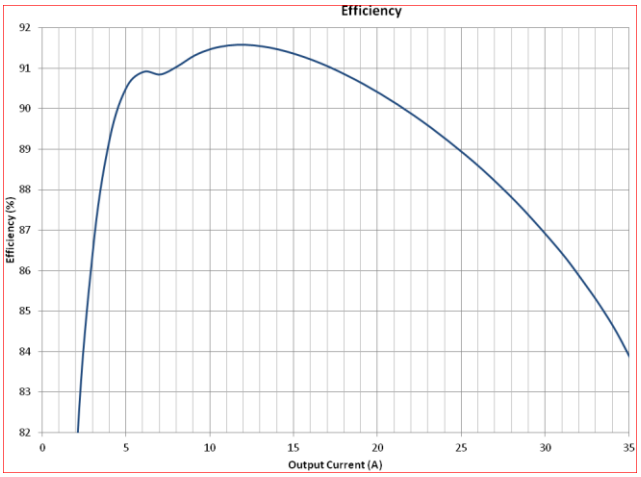

Figure 4. Efficiency − 12 V Input, 1.2 V Output, 500 kHz



Figure 5. Efficiency − 19 V Input, 1.2 V Output, 500 kHz

APPLICATIONS INFORMATION

Theory of Operation

The NCP81382 is an integrated driver and MOSFET module designed for use in a synchronous buck converter topology. The NCP81382 supports numerous application control definitions including ZCD (Zero Current Detect) with Pin enable and alternately PWM Tristate control. A PWM input signal is required to control the drive signals to the high−side and low−side integrated MOSFETs.

Low−Side Driver

The low−side driver drives an internal, ground−referenced low−R_{DS}(on) N−Channel MOSFET. The voltage supply for the low−side driver is internally connected to the VCCD and PGND pins.

High−Side Driver

The high−side driver drives an internal, floating low−R_{DS}(on) N−channel MOSFET. The gate voltage for the high side driver is developed by a bootstrap circuit referenced to Switch Node (VSW, PHASEF and PHASED) pins.

The bootstrap circuit is comprised of the integrated diode and an external bootstrap capacitor and resistor. When the NCP81382 is starting up, the VSW pin is at ground, allowing the bootstrap capacitor to charge up to VCCD through the bootstrap diode (See Figure 1). When the PWM input is driven high, the high−side driver will turn on the high−side MOSFET using the stored charge of the bootstrap capacitor. As the high−side MOSFET turns on, the voltage at the VSW, PHASEF and PHASED pins rise. When the high−side MOSFET is turned fully on, the switch node will settle to VIN and the BST pin will settle to VIN + VCCD (excluding parasitic ringing).

Bootstrap Circuit

The bootstrap circuit relies on an external charge storage capacitor (C_{BST}) and an integrated diode to provide current to the HS Driver. A multi−layer ceramic capacitor (MLCC) with a value greater than 100 nF should be used as the bootstrap capacitor. An 4 Ω resistor in series with C_{BST} is recommended to decrease VSW overshoot.

Power Supply Decoupling

The NCP81382 will source relatively large currents into the MOSFET gates. In order to maintain a constant and stable supply voltage (VCCD) a low−ESR capacitor should be placed near the power and ground pins. A multi layer ceramic capacitor (MLCC) between 1 μF and 4.7 μF is typically used.

A separate supply pin (VCC) is used to power the analog and digital circuits within the driver. A 1 μF ceramic capacitor should be placed on this pin in close proximity to the NCP81382. It is good practice to separate the VCC and VCCD decoupling capacitors with a resistor (10 Ω typical) to avoid coupling driver noise to the analog and digital circuits that control driver function (See Figure 1).

Safety Timer and Overlap Protection Circuit

It is important to avoid cross−conduction of the two MOSFETS which could result in a decrease in the power conversion efficiency or damage to the device.

The NCP81382 prevents cross conduction by monitoring the status of the MOSFET gates and applying the appropriate amount of non−overlap time (the time between the turn−off of one MOSFET and the turn−on of the other MOSFET). When the PWM input pin is driven high, the low−side MOSFET gate (GL) starts to go low after a propagation delay ($tpdl_{GL}$). The time it takes for the low−side MOSFET to turn off is dependent on the low−side MOSFET gate charge. The high−side MOSFET gate begins to rise a fixed time ($tpdh_{GH}$) after the GL voltage falls below the low−side MOSFET gate threshold.

When the PWM input pin is driven low, the high−side MOSFET gate (GH) starts to go low after a propagation delay ($tpdl_{GH}$). The time it takes for the high−side MOSFET to turn off is dependent on the high−side MOSFET gate charge. The low−side MOSFET gate begins to rise a fixed time ($tpdh_{GH}$) after the GH voltage falls below the high−side MOSFET gate threshold.

Zero Current Detect Enable Input (ZCD_EN)

The ZCD_EN pin is a logic input pin with an internal pull−up resistance to VCC.

When ZCD_EN is set low, the NCP81382 will operate in synchronous rectifier (PWM) mode. This means that negative current can flow in the LS MOSFET if the load current is less than ½ delta current in the inductor. When ZCD_EN is set high, Zero Current Detect PWM (ZCD_PWM) mode will be enabled

With ZCD_EN set high, when PWM rises above V_{PWM_HI}, GL will go low and GH will go high after the non−overlap delay. Subsequently, if PWM falls to less than V_{PWM_HI}, but stays above V_{PWM_LO}, GL will go high after the non−overlap delay, and stay high for the duration of the ZCD Blanking + Debounce time (T_{BLNK}). Once this timer has elapsed, VSW will be monitored for zero current, and GL will be pulled low when zero current is detected. The VSW zero current threshold undergoes an auto−calibration cycle every time DISB# is brought from low to high.

PWM Input

The PWM Input pin is a tri−state input used to control the HS MOSFET ON/OFF state. In conjunction with ZCD_EN it also determines the state of the LS MOSFET. See Table1 for logic operation. The PWM in some cases must operate with frequency programming resistances to ground. These resistances can range from 10 kΩ to 300 kΩ depending on the application. When SMOD# is set to > VSMOD#_HI or to < VSMOD#_LO, the input impedance to the PWM input is very high in order to avoid interferences with controllers that must use programming resistances on the PWM pin.

If $V_{SMOD\#_LO}$ < SMOD# < $V_{SMOD\#_HI}$ (Mid−State), internal resistances will set undriven PWM pin voltage to Mid−State.

Disable Input (DISB#)

The DISB# pin is used to disable the GH to the High−Side FET to prevent power transfer. The pin has a pull−down resistance to force a disabled state when it is left unconnected. DISB# can be driven from the output of a logic device or set high with a pull−up resistance to VCC.

VCC Undervoltage Lockout

The VCC pin is monitored by an Undervoltage Lockout Circuit (UVLO). VCC voltage above the rising threshold enables the NCP81382.

Table 2. UVLO/DISB# LOGIC TABLE

UVLO	DISB#	Driver State
L	X	Disabled (GH = GL = 0)
H	L	Disabled (GH = GL = 0)
H	H	Enabled (See Table x)
H	Open	Disabled (GH = GL = 0)

Thermal Warning/Thermal Shutdown Output

The THWN pin is an open drain output. When the temperature of the driver exceeds T_{THWN}, the THWN pin will be pulled low indicating a thermal warning. At this point, the part continues to function normally. When the temperature drops T_{THWN_HYS} below T_{THWN}, the THWN pin will go high. If the driver temperature exceeds T_{THDN}, the part will enter thermal shutdown and turn off both MOSFETs. Once the temperature falls T_{THDN_HYS} below T_{THDN}, the part will resume normal operation.

Skip Mode Input (SMOD#)

The SMOD# tri−state input pin has an internal pull−up resistance to VCC. When driven high, the SMOD# pin enables the low side synchronous MOSFET to operate independently of the internal ZCD function. When the SMOD# pin is set low during the PWM cycle it disables the low side MOSFET to allow discontinuous mode operation.

The NCP81382 has the capability of internally connecting a resistor divider to the PWM pin. To engage this mode, SMOD# needs to be placed into mid−state. While in SMOD# mid−state, the IC logic is equivalent to SMOD# being in the high state.

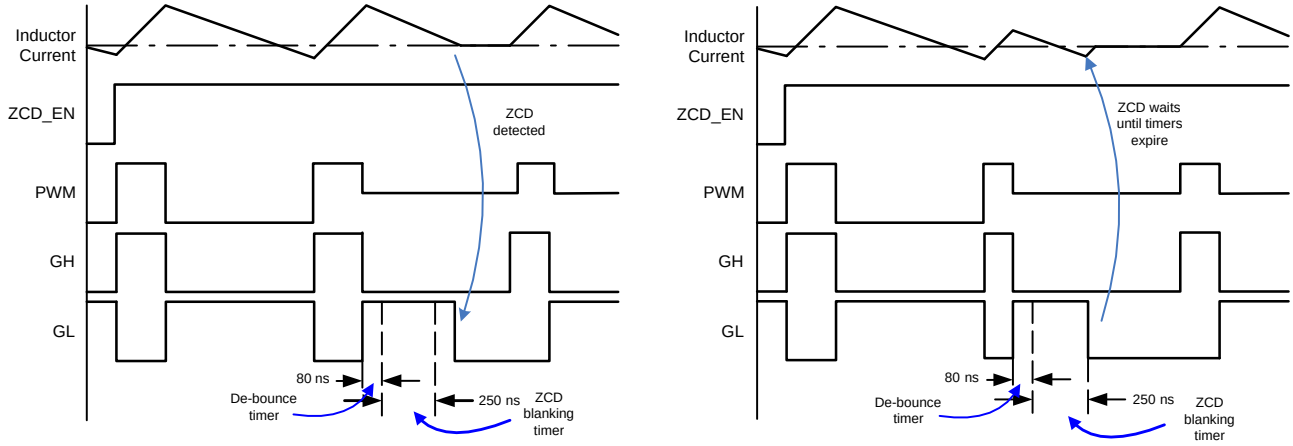

Figure 6. PWM Timing Diagram

NOTES: If the Zero Current Detect circuit detects zero current after the ZCD Wait timer period, the GL is driven low by the Zero Current Detect signal.
If the Zero Current Detect circuit detects zero current before the ZCD Wait timer period has expired, the Zero Current detect signal is ignored and the GL is driven low at the end of the ZCD Wait timer period.

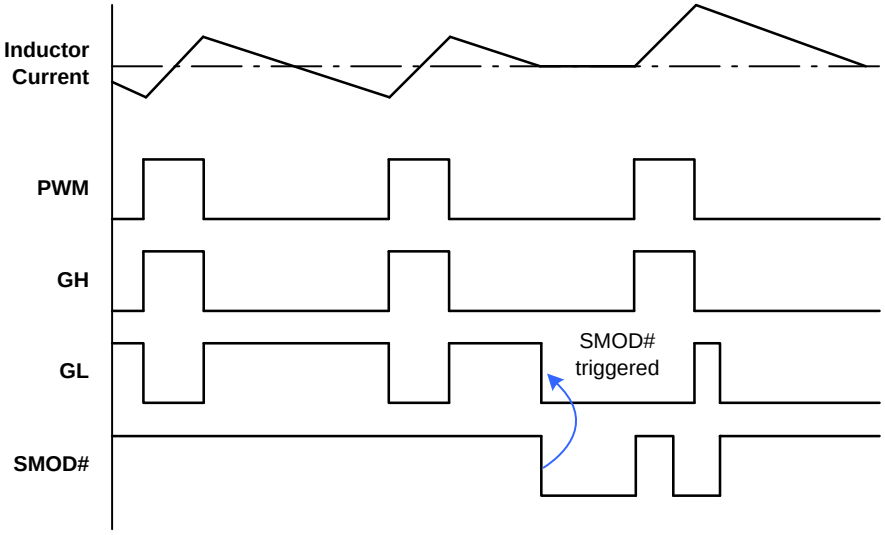

Figure 7. SMOD# Timing Diagram

NOTE: If the SMOD# input is driven low at any time after the GL has been driven high, the SMOD# Falling edge will trigger the GL to go low.
If the SMOD# input is driven low while the GH is high, the SMOD# input is ignored.

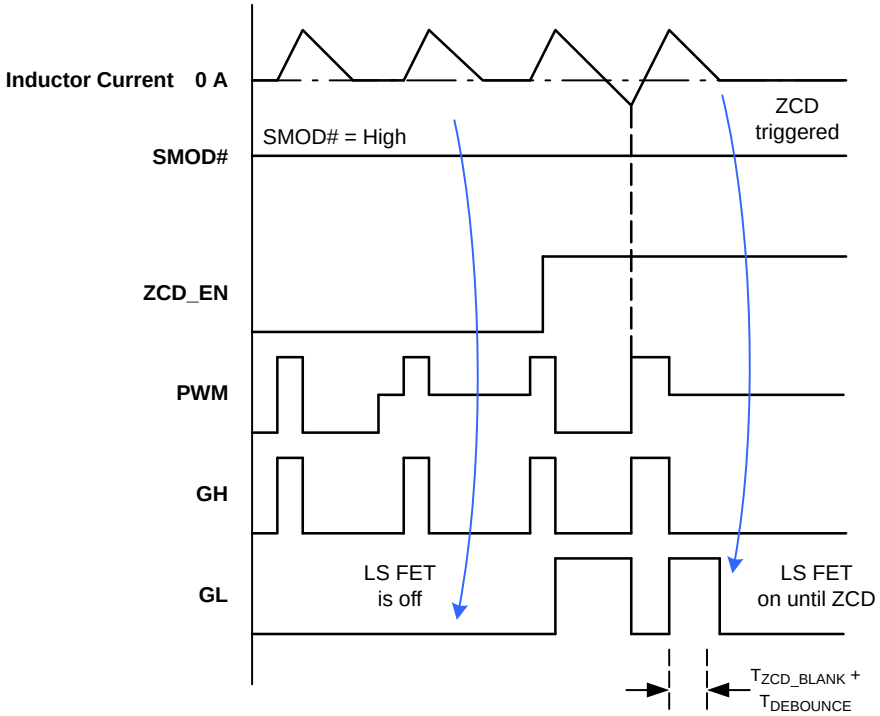

Figure 8. ZCD_EN Timing Diagram

NOTE: When ZCD is enabled by pulling ZCD_EN# high, the NCP81382 keeps the LS FET on until it detects zero current, reducing power loss.

For Use with Controllers with 3−State PWM and No Zero Current Detection Capability:

Table 3. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH NO ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	H	H	ON	OFF
M	H	H	OFF	ZCD
L	H	H	OFF	ON

This section describes operation with controllers that are capable of 3 states in their PWM output and relies on the NCP81382 to conduct zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to either be set to 5 V or left disconnected. The NCP81382 has an internal pull−up resistor that connects to VCC that sets SMOD# to the logic high state if this pin is disconnected.

The ZCD_EN pin needs to either be set to 5 V or left disconnected. The NCP81382 has an internal pull−up resistor connected to VCC that will set ZCD_EN to the logic high state if this pin is left disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. To enter into DCM, PWM needs to be switched to the mid−state.

Whenever PWM transitions to mid−state, GH turns off and GL turns on. GL stays on for the duration of the de−bounce timer and ZCD blanking timers. Once these timers expire, the NCP81382 monitors the SW voltage and turns GL off when SW exceeds the ZCD threshold voltage. By turning off the LS FET, the body diode of the LS FET allows any positive current to go to zero but prevents negative current from conducting.

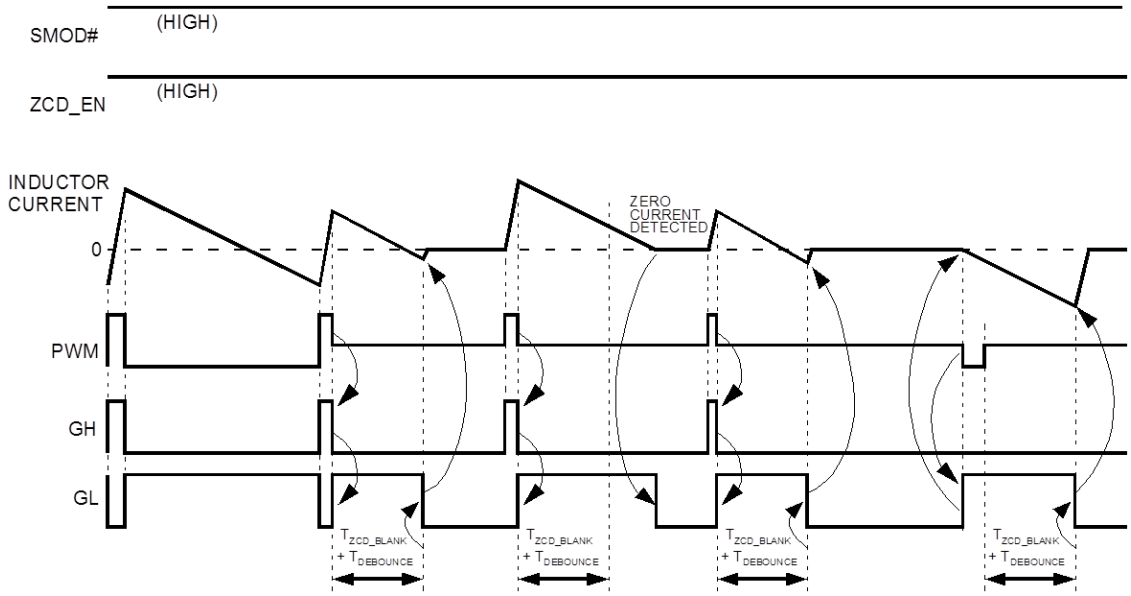

Figure 9. Timing Diagram − 3−state PWM Controller, No ZCD

For Use with Controllers with 3−state PWM and Zero Current Detection Capability:

Table 4. LOGIC TABLE − 3−STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	L	H	ON	OFF
M	L	H	OFF	OFF
L	L	H	OFF	ON

This section describes operation with controllers that are capable of 3 PWM output levels and have zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#_LO}$).

The ZCD_EN pin needs to either be set to 5 V or left disconnected. There is an internal pull−up resistor that connects to VCC and sets ZCD_EN to the logic high state if this pin is left disconnected.

To operate the buck converter in continuous conduction mode (CCM), PWM needs to switch between the logic high and low states. During DCM, the controller is responsible for detecting when zero current has occurred, and then notifying the NCP81382 to turn off the LS FET. When the controller detects zero current, it needs to set PWM to mid−state, which causes the NCP81382 to pull both GH and GL to their off states without delay.

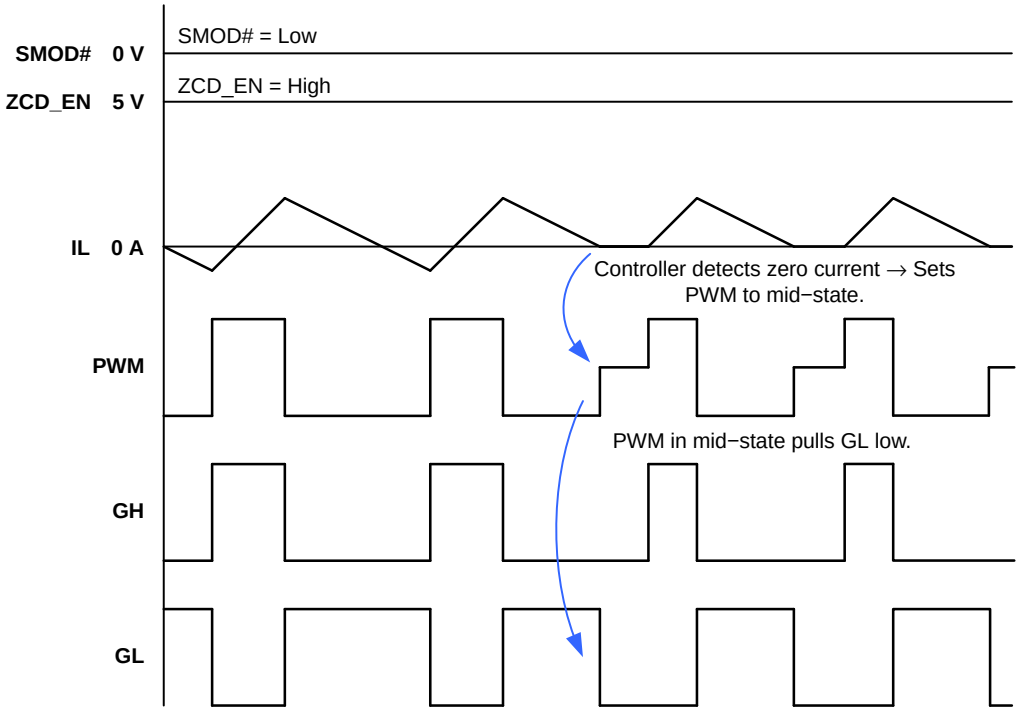

Figure 10. Timing Diagram − 3−state PWM Controller, with ZCD

For Use with Controllers with 2−Level PWM and Zero Current Detection Capability:

Table 5. LOGIC TABLE − 2−STATE PWM CONTROLLERS WITH ZCD

PWM	SMOD#	ZCD_EN	GH	GL
H	L	X	ON	OFF
L	L	H	OFF	ON
L	L	L	OFF	OFF

This section describes operation with controllers that do not have 3−level PWM output capability but are capable of zero current detection during discontinuous conduction mode (DCM).

The SMOD# pin needs to be pulled low (below $V_{SMOD\#_LO}$).

When PWM is high, GH will always be in the high state and GL will always be in the low state, regardless of the state ZCD_EN is in.

When PWM is in the low state, the state of ZCD_EN determines whether the converter is placed into diode emulation mode. When the controller detects positive inductor current, ZCD_EN should be in the high state, allowing the LS FET to be on and conducting. Once the controller detects zero or negative current, ZCD_EN should be placed into the low state, turning off the LS FET. With the LS FET turned off, the body diode of the LS FET allows any positive current that may still be flowing to reach zero, but prevents the current from flowing in the negative direction.

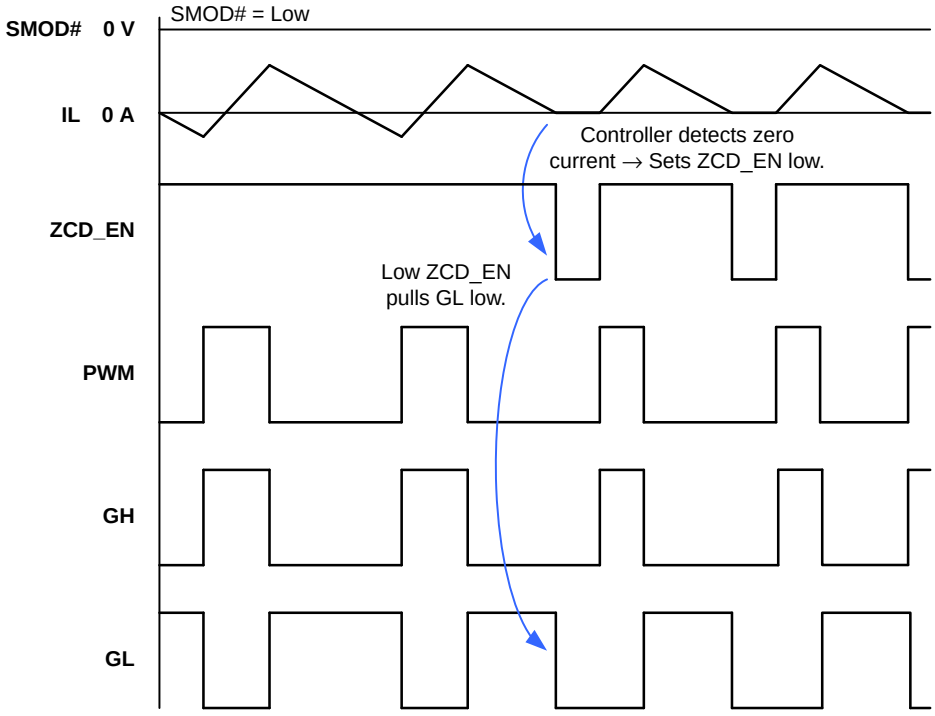

Figure 11. Timing Diagram − 2−state PWM Controller, with ZCD

Recommended PCB Layout
(viewed from top)

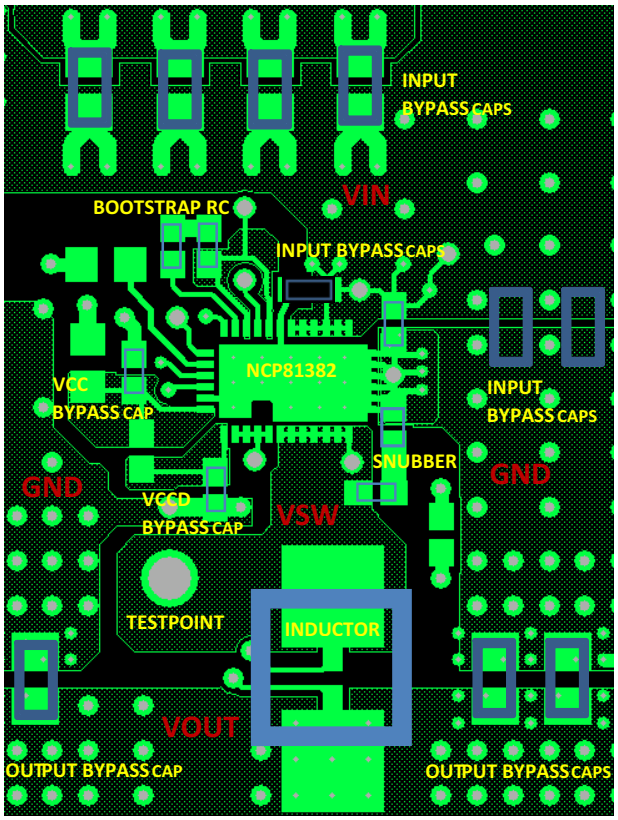

Figure 12. Top Copper Layer

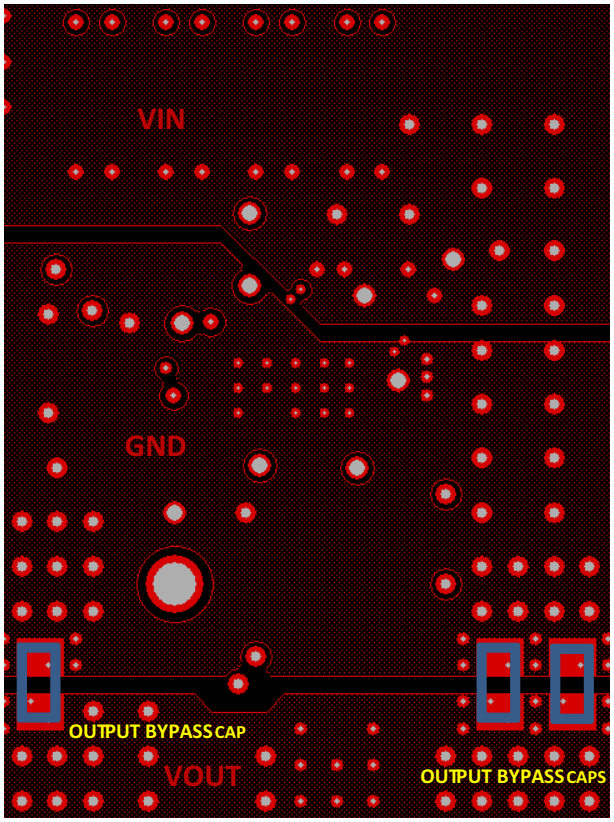

Figure 13. Bottom Copper Layer

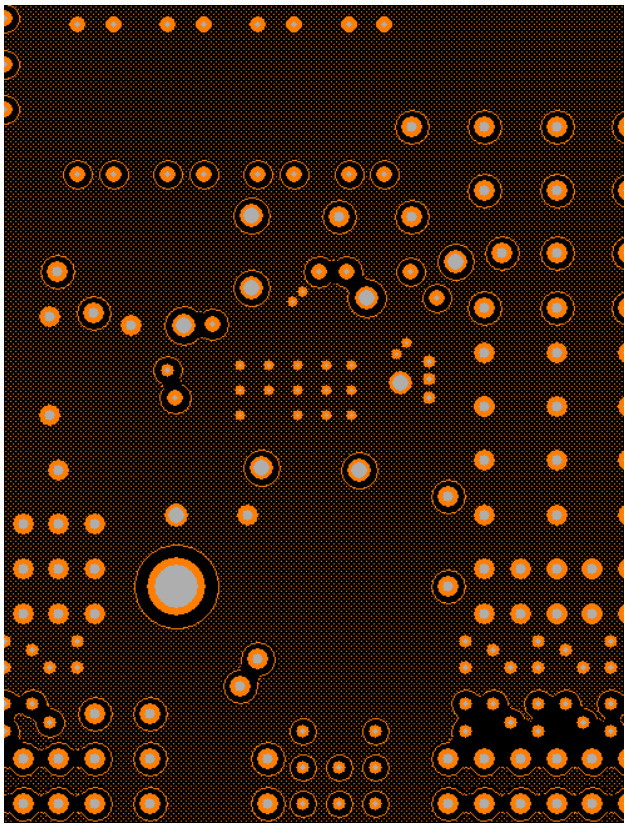

Figure 14. Layer 2 Copper Layer (Ground Plane)

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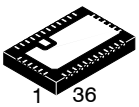
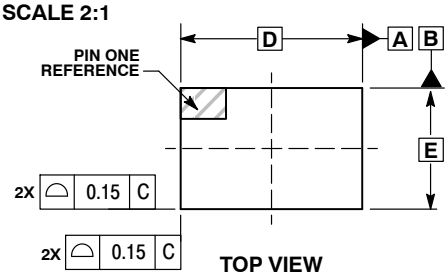
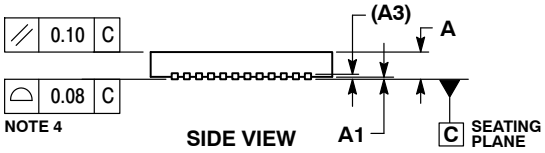
CASE 485DZ
ISSUE A

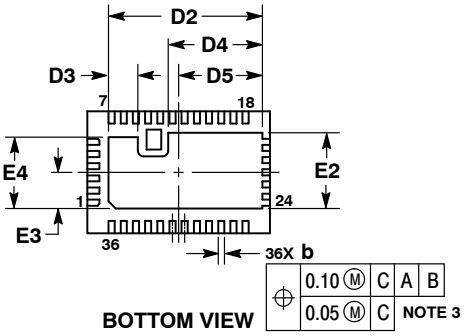
DATE 19 JUN 2015

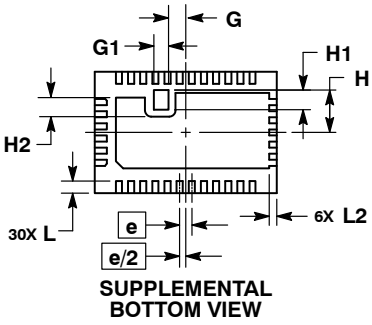


SCALE 2:1





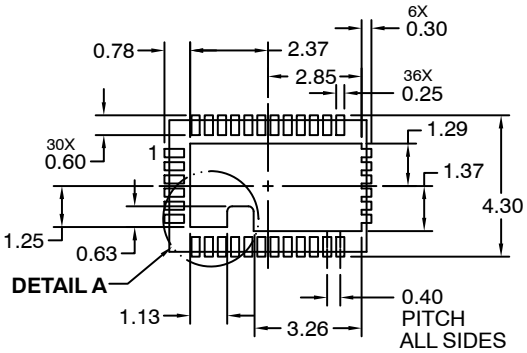


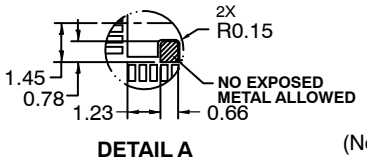


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.20
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.95	5.05
D3	0.91	1.01
D4	3.04	3.14
D5	2.70	2.80
E	4.00 BSC	
E2	2.44	2.54
E3	1.14	1.24
E4	2.29	2.39
e	0.40 BSC	
G	0.52	0.62
G1	0.43	0.53
H	1.35	1.45
H1	0.60	0.70
H2	0.57	0.68
L	0.30	0.50
L2	0.15	0.35

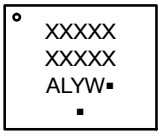
RECOMMENDED SOLDERING FOOTPRINT*





*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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