NCP346

Overvoltage Protection IC

The NCP346 Overvoltage Protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients and power supply faults when used in conjunction with an external P−channel FET. The device is designed to sense an overvoltage condition and quickly disconnect the input voltage supply from the load before any damage can occur. The OVP consists of a precise voltage reference, a comparator with hysteresis, control logic, and a MOSFET gate driver. The OVP is designed on a robust BiCMOS process and is intended to withstand voltage transients up to 30 V.

The device is optimized for applications that have an external AC/DC adapter or car accessory charger to power the product and/or recharge the internal batteries. The nominal overvoltage thresholds are 4.45 and 5.5 V and can be adjusted upward with a resistor divider between the V_{CC}, IN, and GND pins. It is suitable for single cell Li−Ion applications as well as 3/4 cell NiCD/NiMH applications.

Features

- Overvoltage Turn−Off Time of Less Than 1.0 μsec
- Accurate Voltage Threshold of 4.45 V and 5.5 V (Nominal)
- CNTRL Input Compatible with 1.8 V Logic Levels
- These are Pb−Free Devices

Typical Applications

- Cellular Phones
- Digital Cameras
- Portable Computers and PDAs
- Portable CD and other Consumer Electronics

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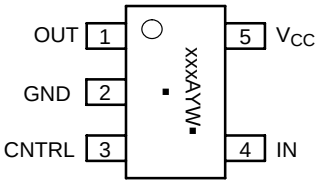
THIN SOT−23−5
SN SUFFIX
CASE 483

PIN CONNECTIONS & MARKING DIAGRAM



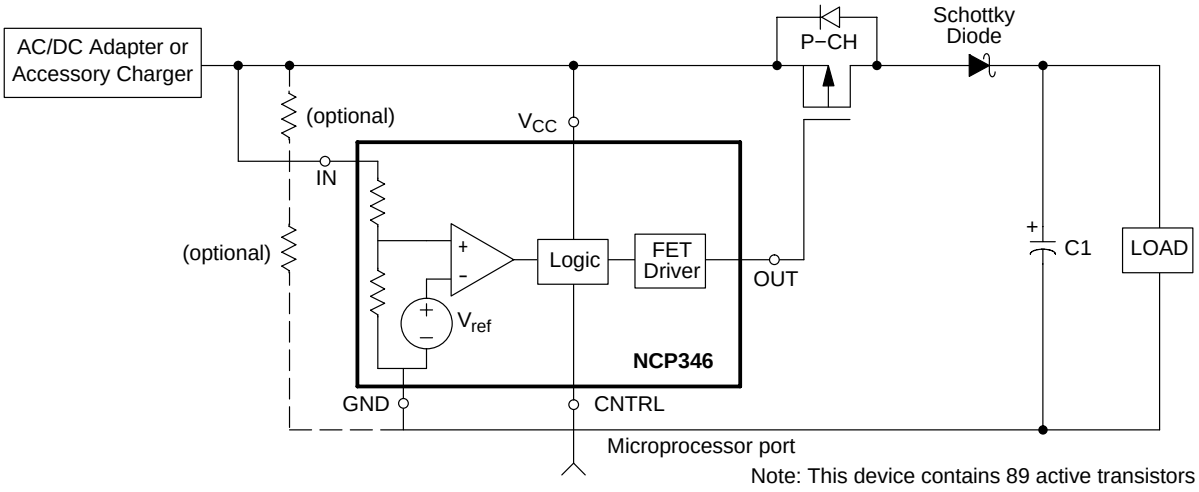
(Top View)

xxx = SQZ for NCP346SN1
= SRD for NCP346SN2
A = Asembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP346SN1T1G	SOT−23−5 (Pb−Free)	3000 / Tape & Reel (7 inch Reel)
NCP346SN2T1G		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



Note: This device contains 89 active transistors

Figure 1. Simplified Application Diagram

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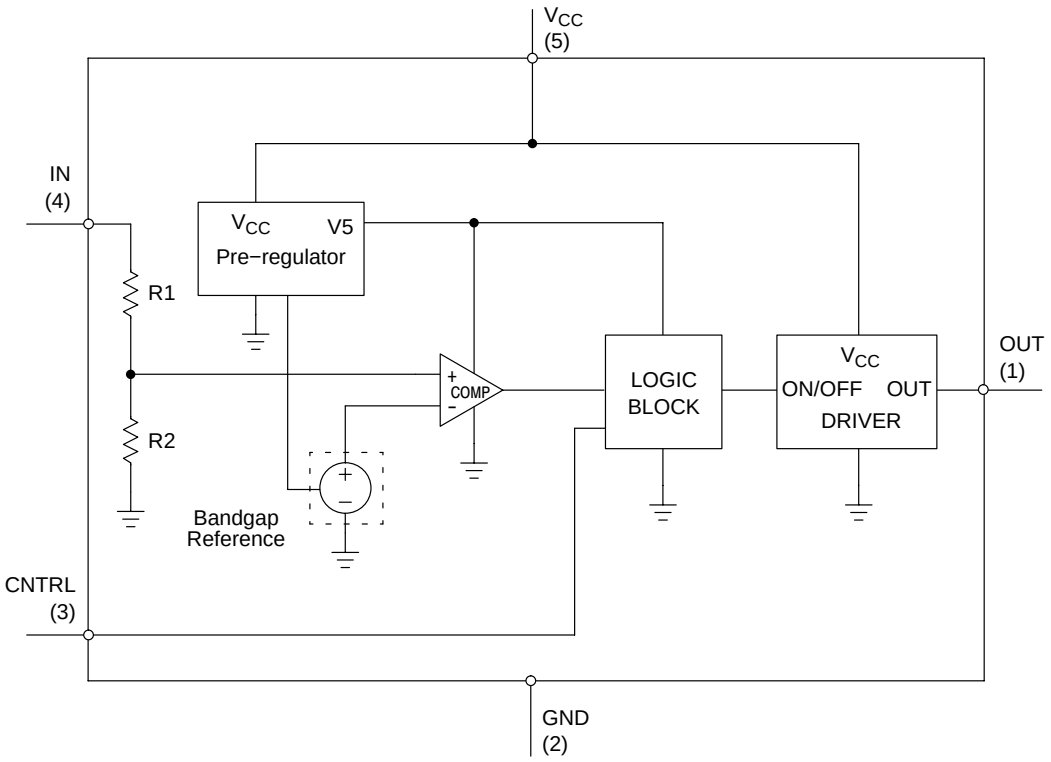


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	OUT	This signal drives the gate of a P−channel MOSFET. It is controlled by the voltage level on IN or the logic state of the CNTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{CC} in less than 1.0 μsec provided that gate and stray capacitance is less than 12 nF.
2	GND	Circuit Ground
3	CNTRL	This logic signal is used to control the state of OUT and turn−on/off the P−channel MOSFET. A logic High results in the OUT signal being driven to within 1.0 V of V_{CC} which disconnects the FET. The input is tied Low via an internal 50 kΩ pull−down resistor. It is recommended that the input be connected to GND if it is not used.
4	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (V_{th}), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the FET. The nominal threshold level can be increased with the addition of an external resistor divider between IN, V_{CC}, and GND.
5	V_{CC}	Positive Voltage supply. OUT is guaranteed to be in low state (MOSFET ON) as long as V_{CC} remains above 2.5 V, and below the overvoltage threshold.

TRUTH TABLE

IN	CNTRL	OUT
$<V_{th}$	L	GND
$<V_{th}$	H	V_{CC}
$>V_{th}$	L	V_{CC}
$>V_{th}$	H	V_{CC}

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	1	V_O	−0.3	30	V
Input and CNTRL Pin Voltage to GND	4 3	V_{input} V_{CNTRL}	−0.3 −0.3	30 13	V
Input Pin Voltage to V_{CC}	4, 5	$V(V_{CC,}$ IN)	−0.3	15	V
V_{CC} Maximum Range	5	$V_{CC(max)}$	−0.3	30	V
Maximum Power Dissipation at T_A = 85°C	−	P_D	−	0.216	W
Thermal Resistance, Junction−to−Air	−	$R_{\theta JA}$	−	300	°C/W
Junction Temperature	−	T_J	−	150	°C
Operating Ambient Temperature	−	T_A	−40	85	°C
V_{CNTRL} Operating Voltage	3	−	0	5.0	V
Storage Temperature Range	−	T_{stg}	−65	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model (HBM) per JEDEC Standard JESD22−A114 Machine Model (MM) per JEDEC Standard JESD22−A114	 ≤ 2.5 kV ≤ 250 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Transistor Count	89
Latchup Current Maximum Rating per JEDEC Standard EIA/JESD78	≤ 150 mA

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

ELECTRICAL CHARACTERISTICS (NCP346SN1T1)
(For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{CC} Operating Voltage Range	5	$V_{CC(opt)}$	2.5	−	25	V
Total Supply Current (IN Connected to V_{CC}; ON Mode, V_{CC} = 4.0 V, CNTRL Pin Floating, Steady State)	4,5	$I_{cc\ on}$	−	650	1200	μA
Total Supply Current (IN Connected to V_{CC}; OFF Mode Driven by CNTRL Pin, V_{CC} = 4.0 V, V_{CNTRL} = 1.5 V, Steady State)	4,5	$I_{cc\ off}$ CNTRL	−	700	1200	μA
Total Supply Current (IN Connected to V_{CC}; OFF Mode Driven by Overvoltage, V_{CC} = 5.0 V, CNTRL Pin Floating, Steady State)	4,5	$I_{cc\ off}$ IN	−	750	1200	μA
Input Threshold (IN Connected to V_{CC}; V_{CC} Increasing)	4	V_{th} (LH)	4.3	4.45	4.6	V
Input Threshold (IN Connected to V_{CC}; V_{CC} Decreasing)	4	V_{th} (HL)	4.3	4.4	4.6	V
Input Hysteresis (IN Connected to V_{CC})	4	V_{hyst}	−	50	−	mV
Input Impedance of IN Pin	4	R_{in}	30	55	85	kΩ
CNTRL Voltage High	3	V_{IH}	1.5	−	−	V
CNTRL Voltage Low	3	V_{IL}	−	−	0.5	V
CNTRL Current High (V_{ih} = 5.0 V)	3	I_{IH}	−	90	200	μA
CNTRL Current Low (V_{il} = 0.5 V)	3	I_{IL}	−	9.0	20	μA
Output Voltage High (IN Connected to V_{CC}, V_{CC} = 5.0 V) I_{source} = 10 mA I_{source} = 0.25 mA I_{source} = 0 mA	1	V_{oh}	 V_{CC} − 1.0 V_{CC} − 0.25 V_{CC} − 0.1	−	−	V
Output Voltage Low (IN Connected to V_{CC}, V_{CC} = 4.0 V, CNTRL Pin Floating) I_{sink} = 0 mA	1	V_{ol}	−	−	0.1	V
Output Sink Current (IN Connected to V_{CC}, V_{CC} = 4.0 V, CNTRL Pin Floating, V_{OUT} = 1.0 V)	1	I_{sink}	4.0	10	16	μA
Turn ON Delay – Input (IN Connected to V_{CC}; V_{CC} Steps Down from 5.0 V to 4.0 V, C_{load} = 12 nF, Measured to V_{out} < 1.0 V)	1	t_{on} IN	−	1.8	3.5	msec
Turn OFF Delay – Input (IN Connected to V_{CC}; V_{CC} Steps Up from 4.0 V to 5.0 V, C_{load} = 12 nF, Measured to V_{OUT} > V_{CC} − 1.0 V)	1	t_{off} IN	−	0.6	1.0	μsec
Turn OFF Delay – CNTRL (IN Connected to V_{CC}; V_{CC} = 4.0 V, V_{CNTRL} Steps from 0.5 V to 2.0 V, C_{load} = 12 nF, Measured to V_{OUT} > V_{CC} − 1.0 V)	1	t_{off} CNTRL	−	0.5	1.0	μsec

ELECTRICAL CHARACTERISTICS (NCP346SN2T1)
(For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{CC} Operating Voltage Range	5	$V_{CC(opt)}$	2.5	−	25	V
Total Supply Current (IN Connected to V_{CC}; ON Mode, V_{CC} = 5.0 V, CNTRL Pin Floating, Steady State)	4, 5	$I_{cc\ on}$	−	650	1200	μA
Total Supply Current (IN Connected to V_{CC}; OFF Mode Driven by CNTRL Pin, V_{CC} = 5.0 V, V_{CNTRL} = 1.5 V, Steady State)	4, 5	$I_{cc\ off}$ CNTRL	−	700	1200	μA
Total Supply Current (IN Connected to V_{CC}; OFF Mode Driven by Overvoltage, V_{CC} = 6.0 V, CNTRL Pin Floating, Steady State)	4, 5	$I_{cc\ off}$ IN	−	750	1200	μA
Input Threshold (IN Connected to V_{CC}; V_{CC} Increasing)	4	V_{th} (LH)	5.3	5.5	5.7	V
Input Threshold (IN Connected to V_{CC}; V_{CC} Decreasing)	4	V_{th} (HL)	5.3	5.45	5.7	V
Input Hysteresis (IN Connected to V_{CC})	4	V_{hyst}	−	50	−	mV
Input Impedance of IN Pin	4	R_{in}	30	60	100	kΩ
CNTRL Voltage High	3	V_{IH}	1.5	−	−	V
CNTRL Voltage Low	3	V_{IL}	−	−	0.5	V
CNTRL Current High (V_{ih} = 5.0 V)	3	I_{IH}	−	95	200	μA
CNTRL Current Low (V_{il} = 0.5 V)	3	I_{IL}	−	9.0	20	μA
Output Voltage High (IN Connected to V_{CC}, V_{CC} = 6.0 V) I_{source} = 10 mA I_{source} = 0.25 mA I_{source} = 0 mA	1	V_{oh}	 V_{CC} − 1.0 V_{CC} − 0.25 V_{CC} − 0.1	−	−	V
Output Voltage Low (IN Connected to V_{CC}, V_{CC} = 5.0 V, CNTRL Pin Floating) I_{sink} = 0 mA	1	V_{ol}	−	−	0.1	V
Output Sink Current (IN Connected to V_{CC}, V_{CC} = 5.0 V, CNTRL Pin Floating, V_{OUT} = 1.0 V)	1	I_{sink}	4.0	10	16	μA
Turn ON Delay – Input (IN Connected to V_{CC}; V_{CC} Steps Down from 6.0 V to 5.0 V, C_{load} = 12 nF, Measured to V_{out} < 1.0 V)	1	t_{on} IN	−	1.8	4.5	msec
Turn OFF Delay – Input (IN Connected to V_{CC}; V_{CC} Steps Up from 5.0 V to 6.0 V, C_{load} = 12 nF, Measured to V_{OUT} > V_{CC} − 1.0 V)	1	t_{off} IN	−	0.5	1.0	μsec
Turn OFF Delay – CNTRL (V_{CNTRL} Steps Up from 0.5 V to 2.0 V, V_{CC} = 5.0 V, C_{load} = 12 nF, Measured to V_{OUT} > V_{CC} − 1.0 V)	1	t_{off} ICNTRL	−	0.6	1.0	μsec

APPLICATION INFORMATION

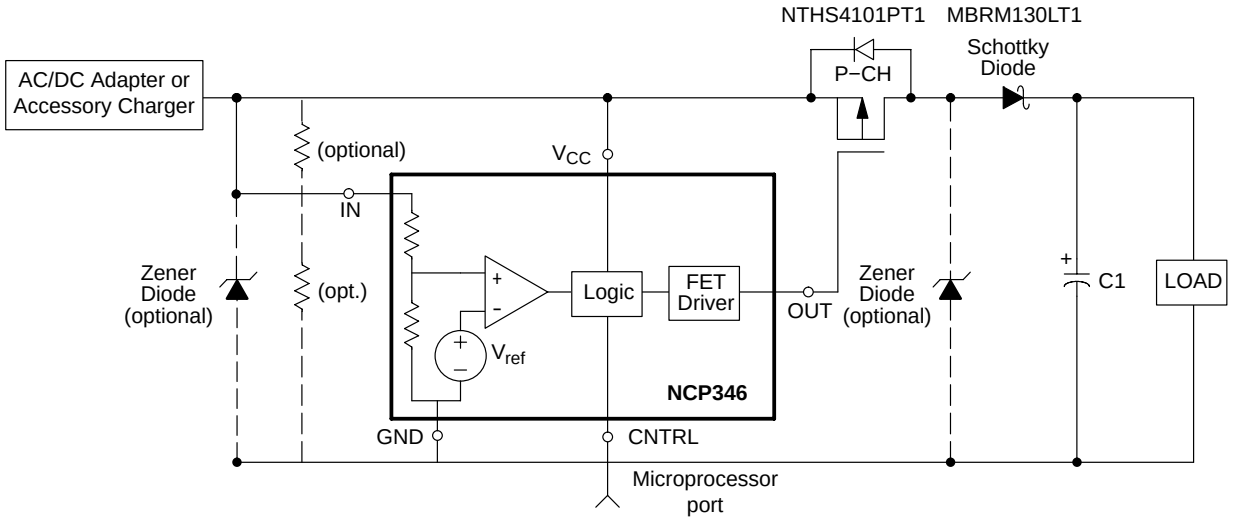


Figure 3.

Introduction

In many electronic products, an external AC/DC wall adapter is used to convert the AC line voltage into a regulated DC voltage or a current limited source. Line surges or faults in the adapter may result in overvoltage events that can damage sensitive electronic components within the product. This is becoming more critical as the operating voltages of many integrated circuits have been lowered due to advances in sub−micron silicon lithography. In addition, portable products with removable battery packs pose special problems since the pack can be removed at any time. If the user removes a pack in the middle of charging, a large transient voltage spike can occur which can damage the product. Finally, damage can result if the user plugs in the wrong adapter into the charging jack. The challenge of the product designer is to improve the robustness of the design and avoid situations where the product can be damaged due to unexpected, but unfortunately, likely events that will occur as the product is used.

Circuit Overview

To address these problems, the protection system above has been developed consisting of the NCP346 Overvoltage Protection IC and a P−channel MOSFET switch such as the MGSF3441. The NCP346 monitors the input voltage and will not turn on the MOSFET unless the input voltage is within a safe operating window that has an upper limit of the overvoltage detection threshold. A Zener diode can be placed in parallel to the load to provide for secondary protection during the brief time that it takes for the NCP346 to detect the overvoltage fault and disconnect the MOSFET. The decision to use this secondary diode is a function of the charging currents expected, load capacitance across the battery, and the desired protection voltage by analyzing the dV/dT rise that occurs during the brief time it takes to turn−off the MOSFET. For battery powered applications, a low−forward voltage Schottky diode such as the MBRM120LT3 can be placed in series with the MOSFET to block the body diode of the MOSFET and prevent shorting the battery out if the input is accidentally shorted to ground. This provides additional voltage margin at the load since there is a small forward drop across this diode that reduces the voltage at the load.

When the protection circuit turns off the MOSFET, there can be a sudden rise in the input voltage of the device. This transient can be quite large depending on the impedance of the supply and the current being drawn from the supply at the time of an overvoltage event. This inductive spike can be clamped with a Zener diode from IN to ground. This diode breakdown voltage should be well above the worst case supply voltage provided from the AC/DC adapter or Cigarette Lighter Adapter (CLA), since the Zener is only intended to clamp the transient. The NCP346 is designed so that the IN and V_{CC} pin can safely protect up to 25 V and withstand transients to 30 V. Since these spikes can be very narrow in duration, it is important to use a high bandwidth probe and oscilloscope when prototyping the product to verify the operation of the circuit under all the transient conditions. A similar problem can result due to contact bounce as the DC source is plugged into the product.

For portable products it is normal to have a capacitor to ground in parallel with the battery. If the product has a battery pack that is easily removable during charging, this scenario should be analyzed. Under that situation, the charging current will go into the capacitor and the voltage may rise rapidly depending on the capacitor value, the charging current and the power supply response time.

Normal Operation

Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The OVP monitors the voltage from the charger and if the voltage exceeds the overvoltage threshold, V_{th}, the OUT signal drives the gate of the MOSFET to within 1.0 V of V_{CC}, thus turning off the FET and disconnecting the source from the load. The nominal time it takes to drive the gate to this state is 400 nsec (1.0 μsec maximum for gate capacitance of < 12 nF). The CNTRL input can be used to interrupt charging and allow the microcontroller to measure the cell voltage under a normal condition to get a more accurate measure of the battery voltage. Once the overvoltage is removed, the NCP346 will turn on the MOSFET. The turn on circuitry is designed to turn on the MOSFET more gradually to limit the in−rush current. This characteristic is a function of the threshold of the MOSFET and will vary depending on the device characteristics such as the gate capacitance.

There are two events that will cause the OVP to drive the gate of the FET to a HIGH state.

- Voltage on IN Rises Above the Overvoltage Detection Threshold
- CNTRL Input is Driven to a Logic HIGH

Adjusting the Overvoltage Detection Point with External Resistors

The separate IN and V_{CC} pins allow the user to adjust the overvoltage threshold, V_{th}, upwards by adding a resistor divider with the tap at the IN pin. However, R_{in} does play a significant role in the calculation since it is several 10's of kΩ. The following equation shows the effects of R_{in}.

$$V_{CC} = V_X(1 + R_1/(R_2//R_{in})) \quad \text{(eq. 1)}$$

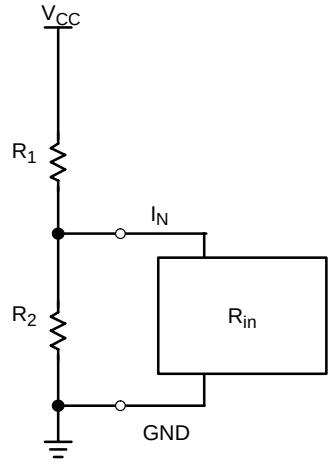


Figure 4. Voltage divider input to adjust overvoltage detection point

which equates to:

$$V_{CC} = V_X(1 + R_1/R_2 + R_1/R_{in}) \quad \text{(eq. 2)}$$

So, as R_{in} approaches infinity:

$$V_{CC} = V_X(1 + R_1/R_2) \quad \text{(eq. 3)}$$

This shows that R_{in} shifts the V_{th} detection point in accordance to the ratio of R_1 / R_{in}. However, if $R_1 << R_{in}$, this shift can be minimized. The following steps show this procedure.

Designing around the Maximum Voltage Rating Requirements, V(V_{CC}, IN)

The NCP346's maximum breakdown voltage between pins V_{CC} and IN is 15 V. Therefore, care must be taken that the design does not exceed this voltage. Normally, the designer shorts V_{CC} to IN, V(V_{CC}, IN) is shorted to 0 V, so there is no issue. However, one must take care when adjusting the overvoltage threshold.

In Figure 4, the R1 resistor of the voltage divider divides the V(V_{CC}, IN) voltage to a given voltage threshold equal to:

$$(V_{CC}, IN) = V_{CC} * (R1/(R1 + (R2//R_{in}))) \quad \text{(eq. 4)}$$

V(V_{CC}, IN) worst case equals 15 V, and V_{CC} worst case equals 30 V, therefore, one must ensure that:

$$R1/(R1 + (R2//R_{in})) < 0.5 \quad \text{(eq. 5)}$$

Where 0.5 = V(V_{CC}, IN)max/V_{CCmax}

Therefore, the NCP346 should only be adjusted to maximum overvoltage thresholds which are less than 15 V. If greater thresholds are desired than can be accommodated by the NCP346, ON Semiconductor offers the NCP345 which can withstand those voltages.

Design Steps for Adjusting the Overvoltage Threshold

1. Use Typical R_{in}, and V_{th} Values from the Electrical Specifications
2. Minimize R_{in} Effect by Selecting $R_1 << R_{in}$ since:

$$V_{OV} = V_{th}(1 + R_1/R_2 + R_1/R_{in}). \quad \text{(eq. 6)}$$

3. Let $X = R_{in} / R_1 = 100$.
4. Identify Required Nominal Overvoltage Threshold.
5. Calculate nominal R_1 and R_2 from Nominal Values:

$$R_1 = R_{in}/X \quad \text{(eq. 7)}$$

$$R_2 = \frac{R_1}{(V_{OV}/V_{th} - R_1/R_{in} - 1)} \quad \text{(eq. 8)}$$

6. Pick Standard Resistor Values as Close as Possible to these Values
7. Use min/max Data and Resistor Tolerances to Determine Overvoltage Detection Tolerance:

$$V_{OVmin} = V_{thmin}(1 + R_{1min}/R_{2max} + R_{1min}/R_{inmax}) \quad \text{(eq. 9)}$$

$$V_{OVtyp} = V_{thtyp}(1 + R_{1typ}/R_{2typ} + R_{1typ}/R_{intyp}) \quad \text{(eq. 10)}$$

$$V_{OVmax} = V_{thmax}(1 + R_{1min}R_{2max} + R_{1max}/R_{inmin}) \quad \text{(eq. 11)}$$

The specification takes into account the hysteresis of the comparator, so the minimum input threshold voltage (V_{th}) is the falling voltage detection point and the maximum is the rising voltage detection point. One should design the input supply such that its maximum supply voltage in normal operation is less than the minimum desired overvoltage threshold.

8. Use worst case resistor tolerances to determine the maximum $V(V_{CC},IN)$

$$V(V_{CC}, IN)\,min = V_{CCmax} * (R1min/(R1min + R2max)) \quad \text{(eq. 12)}$$

$$V(V_{CC}, IN)typ = V_{CCmax} * (R1typ/(R1typ + R2typ)) \quad \text{(eq. 13)}$$

$$V(V_{CC}, IN)\,max = V_{CCmax} * (R1max/(R1max + R2min)) \quad \text{(eq. 14)}$$

This is shown empirically in Tables 2 through 4.

The following tables show an example of obtaining a 6 V detection voltage from the NCP346SN2T2, which has a typical V_{th} of 5.5 V.

Table 1. Design Steps 1−5

Parameter	Typical	Design Steps
IN Pin Input Impedance (I_N)	54000	(1)
Input Threshold (V_{th})	5.5	(1)
Ratio of R_{in} to R_1 (X)	100	(2, 3)
Desired Overvoltage Threshold (V_{OV})	6	(4)
R_1	540	(5)
R_2	6674	(5)

Table 2. Design Steps 6−7 with 1% Resistors

1% Resistors

Parameter	Min	Typical	Max	Design Steps
R_1	543.51	549	554.49	(6)
R_2	6583.5	6650	6716.5	(6)
V_{th}	5.3	5.5	5.7	(6)
R_{in}	30000	54000	100000	(6)
V_{OV}	5.76	6.01	6.29	(7)
$V(V_{CC}, IN)$ @ V_{CCmax}	2.25	2.29	2.33	(8)

Table 3. Design Steps 6−7 with 5% Resistors

5% Resistors

Parameter	Min	Typ	Max	Design Steps
R_1	532	560	588	(6)
R_2	6460	6800	7140	(6)
V_{th}	5.3	5.5	5.7	(6)
R_{in}	30000	54000	100000	(6)
V_{OV}	5.72	6.01	6.33	(7)
$V(V_{CC}, IN)$ @ V_{CCmax}	2.08	2.28	2.50	(8)

Table 4. Design Steps 6−7 with 10% Resistors

10% Resistors

Parameter	Min	Typ	Max	Design Steps
R_1	504	560	616	(6)
R_2	6120	6800	7480	(6)
V_{th}	5.3	5.5	5.7	(6)
R_{in}	30000	54000	100000	(6)
V_{OV}	5.68	6.01	6.39	(7)
$V(V_{CC}, IN)$ @ V_{CCmax}	1.89	2.28	2.74	(8)

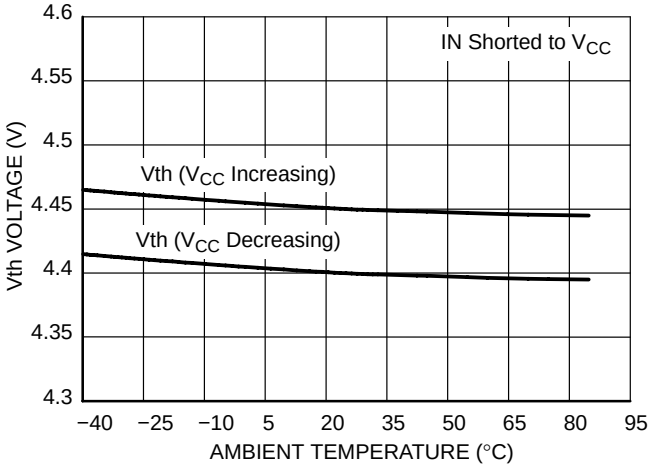


Figure 5. Typical Vth Variation vs. Temperature (NCP346SN1)

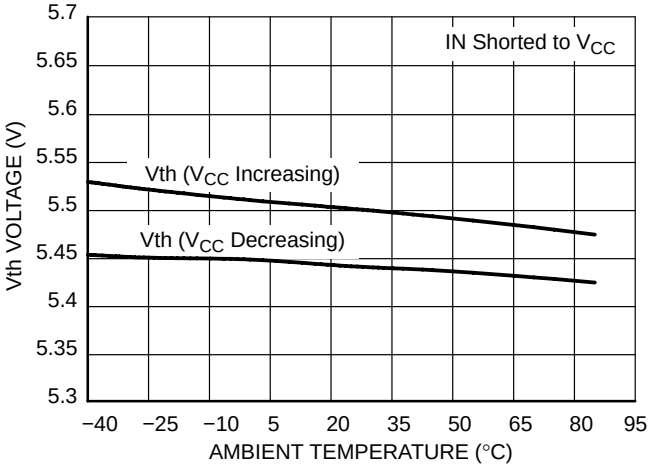


Figure 6. Typical Vth Variation vs. Temperature (NCP346SN2)

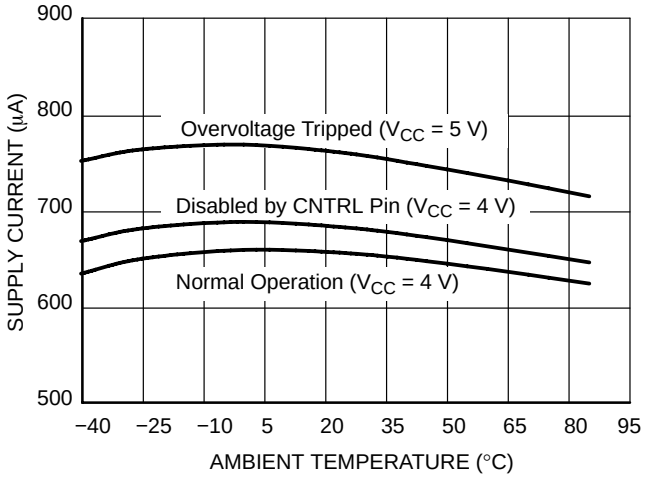


Figure 7. Typical Supply Current (I_{CC} + I_{IN}) vs. Temperature (NCP346SN1)

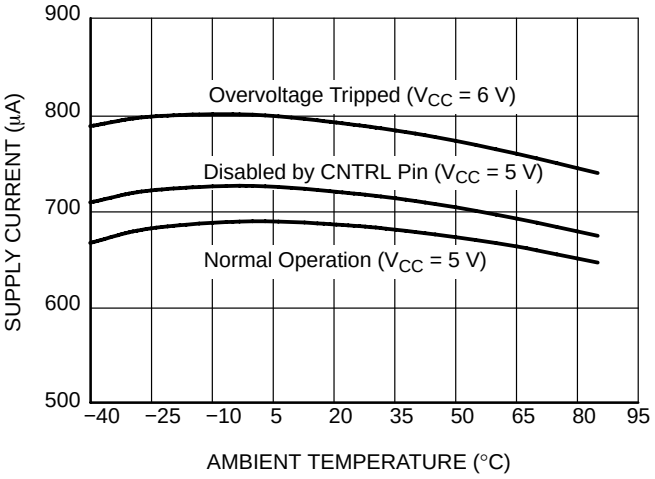


Figure 8. Typical Supply Current (I_{CC} + I_{IN}) vs. Temperature (NCP346SN2)

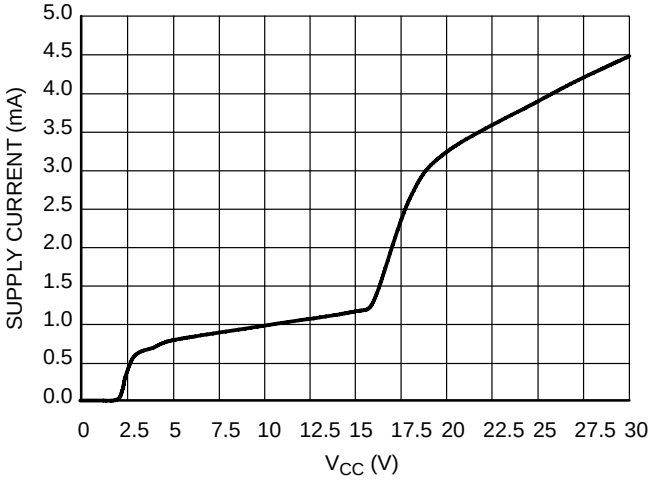


Figure 9. Total Supply Current vs. V_{CC} (NCP346SN1)

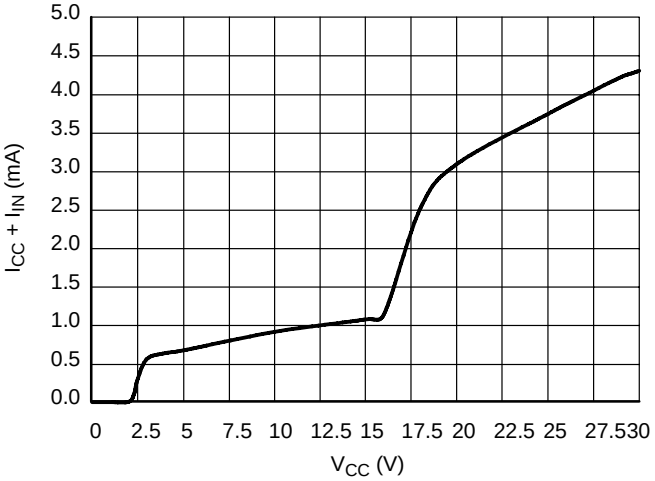


Figure 10. Total Supply Current vs. V_{CC} (NCP346SN2)

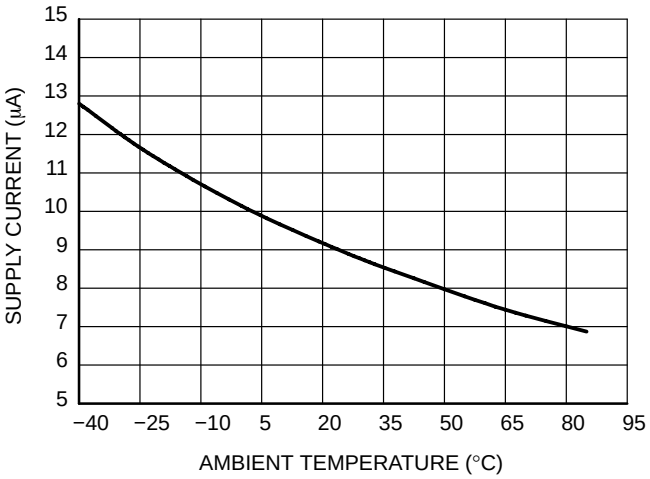


Figure 11. Typical OUT Sink Current vs. Temperature (NCP346SN1)

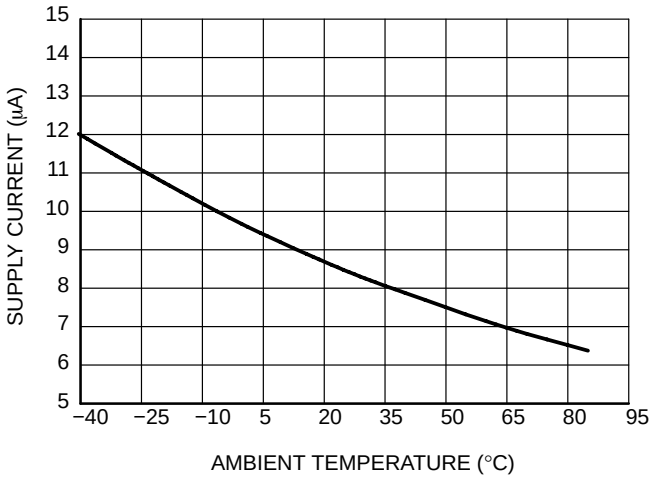


Figure 12. Typical OUT Sink Current vs. Temperature (NCP346SN2)

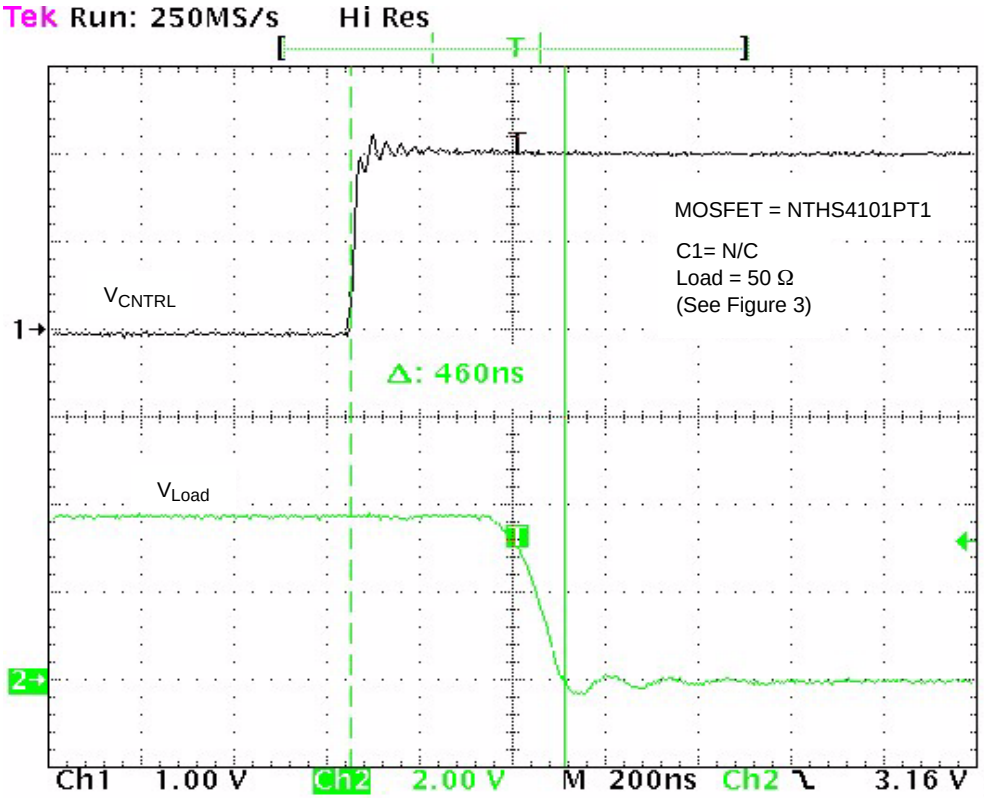


Figure 13. Typical Turn−off Time CNTRL (NCP346SN1)

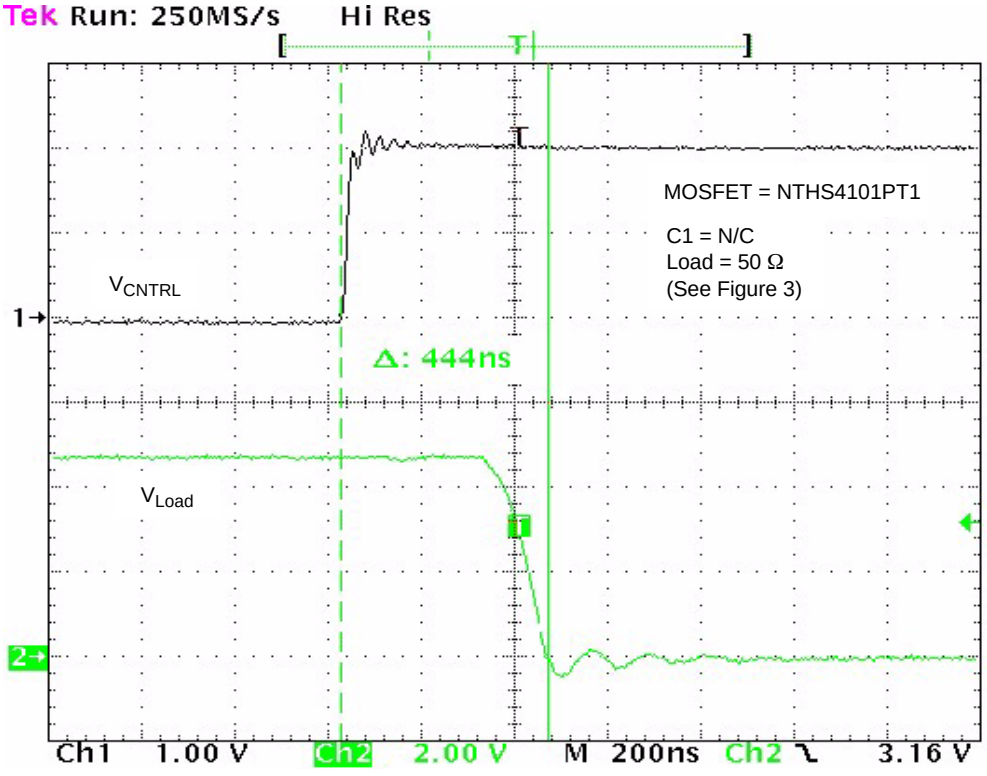


Figure 14. Typical Turn−off Time CNTRL (NCP346SN2)

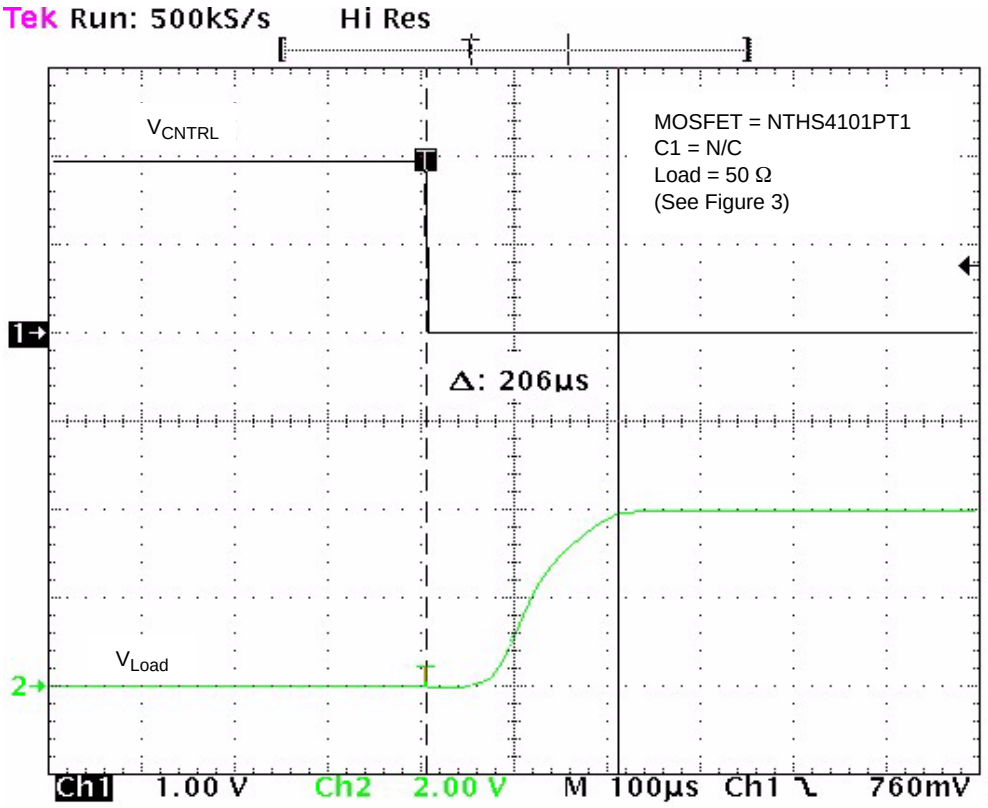


Figure 15. Typical Turn−on Time CNTRL (NCP346SN1)

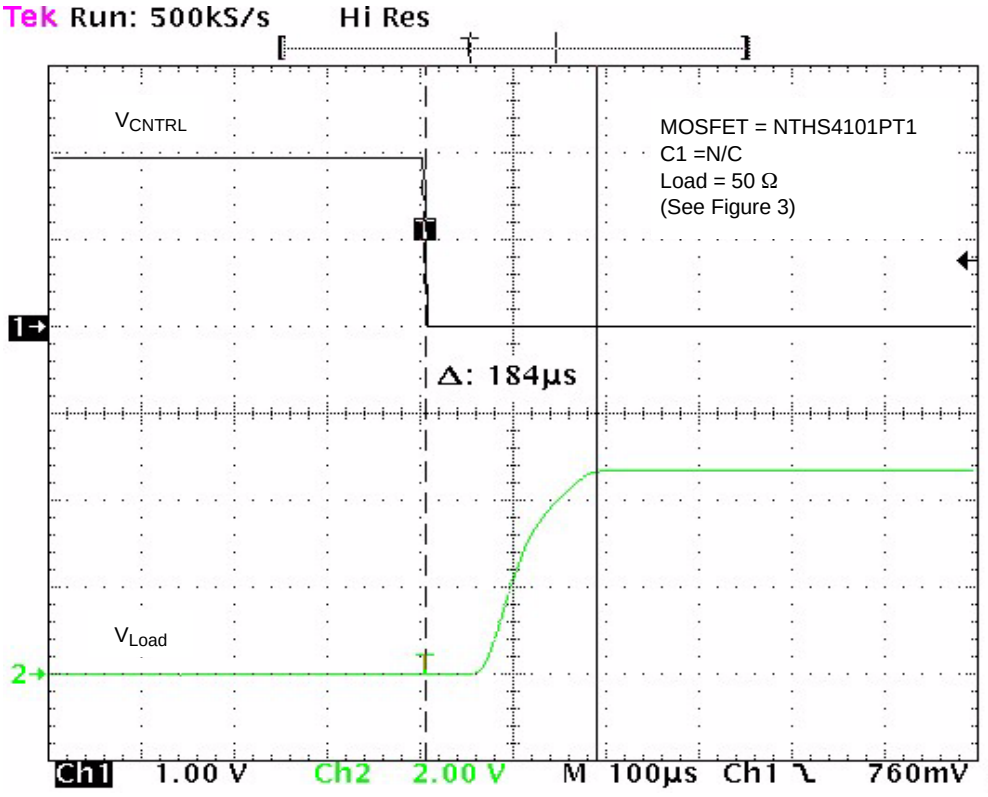


Figure 16. Typical Turn−on Time CNTRL (NCP346SN2)

THIN SOT−23−5 POWER DISSIPATION

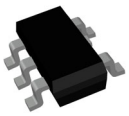
The power dissipation of the Thin SOT−23−5 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the Thin SOT−23−5 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

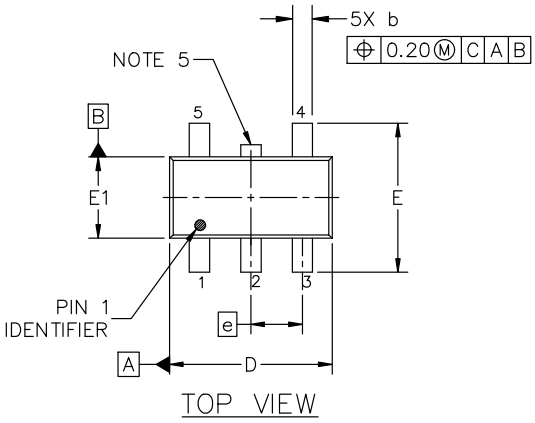
$$P_D = \frac{150°C - 25°C}{300°C/W} = 417 \text{ milliwatts}$$

The 300°C/W for the Thin SOT−23−5 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 417mw.

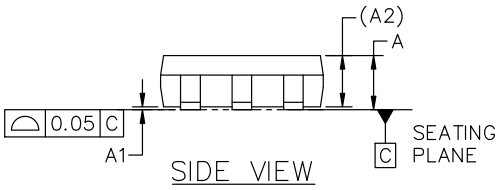


TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

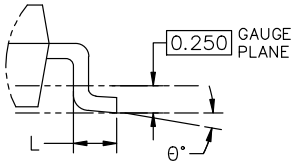
DATE 01 APR 2024



TOP VIEW



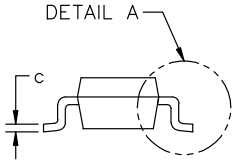
SIDE VIEW



DETAIL "A"
SCALE 2:1

NOTES:

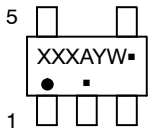
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.



END VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2		0.950 REF.	
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e		0.950 BSC	
L	0.200	0.400	0.600
θ	0°	5°	10°

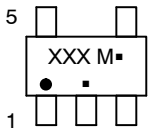
GENERIC
MARKING DIAGRAM*



Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

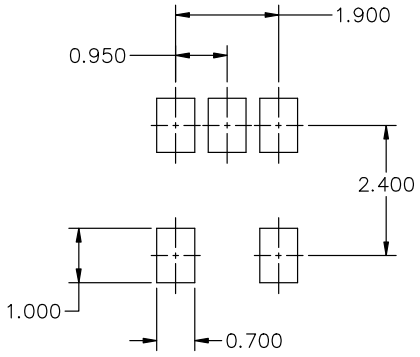
(Note: Microdot may be in either location)



Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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